TEXAS INSTRUMENTS

Wireless and Telecommunications Products

Central Office, Telemetry RF Receivers, and Personal Communications Solutions

Data Book

1996

Mixed-Signal Products

ERRATA

HE WIRELESS AND TELECOMMUNICATIONS PRODUCTS DATA BOOK

(Texas Instruments Literature No. SLWD001, July 1996)

ptimize the system performance of several of our codecs, Texas Instruments has made a design change ons the digital and analog grounds internal to the device. The best codec performance is obtained from ces when these two terminals are at the same voltage potential, which may not be the case if they are used n with seperate analog and digital supply return (ground) lines. The internal connection ensures there is tial voltage between the digital and analog ground terminals.

affects the following data sheets in the Wireless and Telecommunications Products Data Book covering g devices:

-29, TI Literature No. SCTS030D data sheet covering the TCM129C13A, TCM29C13A, 9C14A, TCM29C14A, TCM129C16A, TCM29C16A, TCM129C17A, and TCM29C17A devices.

–29 of the Data Book, in the Terminal Functions table make the following changes to two rows in the table: ANLG GND and DGTL GND rows, remove the word **Not** from the DESCRIPTION column and replace **GND is**

	TERMINAL NO.			I/O	DESCRIPTION
	TCM29C13A TCM129C13A	TCM29C14A TCM129C14A	TCM29C16A TCM29C17A TCM129C16A TCM129C17A		
D	16	20	13		Analog ground return for all internal voice circuits. **Not** internally connected to DGTL GND.
D	10	12	8		Digital ground for all internal logic circuits. **Not** internally connected to ANLG GND.

	TERMINAL NO.			I/O	DESCRIPTION
	TCM29C13A TCM129C13A	TCM29C14A TCM129C14A	TCM29C16A TCM29C17A TCM129C16A TCM129C17A		
D	16	20	13		Analog ground return for all internal voice circuits. **ANLG GND is** internally connected to DGTL GND.
D	10	12	8		Digital ground for all internal logic circuits. **DGTL GND is** internally connected to ANLG GND.

llowing table to the electrical characteristics section (begins on page 2–32):

rminals

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ce between ANLG GND and DGTL GND			34		Ω

- **Page 2–53, TI Literature No. SCTS021C, data sheet covering the TCM29C18, TCM129C18, TCM and TCM129C19 devices.**

On page 2–53 of the Data Book, in the Terminal Functions table make the following changes to two rows in In both the ANLG GND and DGTL GND rows, remove the word **Not** from the DESCRIPTION column ar with **XXXX GND is**

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ANLG GND	13		Analog ground return for all voice circuits. **Not** internally connected to DGTL GND.
DGTL GND	8		Digital ground for all internal logic circuits. **Not** internally connected to ANLG GND.

to give:

ANLG GND	13		Analog ground return for all voice circuits. **ANLG GND is** internally connected to DGTL GND.
DGTL GND	8		Digital ground for all internal logic circuits. **DGTL GND is** internally connected to ANLG GND.

Add the following table to the electrical characteristics section (begins on page 2–55):

ground terminals

PARAMETER	TEST CONDITIONS	MIN	TYP	MA
DC resistance between ANLG GND and DGTL GND			34	

- **Page 2–85, TI Literature No. SCTS029A data sheet covering the TCM129C23 and the TCM29C2 devices.**

On page 2–85 of the Data Book, under the **variable data rate timing** paragraph heading, make the followi to the last word of the second paragraph: remove the **a** from the word **a**synchronous:

> Variable-data-rate timing allows for a flexible data frequency. The frequency of the bit clocks can be v 64 kHz to 4.096 MHz. The bit clocks must be **a**synchronous.

to give:

> Variable-data-rate timing allows for a flexible data frequency. The frequency of the bit clocks can be v 64 kHz to 4.096 MHz. The bit clocks must be synchronous.

- **Page 2–105, TI Literature No. SLWS018, data sheet covering the TCM37C13, TCM37C14, and T devices.**

These parts have been released. The data sheet has been revised to support the production devices an Production Data status. Please contact any TI sales office to obtain the latest data sheet on these or an semiconductor products.

Wireless and Telecommunications Products Data Book

Central Office, Telemetry RF Receivers, and Personal Communications Solutions

TEXAS INSTRUMENTS

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Owensville, Missouri

INTRODUCTION

The 1996 Wireless and Telecommunications Products Data Book has been created to showcase our growing line of analog and digital components for telecommunications and wireless applications. Featured in this data book are most of the components found in the 1993 Telecommunications Circuits Data Book, plus many new and exciting wireless communications, telecom, and RF for telemetry and remote keyless entry products introduced since then.

This new data book is more than a collection of data sheets; it is a tool for locating the best wireless and telecommunications components for a successful design effort. It has been structured into two parts, first telecommunications, then wireless, to help you quickly find the devices best suited to your application.

A complete alphanumeric index at the beginning of the data book makes locating data sheets for known part numbers easy, and separate selection guides for telecom and wireless have abbreviated application information and technical data to assist in your selection process. An extensive glossary is provided for referencing, defining, and clarifying terms used by Texas Instruments and the semiconductor industry that may be new, unfamiliar, or confusing.

While this data book offers design and specification data only for wireless and telecommunications products, complete technical data for any TI semiconductor product is available from your nearest TI Field Sales Office, local authorized TI distributor or by writing directly to:

Texas Instruments, Incorporated
LITERATURE RESPONSE CENTER
Post Office Box 809066
Dallas, TX 75380–9066

or by visiting TI's web site at http://www.ti.com

A complete list of sales offices, distributors, and technology centers is located in the back of this book.

We sincerely believe that the new 1996 Wireless and Telecommunications Circuits Data Book is a valuable and useful addition to your collection of technical literature.

PRODUCT STAGE STATEMENTS

Product stage statements are used on Texas Instruments data sheets to indicate the development stage(s) of the product(s) specified in the data sheets.

If all products specified in a data sheet are at the same development stage, the appropriate statement from the following list is placed in the lower left corner of the first page of the data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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If not all products specified in a data sheet are at the PRODUCTION DATA stage, then the first statement below is placed in the lower left corner of the first page of the data sheet. Subsequent pages of the data sheet containing PRODUCT PREVIEW information or ADVANCE INFORMATION are then marked in the lower left-hand corner with the appropriate statement given below:

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

ADVANCE INFORMATION concerns new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

Contents

NOTES: 1. The following devices have been deleted from this volume: TCM1501B, TCM1506B, TCM1512B, TCM1520A, TCM1531, TCM1532, TCM1536, TCM1539, TCM5087, TCM5087, TCM5089, TCM5092, TCM5094, TLC2470 / TLC2471 / TLC2472 / TLC2047

2. TheTCM3637now appears in the Remote Keyless Entry Data Book.

Introduction

Texas Instruments has been a world leader in central office codec technology since 1979. The combo section of this data book includes our established product line of codecs with on-chip filtering, primarily used in central office (line card) applications that perform the A/D and D/A conversion and filtering required for voice communications. The TP30xx series and TCM29Cxx series of combos provide the industry's best noise levels using TI's advanced switched-capacitor filter technologies. The TCM10xx family of devices compliments our line of codecs by providing protection from voltage transients for the codecs as well as the line cards.

Smaller geometry process technology and sigma-delta conversion technologies are combined this year in our first Advanced Combo™ product offering, the highly integrated QCombo™, TCombo™, and Combo III. The QCombo and TCombo are single-rail 4-channel (quad) and 2-channel (twin) combos-on-a-chip. The Combo III features TCM29C13 functionality with the addition of programmable gain. Texas Instruments is rapidly expanding it's Advanced Combo product family — see our roadmaps for additional information.

For the past 13 years, Texas Instruments has manufactured an advanced line of fixed-code RKE (remote keyless entry) products. This year, Texas Instruments is proud to introduce the MARCSTAR™ (Multi-Channel Advanced Remote-Control Signaling Transmitter And Receiver) family of RKE devices. These devices are advanced ASK/FSK RF receivers and mixed-signal rolling-code encoder/decoders utilizing new and innovative features that are industry first. The MARCSTAR RF section featured in this data book represents a portion of that family that provides turn-key receiver solutions on-a-chip. While primarily targeted at the RKE, GDO (garage door opener), and home security markets, the TRF140xx device family is also well suited to other low-power remote control and general telemetry applications. The MARCSTAR RF devices require a minimum of external components, significantly reducing circuit complexity and footprint compared to the current discrete receiver solutions. Using an RF architecture that is an RKE-industry first, MARCSTAR RF receivers feature no spurious emissions and infinite image rejection.

The MARCSTAR RF family maintains good sensitivity and out-of-band rejection with no manual alignment when used with external SAW filters. For a reduced-cost solution, the device is also compatible with external L/C components. MARCSTAR RF also includes several on-chip features that would normally require additional circuitry in a receiver system design. These include an RF amplifier/comparator for detection and shaping of input signals and decoding logic that provides specially formatted TTL data output, synchronized with a trigger output, for easy interface to any microcontroller when using Manchester-encoded data. The device also outputs raw demodulated AM at TTL levels using any ASK data for interface to self-synchronizing devices such as the TI rolling-code MARCSTAR encoder/decoders (covered in the TI RKE data book).

Texas Instruments is also rapidly expanding its MARCSTAR product family — see our roadmaps in this data book, as well as our separate RKE data book, for further information on the full MARCSTAR RF and encoder/decoder device families.

current TI line-card codec product offering

TCMxxCxx														
Intel Timing														
For Central Office Equipment Use												Interface For DSP		
Direct Intel Replacement				Reduced Noise (by 50% using a patented TI process)				Programmable Gain Reduced Noise			Quad channel QCOMBO	Low Cost		Extended Frequency
		Both μ-Law and A-Law				Both μ-Law and A-Law								
μ-Law	A-Law	8th Bit Signal	Stand-ard	μ-Law	A-Law	8th Bit Signal	Stand-ard	μ-Law	A-Law	μ-Law and A-Law	μ-Law and A-Law Single Voltage Supply (+5V)	μ-Law	μ-Law	μ-Law and A-Law
2.048 MHz	2.048 MHz	1.536 1.544 2.048 MHz	1.536 1.544 2.048 MHz	2.048 MHz	2.048 MHz	1.536 1.544 2.048 MHz	1.536 1.544 2.048 MHz	2.048 MHz	2.048 MHz	1.536 1.544 2.048 MHz	2.048 MHz	2.048 MHz	1.536 MHz	up to 4.096 MHz
TCM 29C16	TCM 29C17	TCM 29C14	TCM 29C13	TCM 29C16A	TCM 29C17A	TCM 29C14A	TCM 29C13A	TCM 37C13	TCM 37C15	TCM 37C14	TCM38C17	TCM 29C18	TCM 29C19	TCM 29C23
PAGE NO. 2–3 LIT. NO. SCTS011G				**PAGE NO. 2–27 LIT. NO. SCTS030D**				**PAGE NO. 2–105 LIT. NO. SLWS018**			**PAGE NO. 2–125 LIT. NO. SLWS040**	**PAGE NO. 2–51 LIT. NO. SCTS021C**		**PAGE NO. 2–69 LIT. NO. SCTS029A**

current TI line-card codec product offering (continued)

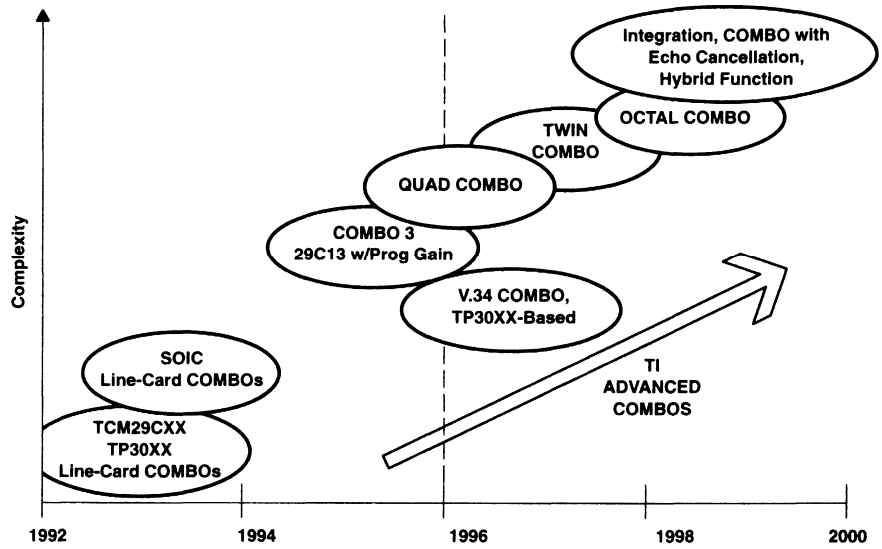
TP30xx								
National Timing								
For Central Office Equipment Use								Interface For DTAD/DSP
Direct National Replacement				Reduced Noise (by 50% using a patented TI process)				
Differential Output		Single Ended Output		Single Ended Output		Differential Output		Single Ended
μ-Law	A-Law	μ-Law	A-Law	μ-Law	A-Law	μ-Law	A-Law	μ-Law
1.536 1.544 2.048 MHz	1.536 1.544 2.048 MHz	1.536 1.544 2.048 MHz	1.536 1.544 2.048 MHz	1.536 1.544 2.048 MHz	1.536 1.544 2.048 MHz	1.536 1.544 2.048 MHz	1.536 1.544 2.048 MHz	1.536 1.544 2.048 MHz
TP3064A	TP3067B	TP3054A	TP3057B	TP3054B	TP3057A	TP3064B	TP3067A	TCM320AC54
			PAGE NO. 2–161 LIT. NO. SCTS042A					
		PAGE NO. 2–145 LIT. NO. SCTS026C						
	PAGE NO. 2–197 LIT. NO. SCTS031D							PAGE NO. 6–43 LIT. NO. SCTS029A
PAGE NO. 2–177 LIT. NO. SCTS025C								

transient voltage suppressors

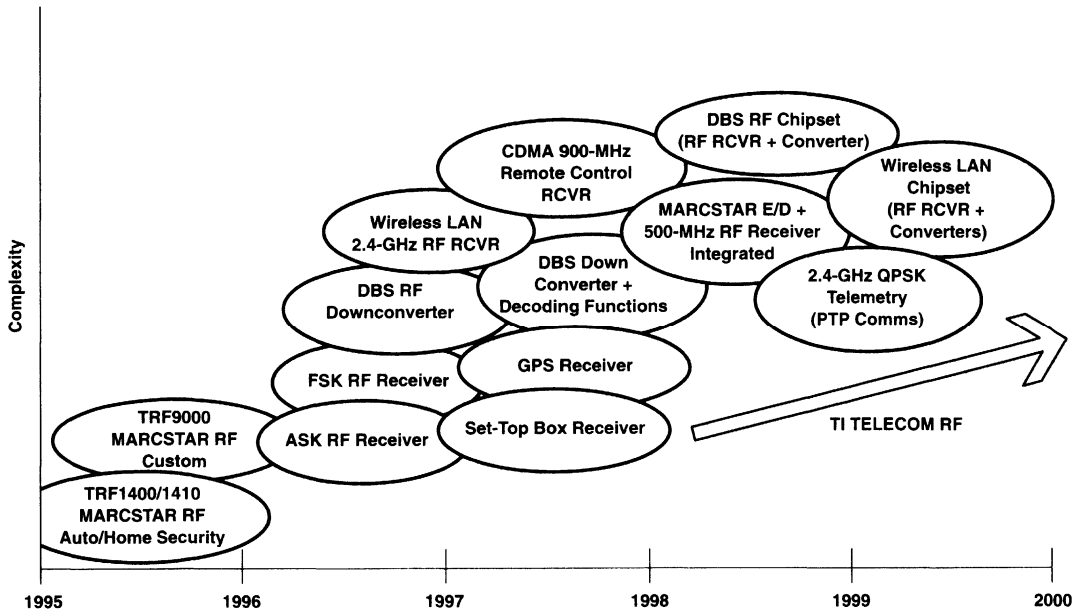
DESCRIPTION	FUNCTION	TECHNOLOGY	SUPPLY VOLTAGE	PRODUCT FEATURES	DEVICE	PAGE
Line card suppressor	Dual transient voltage suppressor	Bipolar	−5 V to −65 V	Firing voltage: −70 V, Max peak surge current: 35 A	TCM1030	3–3
				Firing voltage: −70 V, Max peak surge current: 50 A	TCM1060	3–3

remote keyless entry and general telemetry receivers

DESCRIPTION	FUNCTION	TECHNOLOGY	SUPPLY VOLTAGE	PRODUCT FEATURES	DEVICE	PAGE
VHF/UHF ASK RZ receiver	Remote keyless Entry/General Telemetry	Submicron BiCMOS	5 V	200 Hz to 450 MHz high receiver sensitivity, 500 Hz to 20 KHz data rate, Internal amplifier comparator, No emissions, Infinite image rejection, No manual alignment, Internal Manchester decoder	TRF1400	4–3
VHF/UHF ASK RZ receiver	Remote keyless Entry/General Telemetry	Submicron BiCMOS	5 V	200 Hz to 450 MHz high receiver sensitivity, 500 Hz to 20 KHz data rate, Internal amplifier comparator, No emissions, Infinite image rejection, No manual alignment,	TRF1410	4–21



ADVANCED COMBO ROADMAP



MSP RF Thrust

Introduction

Texas Instruments portfolio of digital signal processor (DSP) solutions addresses the key technologies required to achieve success in today's fast-moving wireless communications market. To help OEMs gain a competitive edge, TI provides system solutions including components, software modules, development tools, demonstration platforms and global development support. Our customizable DSP (cDSP) capability can create highly-integrated, low-power, custom solutions fine-tuned for specific needs.

With worldwide manufacturing capacity and expertise, including high-yielding processes and tight parametric control, Texas Instruments can supply wireless communications OEMs with the large volumes they need to meet their production requirements. We continue to invest in manufacturing capacity to keep pace with our customers' growing needs.

The devices in this databook support the world's most widely adopted standards in analog cellular, digital and dual-mode cellular, personal communications services (PCS), digital cordless telephones, paging, wireless local loop systems, wireless data, and more. The product families addressed in this databook include:

- Baseband Processors for Analog Cellular Handsets
- Voice-Band Audio Processors (VBAP™)
- Radio Frequency (RF) Products For Personal Communcations
- Baseband Interface Circuits
- ASICs
- DSPs
- Microcontrollers
- System Solutions
- Data Converters
- Operational Amplifiers
- Low Drop-Out Regulators
- Power Management Products

The alphanumeric index in this data book provides a means of quickly locating the device type. The selection guide includes a brief description of each device and references to additional literature items about that product family. The glossary describes the symbols, terms, and definitions used in this data book.

Additional literature is available from your nearest Texas Instruments Field Sales Office, local authorized TI distributor, or by writing directly to:

Texas Instruments Incorporated
LITERATURE RESPONSE CENTER
P.O. BOX 809066
Dallas, TX 75380-9066

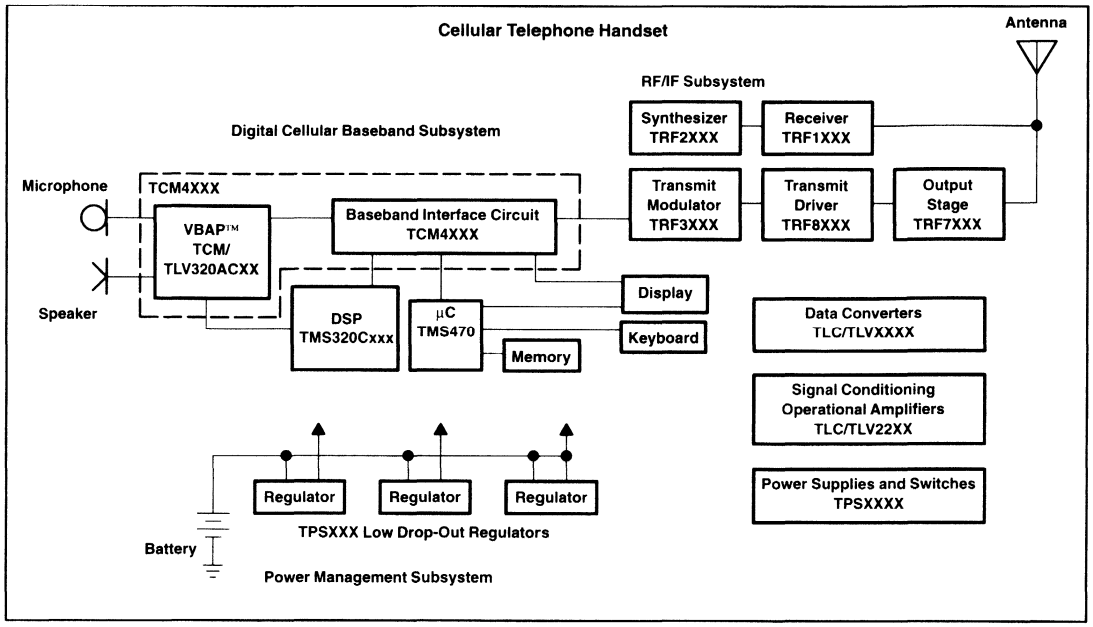
A list of TI sales offices, distributors, and technology centers is located in the back of this book.

In addition, the latest information on wireless communications products is available on the Internet. Visit the TI Wireless Communications home page at http://www.ti.com/sc/docs/wireless/home.htm, or access the full range of TI's Semiconductor products using the TI home page at http://www.ti.com.

Thank you for your interest in wireless personal communications products from Texas Instruments.

VBAP is a trademark of Texas Instruments Incorporated.

selection guide



baseband processors for analog cellular handsets

VOICE PROCESSOR	PAGE	DATA PROCESSOR	SUPPLY VOLTAGE	PAGE
TCM8002	5–3	TCM8010–50	5 V	5–53
		TCM8010–37	3.7 V	5–25
Voice and Data Processor				
TCM8030†			2.7–5.5 V	5–59

† Product Preview

NOTE 1: TCM8000 is obsolete — replace with TCM8010-50 or TCM8010-37.

VBAP™ voice-band audio processor (voice codecs for wireless personal communications)

PRIMARY APPLICATION	13-BIT LINEAR MODE AND μ-LAW	13-BIT LINEAR MODE AND A-LAW	MASTER CLK (MHZ)	SUPPLY	PAGE
IS–19, IS–54/136 and digital cordless	TLV320AC36	TLV320AC37	2.048	3 V	6–63
IS–19, IS–54/136 and digital cordless, noise cancellation disabled	TLV320AC56†	TLV320AC57†	2.048	3 V	6–103
DECT	TLV320AC40†	TLV320AC41†	1.152	3 V	6–83
IS–19, IS–54/136 and digital cordless, noise cancellation disabled	TCM320AC56†	TCM320AC57†	2.048	5 V	6–103
Reduced spec 'AC36	TCM320AC46‡	N/A	2.048	5 V	–
GSM	TCM320AC38	TCM320AC39	2.600	5 V	6–23
IS–19, IS–54/136 and digital cordless	TCM320AC36	TCM320AC37	2.048	5 V	6–3

† Product Preview data
‡ TCM320AC46 is obsolete — replace with TCM320AC36.

additional VBAP literature

	LIT. NO.
Voice-Band Audio Processors Application Report	SLWA001

radio frequency products for wireless personal communications

PRIMARY APPLICATION	FUNCTION	DEVICE	SUPPLY VOLTAGE	PAGE
900 MHz: Analog, Digital, Dual Mode Cellular; Digital Cordless	Receiver front end	TRF1015†	3.5–5.5 V	7–3
900 MHz–1.9 GHz: Analog, Digital, Dual Mode Cellular; PCS	Fractional-N / Integer-N Synthesizer	TRF2040†	2.7–3.6 V	7–13
1.1 GHz: IS–54/IS–136	Fractional–N / Integer-N Synthesizer	TRF2050†	2.7–5.1 V	7–25
900 MHz: Analog, Digital, Dual Mode Cellular; PCS	I/Q and FM Modulator	TRF3020†	3.6–3.9 V	7–37
900 MHz–1.9 GHz: Analog, Digital, Dual Mode Cellular; PCS	GaAs MESFET Output Stage	TRF7000†	3.6 V AMPS 4.8 V GSM/IS–54/IS–136	7–47
900 MHz: Analog, Digital, Dual Mode Cellular	Driver Amplifier	TRF8010†	3.6 V AMPS 4.8 V GSM/IS–54/IS–136	7–57
Analog, Digital, Dual Mode Cellular; PCS	Power Supply for GaAs Power Amplifiers	TPS9103†	2.7–5.5 V	7–65

† Product Preview data

baseband interface circuits for wireless personal communications

PRIMARY APPLICATION	VOICE CODEC	PAGE	RF CODEC	PAGE
IS–54B	TCM320AC36 or TLV320AC36	6–3 6–63	TCM4300†	8–3
IS–136	TCM320AC36 or TLV320AC36	6–3 6–63	TCM4301†	8–51
GSM	TCM4400†			8–113

† Product Preview data

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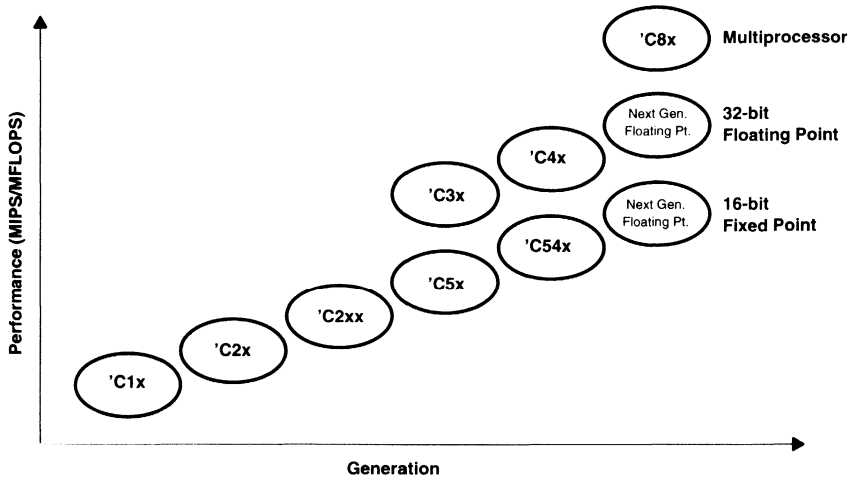
digital signal processors

DSP standard device family roadmap



general DSP literature

		LIT. NO.
	DSP Solutions Selection Guide	SSDV004
TMS320	DSP Production Overview (Flipbook)	SPRZ094C
TMS320	DSP Brochure	SPRB113
TMS320	Revised Software Co-op Data Sheet Package	SPRT111B
TMS320	Development Support Brochure	SPRT096B
TMS320	Development Support Reference Guide	SPRU011D
TMS320	Third Party Support Guide	SPRU052C

TMS320C2xx family

		PAGE
TMS320C203/209	Data Sheet	9–3

TMS320C2xx product specification guide

DEVICE	RAM	(Words) ROM	FLASH	SER	INSTRUCTION CYCLE (ns)	MIPS	PACKAGING
TMS320C203-80	544	Boot	-	2	25	40	100 TQFP
TMS320C204-80	544	4K	-	2	35	40	100 TQFP
TMS320C205-80	4.5	Boot	-	2	25	40	100 TQFP
TMS320C209-57	4.5	4K	-	-	35	28.5	80 TQFP
TMS320F206-80	4.5	4K	32K	2	25	40	100 TQFP
TMS320F207-80	4.5	4K	32K	3	25	40	144 TQFP

NOTE 1: All devices: data/program space = 64kB/64kB, DMA = external, timers = 1, parallel port = 64K x 16.

TMS320C2xx additional literature

		LIT. NO.
'C2XX	User's Guide	SPRU127A
'C2XX	Product Bulletin	SPRT122A

TMS320C5x family

		PAGE
TMS320C5x	Data Sheet	9–67

TMS320C5x product specification guide

DEVICE	RAM	(Words) ROM	SER	COM	INSTRUCTION CYCLE (ns)	MIPS	PACKAGING
TMS320C50-57 †‡	10K	Boot	2	-	35	28.57	132 PQFP
TMS320C50-80 §	10K	Boot	2	-	25	40	132 PQFP
TMS320C51-57 †‡	2K	8K	2	-	35	28.57	132 PQFP 100 TQFP
TMS320C51-100 ‡	2K	8K	2	-	20	50	132 PQFP 100 TQFP
TMS320C52-57 †‡	1K	4K	1	-	35	28.57	100 PQFP 100 TQFP
TMS320C52-80	1K	4K	1	-	25	40	100 PQFP 100 TQFP
TMS320C52-100 ‡	1K	4K	1	-	20	50	100 PQFP 100 TQFP
TMS320C53-80	4K	16K	2	-	25	40	100 PQFP
TMS320C53S57 †‡	4K	16K	2	-	35	28.57	100 TQFP
TMS320C53S80	4K	16K	2	-	25	40	100 TQFP
TMS320LBC56-80	7K	32K	2§	-	25	40	100 TQFP
TMS320LBC57-80	7K	32K	2§	HPI	25	40	128 TQFP
TMS320BC57S-80	7K	Boot	2§	HPI	25	40	144 TQFP

† Extended temperature version available
‡ 3.3 V version available
§ Buffered serial port
NOTE 1: All devices: boot loader available, data/program space = 64kB/16kB, DMA = external, timers = 1, parallel port = 64K x 16.

TMS320C5x additional literature

		LIT. NO.
TMS320C5x	User's Guide	SPRU056B
TMS320C5x	Fixed-Point DSP Production Bulletin	SPRT119A
'C5x	Power Dissipation Application Report	SPRA030
'C5x	DSP Seminar Workbook	SPRW017
'C5x	Telecommunications Appliations With 'C5x	SPRA033
'C5x	On-chip Oscillator With External Resonator	SPRA054

TMS320C54x family

		PAGE
TMS320C54x†	Data Sheet	9–67

† Advance Information data

TMS320C54x product specification guide

Device	DAT/PRO	SER	COM	INSTRUCTION CYCLE (ns)	MIPS	PACKAGING
TMS320C541#-40	64K/64K	2	-	25	40	100 TQFP
TMS320C542#-40	64K/64K	2†‡	HPI	25	40	128, 144 TQFP
TMS320LC541#-50	64K/64K	2	-	20	50	100 TQFP
TMS320LC542#-50	64K/64K	2†‡	HPI	20	50	128, 144 TQFP
TMS320LC543#-50	64K/64K	2†‡	-	20	50	100 TQFP
TMS320LC545#-66	64K/64K	2†	HPI	15	66	128 TQFP
TMS320LC546#-66	64K/64K	2†	-	15	66	100 TQFP
TMS320LC548#-66	4M/64K	3†‡	HPI	15	66	144 TQFP
TMS320VC541#-50	64K/64K	2	-	20	50	100 TQFP
TMS320VC542#-50	64K/64K	2†‡	HPI	20	50	128, 144 TQFP
TMS320VC543#-50	64K/64K	2†‡	-	20	50	100 TQFP
TMS320VC545#-50	64K/64K	2†	HPI	20	50	128 TQFP
TMS320VC546#-50	64K/64K	2†	-	20	50	100 TQFP
TMS320VC548#-50	4M/64K	3†‡	HPI	20	50	144 TQFP

† Buffered serial port (C548 has 2)
‡ 1 TDM serial port
NOTES: 2. All devices: bootloader avaliable, DMA =external, timers = 1, parellel port = 64K x 16, DAT/PRO = data/program space, # = 1 for PLL option 1 or # = 2 PLL for option 2 (see User's Guide for details), LC = 3.3 V, VC = 3 V part

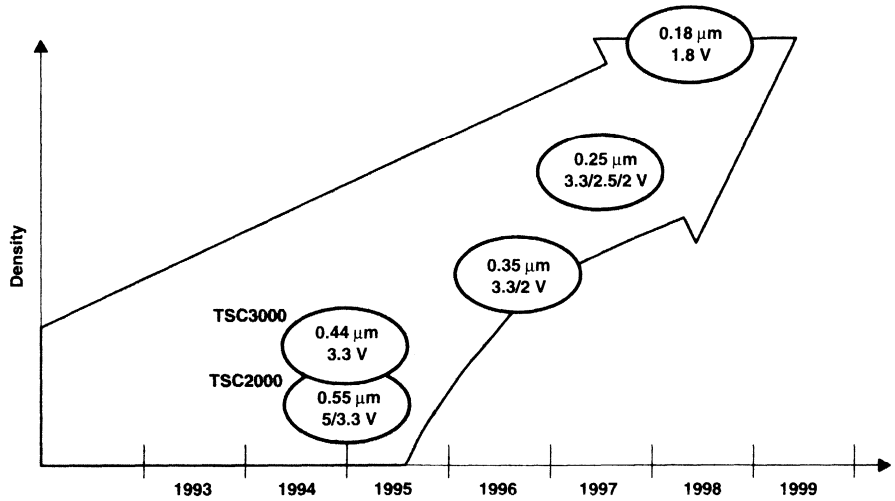
TMS320C54x additional literature

		LIT. NO.
TMS320C54x	Product Bulletin	SPRT121A
TMS320C54x	User's Guide	SPRU131
'C54x	Serial Ports User's Guide Addendum	SPRU156
'C54x	Source Debugger User's Guide	SPRU099A
'C54x	Assembly Language Tools User's Guide	SPRU102A

custom digital baseband solutions

To allow for higher integration levels and to further reduce chip count, power dissipation, and system cost, TI offers the capability to create a custom device around DSP and microcontroller cores. TI's customizable DSP (cDSP) and customizable microcontroller (c470) technologies allow the single-chip integration of the DSP cores with the TMS470 microcontroller core, additional memory, peripherals, logic gates, and analog modules in the ASIC backplane.

ASIC standard cell — family roadmap



Currently, TI is developing the TSC4000 and TSC5000 standard cell ASIC product familes that are optimized for ultra-low power and highly integrated applications. Designers in the wireless market can take full advantage of the low power consumption for extended battery life, high density capability to integrate complex functions, high performance for multiple applications, and leading design tools capabilities that reduce overall design cycle-time.

additional ASIC literature:

DEVICE	STANDARD CELL LITERATURE	LIT. NO.
TSC2000 5-V	Product Information	SRST001
TSC3000 3.3-V	Product Information	SRST002
TSC2000LV 3.3-V	Product Information	SRST003

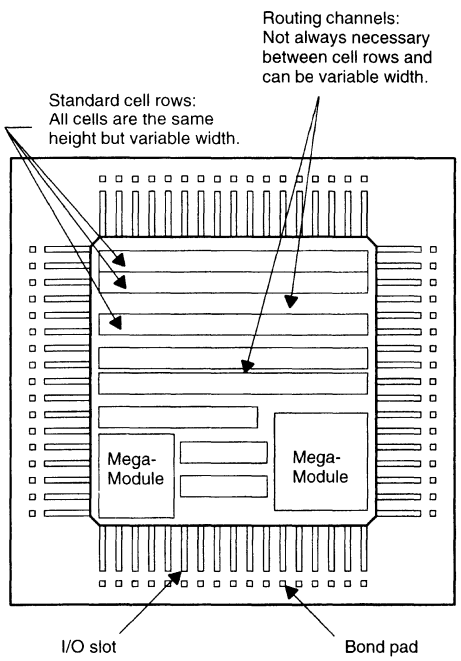
additional microcontroller literature:

DEVICE	MCU LITERATURE	LIT. NO.
TMS470R1X	User's Guide	SPNU134A

TSC2000
5-V 0.55-μm CMOS Standard Cell
Product Information

Overview

- 5-V, 0.55-μm L_{eff}, Triple-Level Metal (TLM) Process
- Core Cell Library Optimized for Synthesis and Low Power
- Digital Signal Processor Cores
- Clock Tree Synthesis
- Support for Synopsys™ DesignPower
- Batch and Graphics Mode Floorplanner
- Third-Party CAD Signoff
- Datapath Function Generation with Interface to Synopsys Through DesignWare™
- Memory Compilers Including Single-Port, Two-Port, Dual-Port, and ROM
- TTL, CMOS, SCSI-20, ATA-2, Ultra-Low-Power and, Ultra-Low-Noise I/Os
- QFP and TQFP Packaging
- 1-μW/MHz/Gate Typical Power Dissipation
- Typical Gate Delays of 165 ps (2-Input NAND, FO = 2)



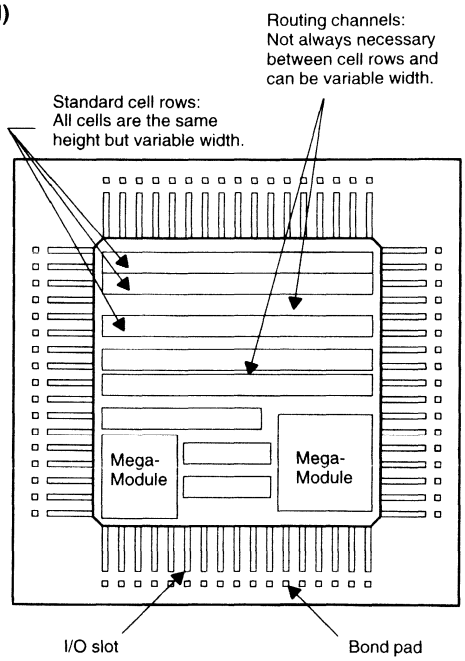
Features and Benefits

FEATURES	BENEFITS
Robust support for leading CAD tools	Third-party CAD signoff
Synthesis-optimized cell library	High-density synthesis results and lower power
Tight coupling between synthesis, floorplanning, and layout	Shorter design cycle time
Support for Synopsys Design Power	Accurate power analysis
Ultra low noise I/Os	Reduced power pin requirements and lower system noise
Ultra low power I/Os	Low power system solutions
Low power cells	Low power system solutions
Clock tree synthesis	Insertion delay and skew management. Low power clock distribution. Support for high number of clocks.
Datapath synthesis	Efficient implementation of datapath logic
Analog cells	System integration
SCSI Fast-20, ATA-2 I/Os	Direct interface to SCSI/ATA-buses

TSC2000LV
3.3-V 0.55-μm CMOS Standard Cell
Product Information

Overview

- **3.3-V, 0.55-μm L_{eff}, Triple-Level Metal (TLM) Process**
- **Core Cell Library Optimized for Synthesis and Low Power**
- **Analog Functions**
- **Clock-Tree Synthesis**
- **Support for Synopsys™ DesignPower™**
- **Batch and Graphics Mode Floorplanner**
- **Third-Party CAD Signoff**
- **Datapath Function Generation with Interface to Synopsys Through DesignWare™**
- **Memory Compilers Including Single-Port, Two-Port, Dual-Port, and ROM**
- **TTL, LVCMOS, Ultra-Low-Power, and Ultra-Low-Noise I/Os**
- **QFP and TQFP Packaging**
- **0.42-μW/MHz/Gate Typical Power Dissipation**
- **Typical Gate Delays of 210 ps (2-Input NAND, FO = 2)**



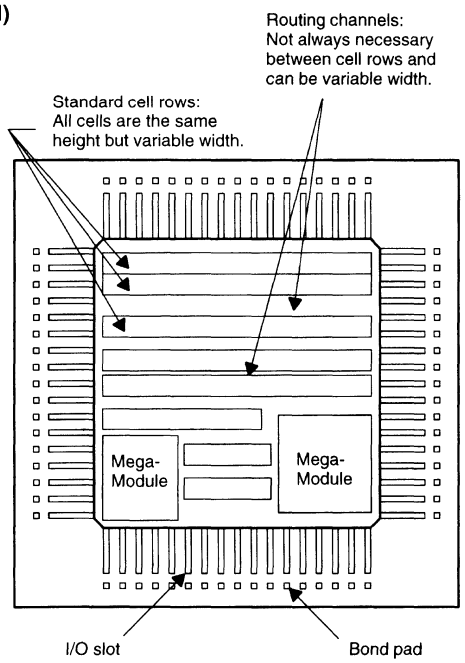
Features and Benefits

FEATURES	BENEFITS
Robust support for leading CAD tools	Third-party CAD signoff
Tight coupling between synthesis, floorplanning, and layout	Shorter design cycle time
Support for Synopsys DesignPower	Accurate power analysis
Ultra-low-noise I/Os	Reduced power pin requirements and lower system noise
Ultra-low-power I/Os	Low-power system solutions
Low-power cells	Low-power system solutions
Clock tree synthesis	Insertion delay and skew management. Low-power clock distribution. Support for high number of clocks.
Datapath synthesis	Efficient implementation of datapath logic
Analog cells	System integration
Level-shifting I/Os	Interface from 3-V core to 5-V signaling environment
Synthesis-optimized library	High-density synthesis results and lower power

TSC3000
3.3-V 0.44-μm CMOS Standard Cell
Product Information

Overview

- **3.3-V, 0.44-μm L_{eff}, Triple-Level Metal (TLM) Process**
- **Core Cell Library Optimized for Synthesis and Low Power**
- **Digital Signal Processor and Microcontroller Cores**
- **Clock-Tree Synthesis**
- **Support for Synopsys™ DesignPower™**
- **Batch and Graphics Mode Floorplanner**
- **Third-Party CAD Signoff**
- **Datapath Function Generation with Interface to Synopsys Through DesignWare™**
- **Memory Compilers Including Single-Port, Two-Port, and Dual-Port**
- **TTL, LVCMOS, 5-V-Tolerant, Ultra-Low-Power, Ultra-Low-Noise I/Os**
- **QFP and TQFP Packaging**
- **0.33-μW/MHz/Gate Typical Power Dissipation**
- **Typical Gate Delays of 120 ps (2-Input NAND, FO = 2)**
- **Tight Max/Min Performance Ratio (2:1 Commercial Conditions)**



Features and Benefits

FEATURES	BENEFITS
Robust support for leading CAD tools	Third-party CAD signoff
Tight coupling between synthesis, floorplanning, and layout	Shorter design cycle time
Support for Synopsys Design Power	Accurate power analysis
Ultra-low-noise I/Os	Reduced power pin requirements and lower system noise
Ultra-low-power I/Os	Low-power system solutions
Low-power cells	Low-power system solutions
Clock-tree synthesis	Insertion delay and skew management. Low-power clock distribution. Support for high number of clocks.
Datapath synthesis	Efficient implementation of datapath logic
5-volt–tolerant cells	Interface to external 5-V logic
Tight min/max performance window due to advanced manufacturing capability	Eases chip and system-level timing issues due to delay spread

operational amplifiers

DEVICE	V_{IO} mV (max)	α_{VIO} µV/°C (typ)	I_{CC} mA (max)	I_{IB} nA (typ)	CMRR dB (typ)	V_n (1 kHz) nV/√Hz (typ)	SR V/µs (typ)	GBW MHz (typ)	TEMP† RANGE	DESCRIPTION
TLC2252A	0.85	0.5	0.063	0.001	83	19	0.12	0.2	I, M	Dual, low power, rail-to-rail output, low noise
TLC2254A	0.85	0.5	0.063	0.001	83	19	0.12	0.2	I, M	Quad, low power, rail-to-rail output, low noise
TLV2252A	0.85	0.5	0.063	0.001	83	19	0.12	0.2	I, M	Dual, low voltage, rail-to-rail output, low noise
TLV2254A	0.85	0.5	0.063	0.001	77	19	0.12	0.2	I, M	Quad, low voltage, rail-to-rail output, low noise
TLC2262	2.5	2	0.25	0.001	80	12	0.55	0.82	C, I	Dual, low power, rail-to-rail output, low noise
TLC2262A	0.95	2	0.25	0.001	80	12	0.55	0.82	C, I	Dual, precision, low power, rail-to-rail output
TLC2264	2.5	2	0.25	0.001	80	12	0.55	0.82	C, I	Quad, low power, rail-to-rail output, low noise
TLC2264A	0.95	2	0.25	0.001	80	12	0.55	0.82	I	Quad, low power, rail-to-rail output, low noise
TLC2272	2.5	2	3	0.001	75	9	3.6	2.18	C, I, M	Dual, rail-to-rail output
TLC2272A	0.95	2	3	0.001	75	9	3.6	2.18	C, I, M	Dual, rail-to-rail output, precision
TLC2274	2.5	2	3	0.001	75	9	3.6	2.18	C, I, M	Quad, rail-to-rail output
TLC2274A	0.95	2	3	0.001	75	9	3.6	2.18	C, I, M	Quad, rail-to-rail output, precision
TLV2262	2.5	2	0.25	0.001	80	12	0.55	0.82	I	Dual, precision, low voltage, low power, rail to rail
TLV2262A	0.95	2	0.25	0.001	80	12	0.55	0.82	I	Dual, precision, low voltage, low power, rail to rail
TLV2264	2.5	2	0.25	0.001	80	12	0.55	0.82	I	Quad, precision, low voltage, low power, rail to rail
TLV2264A	0.95	2	0.25	0.001	80	12	0.55	0.82	I	Quad, precision, low voltage, low power, rail to rail

† C = 0°C to 70°C, I = −40°C to 85°C, M = −55°C to 125°C

fixed output voltage series pass regulators

DEVICE	V_O (V) NOM	I_O (mA) MAX	TOL (%)	I_q (mA) TYP	V_{DO} (V) TYP–MAX	$V_I$max (V)	LDO	SHUT DOWN	SVS†	T_A	DESCRIPTION
POSITIVE OUTPUT VOLTAGE											
TPS7233	3.3	250	2	155 µA	0.14 – 0.18	10	X	X		−40°C to 125°C	Very low dropout PMOS
TPS7333		500	2	340 µA	0.044 – 0.06	10	X	X	X	−40°C to 125°C	Lowest dropout PMOS with SVS†
TPS7133			2	285 µA	0.047 – 0.060	10	X	X		−40°C to 125°C	Lowest droput PMOS
TPS7248	4.85	250	2	155 µA	0.09 – 0.1	10	X	X		−40°C to 125°C	Very low dropout PMOS
TPS7348		500	2	340 µA	0.028 – 0.037	10	X	X	X	−40°C to 125°C	Lowest dropout PMOS with SVS†
TPS7148			2	285 µA	0.03 – 0.037	10	X	X		−40°C to 125°C	Lowest dropout PMOS
TPS7250	5	250	2	155 µA	0.76 – 0.85	10	X	X		−40°C to 125°C	Very low dropout PMOS
TPS7350		500	2	340 µA	0.27 – 0.035	10	X	X	X	−40°C to 125°C	Lowest dropout PMOS with SVS†
TPS7150			2	285 µA	0.27 – 0.033	10	X	X		−40°C to 125°C	Lowest dropout PMOS

† Supply-voltage supervisor

adjustable series pass regulators

DEVICE	V_O (V) MIN–MAX	I_O (mA) MAX	TOL (%)	I_q (mA) TYP	V_{DO} (V) TYP–MAX	$V_I$max (V)	LDO	SHUT DOWN	SVS†	T_A	DESCRIPTION
TPS7201	1.2 – 9.75	250	3	155 µA	0.16–0.27	10	X	X		–40°C to 125°C	Very low dropout PMOS adjustable
TPS7301	1.2 – 9.75	250	3	340 µA	0.052–0.085	10	X	X	X	–40°C to 125°C	Lowest dropout PMOS with SVS†
TPS7101	1.2 – 9.75	500	3	285 µA	0.052–0.085	10	X	X		–40°C to 125°C	Lowest dropout PMOS adjustable

† Supply-voltage supervisor

supply voltage supervisors

DEVICE	V_t (V)	TOL (%)	I_{CC} (mA) MAX	V_I min (V)	PROGRAMMABLE TIME DELAY	COMPLEMENTARY OUTPUTS	DESCRIPTION
TLC7705	4.55	1.5	25 µA	1	X	X	Single micropower SVS (5 V) with programmable time delay and push-pull outputs
TL7705A	4.55	2	3	3.60	X	X	Single SVS for 5 V systems with programmable time delay
TL7705B	4.55	2	3	1	X	X	Single SVS for 5 V systems with programmable time delay

p-channel MOSFETs

DEVICE	V_{DS} (V)	$r_{DS(on)}$ (V_{GS} = –10 V) Ω	$r_{DS(ON)}$ V_{GES} = –10 V) Ω	$r_{DS(ON)}$ V_{GES} = –2.7 V) Ω	ID (A)	DESCRIPTION
	MAX	TYP	TYP	TYP	MAX	
TPS1100	–15	0.18	0.291	0.606	+1.58	Single p-channel enhancement-mode MOSFET
TPS1101	–15	0.09	0.134	0.232	±2.12	Single p-channel enhancement-mode MOSFET
TPS1110	–7	–	0.065	0.100	–6	Single p-channel enhancement-mode MOSFET
TPS1120	–15	0.18	0.291	0.606	±1.7	Dual p-channel enhancement-mode MOSFET

additional Mixed Signal Products literature:

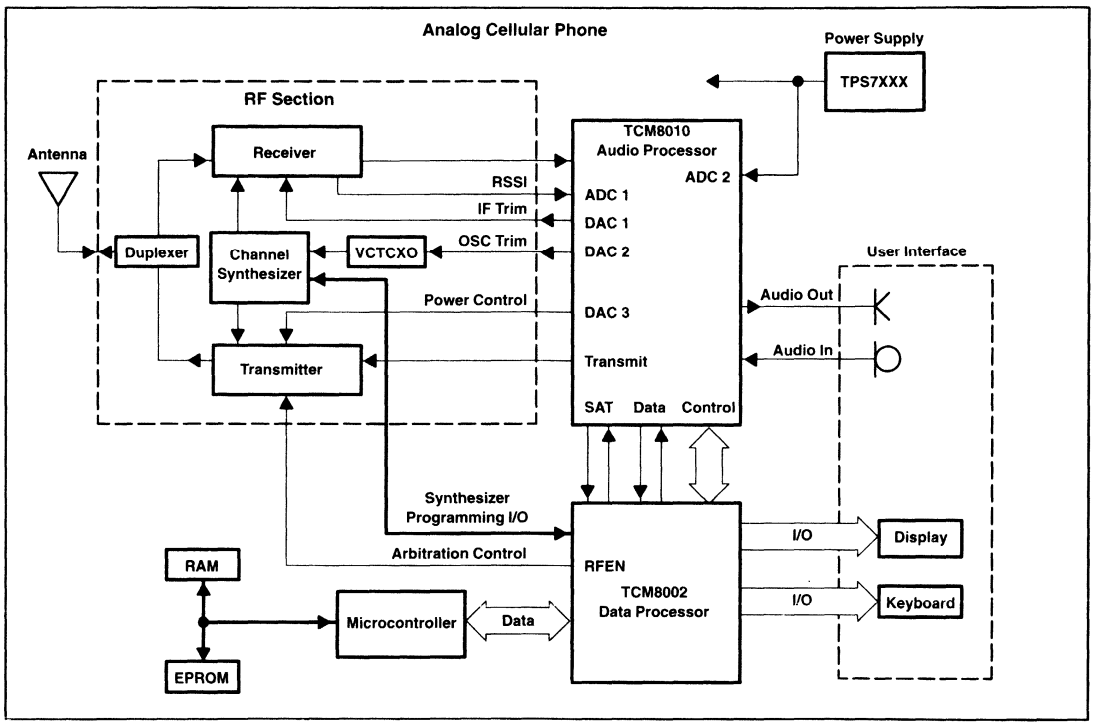
	LIT. NO.
1996 Designer's Guide and Reference	SLYU001
Data Converter Selection Guide	SLAT079
Data Acquistion Data Book	SLAD001
Understand Data Converters Application Report	SLAA013
Supplement to the Linear Circuits 3-V Family	SLYD013
Power Supply Circuits	SLYD002
Operational Amplifiers and Comparators, Volume A	SLVD011
Operational Amplifiers and Comparators, Volume B	SLYD012

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PRODUCT BRIEF LIT. NO. SSTT001

TCM8010/TCM8002

Analog Cellular System Solutions Product Brief



Introduction

TI's analog cellular solution consists of the TCM8010 audio processor and the TCM8002 data processor. Together they comprise a highly integrated baseband system for Advanced Mobile Phone Service (AMPS) and Total Access Communication System (TACS) cellular phones.

Benefits

The optimized architecture reduces the material cost of the phone and minimizes the power consumption in standby mode. Digital trimming significantly reduces the test time and manufacturing cost of a phone, ensuring a competitive, low-cost phone design for the worldwide consumer cellular phone market. Since the TCM8002 implements the required data processing, microcontroller software development is kept to a minimum. The system operates from either a 5-V supply (TCM8010-50) or a 3.7-V supply (TCM8010-37) and needs only one crystal or an external clock for operation.

Chipset Features

TCM8010 audio processor

- An on-chip compander to provide a high-quality voice transmission.
- Two integrated input amplifiers allow handset or hands free operation.
- On-chip DTMF generator provides 16 tones, programmable for level adjustments.
- Two integrated ADCs are used to monitor the RSSI level and battery voltage.

- Three DACs are used to control the transmit output power, to trim the VCTCXO and to adjust the response of the first IF stage.

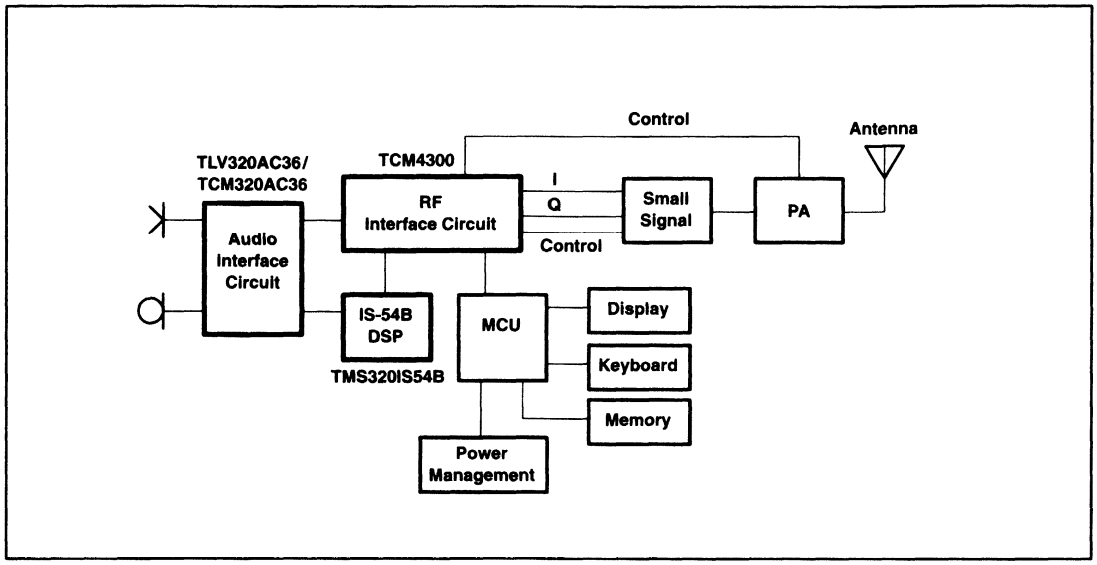
A total of 12 events are microcontroller-interrupt Programmable. The 4-wire serial interface minimizes the number of microcontroller pins required. Programmable 20-pin I/O expansion capabilities provide system support to the keyboard, display, and the RF section.

An on-chip watchdog timer fulfills the requirement of the AMPS/TACS standard for a microcontroller-independent watchdog.

PRODUCT BRIEF LIT. NO. SSTT005

IS-54B

Dual-Mode Cellular Solutions Product Brief



Introduction

The IS-54B technology from Texas Instruments provides a single-DSP baseband solution for the IS-54B standard. With its high level of integration, the solution reduces device count, saves space, and simplifies design, allowing users to design a competitive product with a fast time-to-market. By supporting the IS-54B dual-mode standard, this solution allows seamless integration into the emerging digital cellular telephone market.

The IS-54B solution from TI consists of the IS-54B DSP, a 16-bit fixed-point product from TI's leading family of DSPs; the TCM4300 Advanced RF Cellular Telephone Interface Circuit (ARCTIC™), a high-performance mixed-signal device; and the TLV320AC36 or TCM320AC36 Voice-Band Audio Processor (VBAP™), an audio CODEC manufactured using TI's low-power LinCMOS™ technology.

Benefits

Some of the key benefits you can expect by using the Texas Instruments IS-54B solution include

- Full compliance with the IS-54B dual-mode standard
- Optimized software for complete baseband operations
- Minimized overall system cost
- Flexible microcontroller and RF interfaces
- Bit-error-rate performance exceeding IS-54/IS-55 requirements
- VSELP segmented signal-to-noise-ratio (SNR) performance exceeding IS-85 requirements
- TQFP and SQFP packaging

ARCTIC, VBAP, and LinCMOS are trademarks of Texas Instruments Incorporated.

PRODUCT BRIEF LIT. NO. SSTT005

Features

TI's IS-54B solution simplifies dual-mode cellular design by providing a flexible interface to the microcontrollers and RF designs most commonly used in cellular phones. In addition, our product contains drivers for both the speaker and microphone; no additional buffers or drivers are needed. A 3.3-V power supply and advanced power management techniques allow your products to use smaller, lighter batteries and have longer operating times.

TMS320IS54B DSP:

- FM voice transmission and reception for analog mode operation
- Synchronization and timing control of the chipset in digital mode
- $\pi/4$ DQPSK decoding and demodulation for digital operation
- Channel coding/decoding and interleaving
- VSELP voice coding/decoding
- Robust channel equalization

TCM4300 Advanced RF Cellular Telephone Interface Circuit:

- Single-chip interface to DSP, micro-controller and RF modulator/demodulator in a dual-mode IS-54B cellular telephone
- Performs $\pi/4$ differential quadrature phase-shift keying ($\pi/4$-DQPSK) symbol modulation
- In analog mode, provides all base-band filtering and transmit D/A conversion and receive A/D conversion
- Integrated wide-band data (WBD) demodulator provides DSP power saving in analog mode
- Advanced power control minimizes power consumption of many dual-mode functional blocks
- 3.3 V or 5 V single supply operation

TCM320AC36/TLV320AC36 Auido Interface Circuit:

- Single chip audio PCM CODEC that provides all the filtering and frame sync timing necessary for a standard voice channel
- Standard serial interface to a TMS320 or any other standard DSP
- Transmit and receive directions can be operated independently
- Simple microphone and speaker interfaces
- Operates from a single 5 V (TCM320AC36) or 3 V (TLV320AC36) supply

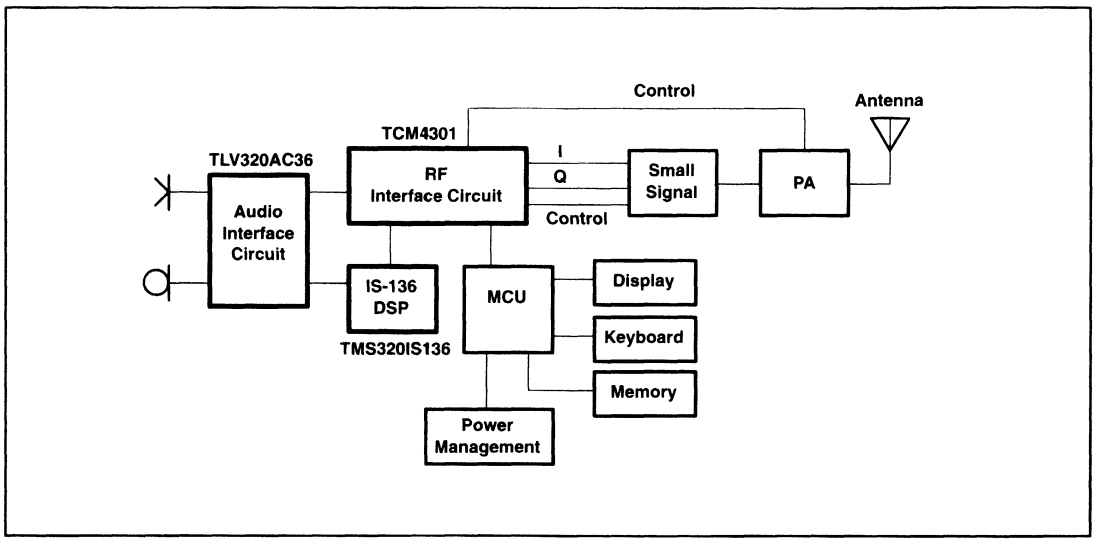
Systems Support

In addition, Texas Instruments has development platforms (which include baseband, microcontroller and RF subsystems for prototype and system testing) and thorough documentation to support you with your digital cellular design.

PRODUCT BRIEF LIT. NO. SSTT003

IS-136

Dual-Mode Cellular / PCS Solutions Product Brief



Introduction

The IS-136 technology from Texas Instruments provides a single-DSP baseband solution for the IS-136 standard. With its high level of integration, the solution reduces device count, saves space, and simplifies design, giving you a competitive product with a fast time-to-market. By supporting the IS-136 dual-mode standard, this solution allows seamless integration into the emerging digital cellular telephone market.

The IS-136 solution from TI consists of an IS-136 DSP, a 16-bit fixed-point product based on TI's leading family of DSPs; TCM4301 (ARCTIC™-136) RF Interface Circuit, a high-performance mixed-signal device; and the TLV320AC36 Voice-Band Audio Processor, (VBAP™) an audio codec manufactured using TI's low-power LinCMOS™ technology.

Benefits

Some of the benefits you can expect by using TI's IS-136 solution include:

- Full compliance with the TIA IS-136 dual-mode cellular standard for North America
- Optimized software for complete baseband operations
- Minimized overall system cost
- Flexible microcontroller and RF interfaces
- Bit-error-rate exceeding IS-136/IS-137 requirements
- VSELP segmented signal-to-noise ratio (SNR) performance exceeding IS-85 requirements
- TQFP and SQFP packaging

Features

TI's IS-136 solution simplifies dual-mode cellular design by providing a flexible interface to the microcontrollers and RF designs most commonly used in cellular phones. In addition, our product contains drivers for both the speaker and microphone; no additional buffers or drivers are needed. A 3.3-V power supply and advanced

power management techniques allow your products to use smaller, lighter batteries and have longer operating times.

TMS320CIS136 DSP:

- Digital control channel encoding and decoding for IS-136 operation as well as search and channel type determination
- FM voice transmission and reception for analog mode operation
- Control and voice channel processing
- Synchronization and timing control of the chipset in digital mode
- $\pi/4$ DQPSK decoding and demodulation for digital operation
- Channel coding/decoding and interleaving
- VSELP voice coding/decoding
- Robust channel equalization

TCM4301 (ARCTIC™-136) RF Interface Circuit:

- Single-chip interface to DSP, microcontroller and RF modulator/demodulator in a dual-mode IS-136 cellular telephone
- Performs $\pi/4$ differential quadrature phase-shift keying ($\pi/4$-DQPSK) symbol modulation
- Sleep mode timer allows the phone to utilize power saving modes of IS-136 paging classes
- In analog mode, provides all baseband filtering and transmit D/A conversion and receive A/D conversion
- Integrated wide-band data (WBD) demodulator provides DSP power savings in analog mode
- Advanced power control minimizes power consumption of many dual-mode functional blocks
- 3.3 V single supply operation

TLV320AC36 Audio Interface Circuit:

- Single chip audio PCM CODEC that provides all the filtering and frame sync timing necessary for a standard voice channel
- Standard serial interface to a TMS320 or any other standard DSP
- Transmit and receive directions can be operated independently
- Simple microphone and speaker interfaces
- Operates from a single 3 V supply

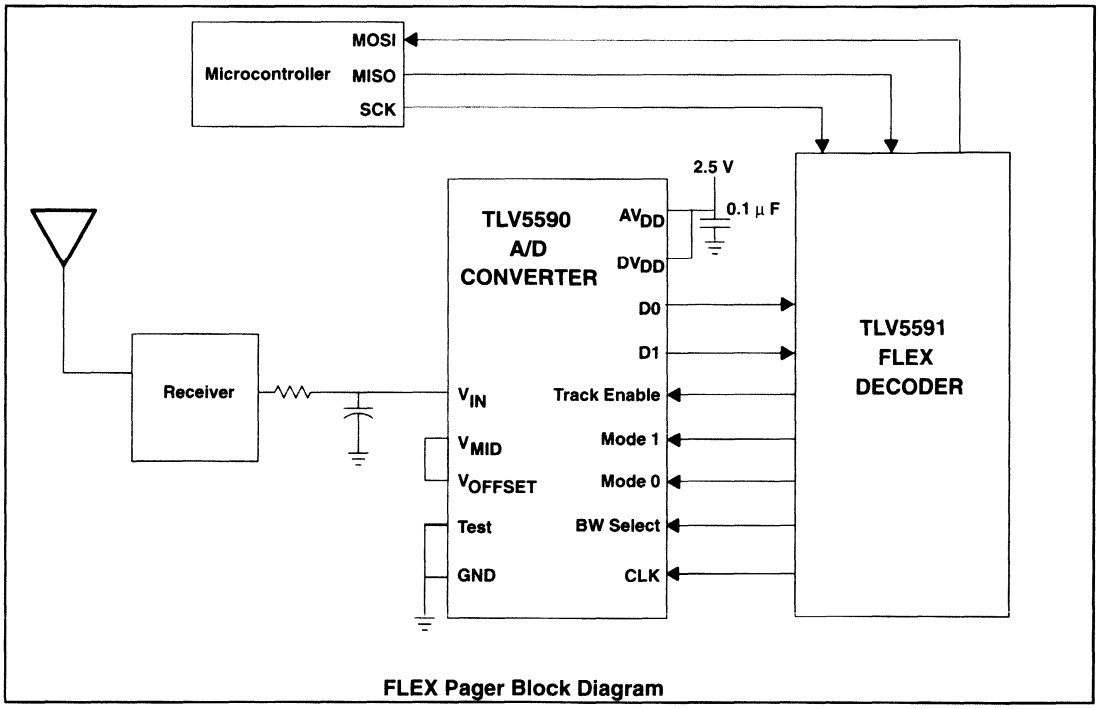
Systems Support

In addition, Texas Instruments has development platforms (which include baseband, microcontroller and RF subsystems for prototype and system testing) and thorough documentation to support you with your digital cellular design.

PRODUCT BRIEF LIT. NO. SSTT004

TMS320FLEX

Chipset Product Brief



FLEX Pager Block Diagram

Introduction

The TMS320FLEX chipset from Texas Instruments allows OEMs in a variety of diverse industries to rapidly develop paging devices conforming with the FLEX™ paging protocol developed by Motorola Inc. In addition to providing a turnkey solution for FLEX pagers, the flexible architecture of the chipset lends itself to integration into equipment as varied as computers, automobiles, and smart home electronics. Embedded paging functionality can open a new realm of applications.

The '320FLEX chipset consists of the TLV5591, a signal processor that decodes the FLEX paging protocol transmission, and the TLV5590, which converts the analog signal from the receiver into a digital signal for decoding by the TLV5591.

Benefits

As paging has become more widely accepted, Motorola developed the FLEX advanced paging protocol to provide a robust form of text and data messaging not previously available with other protocols. Bringing new levels of functionality and service to pagers, the FLEX protocol delivers several key benefits to users:

- Longer battery life (up to 5x) than existing paging standards, enabling improvements in design and miniaturization because of the smaller batteries
- Support for numeric and alphanumeric messages

FLEX is a trademark of Motorola Incorporated.

- Increased signal integrity for error protection and positive message termination
- Advanced features, such as group pages between systems

Paging carriers also realize numerous advantages by converting to the FLEX protocol:

- Support for 1600-, 3200- or 6400-bps transmission
- Carriers can minimize their upgrade costs by migrating gradually from existing standards to FLEX 1600 to FLEX 3200 to FLEX 6400
- Significant increase in the number of subscribers per channel, consequently lowering infrastructure costs

With the substantial benefits of the FLEX protocol, demand for FLEX pagers has been growing steadily. FLEX has become the de facto high-speed paging-protocol standard as 70% of paging operators worldwide have adopted FLEX technology for their next-generation upgrades.

Features

TI's '320FLEX chipset simplifies implementation of the FLEX protocol in a paging application by interfacing directly with most popular off-the-shelf paging receivers and microcontrollers. Paging OEMs can quickly and easily develop a FLEX-compliant product by interfacing the TMS320FLEX chipset to their existing receivers and microcontrollers with virtually no hardware redesign.

To further simplify matters, purchase of the TMS320FLEX chipset satisfies all licensing requirements for the FLEX protocol. No separate license agreement with Motorola is necessary.

TLV5591 FLEX Decoder:

- 16 programmable user-address words
- 16 fixed-temporary addresses
- 1600, 3200, and 6400 bits-per-second decoding
- Any-phase decoding
- Uses standard serial peripheral interface (SPI) in slave mode
- Allows low current STOP mode operation of host processor
- Highly programmable receiver control
- Real-time clock time base
- FLEX fragmentation and group messaging support
- Real-time clock over-the-air update support
- Compatible with synthesized receivers
- Low battery indication (external detector)

TLV5590 A/D converter:

- Selectable dual-bandwidth audio filter
  - 3-pole Butterworth lowpass
  - BW 1 = 1 kHz ±5% (–3db)
  - BW 2 = 2 kHz ±5% (–3db)
- Peak and valley detectors
- Two-bit analog-to-digital converter
- Three modes of operation: fast acquisition, slow acquisition, and hold
- 2.5-V operation with single power supply

Systems Support

FLEX system software to facilitate application development is included with the TMS320FLEX chipset. FLEXstack™ software is specifically designed to support the FLEX decoder. The software runs on a host processor, handles communications with the A/D converter, and interprets the code words passed to the host from the TLV5591.

FLEXstack is a trademark of Motorola Incorporated.

ADC[1]

American Digital Cellular (same as USDC)

ADC[2]

Analog-to-digital converter (also A/D). A converter that uniquely represents all analog input values within a specified total input range by a limited number of digital output codes, each of which exclusively represents a fractional part of the total analog input range.

NOTE: This quantization procedure introduces inherent errors of one-half LSB (least significant bit) in the representation since, within this fractional range, only one analog value can be represented free of error by a single digital output code.

Address

The number dialed by a calling party that identifies the party called. Also a location or destination in a computer program.

Adjacent Channel Interference

Interference caused by the energy from a transmitting channel spilling over into an adjacent channel. This interference can be minimized by applying filters to the transmitting and receiving ends or by simply using non-adjacent frequency channels within a cell. Cellular systems typically transmit on nonadjacent frequencies within a cell in order to prevent adjacent channel interference.

Alert

Constant 10 kHz signaling tone sent on the reverse voice channel (by the mobile), in an analog cellular conversation, while the mobile phone is ringing.

Aliasing

The occurrence of spurious frequencies in the output of a PCM system that were not present in the input-due, to foldover of higher frequencies.

AM (Amplitude Modulation)

A technique for sending information as patterns of amplitude variations of a carrier sinusoid.

Amplifier

An electronic device used to increase signal power or amplitude.

AMPS

A Bell acronym for Advanced Mobile Phone Service, an analog FDMA technology where channels of information are separated by 30 kHz.

Analog

Information represented by continuous and smoothly varying signal amplitude or frequency over a certain range, such as in human speech or music.

Asynchronous

Refers to circuitry and operations without common timing (clock) signals.

Attenuation

Weakening of the signal due to it being partially blocked or absorbed — the decrease in power that occurs when any signal is transmitted. RF signal attenuation is heavily dependent on the frequency of the RF transmission and on the physical characteristics of the material that the transmission interacts with. For example, high frequency microwave transmissions are severely attenuated by rain, but lower frequency cellular transmissions are not.

ASK (Amplitude Shift Key Modulation)

Refers to transmitter on-off data transmission where data is transmitted by turning a radiation source on and off to transfer data over a wireless link.

Audio Frequency

Frequencies detectable by the human ear, usually between 20 and 15,000 Hz.

Bandwidth[1]

The range of signal frequencies that a circuit or network will respond to or pass.

Bandwidth[2]

The amount of frequency allocated for an RF transmission. For example, a cellular channel typically has a bandwidth of 30 kHz, i.e., a cellular system requires 30 kHz of frequency per channel to transmit its signal. One of the fundamental problems associated with RF transmissions is the limited amount of electromagnetic spectrum available. The electromagnetic spectrum is finite, and only a limited portion of the spectrum has been allocated for cellular use by the FCC (Federal Communications Commission). The FCC has allocated only 50 MHz of spectrum for cellular use. Additional capacity can not be achieved by simply taking up more spectrum. Since there is a limited amount of spectrum available for cellular use, additional capacity must be obtained by other means.

BPF

Band-pass filter. Typically used in analog and RF circuitry to pass a specific frequency band and attenuate out of band frequencies.

Baseband

Refers to the data rate or baseband rate of transmitted data.

Base Station

A multichannel transceiver located at the center of a cell and connected via wireline to the mobile telephone switching office (MTSO). Its primary purpose is to handle all incoming and outgoing cellular telephone traffic within the cell.

Baud Rate

Baud rate is the number of carrier signal modulation events (signal changes) per second during data transmission — not necessarily equal to the number of data bits transmitted per second (bps).

Baud Rate versus Bit Rate (Bits Per Second — bps)

Baud rate is the number of carrier signal modulation events (signal changes) per second, which must be within the bandwidth of the transmission medium. For modems using voice-grade telephone lines, the maximum baud rate is approximately 3300, which is approximately the pass band of the voice circuit (3300 Hz). Modulation schemes are employed that provide many bits of data for each carrier modulation event (baud) to increase the number of bits per second that can be transmitted on a pass band-limited voice telephone circuit. A modem running at 2400 baud and encoding four bits of data on each carrier transition (baud), for example, is actually transmitting 9600 bits of data per second.

Bell Tapping

The undesired activation of the ringer circuit of a telephone caused by rotary dial pulses from a parallel telephone. Also known as tinkling.

BER (Bit Error Rate)

Used as a measure to quantify bit error occurrences in a digital communications link.

Bias (Asymmetrical) Distortion

Distortion affecting a binary modulation scheme whereby the actual mark or space has a longer or shorter duration than the corresponding theoretical duration.

Bit Rate

Bit rate is the actual number of bits of data that is transmitted or received per second.

BORSCHT

An acronym for the function that must be performed in the central office (on a line card) when digital voice transmission occurs; **B**attery, **O**vervoltage, **R**inging, **C**oding, **H**ybrid, and **T**est.

Byte

A group of bits (usually 8) treated as a unit or word. Often equivalent to one alphabetic or numeric character.

Call Forwarding

A feature allowing the subscriber to forward a call to another telephone number.

Call Processing

The complete process of routing, originating, terminating cellular telephone calls, along with the necessary billing and statistical collection processes.

Call Record

A record stored on tape containing mobile number, dialed digits, time stamp information, and other data needed to bill or 'ticket' a cellular telephone call.

Call Setup

The call processing events that occur during the time a call is being established, but not yet connected.

Call Waiting

A feature allowing the subscriber to be alerted to the arrival of another call during the current conversation. The user can answer the call waiting and then switch between the two calls, but cannot connect all parties together.

CCIT

International Telegraph and Telephone Consultative Committee. An international forum for establishing communication system standards.

CDMA (Code Division Multiple Access)

In a CDMA system, each voice circuit is labeled with a unique code and transmitted on a single channel simultaneously with many other coded voice circuits. The only distinctions between the multiple voice circuits are the assigned codes. The channel is typically very wide with each voice circuit occupying the entire channel bandwidth. For example, 64 different voice circuits can be simultaneously transmitted on the same channel, with each voice circuit identified by its assigned code.

Cell

The RF coverage area in the cellular system resulting from operation of a single multiple-channel set of base station frequencies. Cell can also refer to the base site equipment servicing this area.

Channel[1]

An electronic communication path. In telecommunications, it is usually a voice bandwidth of 4000 Hz.

Channel[2]

A unique RF frequency that is used for communication between a subscriber unit and a cell site base station. Channels must be assigned by the FCC.

Circuit

An interconnected group of electronic devices or, in telecommunications, the path connecting two or more communications terminals.

Click Tone

A particular progress tone injected onto the forward voice channel (base station transmit, mobile unit receive) to indicate to the subscriber that the call has not been abandoned by the system.

C-Message Weighting

A noise weighting used to measure noise on a line that would be terminated by a 500-type telephone set or similar instrument. The resulting noise reading is in dBrnC.

Class 5 Office

See central office

CO (Central Office)[1]

The switching equipment that provides local-exchange telephone service for a given geographical area and is designated by the first three digits of the telephone number. This is also known as a Class-5 office.

CO (Central Office)[2]

The switching office that connects the MTSO (mobile telephone switching office) to the PSTN (public-switched telephone network). The CO is also known as a Class 5 or 'end' office.

Co-channel Interference

Co-channel interference is the interference caused between two cells transmitting on the same frequency within a network. Since co-channel interference is caused by another cell transmitting the same frequency, the interference cannot simply be filtered out. The co-channel interference can only be minimized through proper cellular network design. A cellular network must be designed to maximize the C/I ratio, which is the carrier-to-co-channel interference ratio. One of the ways to maximize the C/I ratio is to increase the frequency re-use distance, i.e., increase the distance between cells using the same set of transmission frequencies. The C/I ratio, in part, determines the frequency re-use distance of a cellular network.

Codec

An assembly comprising an encoder and a decoder in the same unit. A device that produces a digital coded output from an analog input, and vice versa.

Combo

A single-chip pulse-code-modulated (PCM) encoder and decoder (codec), and PCM line filter.

Common Battery

A system supplying direct current for the telephone set from the central office.

Compander

A combination of a compressor and an expander. The audio signal is compressed at the transmitter, reducing its dynamic range and thereby reducing the dynamic range of the transmitted signal. An expander at the receiver restores the recovered signal to its original dynamic range. Companding is used in communications systems to improve signal-to-noise ratio as a result of the reduced dynamic range that is transmitted. In analog cellular, 2:1 syllabic compression is used to limit the maximum peak voice deviation to ±2.9 kHz.

Constructive Interference

Interference that occurs when waves occupying the same space combine to form a single stronger wave. The strength of the composite wave depends on the how close in phase the two component waves are. For example, if two waves of the same phase, each with an amplitude of 10 are transmitted, they would combine into a composite wave of amplitude 20. Two waves slightly out of phase, however, would combine into a composite wave with an amplitude less than 20.

Control Channel

A unique RF channel used by each cell base station that is dedicated to the transmission of digital control information from the base station to the cellular mobile unit. It is used to assign voice channels, control mobile power, authorize handoffs, etc.

Crossbar Switch

An electromechanical switching machine using a relay mechanism with horizontal and vertical input lines (usually 10 to 20). Uses a contact matrix to connect any vertical to any horizontal.

Crosspoint

The element that actually performs the switching function in a telephone system. It may be mechanical using metal contacts or solid state using integrated circuits.

CT2

Cordless telephone, type 2, or 2nd generation

CTIA

Cellular Telecommunication Industry Association

Cutoff Frequency

The frequency above or below which signals are attenuated below a specified value by a circuit or network.

DAC

Digital-to-analog converter (also D/A). A converter that represents a limited number of different digital input codes by a corresponding number of discrete analog output values.

NOTE: Examples of input code formats are straight binary, two's complement, and binary-coded decimal (BCD).

Data

In telephone systems, any information other than human speech.

Data Set

Telecommunications term for a modem.

dB (Decibel)

A unit of measure of relative power — the logarithmic ratio between two amounts of power, 10 log (P1/P2), or voltage, 20 log (V1/V2), in terms of the ratio of two values. It is typically used in receiver and transmitter ± measurements.

dBm

Decibels referenced to one milliwatt; used in communication work as a measure of absolute power values. Zero dBm equals one milliwatt. (0 dBm = log 1 mW)

dBm0

Noise power referenced to or measured at a zero transmission level point (0TLP).

dBm0p

Noise power in dBm0, measured by a psophometer or noise measuring set having psophometric weighting.

dBrn

Decibels above reference noise. Rated noise power dB referenced to one picowatt. Zero dBrn equals –90 dBm.

dBrnC

Noise power in dBrn, measured by a noise measuring set with C-message weighting.

dBrnC0

Noise power in dBrnC referenced to or measured at a zero transmission level point (0TLP).

dBW

Decibels referenced to one Watt.

Decoder

Any device that modifies transmitted information to a form that can be understood by the receiver.

DECT

Digital European Cordless Telephone

Demultiplexer

A circuit that distributes an input signal to a selected output line (with more than one output line available — one-to-many).

Destructive Interference

Interference that occurs when waves occupying the same space combine to form a single wave with an amplitude that is less that any of the component waves. Destructive interference occurs when the waves that are summed into a single, composite wave are out of phase such that at any given instance, the negative amplitudes summed with the positive amplitudes result in an amplitude of the composite wave that is less than of any of the component waves. Destructive interference can result in attenuations ranging up to 100%, which is the case when two signals of equal amplitude but 180 degrees out of phase are summed together. They completely cancel each other.

Diversity Receive

A method commonly employed by cellular equipment manufacturers to improve the signal strength of received signals. The scheme uses two independent antennas that receive signals that differ in phase and amplitude resulting from the slight difference in antenna positions. These two signals are either summed or the strongest one is accepted by voting.

DTMF

Dual-tone multifrequency, commonly known as touchtones. This in-band signaling system consists of 12 audio tones, each created from two different frequencies (out of a group of 8), that correspond to the digits 0 through 9, and * and # on a subscriber telephone key pad.

Dual-Mode Cellular

Dual-mode cellular telephones operate in either digital or analog cellular systems.

DTX (Discontinuous Transmission)

A cellular telephone subscriber unit feature that allows the mobile unit to disable its RF power amplifier (PA) during conversation when the subscriber is not talking. This reduces the power drawn from the battery and thus increases talk time. The cellular system must support this feature if the subscriber is to be able to use it.

EAMPS

Extended Advanced Mobile Phone Service (AMPS with extended frequency allocation)

EIA

Electronic Industries Association. (2001 Pennsylvania Avenue, N.W., Washington, D.C. 20006)

Electromagnetic Spectrum

The total range of wavelengths or frequencies or electromagnetic radiation, extending from the longest radio waves to the shortest known cosmic rays.

EMI

Electromagnetic interference.

Encoder

Any device that modifies information into the desired pattern or form for a specific method of transmission.

End Office

See central office

Erlang

A dimensionless quantity used in the statistical measurements of the traffic in a cellular system. One Erlang is equivalent to the average number of simultaneous calls, and is equal to 3600 call-seconds per hour or 36 CCS (call century seconds) per hour.

ESN (Electronic Serial Number)

A 32-bit code that is unique to each cellular telephone mobile unit. It is used by the base station to validate the mobile unit. The ESN is not alterable by either the cellular service provider or the end user.

ESS

Electronic Switching System. A telephone switching machine using electronics, often combined with electromechanical crosspoints, and usually with a stored-program computer as the control element.

Equalization

The reduction of frequency distortion and/or phase distortion of a circuit by the introduction of networks to compensate for the difference in attenuation, time delay, or both, at the various frequencies in the transmission band.

Exchange Area

The territory within which telephone service is provided for a basic charge. Also called the local calling area.

Fade

A drop in the received signal strength of a cellular RF transmission signal that results from the RF signal interactions with the transmission environment.

FCC

Federal Communications Commission. A government agency that regulates and monitors the domestic use of the electromagnetic spectrum for communications.

FCC Part 68

A government document describing the types of equipment that must be registered and the electrical and mechanical standards to be met when connecting equipment to the public telephone network.

FDMA (Frequency Division Multiple Access)

A communications scheme where channels of information are separated by frequency and systems transmit one voice circuit per channel. The channels are relatively narrow, usually 30 KHz or less and are defined as either transmit or receive channels. A full-duplex conversation requires a transmit and receive channel pair. For example, if a FDMA system had 200 channels, the system could handle 100 simultaneous full-duplex conversations (100 channels for transmitting and 100 channels for receiving).

Flash Hook

400 ms of signaling tone sent on the reverse voice channel by the cellular mobile unit to request a hook flash.

FOCC (Forward Control Channel)

A control channel from the cellular base station to the mobile unit; also known as the control channel downlink.

Forced Disconnect

A call processing function that forces termination of a cellular call, usually not at the request of the mobile subscriber.

Four-Wire Line

A two-way transmission circuit using two pairs of conductors. This allows full-duplex (simultaneous in both directions) conversation without multiplexing.

Free Space Loss

The power loss of the RF transmission signal as a result of the signal spreading out as it travels through space. As a radio wavefront travels through space, its power diminishes according to the inverse-square law — at twice the distance, there is only one-fourth the power.

FSK (Frequency Shift Keying)

The form of frequency modulation that uses two different audio frequencies to transmit binary ones and zeros by shifting back and forth between the two frequencies.

Full-Duplex

Simultaneous communication in both directions between two points. It uses two communications paths with both points being able to transmit and receive simultaneously.

FVC (Forward Voice Channel)

A voice channel from the cellular base station to the mobile unit; also known as the voice channel downlink.

Glare Hold and Glare Release

A method of glare resolution. Glare occurs when both the local and distant end of a trunk are seized at the same instant, usually resulting in deadlock of the trunk. To prevent this, one end of the trunk is assigned a glare hold status and the other a glare release status. In the event of glare, the glare-hold end holds the trunk and the glare release-end releases the trunk and attempts to seize another. This scheme is used on the wirelines between the MTSO and connecting cellular sites.

Grade of Service

A measure of what percentage of calls placed through an exchange fail to be completed due to congestion of that exchange. In cellular communications, a 2% GOS is usually considered acceptable.

GSM

Groupe Special Mobile (a European format for cellular communications).

Half-Duplex

A circuit that can carry information in both directions but not simultaneously — uses two communications paths with only one point being able to transmit and receive simultaneously.

Handoff (Intercell)

The process by which cellular mobile units traveling through the system coverage area are switched from one cell (and its base station) to the next cell (and to a different channel) that has better coverage for that particular area. The handoff is often triggered by the degradation of the transmission quality due to the mobile unit reaching the edge of the cell's service area or by adverse RF propagation characteristics in the area through which the mobile unit is traveling.

Handoff (Intracell)

The process by which cellular mobile units traveling through a cell's coverage area are switched from one sector in the cell to the next sector in the cell (and to a different channel) that has better coverage for that particular area. The handoff is often triggered by the degradation of the transmission quality due to the mobile unit reaching the edge of the sector's service area or by adverse RF propagation characteristics in the area through which the mobile unit is traveling.

Harmonic Filter

A filter used in the base station and cellular mobile unit transmitter circuits to remove unwanted harmonics (spurious frequencies) from the transmitted signal.

HPF

High-pass filter. Typically used in analog and RF circuitry to pass high frequencies and attenuate lower frequencies.

Hybrid

In telecommunications, a circuit that divides a signal transmission channel into two channels (i.e., one for each direction) or, conversely, combines two channels into one. Typically telecommunications applications are 2-to-4 or 4-to-2 wire hybrids, with two wires being one communication path. Every telephone contains a hybrid circuit to separate ear piece and mouthpiece audio and couple both into a 2-wire circuit that connects to the Central Office. If the hybrid is not balanced properly, echo or 'loop-back' can result in the circuit when the transmitted signal is reflected back into the receive path.

Idle Channel

A channel that is assigned to a cell base station for use but is not currently in service (being used). All idle channels for each cell base station are kept in an 'idle-link-list,' which is constantly updated at the MTSO (Mobile Telephone Switching Office).

Infrastructure

All parts of the cellular system, excluding the subscriber. It includes the MTSO, base stations, cell sites, and all links between them.

In-Band Signaling

A process in which audio tones between 300 and 3400 Hz provide supervisory and/or address signaling between the cell base station and the cellular mobile unit.

IS-54/IS-136

TIA standard for dual-mode cellular telephones. IS-136 is the most recent revision of the standard.

JDC

Japanese Digital Cellular

Lineside

Refers to the portion of the central office that connects to the local loop.

Local Loop

The voice-band channel connecting the subscriber to the central office.

Longitudinal Balance

A measure of symmetry impedance of a balanced network. Improper longitudinal balance results in poor common-mode rejection.

LNA

Low noise amplifier used in data transmission circuits (analog and RF) to set the noise floor of gain stages as low as possible.

Loop Current

Direct current in the local loop. This indicates that a telephone is off-hook (in use).

Loss

Attenuation of a signal due to any cause.

LPF

Low-pass filter. Typically used in analog and RF circuitry to pass low frequencies and attenuate higher frequencies.

Manchester-Encoded Data

Digital data format that reduces noise in RF links.

MARCSTAR

Multichannel Advanced Remote Control Signaling Transmitter and Receiver is a registered trademark of Texas Instruments, Incorporated. Generally refers to a family of remote control devices produced at TI.

Mark

One of the two possible states of a binary information element. The closed circuit and idle stage in a teleprinter circuit. See Space.

Microwave Hop

A microwave RF connection between the MTSO and cell sites in remote locations.

MIN1

The 24-bit number that corresponds to the 7-digit subscriber telephone number.

MIN2

The 10-bit number that corresponds to the 3-digit subscriber area code.

Mobile Attenuation

The power of the cellular mobile unit can be adjusted (or attenuated) dynamically to one of seven discrete power levels (analog cellular). This is done so that when a mobile unit comes closer to a base receiver, its power is reduced to prevent the chance of interfering with other mobile units operating on the same voice channel in another cell (co-channel interference). In addition, this increases the talk usage time of the mobile unit by reducing the amount of power drawn from its battery.

Mobile Coverage Area

Geographical area in which two-way cellular telephone service can be expected (between the cell base station and the cellular mobile unit).

Mobile-ID

The 7-digit cellular mobile unit telephone number. It does not include the area code.

Mobile Origination

The initiation of a telephone call by a cellular mobile unit.

Mobile Unit

The cellular mobile unit is either a handheld or car-mounted transceiver. The mobile unit connects the user to the base station using RF transmission and reception. The mobile unit is also known as the subscriber.

Modem

A contraction of modulator/demodulator. It is a device to convert digital data into an analog signal and vice versa so that two electronic devices (e.g., a computer and a data terminal) may communicate over the telephone system.

MSA (Metropolitan Service Area)

A cellular coverage, defined by the FCC, that resides in a densely populated area.

MTS (Message Telephone Service)

The official name for long distance or toll service.

MTSO (Mobile Telephone Switching Office)

This is the switching office to which all cellular base station sites connect. The MTSO, in turn, interfaces to the PSTN by connection to a CO. Control of all cell sites, all subscriber records, statistics, and billing is maintained at the MTSO.

Mu-Law (μ-Law)

An encoding format for the quantization and digitization of analog signals into Pulse Code Modulation (PCM) signals (A/D) and recovery of analog signals from PCM (D/A). μ-law specifies the parameters for compression and re-expansion of the signals during signal transmission and processing. μ-law PCM encoding is used in North America. A-law is the European format.

Multipath Fading

Multipath fading, also called Rayleigh fading, occurs when the direct-path transmitted wave destructively interferes with its reflections at the receiving end. The destructive interference is a result of the reflected waves arriving at the receiving end later and out of phase with the direct-path transmitted wave. Multipath interference can vary in intensity depending on the amount of destructive interference that takes place.

Multiplexer

A device for accomplishing simultaneous transmission of two or more signals over a common transmission medium (many-to-one).

NADC

North American Digital Cellular

NAMPS

Narrow-band Advanced Mobile Phone Service. An analog FDMA technology in which channels of information are separated by 10 kHz, and provides three times capacity over AMPS, which has 30 Khz cannel spacing.

NMT

Nordic Mobile Telephone

No-Answer Transfer

A feature that allows calls to a cellular mobile unit to be transferred to a predetermined number if the mobile unit does not acknowledge an incoming call or is not answered.

NPA (Numbering Plan Area)

The area code

Off-Hook

The circuit condition caused when the handset is lifted from the switch hook of the telephone set. This condition exists during call setup or conversation.

On-Hook

The normal circuit condition when the handset is on the switch hook of the telephone set.

Operator

In cellular telephony, this is the local service provider that owns the cellular system in that particular area.

Origination

A call that is placed by the cellular mobile subscriber, calling either a land-line circuit or another cellular mobile subscriber.

PABX

Private Automated Branch Exchange. Small local automatic telephone office serving extensions in a business complex providing access to the public network.

Page

A message that is broadcast from a group of cell sites that carries a mobile ID for the purpose of alerting the mobile that a call is waiting.

Parallel Data

The transfer of all bits of a data word simultaneously over two or more wires or transmission links (one for each bit in the word).

Parity

An error-detection scheme in which an extra bit (the parity bit) is added to each data word to make the total of all the bits in the word either even or odd according to whether even or odd parity is called-for. Correct parity (even or odd) of each data word is checked at the receiving end to determine if there were any transmission errors.

PBX

Private Branch Exchange. A telephone exchange serving an individual organization and having connection to a public telephone exchange.

PCM (Pulse Code Modulation)

Process in which the modulating signal is sampled, and the magnitude of each sample (with respect to a fixed reference) is quantized and converted by coding to a digital signal. PCM provides undistorted transmission, even in the presence of noise. The sample frequency must be at least twice the highest modulating frequency for full recovery of the original modulating information (Nyquist).

PCN

Personal Communications Network, also known as PCS (Personal Communications System)

Period

The time or angle that a signal is delayed with respect to some reference position.

Phase

The time or angle that a signal is delayed with respect to some reference position.

PL

The transmitting power level of the cellular mobile unit.

Port Change

A channel change from one sector to another, while staying within the same cell, as a mobile unit moves from one area in a cell to another area in the same cell.

POTS

Plain Old Telephone Service. An acronym used by the telephone industry for conventional telephone service.

PSK (Phase-Shift Keyed Modulation)

A method of placing data on a carrier signal by modifying the phase of the carrier wave.

Psophometric Weighting

A noise-weighting method recommended by the CCITT for use in a noise measuring set or psophometer.

PTP

Point-to-point or line of sight communications link.

Quantization

A process in which the continuous range of values of an analog input signal is divided into nonoverlapping subranges (chords) and to each subrange a discrete value of the output is uniquely assigned a binary number.

Quantizing Distortion

The inherent distortion introduced in the process of quantization.

Quantizing Noise

An undesirable random signal caused by the error of approximation in a quantizing process. It may be regarded as noise arising in the pulse-code modulation process due to the code-derived facsimile not exactly matching the waveform of the original message.

RECC (Reverse Control Channel)

The control channel that is used from the cellular mobile station to the base station direction, also known as the control channel uplink.

Reflections

RF waves can reflect off of hills, buildings, moving cars, the atmosphere, and basically almost anything in the RF transmission environment. The reflections may vary in phase and strength from the original wave. Reflections allow radio waves to reach their targets around corners, behind buildings, under bridges, in parking garages, etc. RF transmissions 'bend' around objects as a result of reflections.

Register

A storage element for one or more bits of digital information.

Remote Control

A term used to describe wireless control of electronics and the systems controlled by these circuits.

RF

Radio frequency. Used to describe frequencies between audio and infrared that are used in communications applications.

Ring

The alerting signal to the subscriber or terminal equipment. Also, the name for one conductor of the wire pair comprising the local loop, designated by R.

Ring Trip

During ring signaling, the detection of the off-hook condition and removal of the ring signal from the line by the switch.

RKE

Remote keyless entry. Primarily used in automobile entry systems, home security systems, and garage door openers.

Roamer

A cellular mobile station that operates in a cellular system other than the one from which the service is subscribed (the home system).

Rolling-code

In many communications links, a code is used to identify a user. Rolling-code means this code changes every time the code is transmitted to improve security of the system or link.

RSA (Rural Service Area)

A cellular coverage, defined by the FCC, that resides in a less populated area.

RSSI (Relative Signal Strength Indication)

Received signal strength indicator — used in RF circuitry to detect the strength of a received signal. In cellular telephony, it is a value representing the received signal strength of both the cellular mobile unit and the base station. This value is used to initiate a power change or handoff.

RVC (Reverse Voice Channel)

The voice channel that is used in the cellular mobile station to base station direction, also known as the voice channel uplink.

SAT (Supervisory Audio Tone)

One of three tones (5970, 6000, and 6030 Hz) that are transmitted by the cell base station and transponded by the cellular mobile station. It is used to evaluate the complete radio path, both forward and reverse voice channels. The SAT received by the mobile unit is actually regenerated by the mobile unit with the same amplitude and noise associated with the actual received SAT.

SAW (Surface Acoustic Wave)

Resonant devices that are used in many communication applications and are well suited for low power RF.

Scan Receiver

A receiver that resides in the cell base station that is dedicated to measuring the signal strength of the cellular mobile units that are communicating via the cell. These measurements are used in the handoff process (but not in the power-up/power-down process, which is handled by each voice transceiver).

SCM (Station Class Mark)

This indicates the cellular mobile station type (mobile/trans/port), and if the station has DTX.

Sector-Receive Cell Site

Six or three directional antennas that are used at a cell site to get the additional gain required to serve cellular mobile units. A mobile unit could move completely around a sector-receive cell site and never change channels; but it would change antennas.

Sector-Sector Cell Site

The cell is broken up into two or more independent sectors that each have their own transmit and receive antennas. A cellular mobile unit moving around a sector-sector cell would change channels (intra-cell handoff).

Sensitivity

A term used to describe the minimum discernible signal a receiver can detect.

Serial Data

The transfer of data over a single wire in a sequential pattern of bits that make up a data word.

SID (System Identification)

A unique digital code assigned to each cellular system. The home system of each mobile is stored in its internal memory so that the mobile unit knows when it is a roamer (outside its normal service area).

Sidetone

An attenuated portion of the transmit audio returned to the originator and subsequently heard in the earpiece of the sender. Sidetone is common, as all telephones produce some sidetone and is caused by unbalanced 2-to-4 wire hybrids. And, sidetone is often intentional to meet the expectations of the user, who is accustomed to hearing it on a 'live' telephone set as an indication that it is 'connected.'

Signal-to-Noise

The ratio of the magnitude of the signal to that of the noise with no signal present, usually expressed in dB.

Simplex

A circuit that can carry information in only one direction (e.g., broadcasting, public address, etc.). Uses one communication path with one only able to transmit and the other end only able to receive.

SLIC

Subscriber line interface circuit. In digital transmission of voice, this circuit that performs some or all of the interface functions at the central office. See BORSCHT.

Source Cell

The cell that a cellular mobile unit is leaving during the handoff process.

Source Channel Falsing

A condition that exists when co-channel SAT (supervisory audio tone) exists on the source channel during handoff, so that the source channel does not squelch during the handoff process. This results in noise during the handoff process (after the hand-off order) that can be heard by both the landline and cellular mobile unit parties.

Space

One of the two possible states of a binary information element: the open-circuit or no-current state of a teleprinter. See Mark.

Spectrum

The electromagnetic spectrum, which is the continuous range of electromagnetic frequencies.

Squelch Circuit

A radio receiver circuit that disables the audio path when the incoming signal strength is below a predetermined threshold.

ST (Signaling Tone)

A 10 kHz tone transmitted by the cellular mobile unit on a voice channel to (1) confirm channel change orders (HO tone, 50 ms ST), (2) request a flash-hook by the mobile (400 ms ST), (3) mobile alert (continuous ST), and (4) mobile ending call (1.8 sec ST).

State

A condition of an electronic device, especially a computer, that is maintained until an internal or external occurrence causes change.

Subscriber

The mobile user of the cellular system.

Subscriber Files

User records stored at the MTSO containing all information pertaining to each subscriber. This includes cellular mobile unit number, home service location, last known location, type of mobile unit, service denial flags, and special feature options available to that subscriber.

Subscriber Loop

See local loop.

TACS

Total Area Coverage Systems

Target Cell

The cell that a mobile unit is going to during the hand off process.

Target Channel Falsing

A condition that exists when a co-channel SAT exists on the target channel during handoff, so that the target channel does not squelch before arrival of the cellular mobile unit during the handoff process. This results in noise during the handoff process (before the handoff order) that can be heard by both the landline and mobile unit parties.

TDM (Time Division Multiplexing)

A communication system technique in which each of multiple channels is sequentially connected to a single-channel transmission link. At the other end, the single-channel transmission link is sequentially connected to each of connected separates information from multiple channel inputs and places them on a carrier in specific positions of time to send.

TDMA (Time Division Multiple Access)

TDMA systems are able to transmit multiple voice circuits on each channel. A TDMA channel is a single FDMA channel divided up into multiple time slots. The channels can vary in bandwidth and, depending on the type of system and the time slots, can transmit all or part of a voice circuit.

TIA

Telecommunications Industry Association

TIP

One conductor of the wire pair composing the local loop and designated by the letter T. Usually, the more positive of the two conductors.

Toll Center

A major telephone distribution center that distributes calls from one major metropolitan area to another. Also known as a class 4 office.

Toll Ticketing

Subscriber records that are kept at the MTSO for billing purposes. They contain subscriber number, time of call, called number, location of call origination, location of call termination, and other important statistics for the proper billing of the subscriber.

Toll Ticketing House

A third-party company that takes the toll ticketing records and actually bills the subscribers. Nonpayment by subscribers is reported to the operating company so denial of service can be performed.

TPC – (Three-Party Conference Circuit)

A TPC is used in a 3-party conference, but more important, it is used during every handoff so that the channel-change transition can be made with less noise by connecting the audio of the source and target cells together before the handoff order is sent. When a handoff is made during a 3-party conference call and the TPC is being used, 'hard handoffs' occur and the potential for noise during channel changes increases significantly.

Transmission Link

The path over which information flows from sender to receiver.

Transhybrid Loss

In a telephone hybrid, the measure of the isolation between the receive and transmit ports. It is also a measure of the balance between the two matched windings of a hybrid transformer.

Transmission Link

The path over which information flows from sender to receiver.

Trunk

A transmission channel connecting two switching machines. In cellular systems, this is the connection between the MTSO and CO and the connections between the MTSO and cell sites.

Trunkside

That portion of the central office that connects to trunks going to other switching offices.

Tumbling ESN (Electronic Serial Number)

Fraudulent hardware that changes the cellular mobile unit ESN every time a call is originated. Since often only the FIRST call of a roamer is screened for a bad ESN, an infinite number of fraudulent calls can be placed using a tumbling ESN.

UHF

Ultra high frequency range from 300 to 1000 MHz.

USDC

U.S. Digital Cellular

Validation

The method of determining if a cellular mobile unit should be given service by the cellular system. Validation often requires matching the ESN (electronic serial number) of the mobile with its mobile ID, and then checking the mobile unit against files that contain subscribers who should be denied service.

VBAP (Voice-Band Audio Processor)

TI trademark for device that provides A/D and D/A conversion, along with the filtering necessary for voice-band communications.

VHF

Very high frequency range from 100 to 300 MHz.

VMAC (Voice Mobile Attenuation Code)

One of eight discrete cellular mobile unit transmit power levels that are dynamically selected during a cellular telephone conversation. These power steps are in 4 dB increments.

Voice Circuit

Half of a full-duplex conversation, i.e., one-half of a two-way conversation. For example, if two people are talking by phone, each of their voices is considered a separate voice circuit.

Voice-Grade Line

A local loop or trunk having a band pass of approximately 300 Hz to 3000 Hz.

Wide-Band Circuit

A transmission facility having a bandwidth greater than that of a voice-grade line.

2 Central Office Codecs

- **Replaces Use of TCM2910A in Tandem With TCM2912C**
- **Reliable Silicon-Gate CMOS Technology**
- **Low Power Consumption:**
  Operating Mode . . . 80 mW Typical
  Power-Down Mode . . . 5 mW Typical
- **Excellent Power-Supply Rejection Ratio Over Frequency Range of 0 Hz to 50 kHz**
- **No External Components Needed for Sample, Hold, and Autozero Functions**
- **Precision Internal Voltage References**
- **Direct Replacement for Intel 2913, 2914, 2916, and 2917**
- **Recommended for Direct Voice Applications**

FEATURES TABLE

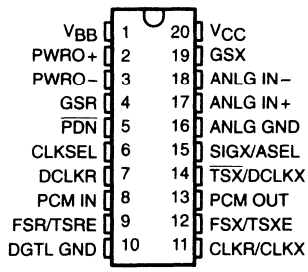
FEATURE	29C13 129C13	29C14 129C14	29C16 129C16	29C17 129C17
Number of Pins:				
24		X		
20	X			
16			X	X
μ-Law/A-Law Coding:				
μ-Law	X	X	X	
A-Law	X	X		X
Gain Timing Rates:				
Variable Mode				
64 kHz to 2.048 MHz	X	X	X	X
Fixed Mode				
1.536 MHz	X	X		
1.544 MHz	X	X		
2.048 MHz	X	X	X	X
Loopback Test Capability		X		
8th-Bit Signaling		X		

description

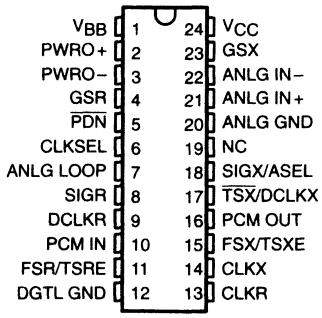
The TCM29C13, TCM29C14, TCM29C16, TCM29C17, TCM129C13, TCM129C14, TCM129C16, and TCM129C17 are single-chip PCM codecs (pulse-code-modulated encoders and decoders) and PCM line filters. They provide all the functions required to interface a full-duplex (4-wire) voice telephone circuit with a TDM (time-division-multiplexed) system, and are intended to replace the TCM2910A in tandem with the TCM2912C. Primary applications include:

- Line interface for digital transmission and switching of T1 carrier, PABX, and central office telephone systems
- Subscriber line concentrators
- Digital-encryption systems
- Digital voice-band data-storage systems
- Digital signal processing

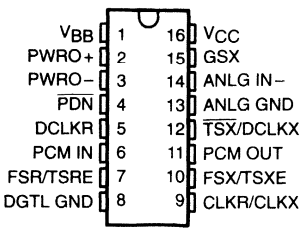
TCM29C13, TCM129C13
DW OR N PACKAGE
(TOP VIEW)



TCM29C14, TCM129C14
DW PACKAGE
(TOP VIEW)



TCM29C16, TCM29C17,
TCM129C16, TLC129C17
DW OR N PACKAGE
(TOP VIEW)



NC – No internal connection

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

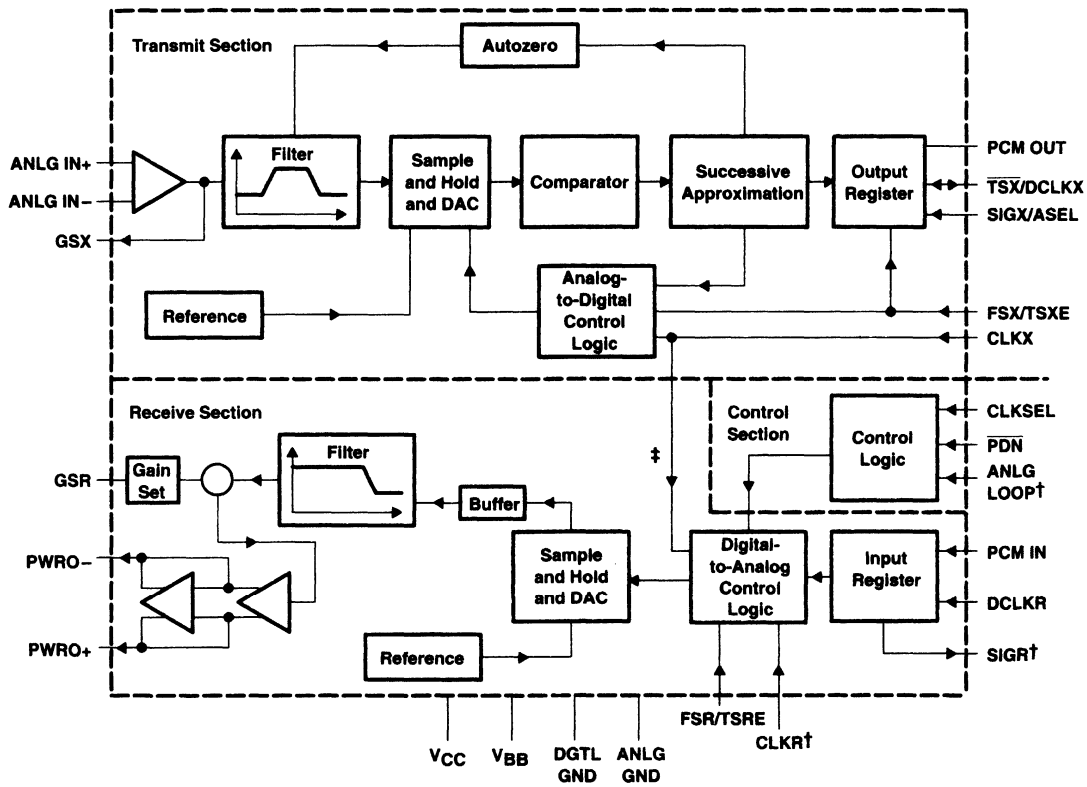
description (continued)

These devices are designed to perform the transmit encoding (A/D conversion) and receive decoding (D/A conversion) as well as the transmit and receive filtering functions in a pulse-code-modulated system. They are intended to be used at the analog termination of a PCM line or trunk.

The TCM129C13, TCM129C14, TCM129C16, TCM129C17, TCM29C13, TCM29C14, TCM29C16, and TCM29C17 provide the band-pass filtering of the analog signals prior to encoding and after decoding. These combination devices perform the encoding and decoding of voice and call progress tones as well as the signaling and supervision information.

The TCM29C13, TCM29C14, TCM29C16, and TCM29C17 are characterized for operation from 0°C to 70°C. The TCM129C13, TCM129C14, TCM129C16, and TCM129C17 are characterized for operation from –40°C to 85°C.

functional block diagram



† TCM29C14 and TCM129C14 only
‡ TCM29C13, TCM29C16, TCM29C17, TCM129C13, TCM129C16, and TCM129C17 only

Terminal Functions

TERMINAL NO.				I/O	DESCRIPTION
NAME	TCM29C13 TCM129C13	TCM29C14 TCM129C14	TCM29C16 TCM29C17 TCM129C16 TCM129C17		
ANLG GND	16	20	13		Analog ground return for all internal voice circuits. Not internally connected to DGTL GND.
ANLG IN+	17	21		I	Noninverting analog input to uncommitted transmit operational amplifier. Internally connected to ANLG GND on TCM129C16, TCM29C16, TCM129C17, and TCM29C17.
ANLG IN–	18	22	14	I	Inverting analog input to uncommitted transmit operational amplifier.
ANLG LOOP		7		I	Provides loopback test capability. When this input is high, PWRO+ is internally connected to ANLG IN.
CLKR	11	13	9	I	Receive master clock and data clock for the fixed-data-rate mode. Receive master clock only for variable-data-rate mode. CLKR and CLKX are internally connected together for TCM129C13, TCM129C16, TCM129C17, TCM29C13, TCM29C16, and TCM29C17.
CLKSEL	6	6		I	Clock-frequency selection. Input must be connected to V_{BB}, V_{CC}, or ground to reflect the master-clock frequency. When tied to V_{BB}, CLK is 2.048 MHz. When tied to GND, CLK is 1.544 MHz. When tied to V_{CC}, CLK is 1.536 MHz.
CLKX	11	14	9	I	Transmit master clock and data clock for the fixed-data-rate mode. Transmit master clock only for variable-date-rate mode. CLKR and CLKX are internally connected for the TCM129C13, TCM129C16, TCM129C17, TCM29C13, TCM29C16, and TCM29C17.
DCLKR	7	9	5	I	Fixed or variable-data-rate operation select. When connected to V_{BB}, the device operates in the fixed-data-rate mode. When DCLKR is not connected to V_{BB}, the device operates in the variable-data-rate mode, and DCLKR becomes the receiver data clock. DCLKR then operates at frequencies from 64 kHz to 2.048 MHz.
DGTL GND	10	12	8		Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
FSR/TSRE	9	11	7	I	Frame synchronization clock input/time-slot enable for receive channel. In the fixed-data-rate mode, FSR distinguishes between signaling and nonsignaling frames by a double- or single-length pulse, respectively. In the variable-data-rate mode, this signal must remain high for the duration of the time slot. The receive channel enters the standby state when FSR is TTL low for 300 ms.
FSX/TSXE	12	15	10	I	Frame-synchronization clock input/time-slot enable for transmit channel. Operates independently of, but in an analagous manner to, FSR/TSRE. The transmit channel enters the standby state when FSX is low for 300 ms.
GSR	4	4		I	Input to the gain-setting network on the output power amplifier. Transmission level can be adjusted over a 12-dB range depending on the voltage at GSR.
GSX	19	23	15	O	Output terminal of internal uncommitted operational amplifier. Internally, this is the voice signal input to the transmit filter.
PCM IN	8	10	6	I	Receive PCM input. PCM data is clocked in on eight consecutive negative transitions of the receive data clock, which is CLKR in fixed-data-rate timing and DCLKR in variable-data-rate timing.
PCM OUT	13	16	11	O	Transmit PCM output. PCM data is clocked out on this output on eight consecutive positive transitions of the transmit data clock, which is CLKX in fixed-data-rate timing and DCLKX in variable-data-rate timing.

Terminal Functions

TERMINAL NO.				I/O	DESCRIPTION
NAME	TCM29C13 TCM129C13	TCM29C14 TCM129C14	TCM29C16 TCM29C17 TCM129C16 TCM129C17		
$\overline{PDN}$	5	5	4	I	Power-down select. The device is inactive with a TTL low-level input to this terminal and active with a TTL high-level input to the terminal.
PWRO+	2	2	2	O	Noninverting output of power amplifier. Can drive transformer hybrids or high-impedance loads directly in either a differential or a single-ended configuration
PWRO–	3	3	3	O	Inverting output of power amplifier. Functionally identical with and complementary to PWRO+.
SIGR		8		O	Signaling bit output, receive channel. In a fixed-data-rate mode, outputs the logical state of the 8th bit (LSB) of the PCM word in the most recent signaling frame.
SIGX/ASEL	15	18		I	A-law and μ-law operation select. When connected to V_{BB}, A-law is selected. When connected to V_{CC} or GND, μ-law is selected. When not connected to V_{BB}, a TTL-level input is transmitted as the eighth bit (LBS) of the PCM word during signaling frames on PCM OUT (TCM29C14 and TCM129C14 only). SIGX/ASEL is internally connected to provide μ-law operational for TCM29C16 and TCM129C16 and A-law operation for TCM29C17 and TCM129C17.
$\overline{TSX}$/DCLKX	14	17	12	I/O	Transmit channel time-slot strobe (output) or data clock (input) for the transmit channel. In the fixed-data-rate mode, this terminal is an open-drain output to be used as an enable signal for a 3-state output buffer. In the variable-data rate mode, DCLKX becomes the transmit data clock, which operates at TTL level from 64 kHz to 2.048 MHz.
V_{BB}	1	1	1		Most negative supply voltage. Input is –5 V ±5%.
V_{CC}	20	24	16		Most positive supply voltage. Input is 5 V ±5%

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.3 V to 15 V
Output voltage range, V_O . . . . . −0.3 V to 15 V
Input voltage range, V_I . . . . . −0.3 V to 15 V
Digital ground voltage range . . . . . −0.3 V to 15 V
Continuous total dissipation at (or below) 25°C free-air temperature . . . . . 1375 mW
Operating free-air temperature range, T_A: TCM29Cxx . . . . . 0°C to 70°C
TCM129Cxx . . . . . −40°C to 85°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values for maximum ratings are with respect to V_{BB}.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see Note 3)		4.75	5	5.25	V
Supply voltage, V_{BB}		−4.75	−5	−5.25	V
Digital ground voltage with respect to ANGL GND			0		V
High-level input voltage, V_{IH} (all inputs except CLKSEL)		2.2			V
Low-level input voltage, V_{IL} (all inputs except CLKSEL)				0.8	V
Clock-select input voltage	2.048 MHz	V_{BB}		V_{BB} +0.5	V
	1.544 MHz	0		0.5	
	1.536 MHz	V_{CC} −0.5		V_{CC}	
Load resistance, R_L	GSX	10			kΩ
	PWRO+ and/or PWRO−	300			Ω
Load capacitance, C_L	GSX			50	pF
	PWRO+ and/or PWRO−			100	
Operating free-air temperature, T_A	TCM29Cxx	0		70	°C
	TCM129Cxx	−40		85	

NOTES: 2. To avoid possible damage to these CMOS devices and resulting reliability problems, the power-up procedure described in the device power-up sequence paragraphs later in this document should be followed.
3. Voltage at analog inputs and outputs, V_{CC} and V_{BB} terminals, are with respect to the ANLG GND terminal. All other voltages are referenced to the digital ground terminal unless otherwise noted.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

supply current, f_{DCLK} = 2.048 MHz, outputs not loaded

PARAMETER			TEST CONDITIONS	TCM29Cxx			TCM129Cxx			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{CC}	Supply current from V_{CC}	Operating			7	9		8	13	mA
		Standby	FSX, FSR = V_{IL} after 300 ms		0.5	1		0.7	1.5	
		Power down	$\overline{PDN}$ = V_{IL} after 10 µs		0.3	0.8		0.4	1	
I_{BB}	Supply current from V_{BB}	Operating			−7	−9		−8	−13	mA
		Standby	FSX, FSR = V_{IL} after 300 ms		−0.5	−1		−0.7	−1.5	
		Power down	$\overline{PDN}$ = V_{IL} after 10 µs		−0.3	−0.8		−0.4	−1	
P_D	Power dissipation	Operating			70	90		80	130	mW
		Standby	FSX, FSR = V_{IL} after 300 ms		5	10		7	15	
		Power down	$\overline{PDN}$ = V_{IL} after 10 µs		3	8		4	10	

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

digital interface

PARAMETER			TEST CONDITIONS	TCM29Cxx			TCM129Cxx			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	PCM OUT	I_{OH} = −9.6 mA	2.4			2.4			V
		SIGR	I_{OH} = −1.2 mA	2.4			2.4			
V_{OL}	Low-level output voltage at PCM OUT, TSX, SIGR		I_{OL} = 3.2 mA			0.4			0.5	V
I_{IH}	High-level input current, any digital input		V_I = 2.2 V to V_{CC}			10			12	µA
I_{IL}	Low-level input current, any digital input		V_I = 0 to 0.8 V			10			12	µA
C_i	Input capacitance				5	10		5	10	pF
C_o	Output capacitance				5			5		pF

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

transmit amplifier input

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input current at ANLG IN+, ANLG IN −	V_I = −2.17 V to 2.17 V			±100	nA
Input offset voltage at ANLG IN+, ANLG IN −				±25	mV
Common-mode rejection at ANLG IN +, ANLG IN −		55			dB
Open-loop voltage amplification at GSX		5000			
Open-loop unity-gain bandwidth at GSX			1		MHz
Input current at ANLG IN+, ANLG IN −		10			MΩ

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

receive filter output

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output offset voltage PWRO+, PWRO− (single ended)	Relative to ANLG GND		80	180	mV
Output resistance at PWRO+, PWRO−			1		Ω

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

gain and dynamic range, V_{CC} = 5 V, V_{BB} = 5 V, T_A = 25°C (unless otherwise noted) (see Notes 4, 5, and 6)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Encoder milliwatt response (transmit gain tolerance)		Signal input = 1.064 Vrms for μ-law, Signal input = 1.068 Vrms for A-law		±0.04	±0.02	dBm0
Encoder milliwatt response additional tolerance (nominal supplies and temperature)		T_A = 0°C to 70°C, Supplies = ± 5%			± 0.08	dB
Digital milliwatt response (receive tolerance gain) relative to zero-transmission-level point		Signal input per CCITT G.711, Output signal = 1 kHz		±0.04	±0.02	dBm0
Digital milliwatt response variation with temperature and supplies		T_A = 0°C to 70°C, Supplies = ± 5%			± 0.08	dB
Zero-transmission-level point, transmit channel (0 dBm0)	μ-law	R_L = 600 Ω		2.76		dBm
	A-law			2.79		
	μ-law	R_L = 900 Ω		1		
	A-law			1.03		
Zero-transmission-level point, receive channel (0 dBm0)	μ-law	R_L = 600 Ω		5.76		dBm
	A-law			5.79		
	μ-law	R_L = 900 Ω		4		
	A-law			4.03		

NOTES: 4. Unless otherwise noted, the analog input is a 0-dBm0, 1020-Hz sine wave, where 0 dBm0 is defined as the zero-reference point of the channel under test. This corresponds to an analog signal input of 1.064 Vrms or an output of 1.503 Vrms.

5. The input amplifier is set for noninverting unity gain. The digital input is a PCM bit stream generated by passing a 0-dBm0, 1020-Hz sine wave through an ideal encoder.

6. Receive output is measured single ended in the maximum gain configuration. To set the output amplifier for maximum gain, GSR is connected to PWRO– and the output is taken at PWRO+. All output levels are (sin x)/x corrected.

gain tracking over recommended ranges of supply voltage and operating free-air temperature, reference level = –10 dBm0

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit gain-tracking error, sinusoidal input	3 ≥ input level ≥ –40 dBm0		±0.25	dB
	–40 > input level ≥ –50 dBm0		±0.5	
	–50 > input level ≥ –55 dBm0		±1.2	
Receive gain-tracking error, sinusoidal input	3 ≥ input level ≥ –40 dBm0		±0.25	dB
	–40 > input level ≥ –50 dBm0		±0.5	
	–50 > input level ≥ –55 dBm0		±1.2	

noise over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise, C-message weighted	ANLG IN+ = ANLG GND, ANLG IN– = GSX		15	dBrnC0
Transmit noise, C-message weighted with 8-bit-signaling (TCM29C14 and TCM129C14 only)	ANLG IN+ = ANLG GND, ANLG IN– = GSX, 6th frame signaling		18	dBrnC0
Transmit noise, psophometrically weighted	ANLG IN+ = ANLG GND, ANLG IN– = GSX		–69	dBm0p
Receive noise, C-message-weighted quiet code	PCM IN = 11111111 (μ-law), PCM IN = 10101010 (A-law), measured at PWRO+		11	dBrnC0
Receive noise, C-message-weighted sign bit toggled	Input to PCM IN is zero code with sign bit toggled at 1-kHz rate		12	dBrmC0
Receive noise, psophometrically weighted	PCM = lowest positive decode level		–79	dBm0p

power-supply rejection ratio and crosstalk attenuation over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{CC} supply-voltage rejection ratio, transmit channel	0 ≤ f < 30 kHz	Idle channel, Supply signal = 200 $mV_{(peak-to-peak)}$, f measured at PCM OUT		–30		dB
	30 ≤ f < 50 kHz			–45		
V_{BB} supply-voltage rejection ratio, transmit channel	0 ≤ f < 30 kHz	Idle channel, Supply signal = 200 $mV_{(peak-to-peak)}$, f measured at PCM OUT		–30		dB
	30 ≤ f < 50 kHz			–55		
V_{CC} supply-voltage rejection ratio, receive channel (single ended)	0 ≤ f < 30 kHz	Idle channel, Supply signal = 200 $mV_{(peak-to-peak)}$, f measured at PWRO+		–20		dB
	30 ≤ f < 50 kHz			–45		
V_{BB} supply-voltage rejection ratio, receive channel (single ended)	0 ≤ f < 30 kHz	Idle channel, Supply signal = 200 $mV_{(peak-to-peak)}$, Narrow band, f measured at PWRO+		–20		dB
	30 ≤ f < 50 kHz			–45		
Crosstalk attenuation, transmit to receive (single ended)		ANLG IN+ = 0 dBm0, f = 1.02 kHz, Unity gain, PCM IN = lowest decode level, Measured at PWRO+	71			dB
Crosstalk attenuation, receive to transmit (single ended)		PCM IN = 0 dBm0, f = 1.02 kHz, Measured at PCM OUT	71			dB

† All typical values are at V_{BB} = –5 V, V_{CC} = 5 V, and T_A = 25°C.

distortion over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit signal-to-distortion ratio, sinusoidal input (CCITT G.712 – Method 2)	0 dBm0 ≥ ANLG IN+ ≥ −30 dBm0	36			dB
	−30 dBm0 > ANLG IN+ ≥ −40 dBm0	30			
	−40 dBm0 > ANLG IN+ ≥ −45 dBm0	25			
Receive signal-to-distortion ratio, sinusoidal input (CCITT G.712 – Method 2)	0 dBm0 ≥ ANLG IN+ ≥ −30 dBm0	36			dB
	−30 dBm0 > ANLG IN+ ≥ −40 dBm0	30			
	−40 dBm0 > ANLG IN+ ≥ −45 dBm0	25			
Transmit single-frequency distortion products	AT&T Advisory #64 (3.8), Input signal = 0 dBm0			−46	dBm0
Receive single-frequency distortion products	AT&T Advisory #64 (3.8), Input signal = 0 dBm0			−46	dBm0
Intermodulation distortion, end-to-end spurious out-of-band signals, end-to-end	CCITT G.712 (7.1)			−35	dBm0
	CCITT G.712 (7.2)			−49	
	CCITT G.712 (6.1)			−25	
	CCITT G.712 (9)			−40	
Transmit absolute delay time to PCM OUT	Fixed-data rate, f_{CLKX} + 2.048 MHz, Input to ANLG IN + 1.02 kHz at 0 dBm0		245		µs
Transmit differential envelope delay time relative to transmit absolute delay time	f = 500 Hz to 600 Hz		170		µs
	f = 600 Hz to 1000 Hz		95		
	f = 1000 Hz to 2600 Hz		45		
	f = 2600 Hz to 2800 Hz		105		
Receive absolute delay time to PWRO+	Fixed-data rate, f_{CLKR} + 2.048 MHz, Digital input is DMW code		190		µs
Receive differential envelope delay time relative to transmit absolute delay time	f = 500 Hz to 600 Hz		45		µs
	f = 600 Hz to 1000 Hz		35		
	f = 1000 Hz to 2600 Hz		85		
	f = 2600 Hz to 2800 Hz		110		

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

transmit filter transfer over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	Input amplifier set for unity gain, Noninverting maximum gain output, Input signal at ANLG IN+ is 0 dBm0	f = 16.67 Hz		−30	dB
		f = 50 Hz		−25	
		f = 60 Hz		−23	
		f = 200 Hz	−1.8	−0.125	
		f = 300 Hz to 3 kHz	−0.15	0.15	
		f = 3.3 kHz	−0.35	0.15	
		f = 3.4 kHz	−1	−0.1	
		f = 4 kHz		−14	
		f = 4.6 kHz and above		−32	

receive filter transfer over recommended ranges of supply voltage and operating free-air temperature (see Figure 2)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	Input signal at PCM IN is 0 dBm0	f < 200 Hz		0.15	dB
		f = 200 Hz	−0.5	0.15	
		f = 300 Hz to 3 kHz	−0.15	0.15	
		f = 3.3 kHz	−0.35	0.15	
		f = 3.4 kHz	−1	−0.1	
		f = 4 kHz		−14	
		f ≥ 4.6 kHz		−30	

timing requirements

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 3 and 4)

		MIN	TYP†	MAX	UNIT
$t_{c(CLK)}$	Clock period for CLKX, CLKR (2.048-MHz systems)	488			ns
t_r, t_f	Rise and fall times for CLKX and CLKR		5	30	ns
$t_{w(CLK)}$	Pulse duration for CLKX and CLKR (see Note 7)	220			ns
$t_{w(DCLK)}$	Pulse duration, DCLK (f_{DCLK} = 64 kHz to 2.048 MHz) (see Note 7)	220			ns
	Clock duty cycle, $[t_{w(CLK)}/t_{c(CLK)}]$ for CLKX and CLKR	45%	50%	55%	

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.
NOTE 7: FSX CLK must be phase locked with CLKX. FSR CLK must be phase locked with CLKR.

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 3)

		MIN	MAX	UNIT
$t_{d(FSX)}$	Frame-sync delay time	100	$t_{c(CLK)}$ −100	ns
$t_{su(SIGX)}$	Setup time before bit 7 falling edge of CLKX (TMC29C14 and TCM129C14 only)	0		ns
$t_{h(SIGX)}$	Hold time after bit 8 falling edge of CLKX (TCM29C13 and TCM129C14 only)	0		ns

receive timing requirements over recommended ranges of supply voltages and operating free-air temperature, fixed-data-rate mode (see Figure 4)

PARAMETER		MIN	MAX	UNIT
$t_{d(FSR)}$	Frame-sync delay time	100	$t_{c(CLK)}$−100	ns
$t_{su(PCM\ IN)}$	Setup time before bit 1 falling edge (TCM129C14 and TCM29C14 only)	10		ns
$t_{h(PCM\ IN)}$	Hold time after bit 1 falling edge (TCM129C14 and TCM29C14 only)	60		ns

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 5)

PARAMETER		MIN	MAX	UNIT
$t_{d(TSDX)}$	Time-slot delay time from DCLKX (see Note 8)	140	$t_{d(DCLKX)}$−140	ns
$t_{d(FSX)}$	Frame-sync delay time	100	$t_{c(CLK)}$−100	ns
$t_{c(DCLKX)}$	Clock period for DCLKX	488	15620	ns

NOTE 8: t_{FSLX} minimum requirement overrides the $t_{d(TSDX)}$ maximum requirement for 64-kHz operation.

receive timing requirements over recommended ranges of supply voltages and operating free-air temperature, variable-data-rate mode (see Figure 6)

PARAMETER		MIN	MAX	UNIT
$t_{d(TSDR)}$	Time-slot delay time from DCLKR (see Note 9)	140	$t_{d(DCLKR)}-140$	ns
$t_{d(FSR)}$	Frame-sync delay time	100	$t_{c(CLK)}-100$	ns
$t_{su(PCM\ IN)}$	Setup time before bit 3 falling edge	10		ns
$t_{h(PCM\ IN)}$	Hold time after bit 4 falling edge	60		ns
$t_{c(DCLKR)}$	Data clock period	488	15620	ns
t_{SER}	Time-slot end receive time	0		ns

NOTE 9: t_{FSLR} minimum requirement overrides the $t_{d(TSDR)}$ maximum requirement for 64-kHz operation.

64-kbit operation timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{FSLX}	Transmit frame-sync minimum down time	FSX = TTL high for remainder of frame	488		ns
t_{FSLR}	Receive frame-sync minimum down time	FSR = TTL high for remainder of frame	1952		ns
$t_{w(DCLK)}$	Pulse duration, data clock			10	µs

switching characteristics

propagation delay times over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figures 3 and 4)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	From rising edge of transmit clock to bit 1 data valid at PCM OUT (data enable time on time-slot entry) (see Note 10)	C_L = 0 to 100 pF	0	145	ns
t_{pd2}	From rising edge of transmit clock bit n to bit n data valid at PCM OUT (data valid time)	C_L = 0 to 100 pF	0	145	ns
t_{pd3}	From falling edge of transmit clock bit 8 to bit 8 Hi-Z at PCM OUT (data float time on time-slot exit) (see Note 10)	C_L = 0	60	215	ns
t_{pd4}	From rising edge of transmit clock bit 1 to TSX active (low) (time-slot enable time)	C_L = 0 to 100 pF	0	145	ns
t_{pd5}	From falling edge of transmit clock bit 8 to TSX inactive (high) (time-slot disable time) (see Note 10)	C_L = 0	60	190	ns
t_{pd6}	From rising edge of channel time slot to SIGR update (TCM129C14 and TCM29C14 only)		0	2	µs

NOTE 10: Timing parameters t_{pd1}, t_{pd3}, and t_{pd5} are referenced to the high-impedance state.

propagation delay times over recommended ranges of operating conditions, variable-data-rate mode (see Note 11 and Figure 5)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd7}	Data delay time from DCLKX	C_L = 0 to 100 pF	0	100	ns
t_{pd8}	Data delay time from time-slot enable to PCM OUT	C_L = 0 to 100 pF	0	50	ns
t_{pd9}	Data delay time from time-slot disable to PCM OUT	C_L = 0 to 100 pF	0	80	ns
t_{pd10}	Data delay time from FSX	$t_{d(TSDX)}$ = 80 ns	0	140	ns

NOTE 11: Timing parameters t_{pd8} and t_{pd9} are referenced to a high-impedance state.

PARAMETER MEASUREMENT INFORMATION

CLKR and CLKX selection requirements for DSP-based applications

1. Note that CLKX and CLKR must be selected as follows:

CLKSEL	CLKR, CLKX (BETWEEN 1 MHz to 3 MHz)	DEVICE TYPE
–5 V†	= (256) × (frame-sync frequency)	TCM29C13/14/16/17
		TCM129C13/14/16/17
0 V	= (193) × (frame-sync frequency)	TCM29C13/14
		TCM129C13/14
5 V	= (192) × (frame-sync frequency)	TCM29C13/14
		TCM129C13/14

e. g., for frame-sync frequency = 9.6 kHz

CLKSEL	CLKR, CLKX (BETWEEN 1 MHz to 3 MHz)	DEVICE TYPE
–5 V†	= 2.4576 MHz	TCM29C13/14/16/17
		TCM129C13/14/16/17
0 V	= 1.8528 MHz	TCM29C13/14
		TCM129C13/14
5 V	= 1.8432 MHz	TCM29C13/14
		TCM129C13/14

† CLKSEL is internally set to –5 V for TCM129C16/17 and TCM29C16/17.

2. Corner frequency at 8-kHz frame-sync frequency = 3 kHz
   Therefore, the corner frequency = (3/8) × (frame-sync frequency for nonstandard frame sync).

PARAMETER MEASUREMENT INFORMATION

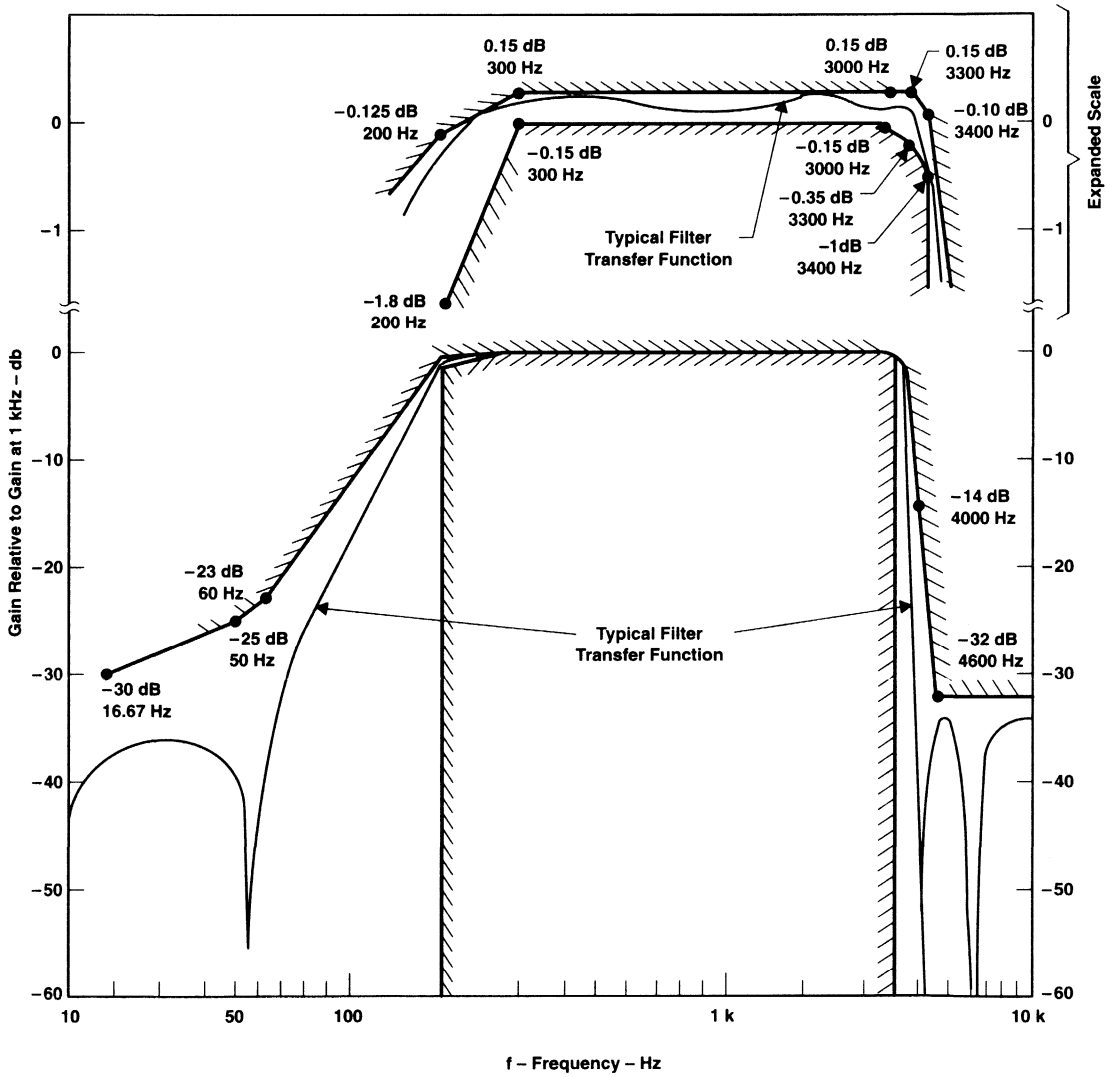
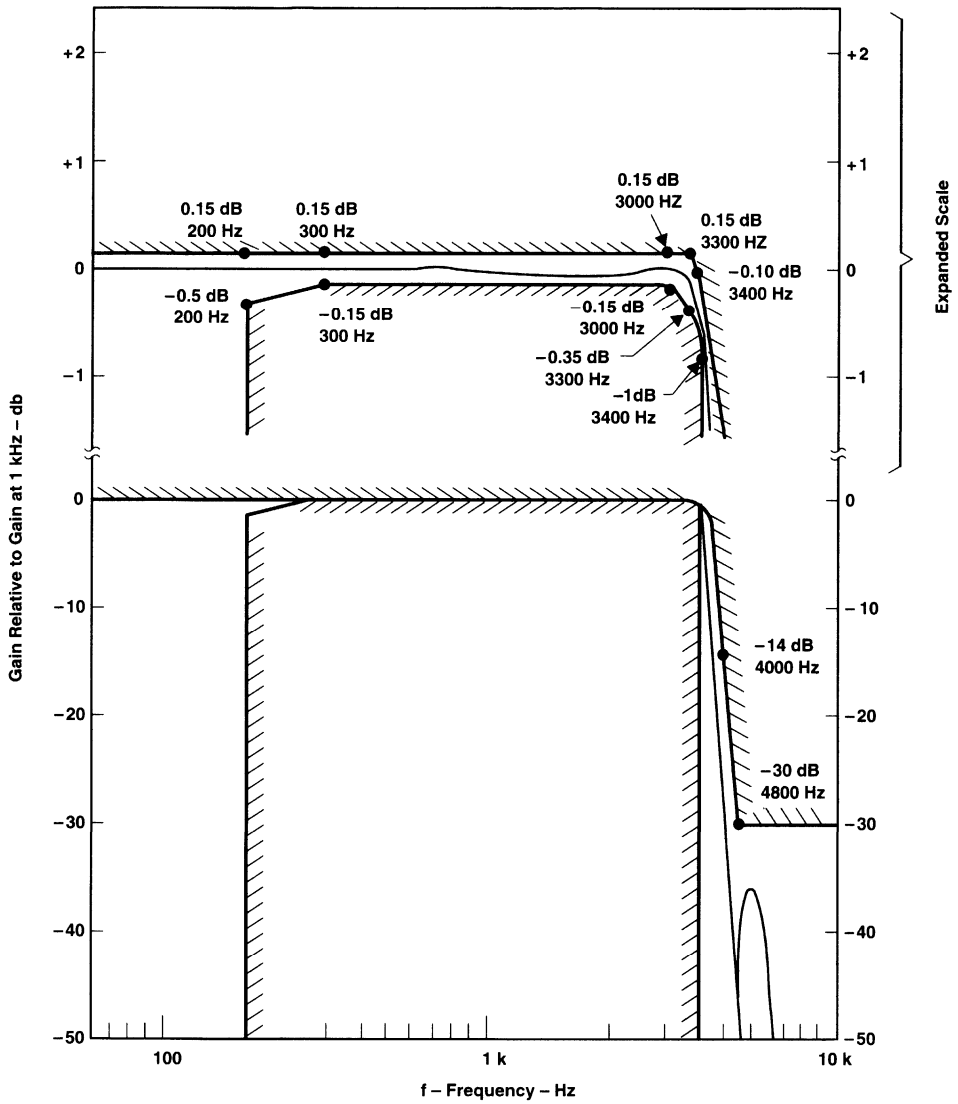


Figure 1. Transfer Characteristics of the Transmit Filter

PARAMETER MEASUREMENT INFORMATION



NOTE A: This is a typical transfer function of the receive filter component.

Figure 2. Transfer Characteristics of the Receive Filter

PARAMETER MEASUREMENT INFORMATION

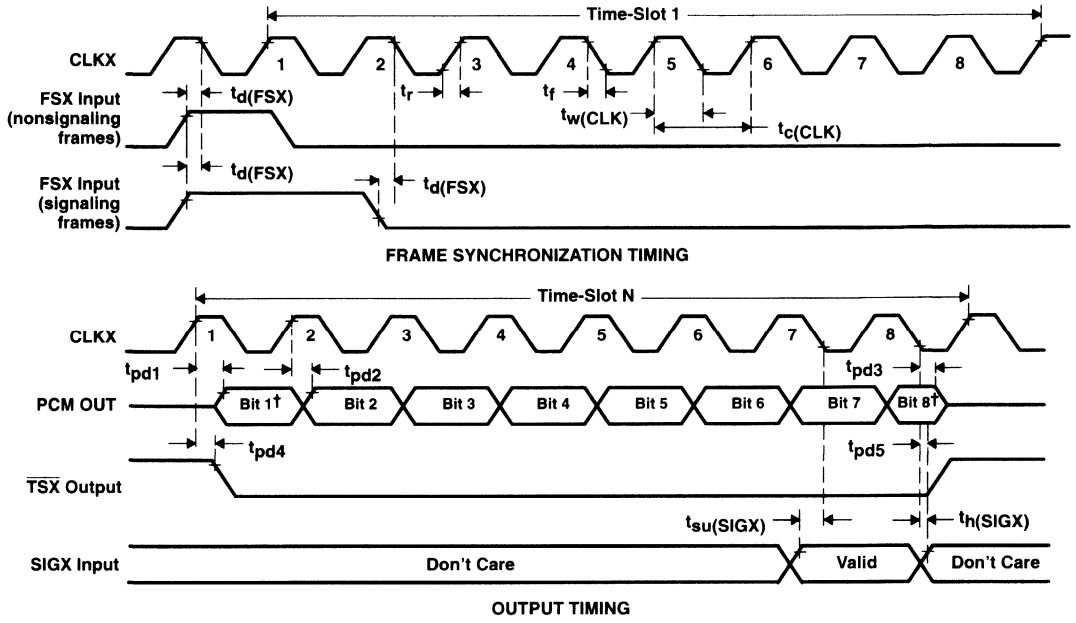


Figure 3. Transmit Timing (Fixed-Data Rate)

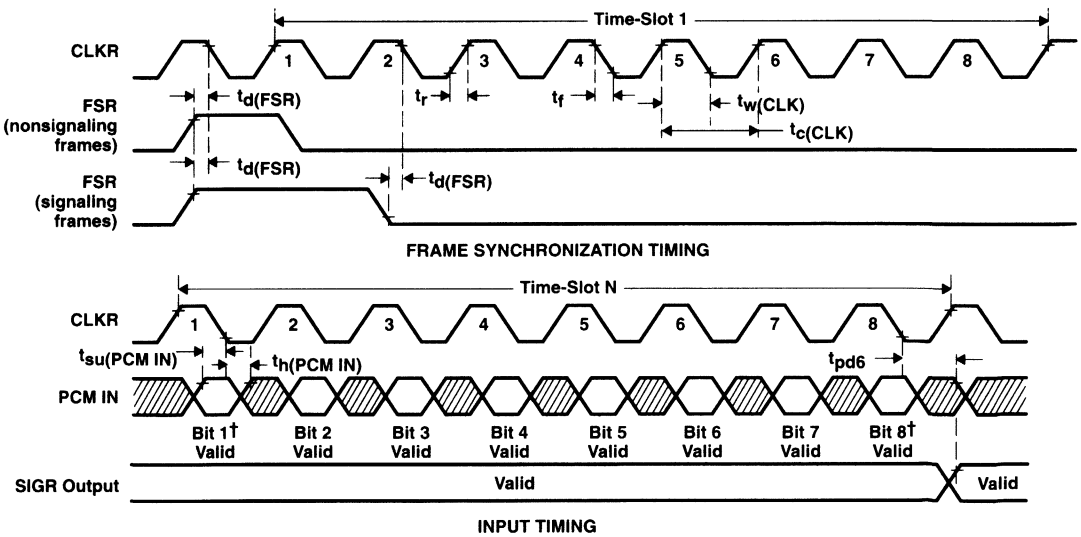


Figure 4. Receive Timing (Fixed-Data Rate)

† Bit 1 = MSB = sign bit and is clocked in first on PCM IN or clocked out first on PCM OUT. Bit 8 = LSB = least significant bit and is clocked in last on PCM IN or is clocked out last on PCM OUT.

NOTE A: Inputs are driven from 0.45 V to 2.4 V. Time intervals are referenced to 2 V if the high level is indicated and 0.8 V if the low level is indicated.

PARAMETER MEASUREMENT INFORMATION

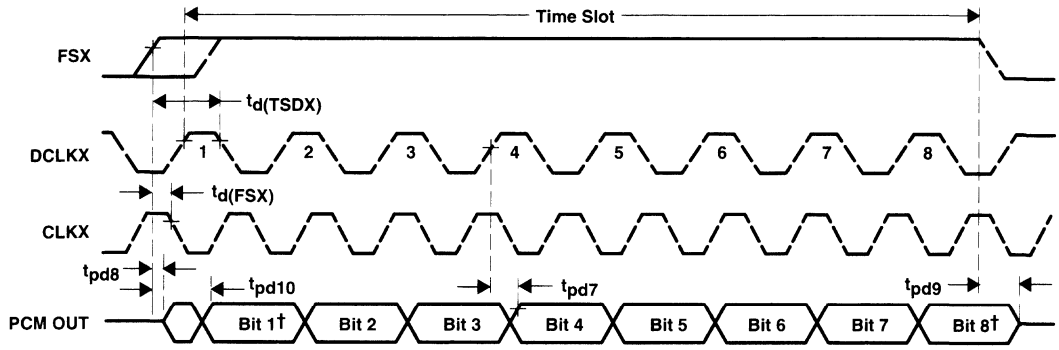


Figure 5. Transmit Timing (Variable-Data-Rate)

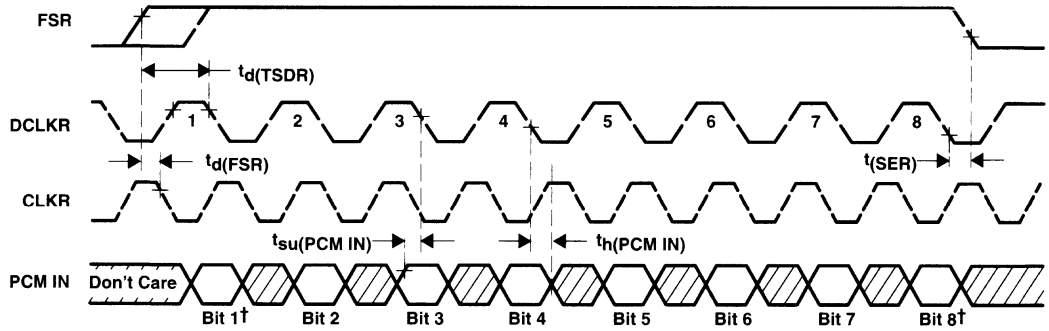


Figure 6. Receive Timing (Variable-Data-Rate)

† Bit 1 = MSB = sign bit and is clocked in first on PCM IN or clocked out first on PCM OUT. Bit 8 = LSB = least significant bit and is clocked in last on PCM IN or is clocked out last on PCM OUT.

NOTE A: All timing parameters are referenced to V_{IH} and V_{IL} except t_{pd8} and t_{pd9}, which references the high-impedance state.

PRINCIPLES OF OPERATION

system reliability and design considerations

General TCM29C13, TCM29C14, TCM29C16, TCM29C17, TCM129C13, TCM129C14, TCM129C16, and TCM129C17 system reliability and design considerations are described in the following paragraphs.

latch-up

Latch-up is possible in all CMOS devices. It is caused by the firing of a parasitic SCR that is present due to the inherent nature of CMOS. When a latch-up occurs, the device draws excessive amounts of current and will continue to draw heavy current until power is removed. Latch-up can result in permanent damage to the device if supply current to the device is not limited.

Even though the TCM29Cxx and TCM129Cxx are heavily protected against latch-up, it is still possible to cause latch-up under certain conditions in which excess current is forced into or out of one or more terminals. Latch-up can occur when the positive supply voltage drops momentarily below ground, when the negative supply voltage rises momentarily above ground, or possibly if a signal is applied to a terminal after power has been applied but before the ground is connected. This can happen if the device is hot-inserted into a card with the power applied, or if the device is mounted on a card that has an edge connector, and the card is hot-inserted into a system with the power on.

To help ensure that latch-up does not occur, it is considered good design practice to connect a reverse-biased Schottky diode (with a forward voltage drop of less than or equal to 0.4 V — 1N5711 or equivalent), between each power supply and GND (see Figure 7). If it is possible that a TCM29Cxx- or TCM129Cxx-equipped card that has an edge connector could be hot-inserted into a powered-up system, it is also important to ensure that the ground edge connector traces are longer than the power and signal traces so that the card ground is always the first to make contact.

device power-up sequence

Latch-up can also occur if a signal source is connected without the device being properly grounded. A signal applied to one terminal could then find a ground through another signal terminal on the device. To ensure proper operation of the device and as a safeguard against this sort of latch-up, it is recommended that the following power-up sequence always be used:

1. Ensure no signals are applied to the device before the power-up sequence is complete.
2. Connect GND.
3. Apply V_{BB} (most negative voltage).
4. Apply V_{CC} (most positive voltage).
5. Force a power down condition in the device.
6. Connect the clocks.
7. Release the power-down condition.
8. Apply FSX and/or FXR synchronization pulses.
9. Apply signal inputs.

When powering down the device, this procedure should be followed in the reverse order.

PRINCIPLES OF OPERATION

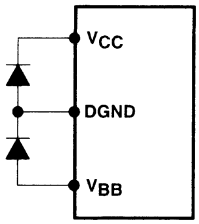


Figure 7. Diode Configuration for Latch-Up Protection Circuitry

internal sequencing

On the transmit channel, digital outputs PCM OUT and $\overline{TSX}$ are held in the high-impedance state for approximately four frames (500 µs) after power up or application of V_{BB} or V_{CC}. After this delay, PCM OUT, $\overline{TSX}$, and signaling are functional and occur in the proper time slot. The analog circuits on the transmit side require approximately 60 ms to reach their equilibrium value due to the autozero circuit settling time. Therefore, valid digital information, such as on/off hook detection, is available almost immediately while analog information is available after some delay.

On the receive channel, the digital output SIGR is also held low for a maximum of four frames after power up or application of V_{BB} or V_{CC}. SIGR remains low until it is updated by a signaling frame.

To further enhance system reliability, PCM OUT and $\overline{TSX}$ are placed in the high-impedance state approximately 20 µs after an interruption of CLKX. SIGR is held low approximately 20 µs after an interruption of CLKR. These interruptions could possibly occur with some kind of fault condition.

power-down and standby operations

To minimize power consumption, a power-down mode and three standby modes are provided.

For power down, an external low signal is applied to $\overline{PDN}$. In the absence of a signal, $\overline{PDN}$ is internally pulled up to a high logic level and the device remains active. In the power-down mode, the average power consumption is reduced to 5 mW.

Three standby modes give the user the options of placing the entire device on standby, placing only the transmit channel on standby, or placing only the receive channel on standby. To place the entire device on standby, both FSX and FSR are held low. For transmit-only operation (receive channel on standby), FSX is high and FSR is held low. For receive-only operation (transmit section on standby), FSR is high and FSX is held low. When the entire device is in standby mode, power consumption is reduced to an average of 3 mW. See Table 1 for power-down and standby procedures.

Table 1. Power-Down and Standby Procedures

DEVICE STATUS	PROCEDURE	TYPICAL POWER CONSUMPTION	DIGITAL OUTPUT STATUS
Power down	$\overline{PDN}$ low	3 mW	$\overline{TSX}$ and PCM OUT are in the high-impedance state; SIGR goes low within 10 µs.
Entire device on standby	FSX and FSR are low	3 mW	$\overline{TSX}$ and PCM OUT are in the high-impedance state; SIGR goes low within 300 ms.
Only transmit on standby	FSX is low, FSR is high	40 mW	$\overline{TSX}$ and PCM OUT are placed in the high-impedance state within 300 ms.
Only receive on standby	FSR is low, FSX is high	30 mW	SIGR is placed in the high-impedance state within 300 ms.

PRINCIPLES OF OPERATION

fixed-data-rate timing (see Figure 8)

Fixed-data-rate timing is selected by connecting DCLKR to V_{BB} and uses master clocks CLKX and CLKR, frame-synchronizer clocks FSX and FSR, and output $\overline{TSX}$. FSX and FSR are 8-kHz inputs that set the sampling frequency and distinguish between signaling and nonsignaling frames by their pulse durations. A frame synchronization pulse one master-clock period long designates a nonsignaling frame, while a double-length sync pulse enables the signaling function (TCM29C14 and TCM129C14 only). Data is transmitted on PCM OUT on the first eight positive transitions of CLKX following the rising edge of FSR. Data is received on PCM IN on the first eight falling edges of CLKR following FSR. A digital-to-analog (D/A) conversion is performed on the received digital word, and the resulting analog sample is held on an internal sample-and-hold capacitor until transferred to the receive filter.

The clock-selection pin (CLKSEL) is used to select the frequency of CLKX and CLKR (TCM29C13, TCM29C14, TCM129C13, and TCM129C14 only). The TCM29C13, TCM29C14, TCM129C13, and TCM129C14 fixed-data-rate mode can operate with frequencies of 1.536 MHz, 1.544 MHz, or 2.048 MHz. The TCM29C16, TCM29C17, TCM129C16, and TCM129C17 fixed-data-rate mode operates at 2.048 MHz only.

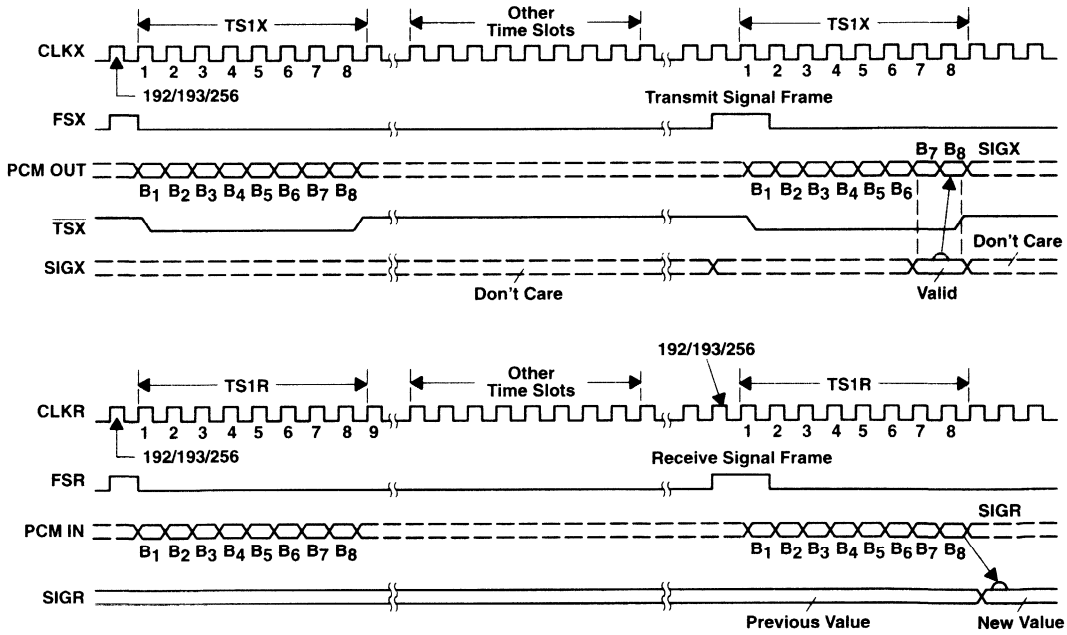


Figure 8. Signaling Timing (Fixed-Data-Rate Only)

PRINCIPLES OF OPERATION

variable-data-rate timing

Variable-data-rate timing is selected by connecting DCLKR to the bit clock for the receive PCM highway rather than to V_{BB}. It uses master clocks CLKX and CLKR, bit clocks DCLKX and DCLKR, and frame-synchronization clocks FSX and FSR.

Variable-data-rate timing allows for a flexible data frequency. The frequency of the bit clocks can be varied from 64 kHz to 2.048 MHz. Master clocks in the TCM29C13, TCM29C14, TCM129C13, and TCM129C14 are restricted to frequencies of operation of 1.536 MHz, 1.544 MHz, or 2.048 MHz as in the fixed-data-rate timing mode. The master clock for the TCM29C16, TCM29C17, TCM129C16, and TCM129C17 is restricted to 2.048 MHz.

When the FSX/TSXE is high, PCM data is transmitted from PCM OUT onto the highway on the next eight consecutive positive transitions of DCLKX. Similarly, while the FSR/TSRE input is high, the PCM word is received from the highway by PCM IN on the next eight consecutive negative transitions of DCLKR.

The transmitted PCM word is repeated in all remaining time slots in the 125-μs frame as long as DCLKX is pulsed and FSX is held high. This feature, which allows the PCM word to be transmitted to the PCM highway more than once per frame if desired, is available only with variable-data-rate timing. Signaling is allowed only in the fixed-data-rate mode because the variable-data-rate mode provides no means with which to specify a signaling frame.

signaling

The TCM29C14 (only) provides 8th-bit signaling in the fixed-data-rate timing mode. Transmit and receive signaling frames are independent of each other and are selected by a double-width frame-sync pulse on the appropriate channel. During a transmit signaling frame, the signal present on SIGX is substituted for the least significant bit (LSB) of the encoded PCM word. In a receive signaling frame, the codec decodes the seven most significant bits in accordance with CCITT G.733 recommendations and outputs the logical state of the LSB on SIGR until it is updated in the next signaling frame. Timing relationships for signaling operations are shown in Figure 8. The signaling path is used to transmit digital signaling information such as ring control, rotary dial pulses, and off-hook and disconnect supervision. The voice path is used to transmit prerecorded messages as well as the call progress tones: dial tone, ring-back tone, busy tone, and reorder tone.

PRINCIPLES OF OPERATION

analog loopback

A distinctive feature of the TCM29C14 and TCM129C14 is the analog loopback capability. With this feature, the user can test the line circuit remotely by comparing the signals sent into the receive channel (PCM IN) with those generated on the transmit channel (PCM OUT). The test is accomplished by sending a control signal that internally connects the analog input and output ports. When ANLG LOOP is TTL high, the receive output (PWRO+) is internally connected to ANLG IN+, GSR is internally connected to PWRO–, and ANLG IN– is internally connected to GSX (see Figure 9).

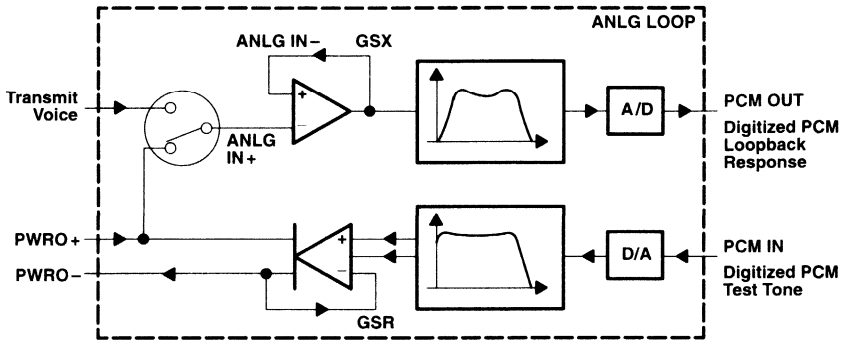


Figure 9. TCM129C14 and TCM29C14 Analog Loopback Configuration

Due to the difference in the transmit and receive transmission levels, a 0-dBm0 code into PCM IN emerges from PCM OUT as a 3-dBm0 code, an implicit gain of 3 dB. Because of this, the maximum signal that can be tested by analog loopback is 0 dBm0.

precision voltage references

Voltage references that determine the gain dynamic range characteristics of the device are generated internally. No external components are required to provide the voltage references. A difference in subsurface charge density between two suitably implanted MOS device is used to derive a temperature- and bias-stable reference voltage, which is calibrated during the manufacturing process. Separate references are supplied to the transmit and receive sections, and each is calibrated independently. Each reference value is then further trimmed in the gain-setting operational amplifiers to a final precision value. Manufacturing tolerances of typically ±0.04 dB can be achieved in absolute gain for each half channel, providing the user a significant margin to compensate for error in other system components.

PRINCIPLES OF OPERATION

conversion laws

The TCM29C13, TCM29C14, TCM129C13, and TCM129C14 provide pin-selectable μ-law or A-law operation as specified by CCITT G.711 recommendation. A-law operation is selected when ASEL is connected to V_{BB}, and μ-law operation is selected by connecting ASEL to V_{CC} or GND. Signaling is not allowed during A-law operation. If μ-law operation is selected, SIGX is a TTL-level input that can be used in the fixed-data-rate timing mode to modify the LSB of the PCM output is signaling frames.

The TCM29C16 and TCM129C16 are μ-law only; the TCM29C17 and TCM129C17 are A-law only.

transmit operation

transmit filter

The input section provides gain adjustment in the pass band by means of an on-chip uncommitted operational amplifier. The load impedance to ground (ANLG GND) at the amplifier output (GSX) must be greater than 10 kΩ in parallel with less than 50 pF. The input signal on ANLG IN+ can be either ac or dc coupled. The input operational amplifier can also be used in the inverting mode or differential amplifier mode.

A low-pass antialiasing filter section is included on the device. This section provides 35-dB attenuation at the sampling frequency. No external components are required to provide the necessary antialiasing function for the switched-capacitor section of the transmit filter.

The pass-band section provides flatness and stop-band attenuation that fulfills the AT&T D3/D4 channel bank transmission specification and CCITT recommendation G.712. The device specifications meet or exceed digital class 5 central office switching-systems requirements.

A high-pass section configuration has been chosen to reject low-frequency noise from 50- and 60-Hz power lines, 17-Hz European electric railroads, ringing frequencies and their harmonics, and other low-frequency noise. Even with the high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200 Hz. This feature allows the use of low-cost transformer hybrids without external components.

encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample-and-hold capacitor. The encoder performs an analog-to-digital conversion on a switched-capacitor array. Digital data representing the sample is transmitted on the first eight data clock bits of the next frame.

The autozero circuit corrects for dc offset on the input signal to the encoder. The autozero circuit uses the sign-bit-averaging technique. The sign bit from the encoder output is long-term averaged and subtracted from the input to the encoder. All dc offset is removed from the encoder input waveform.

receive operation

decoding

The serial PCM word is received at PCM IN on the first eight data clock bits of the frame. Digital-to-analog conversion is performed, and the corresponding analog sample is held on an internal sample-and-hold capacitor. This sample is transferred to the receive filter.

receive filter

The receive section of the filter provides pass-band flatness and stop-band rejection that fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin x)/x response of such decoders.

PRINCIPLES OF OPERATION

receive output power amplifiers

A balanced-output amplifier is provided to allow maximum flexibility in output configuration. Either of the two outputs can be used single ended (i.e., referenced to ANLG GND) to drive single-ended loads. Alternatively, the differential output directly drives a bridged load. The output stage is capable of driving loads as low as 300-Ω single-ended to a level of 12 dBm or 600 Ω differentially to a level of 15 dBm.

The receive channel transmission level may be adjusted between specified limits by manipulation of the GSR input. GSR is internally connected to an analog gain-setting network. When GSR is connected to PWRO–, the receive level is maximum. When GSR is connected to PWRO+, the level is minimum. The output transmission level is adjusted between 0 and –12 dB as GSR is adjusted (with an adjustable resistor) between PWRO+ and PWRO–.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions (i.e., when the digital input at PCM IN is the eight-code sequence specified in CCITT recommendation G.711).

APPLICATION INFORMATION

output gain-set design considerations (see Figure 9)

PWRO+ and PWRO– are low-impedance complementary outputs. The voltages at the nodes are:

V_{O+} at PWRO+
V_{O-} at PWRO–
$V_{OD} = V_{O+} - V_{O-}$ (total differential response)

R1 and R2 are a gain-setting resistor network with the center tap to the GSR input.

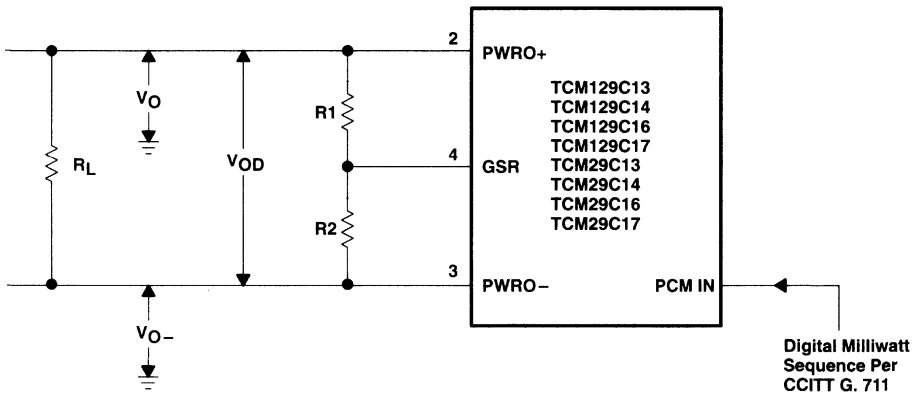
A value greater than 10 kΩ and less than 100 kΩ for R1 + R2 is recommended because of the following:

The parallel combination of R1 + R2 and R_L sets the total loading.
The total capacitance at the GSR input and the parallel combination of R1 and R2 define a time constant that has to be minimized to avoid inaccuracies.

V_A represents the maximum available digital milliwatt output response (V_A = 3.006 Vrms).

$$V_{OD} = A \times V_A$$

$$\text{where } A = \frac{1 + (R1/R2)}{4 + (R1/R2)}$$



Pin numbers shown are for the TCM29C13, TCM29C14, TCM129C13, and TCM129C14 package only.

Figure 10. Gain-Setting Configuration

TCM29C13A, TCM29C14A, TCM29C16A, TCM29C17A, TCM129C13A, TCM129C14A, TCM129C16A, TCM129C17A COMBINED SINGLE-CHIP PCM CODEC AND FILTER

SCTS030D – AUGUST 1989 – REVISED JULY 1996

- **Replace Use of TCM2910A and TCM2911A in Tandem With TCM2912B/C**
- **Reliable Silicon-Gate CMOS Technology**
- **Low Power Consumption:**
  Operating Mode . . . 80 mW Typical
  Power-Down Mode . . . 5 mW Typical
- **Excellent Power-Supply Rejection Ratio Over Frequency Range of 0 Hz to 50 kHz**
- **No External Components Needed for Sample, Hold, and Autozero Functions**
- **Precision Internal Voltage References**
- **Improved Version of TCM29C13 Series and TCM129C13 Series**

FEATURES TABLE

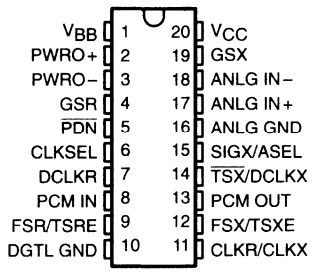
FEATURE	29C13A 129C13A	29C14A 129C14A	29C16A 129C16A	29C17A 129C17A
Number of Pins:				
24		X		
20	X			
16			X	X
μ-Law/A-Law Coding:				
μ-Law	X	X	X	
A-Law	X	X		
Gain Timing Rates:				
Variable Mode				
64 kHz to 2.048 MHz	X	X	X	X
Fixed Mode				
1.536 MHz	X	X		
1.544 MHz	X	X		
2.048 MHz	X	X	X	X
Loopback Test Capability		X		
8th-Bit Signaling		X		

description

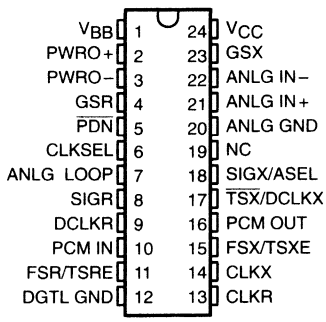
The TCM29C13A, TCM29C14A, TCM29C16A, TCM29C17A, TCM129C13A, TCM129C14A, TCM129C16A, and TCM129C17A are single-chip PCM codecs (pulse-code-modulated encoders and decoders) and PCM line filters. These devices provide all the functions required to interface a full-duplex (4-wire) voice telephone circuit with a time-division-multiplexed (TDM) system. These devices are intended to replace the TCM2910A or TCM2911A in tandem with the TCM2912C. Primary applications include:

- Line interface for digital transmission and switching of T1 carrier, PABX, and central office telephone systems
- Subscriber line concentrators
- Digital-encryption systems
- Digital voice-band data storage systems
- Digital signal processing

TCM29C13A, TCM129C13A
DW OR N PACKAGE
(TOP VIEW)

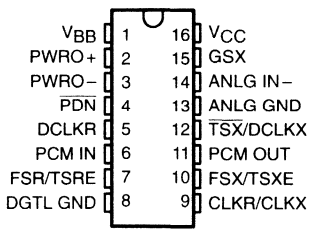


TCM29C14A, TCM129C14A
DW PACKAGE
(TOP VIEW)



NC – No internal connection

TCM29C16, TCM29C16A,
TCM129C16, TCM129C17A
DW OR N PACKAGE
(TOP VIEW)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

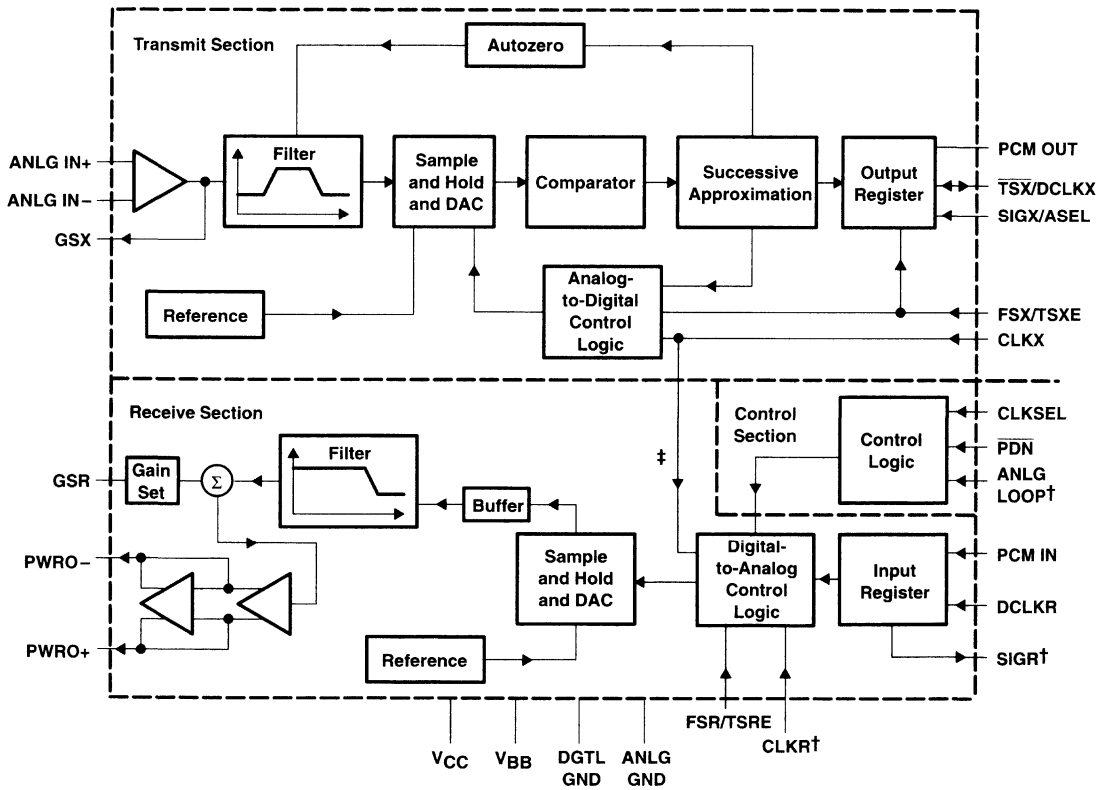
description (continued)

These devices are designed to perform the transmit encoding (A/D conversion) and receive decoding (D/A conversion) as well as the transmit and receive filtering functions in a pulse-code-modulated system. They are intended to be used at the analog termination of a PCM line or trunk.

The TCM29C13A, TCM29C13A, TCM29C16A, TCM29C17A, TCM129C13A, TCM129C14A, TCM129C16A, and TCM129C17A provide the band-pass filtering of the analog signals prior to encoding and after decoding. These combination devices perform the encoding and decoding of voice and call progress tones as well as the signaling and supervision information. These devices contain patented circuitry to achieve low transmit channel idle noise and are not recommended for applications in which the composite signals on the transmit side are below −55 dBm0.

The TCM29C13A, TCM29C14A, TCM29C16A, and TCM29C17A are characterized for operation from 0°C to 70°C. The TCM129C13A, TCM129C14A, TCM129C16A, and TCM129C17A are characterized for operation from −40°C to 85°C.

functional block diagram



† TCM29C14A and TCM129C14A only.
‡ TCM29C13A, TCM29C16A, TCM29C17A, TCM129C13A, TCM129C16A, and TCM129C17A only

Terminal Functions

NAME	TERMINAL NO.			I/O	DESCRIPTION
	TCM29C13A TCM129C13A	TCM29C14A TCM129C14A	TCM29C16A TCM29C17A TCM129C16A TCM129C17A		
ANLG GND	16	20	13		Analog ground return for all internal voice circuits. Not internally connected to DGTL GND.
ANLG IN+	17	21		I	Noninverting analog input to uncommitted transmit operational amplifier. Internally connected to ANLG GND on TCM29C16A, TCM129C16A, TCM29C17A, and TCM129C17A.
ANLG IN–	18	22	14	I	Inverting analog input to uncommitted transmit operational amplifier.
ANLG LOOP		7		I	Provides loopback test capability. When this input is high, PWRO+ is internally connected to ANLG IN.
CLKR	11	13	9	I	Receive master clock and data clock for the fixed-data-rate mode. Receive master clock only for variable-data-rate mode. CLKR and CLKX are internally connected together for TCM29C13A, TCM29C16A, TCM29C17A, TCM129C13A, TCM129C16A, and TCM129C17A.
CLKSEL	6	6		I	Clock-frequency selection. Input must be connected to V_{BB}, V_{CC}, or ground to reflect the master clock frequency. When tied to V_{BB}, CLK is 2.048 MHz. When tied to ground, CLK is 1.544 MHz. When tied to V_{CC}, CLK is 1.536 MHz.
CLKX	11	14	9	I	Transmit master clock and data clock for the fixed-data-rate mode. Transmit master clock only for variable-date-rate mode. CLKR and CLKX are internally connected for the TCM29C13A, TCM29C16A, TCM29C17A, TCM129C13A, TCM129C16A, and TCM129c17A.
DCLKR	7	9	5	I	Selects fixed- or variable-data-rate operation. When DCLKR is connected to V_{BB}, the device operates in the fixed-data-rate mode. When DCLKR is not connected to V_{BB}, the device operates in the variable-data-rate mode and DCLKR becomes the receiver data clock, which operates at frequencies from 64 kHz to 2.048 MHz.
DGTL GND	10	12	8		Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
FSR/TSRE	9	11	7	I	Frame-synchronization clock input/time-slot enable for receive channel. In the fixed-data-rate mode, FSR distinguishes between signaling and nonsignaling frames by a double- or single-length pulse, respectively. In the variable-data-rate mode, this signal must remain high for the duration of the time slot. The receive channel enters the standby state when FSR is TTL low for 300 ms.
FSX/TSXE	12	15	10	I	Frame-synchronization clock input/time-slot enable for transmit channel. Operates independently of, but in an analagous manner to, FSR/TSRE. The transmit channel enters the standby state when FSX is low for 300 ms.
GSR	4	4		I	Input to the gain-setting network on the output power amplifier. Transmission level can be adjusted over a 12-dB range depending upon the voltage at GSR.
GSX	19	23	15	O	Output terminal of internal uncommitted operational amplifier. Internally, this is the voice signal input to the transmit filter.

Terminal Functions (Continued)

NAME	TERMINAL			I/O	DESCRIPTION
	TCM29C13A TCM129C13A	TCM29C14A TCM129C14A	TCM29C16A TCM29C17A TCM129C16A TCM129C17A		
PCM IN	8	10	6	I	Receive PCM input. PCM data is clocked in on this terminal on eight consecutive negative transitions of the receive data clock, which is CLKR in fixed-data-rate timing and DCLKR in variable-data-rate timing.
PCM OUT	13	16	11	O	Transmit PCM output. PCM data is clocked out on this output on eight consecutive positive transitions of the transmit data clock, which is CLKX in fixed-data-rate timing and DCLKX in variable-data-rate timing.
$\overline{\text{PDN}}$	5	5	4	I	Power-down select. The device is inactive with a TTL low-level input to this terminal and active with a TTL high-level input to this terminal.
PWRO+	2	2	2	O	Noninverting output of power amplifier. Can drive transformer hybrids or high-impedance loads directly in either a differential or a single-ended configuration.
PWRO–	3	3	3	O	Inverting output of power amplifier; functionally identical with and complementary to PWRO+.
SIGR		8		O	Signaling bit output, receive channel. In the fixed-data-rate mode, outputs the logical state of the 8th bit (LSB) of the PCM word in the most recent signaling frame.
SIGX/ASEL	15	18		I	A-law and μ-law operation select. When connected to V_{BB}, A-law is selected. When connected to V_{CC} or ground, μ-law is selected. When not connected to V_{BB}, it is a TTL-level input that is transmitted as the eighth bit (LBS) of the PCM word during signaling frames on PCM OUT (TCM29C14A and TCM129C14A only). SIGX/ASEL is internally connected to provide μ-law operational for TCM29C16A and TCM129C16A and A-law operation for TCM29C17A and TCM129C17A.
$\overline{\text{TSX}}$/DCLKX	14	17	12	I/O	Transmit channel time-slot strobe (output) or data clock (input) for the transmit channel. In the fixed-data-rate mode, this terminal is an open-drain output to be used as an enable signal for a 3-state output buffer. In the variable-data-rate mode, DCLKX becomes the transmit data clock, which operates at a TTL level from 64 kHz to 2.048 MHz.
V_{BB}	1	1	1		Most negative supply voltage. Input is –5 V ±5%.
V_{CC}	20	24	16		Most positive supply voltage. Input is 5 V ±5%.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.3 V to 15 V
Output voltage range, V_O . . . . . −0.3 V to 15 V
Input voltage range, V_I . . . . . −0.3 V to 15 V
Digital ground voltage range . . . . . −0.3 V to 15 V
Continuous total dissipation at (or below) 25°C free-air temperature . . . . . 1375 mW
Operating free-air temperature range, T_A: TCM29CxxA . . . . . 0°C to 70°C
TCM129CxxA . . . . . −40°C to 85°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values for maximum ratings are with respect to V_{BB}.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 3)		4.75	5	5.25	V
V_{BB}	Supply voltage		−4.75	−5	−5.25	V
	Digital ground voltage with respect to ANLG GND			0		V
V_{IH}	High-level input voltage, all inputs except CLKSEL		2.2			V
V_{IL}	Low-level input voltage, all inputs except CLKSEL				0.8	V
	CLKSEL input voltage	2.048 MHz	V_{BB}		V_{BB} +0.5	V
		1.544 MHz	0		0.5	
		1.536 MHz	V_{CC} −0.5		V_{CC}	
R_L	Load resistance	GSX	10			kΩ
		PWRO+ and/or PWRO−	300			Ω
C_L	Load capacitance	GSX			50	pF
		PWRO+ and/or PWRO−			100	
T_A	Operating free-air temperature	TCM29CxxA	0		70	°C
		TCM129CxxA	−40		85	

NOTES: 2. To avoid possible damage to these CMOS devices and resulting reliability problems, the power-up procedure described in the device power-up sequence paragraphs later in this document should be followed.
3. Voltage is at analog inputs and outputs. V_{CC} and V_{BB} terminals are with respect to ANLG GND. All other voltages are referenced to the digital ground unless otherwise noted.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

supply current, f_{DCLK} = 2.048 MHz, outputs not loaded

PARAMETER			TEST CONDITIONS	TCM29xxCA			TCM129xxCA			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{CC}	Supply current from V_{CC}	Operating			7	9		8	13	mA
		Standby	FSX or FSR at V_{IL} after 300 ms		0.5	1.1		0.7	1.5	
		Power down	$\overline{PDN}$ V_{IL} after 300 ms		0.3	0.9		0.4	1	
I_{BB}	Supply current from V_{BB}	Operating			−7	−9		−8	−13	mA
		Standby	FSX or FSR at V_{IL} after 300 ms		−0.5	−1		−0.7	−1.5	
		Power down	$\overline{PDN}$ V_{IL} after 300 ms		−0.3	−0.9		−0.4	−1.1	
P_D	Power dissipation	Operating			70	90		80	130	mW
		Standby	FSX or FSR at V_{IL} after 300 ms		5	10		7	15	
		Power down	$\overline{PDN}$ V_{IL} after 300 ms		3	8		4	10	

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

digital interface

PARAMETER			TEST CONDITIONS	TCM29xxCA			TCM129xxCA			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	PCM OUT	I_{OH} = −9.6 mA	2.4			2.4			V
		SIGR	I_{OH} = −1.2 mA	2.4			2.4			
V_{OL}	Low-level output voltage at PCM OUT, TSX, SIGR		I_{OL} = 3.2 mA			0.4			0.5	V
I_{IH}	High-level input current, any digital input		V_I = 2.2 V to V_{CC}			10			12	μA
I_{IL}	Low-level input current, any digital input		V_I = 0 to 0.8 V			10			12	μA
C_i	Input capacitance				5	10		5	10	pF
C_o	Output capacitance				5			5		pF

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

transmit amplifier input

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input current at ANLG IN+, ANLG IN−	V_I = −2.17 V to 2.17 V			±100	nA
Input offset voltage at ANLG IN+, ANLG IN−				±25	mV
Common-mode rejection at ANLG IN +, ANLG IN −		55			dB
Open-loop voltage amplification at GSX		5000			
Open-loop unity-gain bandwidth at GSX			1		MHz
Input resistance at ANLG IN+, ANLG IN−		10			MΩ

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

receive filter output

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output offset voltage at PWRO+, PWRO− (single ended)	Relative to ANLG GND		80	180	mV
Output resistance at PWRO+, PWRO−			1		Ω

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

gain and dynamic range, V_{CC} = 5 V, V_{BB} = 5 V, T_A = 25°C (see Notes 4, 5, and 6) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Encoder milliwatt response (transmit gain tolerance)		Signal input = 1.064 Vrms for μ-law, Signal input = 1.068 Vrms for A-law		±0.04	±0.2	dBm0
Encoder milliwatt response (nominal supplies and temperature)		T_A = 0°C to 70°C, Supplies = ± 5%			± 0.08	dB
Digital milliwatt response (receive tolerance gain) relative to zero-transmission level point		Signal input per CCITT G.711, Output signal = 1 kHz		±0.04	±0.2	dBm0
Digital milliwatt response variation with temperature and supplies		T_A = 0°C to 70°C, Supplies = ± 5%			± 0.08	dB
Zero-transmission-level point, transmit channel (0 dBm0)	μ-law	R_L = 600 Ω		2.76		dBm
	A-law			2.79		
	μ-law	R_L = 900 Ω		1		
	A-law			1.03		
Zero-transmission-level point, receive channel (0 dBm0)	μ-law	R_L = 600 Ω		5.76		dBm
	A-law			5.79		
	μ-law	R_L = 900 Ω		4		
	A-law			4.03		

NOTES: 4. Unless otherwise noted, the analog input is a 0-dBm0, 1020-Hz sine wave, where 0 dBm0 is defined as the zero-reference point of the channel under test. This corresponds to an analog signal input of 1.064 Vrms or an output of 1.503 Vrms.
5. The input amplifier is set for noninverting unity gain. The digital input is a PCM bit stream generated by passing a 0-dBm0, 1020-Hz sine wave through an ideal encoder.
6. Receive output is measured single ended in the maximum-gain configuration. To set the output amplifier for maximum gain, GSR is connected to PWRO– and the output is taken at PWRO+. All output levels are (sin x)/x corrected.

gain tracking over recommended ranges of supply voltage and operating free-air temperature, reference level = –10 dBm0

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit gain-tracking error, sinusoidal input	3 ≥ input level ≥ –40 dBm0		±0.25	dB
	–40 > input level ≥ –50 dBm0		±0.5	
	–50 > input level ≥ –55 dBm0		±1.2	
Receive gain-tracking error, sinusoidal input	3 ≥ input level ≥ –40 dBm0		±0.25	dB
	–40 > input level ≥ –50 dBm0		±0.5	
	–50 > input level ≥ –55 dBm0		±1.2	

noise over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit noise, C-message weighted‡	ANLG IN+ = ANLG GND, ANLG IN– = GSX		1	7	dBrnC0
Transmit noise, C-message weighted with eight-bit signaling (TCM129C14A and TCM29C14A only)	ANLG IN+ = ANLG GND, ANLG IN– = GSX, 6th frame signaling			13	dBrnC0
Transmit noise, psophometrically weighted‡	ANLG IN+ = ANLG GND, ANLG IN– = GSX		–82	–80	dBm0p
Receive noise, C-message-weighted quiet code	PCM IN = 11111111 (μ-law), PCM IN = 10101010 (A-law), Measured at PWRO+		2	5	dBrnC0
Receive noise, C-message-weighted sign bit toggled	Input to PCM IN is zero code with sign bit toggled at 1-kHz rate		3	6	dBrnC0
Receive noise, psophometrically weighted	PCM = lowest positive decode level			–81	dBm0p

† All typical values are at V_{BB} = –5 V, V_{CC} = 5 V, and T_A = 25°C.
‡ This parameter is achieved through the use of patented circuitry and is not recommended for applications in which composite signals on the transmit side are below –55 dBm0.

power supply rejection ratio and crosstalk attenuation over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{CC} supply-voltage rejection ratio, transmit channel	0 ≤ f < 30 kHz	Idle channel, Supply signal = 200 $mV_{(peak-to-peak)}$, f measured at PCM OUT		–40		dB
	30 ≤ f < 50 kHz			–45		
V_{BB} supply-voltage rejection ratio, transmit channel	0 ≤ f < 30 kHz	Idle channel, Supply signal = 200 $mV_{(peak-to-peak)}$, f measured at PCM OUT		–35		dB
	30 ≤ f < 50 kHz			–55		
V_{CC} supply-voltage rejection ratio, receive channel (single ended)	0 ≤ f < 30 kHz	Idle channel, Supply signal = 200 $mV_{(peak-to-peak)}$, f measured at PWRO+		–40		dB
	30 ≤ f < 50 kHz			–45		
V_{BB} supply-voltage rejection ratio, receive channel (single ended)	0 ≤ f < 30 kHz	Idle channel, Supply signal = 200 $mV_{(peak-to-peak)}$, Narrow-band f measured at PWRO+		–40		dB
	30 ≤ f < 50 kHz			–45		
Crosstalk attenuation, transmit to receive (single ended)		ANLG IN+ = 0 dBm0, f = 1.02 kHz, Unity gain, PCM IN = lowest decode level, Measured at PWRO+	75			dB
Crosstalk attenuation, receive to transmit (single ended)		PCM IN = 0 dBm0, f = 1.02 kHz, Measured at PCM OUT	75			dB

† All typical values are at V_{BB} = –5 V, V_{CC} = 5 V, and T_A = 25°C.

distortion over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit signal-to-distortion ratio, sinusoidal input (CCITT G.712 – Method 2)	0 ≥ ANLG IN+ ≥ −30 dBm0	36			dB
	−30 > ANLG IN+ ≥ −40 dBm0	30			
	−40 > ANLG IN+ ≥ −45 dBm0	25			
Receive signal-to-distortion ratio, sinusoidal input (CCITT G.712 – Method 2)	0 ≥ ANLG IN+ ≥ −30 dBm0	36			dB
	−30 > ANLG IN+ ≥ −40 dBm0	30			
	−40 > ANLG IN+ ≥ −45 dBm0	25			
Transmit single-frequency distortion products	AT&T Advisory #64 (3.8), Input signal = 0 dBm0			−46	dBm0
Receive single-frequency distortion products	AT&T Advisory #64 (3.8), Input signal = 0 dBm0			−46	dBm0
Intermodulation distortion, end to end spurious out-of-band signals, end to end	CCITT G.712 (7.1)			−35	dBm0
	CCITT G.712 (7.2)			−49	
	CCITT G.712 (6.1)			−25	
	CCITT G.712 (9)			−40	
Transmit absolute delay time to PCM OUT	Fixed-data rate, f_{CLKX} = 2.048 MHz, Input to ANLG IN+ 1.02 kHz at 0 dBm0		245		µs
Transmit differential envelope delay time relative to transmit absolute delay time	f = 500 Hz to 600 Hz		170		µs
	f = 600 Hz to 1000 Hz		95		
	f = 1000 Hz to 2600 Hz		45		
	f = 2600 Hz to 2800 Hz		105		
Receive absolute delay time to PWRO+	Fixed data rate, f_{CLKR} = 2.048 MHz, Digital input is DMW codes		190		µs
Receive differential envelope delay time relative to transmit absolute delay time	f = 500 Hz to 600 Hz		45		µs
	f = 600 Hz to 1000 Hz		35		
	f = 1000 Hz to 2600 Hz		85		
	f = 2600 Hz to 2800 Hz		110		

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

transmit filter transfer over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	Input amplifier set for unity gain, Noninverting maximum gain output, Input signal at ANLG IN+ is 0 dBm0	16.67 Hz		−30	dB
		50 Hz		−25	
		60 Hz		−23	
		200 Hz	−1.8	−0.125	
		300 Hz to 3 kHz	−0.15	0.15	
		3.3 kHz	−0.35	0.15	
		3.4 kHz	−1	−0.1	
		4 kHz		−14	

receive filter transfer over recommended ranges of supply voltage and operating free-air temperature (see Figure 2)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	Input signal at PCM IN is 0 dBm0	Below 200 Hz		0.15	dB
		200 Hz	−0.5	0.15	
		300 Hz to 3 kHz	−0.15	0.15	
		3.3 kHz	−0.35	0.15	
		3.4 kHz	−1	−0.1	
		4 kHz		−14	
		4.6 kHz		−30	

timing requirements

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figure 3)

		MIN	TYP†	MAX	UNIT
$t_{c(CLK)}$	Clock period for CLKX, CLKR (2.048-MHz systems)	488			ns
t_r, t_f	Rise and fall times for CLKX and CLKR		5	30	ns
$t_{w(CLK)}$	Pulse duration for CLKX and CLKR (see Note 7)	220			ns
$t_{w(DCLK)}$	Pulse duration, DCLK (f_{DCLK} = 64 Hz to 2.048 MHz) (see Note 7)	220			ns
	Clock duty cycle, [$t_{w(CLK)}/t_{c(CLK)}$] for CLKX and CLKR	45%	50%	55%	

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.
NOTE 7: FSX CLK must be phase locked with CLKX. FSR CLK must be phase locked with CLKR.

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 3)

		MIN	MAX	UNIT
$t_{d(FSX)}$	Frame-sync delay time	100	$t_{c(CLK)}-100$	ns
$t_{su(SIGX)}$	Setup time before bit 7 falling edge of CLKX (TMC29C14A and TCM129C14A only)	0		ns
$t_{h(SIGX)}$	Hold time after bit 8 falling edge of CLKX (TCM29C14A and TCM129C14A only)	0		ns

receive timing requirements over recommended ranges of supply voltages and operating free-air temperature, fixed-data-rate mode (see Figure 6)

PARAMETER		MIN	MAX	UNIT
$t_{d(FSR)}$	Frame-sync delay time	100	$t_{c(CLK)}-100$	ns
$t_{su(PCM\ IN)}$	Receive data setup time	50		ns
$t_{h(PCM\ IN)}$	Receive data hold time	60		ns

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 5)

PARAMETER		MIN	MAX	UNIT
$t_{d(TSDX)}$	Time-slot delay time from DCLKX (see Note 8)	140	$t_{d(DCLKX)}-140$	ns
$t_{d(FSX)}$	Frame sync delay time	100	$t_{c(CLK)}-100$	ns
$t_{c(DCLKX)}$	Clock period for DCLKX	488	15620	ns

NOTE 8: t_{FSLX} minimum requirement overrides the $t_{d(TSDX)}$ maximum requirement for 64-kHz operation.

receive timing requirements over recommended ranges of supply voltages and operating free-air temperature, variable-data-rate mode (see Figure 6)

PARAMETER		MIN	MAX	UNIT
$t_{d(TSDR)}$	Time-slot delay time from DCLKR (see Note 9)	140	$t_{d(DCLKR)}-140$	ns
$t_{d(FSR)}$	Frame-sync delay time	100	$t_{c(CLK)}-100$	ns
$t_{su(PCM\ IN)}$	Receive data setup time	50		ns
$t_{h(PCM\ IN)}$	Receive data hold time	60		ns
$t_{c(DCLKR)}$	Data clock period	488	15620	ns
t_{SER}	Time-slot end receive time	0		ns

NOTE 9: t_{FSLR} minimum requirement overrides the $t_{d(TSDR)}$ maximum requirement for 64-kHz operation.

64-kbit operation timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{FSLX}	Transmit frame-sync minimum down time	FSX = TTL high for remainder of frame	488		ns
t_{FSLR}	Receive frame-sync minimum down time		1952		ns
$t_{w(DCLK)}$	Pulse duration, data clock			10	µs

switching characteristics

propagation delay times over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 3 and 4)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	From rising edge of transmit clock to bit 1 data valid at PCM OUT (data enable time on time-slot entry) (see Note 10)	C_L = 0 to 100 pF	0	145	ns
t_{pd2}	From rising edge of transmit clock bit n to bit n data valid at PCM OUT (data valid time)	C_L = 0 to 100 pF	0	145	ns
t_{pd3}	From falling edge of transmit clock bit 8 to bit 8 Hi-Z at PCM OUT (data float time on time-slot exit) (see Note 10)	C_L = 0	60	215	ns
t_{pd4}	From rising edge of transmit clock bit 1 to TSX active (low) (time-slot enable time)	C_L = 0 to 100 pF	0	145	ns
t_{pd5}	From falling edge of transmit clock bit 8 to TSX inactive (high) (time-slot disable time) (see Note 10)	C_L = 0	60	190	ns
t_{pd6}	From rising edge of channel time slot to SIGR update (TCM29C14A and TCM129C14A only)		0	2	µs

NOTE 10: Timing parameters t_{pd1}, t_{pd3}, and t_{pd5} are referenced to the high-impedance state.

propagation delay times over recommended ranges of operating conditions, variable-data-rate mode (see Note 11 and Figure 5)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd7}	Data delay time from DCLKX	C_L = 0 to 100 pF	0	100	ns
t_{pd8}	Data delay from time-slot enable to PCM OUT		0	50	ns
t_{pd9}	Data delay from time-slot disable to PCM OUT		0	80	ns
t_{pd10}	Data delay time from FSX	$t_{d(TSDX)}$ = 80 ns	0	140	ns

NOTE 11: Timing parameters t_{pd8} and t_{pd9} are referenced to the high-impedance state.

PARAMETER MEASUREMENT INFORMATION

CLKR and CLKX selection requirements for DSP-based applications

1. Note that CLKX and CLKR must be selected as follows:

CLKSEL	CLKR, CLKX (BETWEEN 1 MHz to 3 MHz)	DEVICE TYPE
−5 V†	= (256) × (frame-sync frequency)	TCM29C13A/14A/16A/17A
		TCM129C13A/14A/16A/17A
0 V	= (193) × (frame-sync frequency)	TCM29C13A/14A
		TCM129C13A/14A
5 V	= (192) × (frame-sync frequency)	TCM29C13A/14A
		TCM129C13A/14A

† CLKSEL is internally set to −5 V for TCM29C16A/1A7 and TCM129C16A/17A.

e. g., for frame-sync frequency = 9.6 kHz

CLKSEL	CLKR, CLKX (BETWEEN 1 MHz to 3 MHz)	DEVICE TYPE
−5 V†	= 2.4576 MHz	TCM29C13A/14A/16A/17A
		TCM129C13A/14A/16A/17A
0 V	= 1.8528 MHz	TCM29C13A/14A
		TCM129C13A/14A
5 V	= 1.8432 MHz	TCM29C13A/14A
		TCM129C13A/14A

† CLKSEL is internally set to −5 V for TCM29C16A/1A7 and TCM129C16A/17A.

2. Corner frequency at 8-kHz frame-sync frequency = 3 kHz
   Therefore, the corner frequency = (3/8) × (frame-sync frequency for nonstandard frame sync).

PARAMETER MEASUREMENT INFORMATION

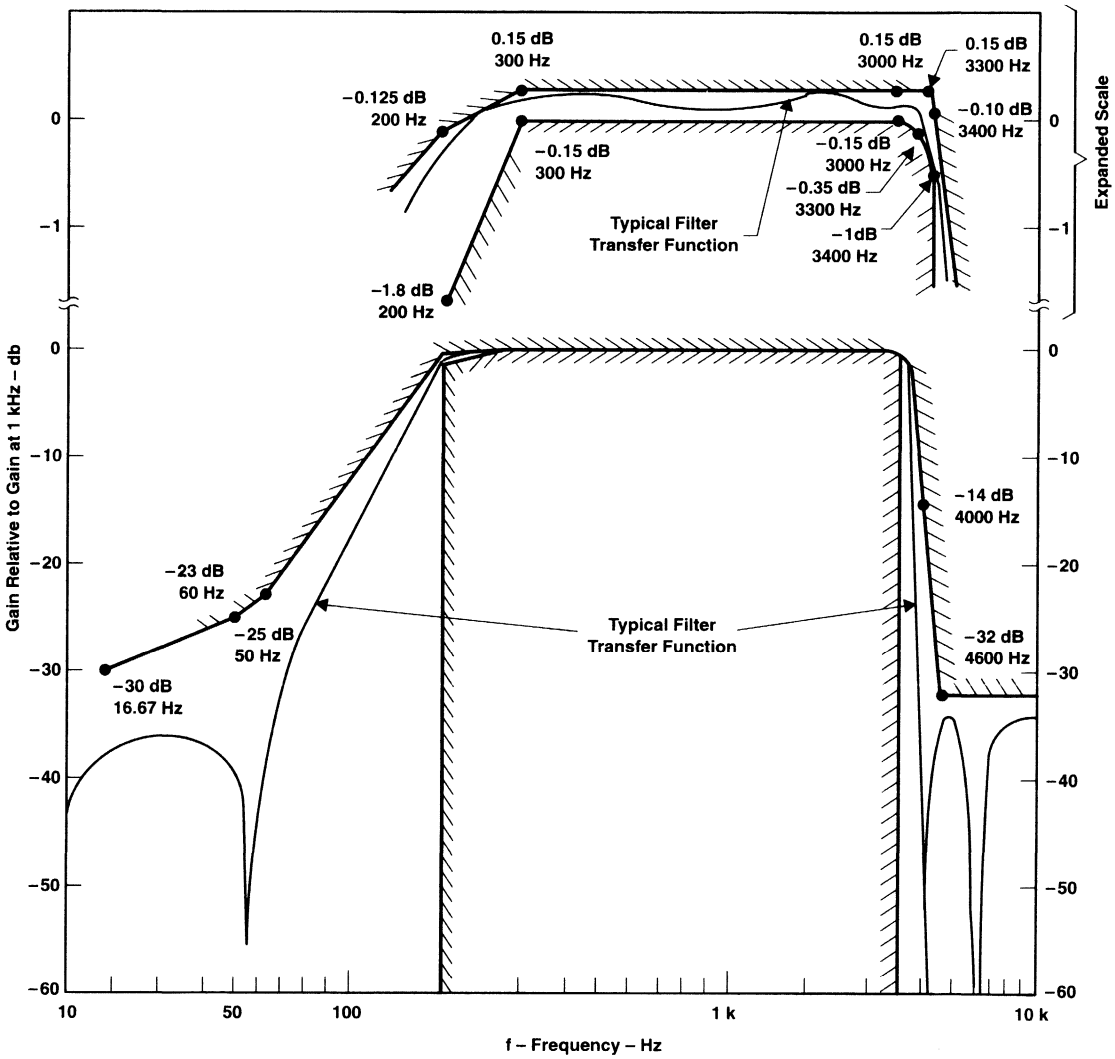
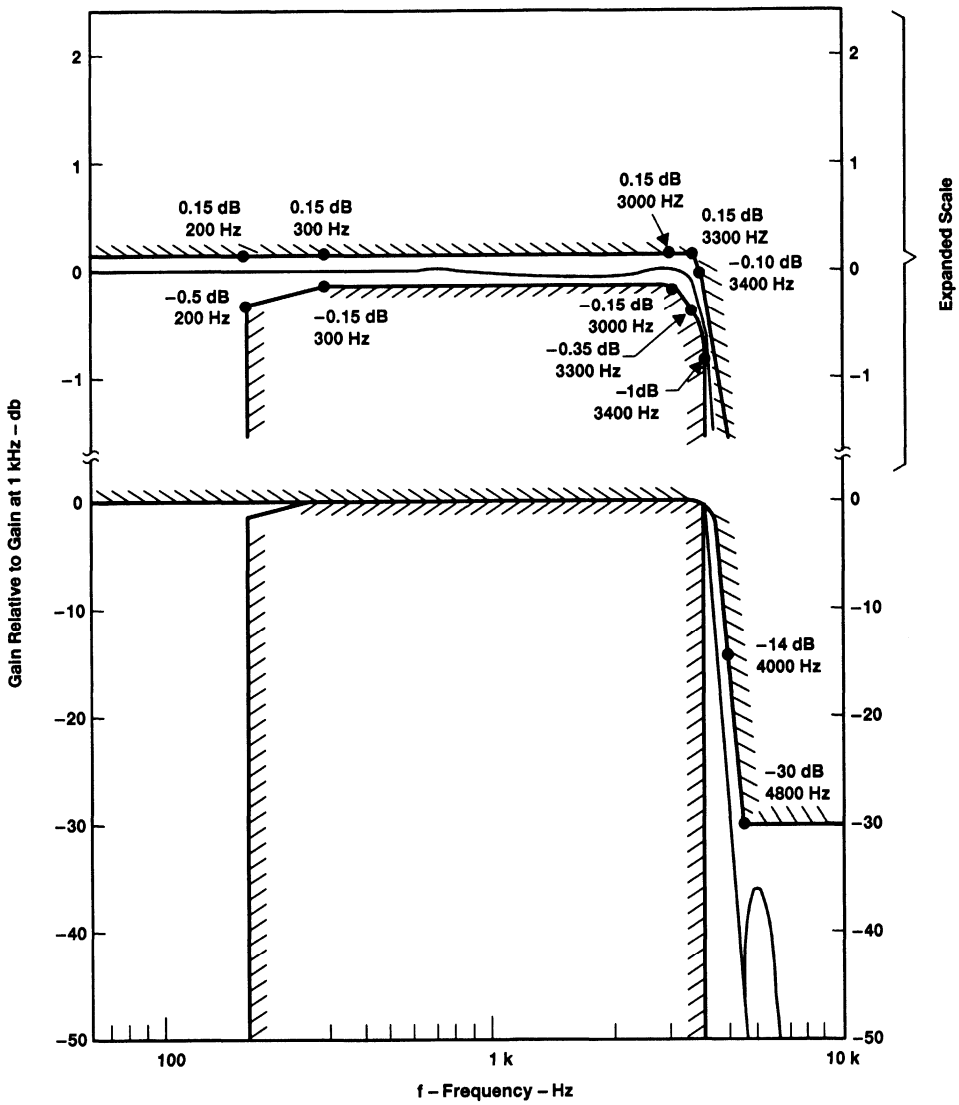


Figure 1. Transfer Characteristics of the Transmit Filter

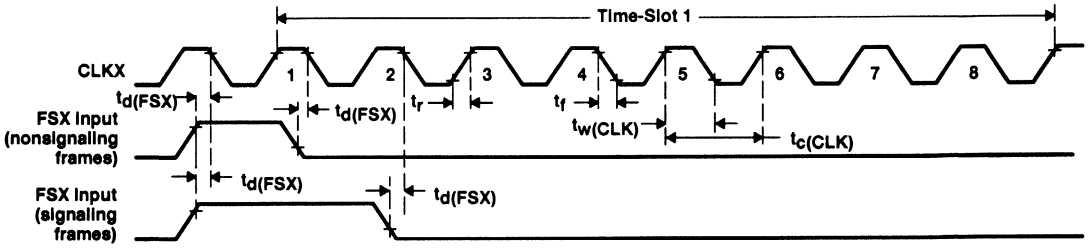
PARAMETER MEASUREMENT INFORMATION



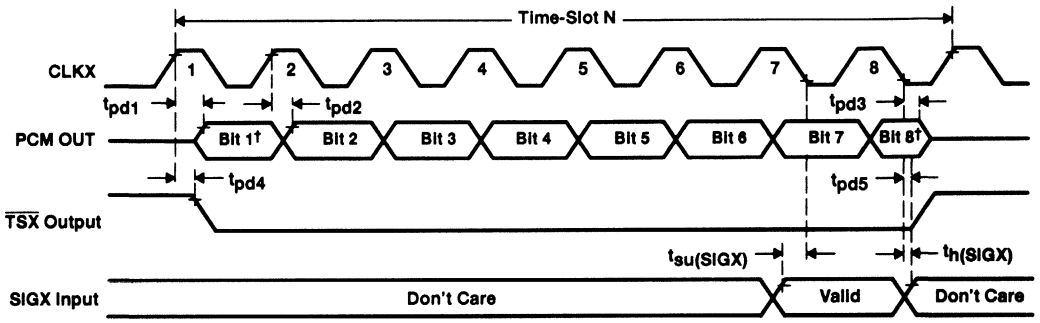
NOTE A: This is a typical transfer function of the receive filter component.

Figure 2. Transfer Characteristics of the Receive Filter

PARAMETER MEASUREMENT INFORMATION



FRAME SYNCHRONIZATION TIMING



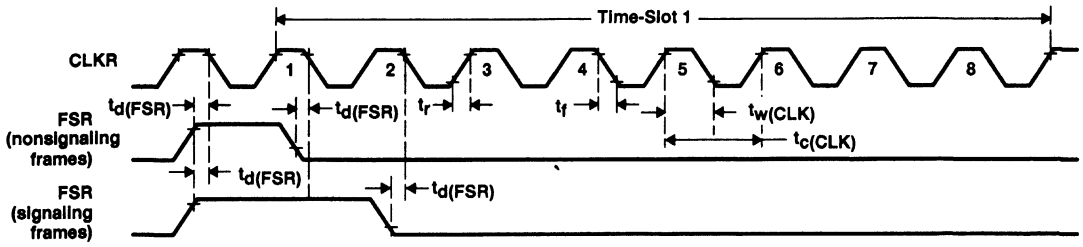
OUTPUT TIMING

† Bit 1 = MSB = sign bit and is clocked in first on PCM IN or clocked out first on PCM OUT. Bit 8 = LSB = least significant bit and is clocked in last on PCM IN or is clocked out last on PCM OUT.

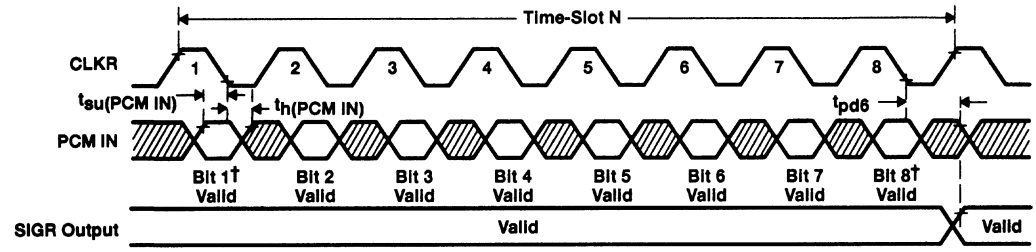
NOTE A: Inputs are driven from 0.45 V to 2.4 V. Time intervals are referenced to 2 V if the high level is indicated and 0.8 V if the low level is indicated.

Figure 3. Transmit Timing (Fixed-Data Rate)

PARAMETER MEASUREMENT INFORMATION



FRAME SYNCHRONIZATION TIMING



INPUT TIMING

† Bit 1 = MSB = sign bit and is clocked in first on PCM IN or clocked out first on PCM OUT. Bit 8 = LSB = least significant bit and is clocked in last on PCM IN or is clocked out last on PCM OUT.

NOTE A: Inputs are driven from 0.45 V to 2.4 V. Time intervals are referenced to 2 V if the high level is indicated and 0.8 V if the low level is indicated.

Figure 4. Receive Timing (Fixed-Data Rate)

PARAMETER MEASUREMENT INFORMATION

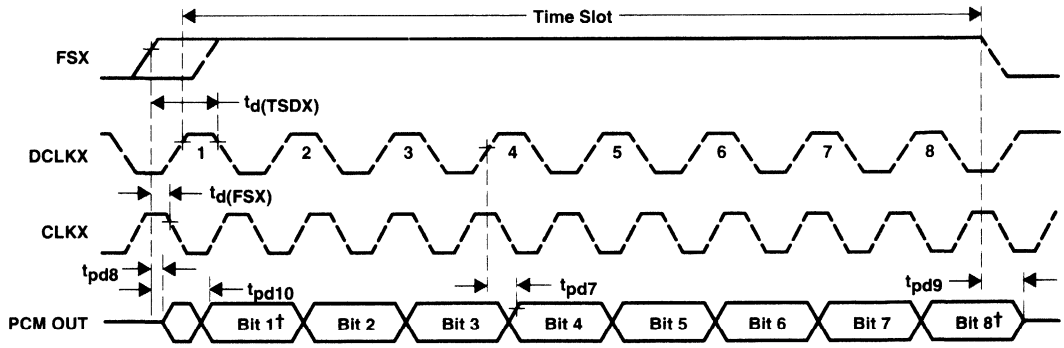


Figure 5. Transmit Timing (Variable-Data Rate)

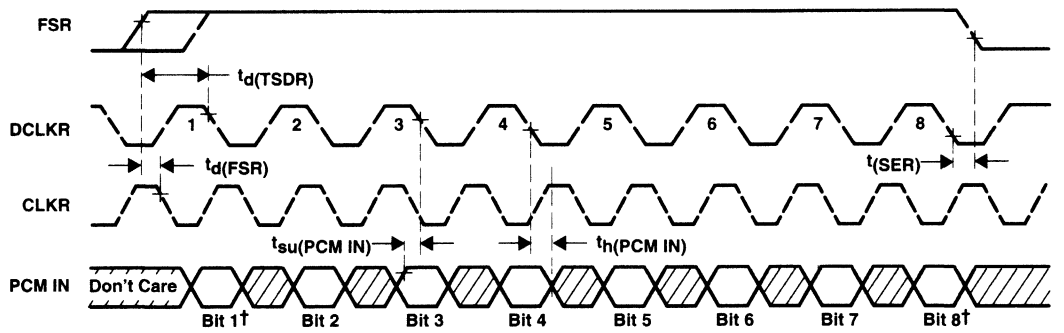


Figure 6. Receive Timing (Variable-Data Rate)

† Bit 1 = MSB = sign bit and is clocked in first on PCM IN or clocked out first on PCM OUT. Bit 8 = LSB = least significant bit and is clocked in last on PCM IN or is clocked out last on PCM OUT.

NOTE A: All timing parameters are referenced to V_{IH} and V_{IL} except t_{pd8} and t_{pd9}, which references the high-impedance state.

PRINCIPLES OF OPERATION

system reliability and design considerations

General TCM29C13A, TCM29C14A, TCM29C16A, TCM29C17A, TCM129C13A, TCM129C14A, TCM129C16A, and TCM129C17A system reliability and design considerations are described in the following paragraphs.

latch-up

Latch-up is possible in all CMOS devices. It is caused by the firing of a parasitic SCR that is present due to the inherent nature of CMOS. When a latch-up occurs, the device draws excessive amounts of current and will continue to draw heavy current until power is removed. Latch-up can result in permanent damage to the device if supply current to the device is not limited.

Even though the TCM29CxxA and TCM129CxxA devices are heavily protected against latch-up, it is still possible to cause latch-up under certain conditions in which excess current is forced into or out of one or more terminals. Latch-up can occur when the positive supply voltage drops momentarily below ground, when the negative supply voltage rises momentarily above ground, or possibly if a signal is applied to a terminal after power has been applied but before the ground is connected. This can happen if the device is hot-inserted into a card with the power applied, or if the device is mounted on a card that has an edge connector, and the card is hot-inserted into a system with the power on.

To help ensure that latch-up does not occur, it is considered good design practice to connect a reverse-biased Schottky diode (with a forward voltage drop of less than or equal to 0.4 V — 1N5711 or equivalent), between each power supply and GND (see Figure 7). If it is possible that a TCM29CxxA- or TCM129CxxA-equipped card that has an edge connector could be hot-inserted into a powered-up system, it is also important to ensure that the ground edge connector traces are longer than the power and signal traces so that the card ground is always the first to make contact.

device power-up sequence

Latch-up can also occur if a signal source is connected without the device being properly grounded. A signal applied to one terminal could then find a ground through another signal terminal on the device. To ensure proper operation of the device and as a safeguard against this sort of latch-up, it is recommended that the following power-up sequence always be used:

1. Ensure no signals are applied to the device before the power-up sequence is complete.
2. Connect GND.
3. Apply V_{BB} (most negative voltage).
4. Apply V_{CC} (most positive voltage).
5. Force a power down condition in the device.
6. Connect clocks.
7. Release the power-down condition.
8. Apply FSX and/or FXR synchronization pulses.
9. Apply signal inputs.

When powering down the device, this procedure should be followed in the reverse order.

PRINCIPLES OF OPERATION

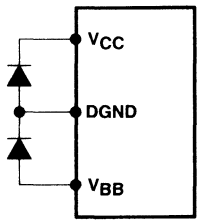


Figure 7. Diode Configuration for Latch-Up Protection Circuitry

internal sequencing

On the transmit channel, digital outputs PCM OUT and $\overline{TSX}$ are held in the high-impedance state for approximately four frames (500 µs) after power up or application of V_{BB} or V_{CC}. After this delay, PCM OUT, $\overline{TSX}$, and signaling are functional and occur in the proper time slot. The analog circuits on the transmit side require approximately 60 ms to reach their equilibrium value due to the autozero circuit settling time. Therefore, valid digital information, such as on/off hook detection, is available almost immediately, while analog information is available after some delay.

On the receive channel, the digital output SIGR is also held low for a maximum of four frames after power up or application of V_{BB} or V_{CC}. SIGR remains low until it is updated by a signalling frame.

To further enhance system reliability, PCM OUT and $\overline{TSX}$ are placed in the high-impedance state approximately 20 µs after an interruption of CLKX. SIGR is held low approximately 20 µs after an interruption of CLKR. These interruptions could possibly occur with some kind of fault condition.

power-down and standby operations

To minimize power consumption, a power-down mode and three standby modes are provided.

For power down, an external low signal is applied to $\overline{PDN}$. In the absence of a signal, $\overline{PDN}$ is internally pulled up to a high logic level and the device remains active. In the power-down mode, the average power consumption is reduced 15 mW.

Three standby modes give the user the options of placing the entire device on standby, placing only the transmit channel on standby, or placing only the receive channel on standby. to place the entire device on standby, both FSX and FSR are held low. For transmit-only operation (receive channel on standby), FSX is high and FSR is held low. For receive-only operation (transmit section on standby), FSR is high and FSX is held low. When the entire device is in standby mode, power consumption is reduced to an average of 3 mW. See Table 1 for power-down and standby procedures.

Table 1. Power-Down and Standby Procedures

DEVICE STATUS	PROCEDURE	TYPICAL POWER CONSUMPTION	DIGITAL OUTPUT STATUS
Power down	$\overline{PDN}$ low	3 mW	$\overline{TSX}$ and PCM OUT are in the high-impedance state; SIGR goes low within 10 µs.
Entire device on standby	FSX and FSR are low	3 mW	$\overline{TSX}$ and PCM OUT are in the high-impedance state; SIGR goes low within 300 ms.
Only transmit on standby	FSX is low, FSR is high	40 mW	$\overline{TSX}$ and PCM OUT are placed in the high-impedance state within 300 ms.
Only receive on standby	FSR is low, FSX is high	30 mW	SIGR is placed in the high-impedance state within 300 ms.

PRINCIPLES OF OPERATION

fixed-data-rate timing (see Figure 8)

Fixed-data-rate timing is selected by connecting DCLKR to V_{BB} and uses master clocks CLKX and CLKR, frame-synchronizer clocks FSX and FSR, and the output $\overline{TSX}$. FSX and FSR are 8-kHz inputs that set the sampling frequency and distinguish between signaling and nonsignaling frames by their pulse durations. A frame- synchronization pulse one master-clock period long designates a nonsignaling frame, while a double-length sync pulse enables the signaling function (TCM12914A and TCM29C14A only). Data is transmitted on PCM OUT on the first eight positive transitions of CLKX following the rising edge of FSX. Data is received on PCM IN on the first eight falling edges of CLKR following FSR. A digital-to-analog (D/A) conversion is performed on received digital word, and the resulting analog sample is held on an internal sample-and-hold capacitor until transferred to the receive filter.

The clock-selection terminal (CLKSEL) is used to select the frequency of CLKX and CLKR (TCM29C13A, TCM29C14A, TCM129C13A, and TCM129C14A only). The TCM29C13A, TCM29C14A, TCM129C13A, and TCM129C14A fixed-data-rate mode can operate with frequencies of 1.536 MHz, 1.544 MHz, or 2.048 MHz. The TCM29C16A, TCM29C17A, TCM129C16A, and TCM129C17A fixed-data-rate mode operates at 2.048 MHz only.

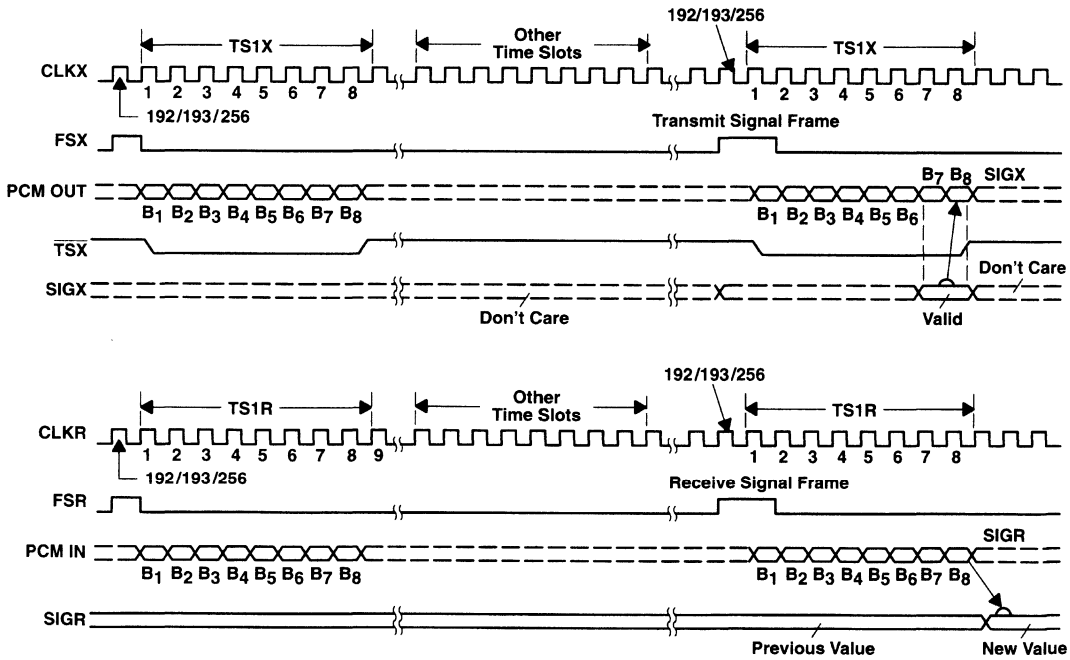


Figure 8. Signaling Timing (Fixed-Data Rate Only)

PRINCIPLES OF OPERATION

variable-data-rate timing

Variable-data-rate timing is selected by connecting DCLKR to the bit clock for the receive PCM highway rather than to V_{BB}. It uses master clocks CLKX and CLKR, bit clocks DCLKX and DCLKR, and frame-synchronization clocks FSX and FSR.

Variable-data-rate timing allows for a flexible data frequency. The frequency of the bit clocks can be varied from 64 kHz to 2.048 MHz. Master clocks in the TCM129C13A, TCM129C14A, TCM29C13A, and TCM29C14A are restricted to frequencies of operation of 1.536 MHz, 1.544 MHz, or 2.048 MHz as in the fixed-data-rate timing mode. The master clock for the TCM129C16A, TCM129C17A, TCM29C16A, and TCM29C17A is restricted to 2.048 MHz.

When the FSX/TSXE is high, PCM data is transmitted from PCM OUT onto the highway on the next eight consecutive positive transitions of DCLKX. Similarly, while the FSR/TSRE input is high, the PCM word is received from the highway by PCM IN on the next eight consecutive negative transitions of DCLKR.

The transmitted PCM word is repeated in all remaining time slots in the 125-μs frame as long as DCLKX is pulsed and FSX is held high. This feature, which allows the PCM word to be transmitted to the PCM highway more than once per frame if desired, is available only with variable-data-rate timing. Signaling is allowed only in the fixed-data-rate mode because the variable-data-rate mode provides no means with which to specify a signaling frame.

signaling

The TCM29C14A (only) provides 8th-bit signaling in the fixed-data-rate timing mode. Transmit and receive signaling frames are independent of each other and are selected by a double-width frame-sync pulse on the appropriate channel. During a transmit signaling frame, the signal present on SIGX is substituted for the least significant bit (LSB) of the encoded PCM word. In a receive signaling frame, the codec decodes the seven most significant bits in accordance with CCITT G.733 recommendations and outputs the logical state of the LSB on SIGR until it is updated in the next signaling frame. Timing relationships for signaling operations are shown in Figure 8. The signaling path is used to transmit digital signaling information such as ring control, rotary dial pulses, and off-hook and disconnect supervision. The voice path is used to transmit prerecorded messages as well as the call progress tones: dial tone, ring-back tone, busy tone, and reorder tone.

PRINCIPLES OF OPERATION

analog loopback

A distinctive feature of the TCM29C14A and TCM129C14A is the analog loopback capability. With this feature, the user can test the line circuit remotely by comparing the signals sent into the receive channel (PCM IN) with those generated on the transmit channel (PCM OUT). The test is accomplished by sending a control signal that internally connects the analog input and output ports. When ANLG LOOP is TTL high, the receive output (PWRO+) is internally connected to ANLG IN+, GSR is internally connected to PWRO–, and ANLG IN– is internally connected to GSX (see Figure 8).

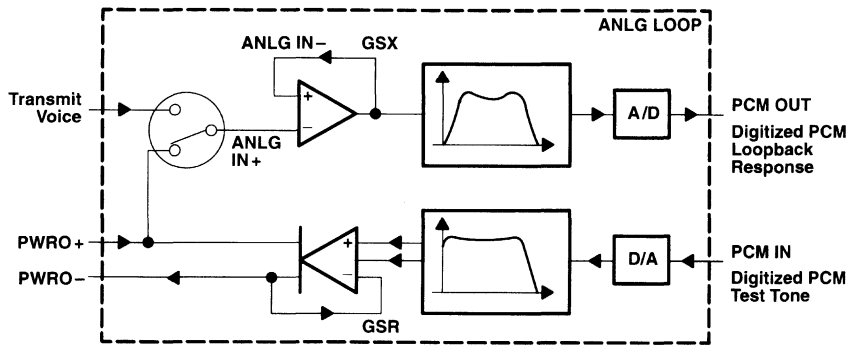


Figure 9. TCM29C14A and TCM129C14A Analog Loopback Configuration

Due to the difference in the transmit and receive transmission levels, a 0-dBm0 code into PCM IN emerges from PCM OUT as a 3-dBm0 code, an implicit gain of 3 dB. Because of this, the maximum signal that can be tested by analog loopback is 0 dBm0.

precision voltage references

Voltage references that determine the gain dynamic range characteristics of the device are generated internally. No external components are required to provide the voltage references. A difference in subsurface charge density between two suitably implanted MOS device is used to derive a temperature- and bias-stable reference voltage, which are calibrated during the manufacturing process. Separate references are supplied to the transmit and receive sections, and each is calibrated independently. Each reference value is then further trimmed in the gain-setting operational amplifiers to a final precision value. Manufacturing tolerances of typically ±0.04 dB can be achieved in absolute gain for each half channel, providing the user a significant margin to compensate for error in other system components.

conversion laws

The TCM29C13A, TCM29C14A, TCM129C13A, and TCM129C14A provide pin-selectable μ-law operation as specified by CCITT G.711 recommendation. A-law operation is selected when ASEL is connected to V_{BB}, and μ-law operation is selected by connecting ASEL to V_{CC} or GND. Signaling is not allowed during A-law operation. If μ-law operation is selected, SIGX is a TTL-level input that can be used in the fixed-data-rate timing mode to modify the LSB of the PCM output is signaling frames.

The TCM29C16A and TCM129C16A are μ-law only; the TCM29C17A and TCM129C17A are A-law only.

PRINCIPLES OF OPERATION

transmit operation

transmit filter

The input section provides gain adjustment in the pass band by means of an on-chip uncommitted operational amplifier. The load impedance to ground (ANLG GND) at the amplifier output (GSX) must be greater than 10 kΩ in parallel with less than 50 pF. The input signal on ANLG IN+ can be either ac or dc coupled. The input operational amplifier can also be used in the inverting mode or differential amplifier mode.

A low-pass antialiasing filter section is included on the device. This section provides 35-dB attenuation at the sampling frequency. No external components are required to provide the necessary antialiasing function for the switched-capacitor section of the transmit filter.

The pass-band section provides flatness and stop-band attenuation that fulfills the AT&T D3/D4 channel bank transmission specification and CCITT recommendation G.712. The device specifications meet or exceed digital class 5 central office switching-systems requirements.

A high-pass section configuration has been chosen to reject low-frequency noise from 50-Hz and 60-Hz power lines, 17-Hz European electric railroads, ringing frequencies and their harmonics, and other low-frequency noise. Even with the high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200 Hz. This feature allows the use of low-cost transformer hybrids without external components.

encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample-and-hold capacitor. The encoder performs an analog-to-digital conversion on a switched-capacitor array. Digital data representing the sample is transmitted on the first eight data clock bits of the next frame.

The autozero circuit corrects for dc offset on the input signal to the encoder. The autozero circuit uses the sign-bit-averaging technique. The sign bit from the encoder output is long-term averaged and subtracted from the input to the encoder. All dc offset is removed from the encoder input waveform.

receive operation

decoding

The serial PCM word is received at PCM IN on the first eight data clock bits of the frame. Digital-to-analog conversion is performed, and the corresponding analog sample is held on an internal sample-and-hold capacitor. This sample is transferred to the receive filter.

receive filter

The receive section of the filter provides pass-band flatness and stop-band rejection that fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin x)/x response of such decoders.

PRINCIPLES OF OPERATION

receive output power amplifiers

A balanced-output amplifier is provided to allow maximum flexibility in output configuration. Either of the two outputs can be used single ended (i.e., referenced to ANLG GND) to drive single-ended loads. Alternatively, the differential output directly drives a bridged load. The output stage is capable of driving loads as low as 300-Ω single-ended to a level of 12 dBm or 600 Ω differentially to a level of 15 dBm.

The receive channel transmission level may be adjusted between specified limits by manipulation of GSR. GSR is internally connected to an analog gain-setting network. When GSR is connected to PWRO–, the receive level is maximum. When GSR is connected to PWRO+, the level is minimum. The output transmission level is adjusted between 0 and –12 dB as GSR is adjusted (with an adjustable resistor) between PWRO+ and PWRO–.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions (i.e., when the digital input at PCM IN is the eight-code sequence specified in CCITT recommendation G.711).

APPLICATION INFORMATION

output gain-set design considerations (see Figure 9)

PWRO+ and PWRO– are low-impedance complementary outputs. The voltages at the nodes are:

V_{O+} at PWRO+
V_{O-} at PWRO–
$V_O = V_{O+} - V_{O-}$ (total differential response)

R1 and R2 are a gain-setting resistor network with the center tap connected to the GSR input.

A value greater than 10 kΩ and less than 100 kΩ for R1 + R2 is recommended because of the following:

The parallel combination of R1 + R2 and R_L sets the total loading.
The total capacitance at the GSR input and the parallel combination of R1 and R2 define a time constant that has to be minimized to avoid inaccuracies.

V_A represents the maximum available digital milliwatt output response (V_A = 3.006 Vrms).

$$V_{OD} = A \cdot V_A$$

$$\text{where } A = \frac{1 + (R1/R2)}{4 + (R1/R2)}$$

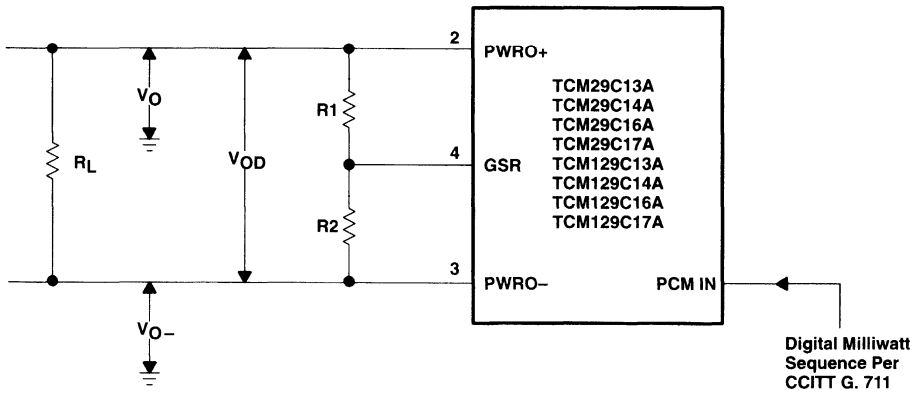


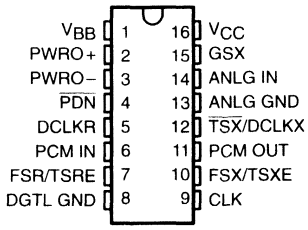
Figure 10. Gain-Setting Configuration

TCM29C18, TCM29C19, TCM129C18, TCM129C19
ANALOG INTERFACE FOR DSP

SCTS021C –AUGUST 1987 –REVISED JULY 1996

- **Reliable Silicon-Gate CMOS Technology**
- **Low Power Consumption**
  - **Operating Mode . . . 80 mW**
  - **Power-Down Mode . . . 5 mW**
- **μ-Law Coding**
- **Excellent Power-Supply Rejection Ratio Over Frequency Range of 0 Hz to 50 kHz**
- **No External Components Needed for Sample, Hold, and Autozero Functions**
- **Precision Internal Voltage Reference**
- **Single Chip Contains A/D, D/A, and Associated Filters**

DW OR N PACKAGE
(TOP VIEW)



FEATURES TABLE

Number of Pins: 16
Coding Law: μ-Law
Variable Mode: 64 kHz to 2.048 MHz
Fixed Mode: 2.048 MHz (TCM29C18, TCM129C18), 1.536 MHz (TCM29C19, TCM129C19) 8-Bit Resolution 12-Bit Dynamic Range

description

The TCM29C18, TCM29C19, TCM129C18, and TCM129C19 are low-cost single-chip PCM codecs (pulse-code-modulated encoders and decoders) and PCM line filters. These devices incorporate both the A/D and D/A functions, an antialiasing filter (A/D), and a smoothing filter (D/A). They are ideal for use with the TMS320 DSP family members, particularly those featuring a serial port such as the TMS32020, TMS32011, and TMS320C25.

Primary applications include:

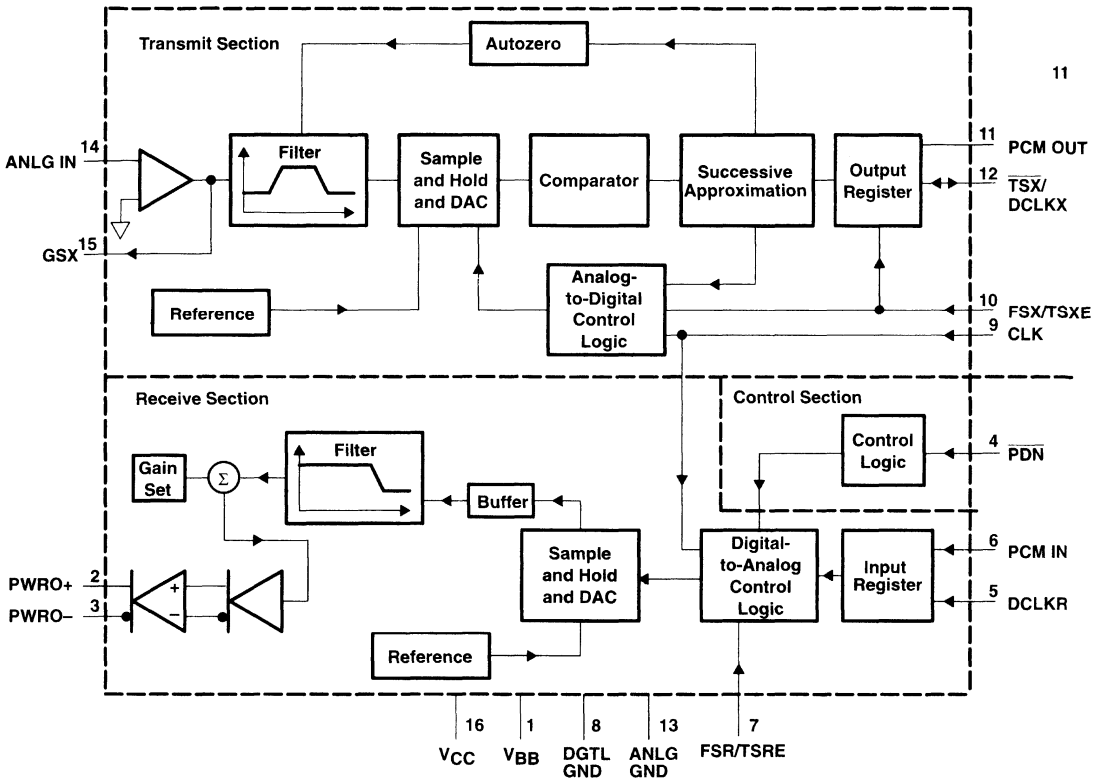
- Digital encryption systems
- Digital voice-band data storage systems
- Digital signal processing

These devices are designed to perform encoding of analog input signals (A/D conversion) and decoding of digital PCM signals (D/A conversion). They are useful for implementation in the analog interface of a digital signal processing system. Both devices also provide band-pass filtering of the analog signals prior to encoding, and smoothing after decoding.

The TCM29C18 and TCM29C19 are characterized for operation over the temperature range of 0°C to 70°C. The TCM129C18 and TCM129C19 are characterized for operation over the temperature range of –40°C to 85°C.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ANLG IN	14	I	Inverting analog input. Input to uncommitted transmit operational amplifier.
ANLG GND	13		Analog ground return for all voice circuits. Not internally connected to DGTL GND.
CLK	9	I	Master clock and data clock input for the fixed-data-rate mode. Master (filter) clock only for variable-data-rate mode. This clock is used for both the transmit and receive sections.
DCLKR	5	I	Fixed data rate mode—variable data rate mode select. When connected to V_{BB}, the device operates in the fixed-data-rate mode. When DCLKR is not connected to V_{BB}, the device operates in the variable-data-rate mode and DCLKR becomes the receive data clock, which operates at frequencies from 64 kHz to 2.048 MHz.
DGTL GND	8		Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
FSR/TSRE	7	I	Frame-synchronization clock input/time-slot enable for the receive channel. In the variable-data-rate mode, this signal must remain high for the duration of the time slot. The receive channel enters the standby state when FSR is TTL low for 30 ms.
FSX/TSXE	10	I	Frame-synchronization clock input/time-slot enable for transmit channel. Operated independently of, but in an analogous manner to FSR/TSRE. The transmit channel enters the standby state when FSX is low for 300 ms.
GSX	15	O	Output terminal of internal uncommitted operational amplifier. Internally, this is the voice signal input to the transmit filter.
PCM IN	6	I	Receive PCM input. PCM data is clocked in on eight consecutive negative transitions of the receive data clock, which is CLKR in fixed-data-rate timing and DCLKR in variable-data-rate timing.
PCM OUT	11	O	Transmit PCM output. PCM data is clocked out of this output on eight consecutive positive transition of the transmit data clock, which is CLKX in fixed-data-rate timing and DCLKX in variable-data-rate timing.
$\overline{PDN}$	4	I	Power-down select. On the TCM29C18 and the TCM129C18, the device is inactive with a TTL low-level input and active with a TTL high-level input to the terminal. On the TCM29C19 and the TCM129C19, this terminal must be connected to a TTL high level.
PWRO+	2	O	Noninverting output of power amplifier. PWRO+ can drive transformer hybrids or high-impedance loads directly in either a differential or single-ended configuration.
PWRO–	3	O	Inverting output of power amplifier—functionally identical to PWRO+.
$\overline{TSX}$/DCLKX	12	I/O	Transmit channel time-slot strobe (output) or data clock (input). In the fixed-data-rate mode, this is an open-drain output to be used as an enable signal for a 3-state buffer. In the variable-data-rate mode, DCLKX becomes the transmit data clock, which operates at TTL levels from 64 kHz to 2.048 MHz.
V_{BB}	1		Negative supply voltage, –5 V ±5%.
V_{CC}	16		Positive supply voltage, 5 V ±5%.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.3 V to 15 V
Output voltage range, V_O . . . . . −0.3 V to 15 V
Input voltage range, V_I . . . . . −0.3 V to 15 V
Digital ground voltage range . . . . . −0.3 V to 15 V
Operating free-air temperature range, T_A: TCM29C18, TCM29C19 . . . . . 0°C to 70°C
TCM129C18, TCM129C19 . . . . . −40°C to 85°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values for maximum ratings are with respect to V_{BB}.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 3)		4.75	5	5.25	V
V_{BB}	Supply voltage		−4.75	−5	−5.25	V
	DGTL GND voltage with respect to ANLG GND			0		V
V_{IH}	High-level input voltage, all inputs except ANLG IN		2.2			V
V_{IL}	Low-level input voltage, all inputs except ANLG IN				0.8	V
$V_{I(PP)}$	Peak-to-peak analog input voltage (see Note 4)				4.2	V
R_L	Load resistance	GSX	10			kΩ
		PWRO+ and/or PWRO−	300			Ω
C_L	Load capacitance	GSX			50	pF
		PWRO+ and/or PWRO−			100	
T_A	Operating free-air temperature	TCM29C18 or TCM29C19	0		70	°C
		TCM129C18 or TCM129C19	−40		85	

NOTES: 2. To avoid possible damage to these CMOS devices and resulting reliability problems, the power-up procedure described in the device power-up sequence paragraphs later in this document should be followed.
3. Voltages at analog inputs and outputs and V_{CC} and V_{BB} terminals are with respect to ANLG GND. All other voltages are referenced to DGTL GND unless otherwise noted.
4. Analog inputs signals that exceed 4.2 V peak to peak may contribute to clipping and preclude correct A/D conversion. The digital code representing values higher than 4.2 V is 10000000. For values more negative than 4.2 V, the code is 0000000.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

supply current, f_{DCLK} = 2.048 MHz, outputs not loaded

PARAMETER			TEST CONDITIONS	TCM29Cxx		TCM129Cxx		UNIT
				MIN	MAX	MIN	MAX	
I_{CC}	Supply current from V_{CC}	Operating			10		14	mA
		Standby	FSX or FSR at V_{IL} after 300 ms		1.2		1.5	
		Power down	$\overline{PDN}$ at V_{IL} after 10 µs		1		1.2	
I_{BB}	Supply current from V_{BB}	Operating			−10		−14	mA
		Standby	FSX or FSR at V_{IL} after 300 ms		−1.2		−1.5	
		Power down	$\overline{PDN}$ at V_{IL} after 10 µs		−1		−1.2	

digital interface

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage, PCM OUT	I_{OH} = −9.6 mA	2.4			V
		I_{OH} = −0.1 mA	3.5			
V_{OL}	Low-level output voltage, $\overline{TSX}$	I_{OL} = 3.2 mA			0.5	V
I_{IH}	High-level input current, any digital input	V_I = 2.2 V to V_{CC}			12	µA
I_{IL}	Low-level input current, any digital input	V_I = 0 to 0.8 V			12	µA
C_i	Input capacitance			5	10	pF
C_o	Output capacitance			5		pF

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

transmit side (A/D) characteristics

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Input offset voltage at ANLG IN	V_I = −2.17 V to 2.17 V				±25	mV
Input offset current at ANLG IN	V_I = −2.17 V to 2.17 V			1		pA
Input bias current	V_I = −2.17 V to 2.17 V				±100	nA
Open-loop voltage amplification at GSX			5000			
Unity-gain bandwidth at GSX				1		MHz
Input resistance at ANLG IN			10			MΩ
Gain-tracking error with sinusoidal input (see Notes 5, 6, and 7)	−3 ≥ dBm0 input level ≥ −40 dBm0,	Ref level = −10 dBm0			±0.5	dB
	−40 > dBm0 input level ≥ −50 dBm0,	Ref level = −10 dBm0			±25	
Transmit gain tolerance	V_I = 1.06 V,	f = 1.02 kHz	0.95		1.19	Vrms
Noise	Ref max output level: 200 Hz to 3 kHz				−70	dB
Supply-voltage rejection ratio, V_{CC} to V_{BB}	f = 0 Hz to 30 kHz (measured at PCM OUT) idle channel, Supply signal = 200 mV peak to peak		−20			dB
Crosstalk attenuation, transmit to receive (single ended)	ANLG IN = 0 dBm, PCM IN = lowest decode level,	f = 1 kHz unity gain, Measured at PWRO+	62			dB
Signal-to-distortion ratio, sinusoidal input (see Note 8)	0 dBm0 ≥ ANLG IN ≥ −30 dBm0		33			dB
	−30 dBm0 > ANLG IN ≥ −40 dBm0		27			
	−40 dBm0 > ANLG IN ≥ −45 dBm0		22			
Absolute delay time to PCM OUT	Fixed data rate, Input to ANLG IN = 1 kHz at 0 dB	f_{CLKX} = 2.048 MHz,		245		µs

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

NOTES: 5. Unless otherwise noted, the analog input is a 0-dBm0, 1020-Hz sine wave, where 0 dBm0 is defined as the zero-reference point of the channel under test. This corresponds to an analog signal input of 1.064 Vrms or an output of 1.503 Vrms.
6. The input amplifier is set for unity gain. The digital input is a PCM bit stream generated by passing a 0-dBm0, 1020-Hz sine wave through an ideal encoder.
7. The TCM29C18, TCM29C19, TCM129C18, and TCM129C19 are internally connected to set PWRO+ and PWRO− to 0 dBM. All output levels are (sin x)/x corrected.
8. CCITT G.712 – Method 2.

receive side (D/A) characteristics (see Note 9)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Output offset voltage PWRO+ and PWRO– (single ended)	Relative to ANLG GND				±200	mV
Output resistance at PWRO+ and PWRO–				1	2	Ω
Gain-tracking error with sinusoidal input (see Notes 5, 6, and 7)	–3 dBm0 ≥ input level ≥ –40 dBm0,	Ref level = –10 dBm0			±0.5	dB
	–40 dBm0 > input level ≥ –50 dBm0,	Ref level = –10 dBm0			±25	
Receive gain tolerance	V_I = 1.06 V,	f = 1.02 kHz	1.34		1.69	Vrms
Noise	Ref max output level: 200 Hz to 3 kHz				–70	dB
Supply voltage rejection ratio, V_{CC} to V_{BB} (single-ended)	f = 0 Hz to 30 kHz, Supply signal = 200 mV peak to peak, Frequency at PWRO+	Idle channel, Narrow band,	–20			dB
Crosstalk attenuation, receive to transmit (single ended)	PCM IN = 0 dB, Frequency = 1 kHz at PCM OUT		60			dB
Signal-to-distortion ratio, sinusoidal input (see Note 8)	0 dBm0 ≥ ANLG IN ≥ –30 dBm0		33			dB
	–30 dBm0 > ANLG IN ≥ –40 dBm0		27			
	–40 dBm0 > ANLG IN ≥ –45 dBm0		22			
Absolute delay time to PWRO+	Fixed data rate,	f_{CLKX} = 2.048 MHz		190		µs

† All typical values are at V_{BB} = –5 V, V_{CC} = 5 V, and T_A = 25°C.

NOTES: 5. Unless otherwise noted, the analog input is a 0-dBm0, 1020-Hz sine wave, where 0 dBm0 is defined as the zero-reference point of the channel under test. This corresponds to an analog signal input of 1.064 Vrms or an output of 1.503 Vrms.
6. The input amplifier is set for unity gain. The digital input is a PCM bit stream generated by passing a 0-dBm0, 1020-Hz sine wave through an ideal encoder.
7. The TCM29C18, TCM29C19, TCM129C18, and TCM129C19 are internally connected to set PWRO+ and PWRO– to 0 dBM. All output levels are (sin x)/x corrected.
8. CCITT G.712 – Method 2.
9. The receive side (D/A) characteristics are referenced to a 600-Ω termination.

timing requirements

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 3 and 4)

		MIN	TYP†	MAX	UNIT
$t_{c(CLK)}$	Clock period for CLK (2.048-MHz systems)	488			ns
t_r, t_f	Rise and fall times for CLK	5		30	ns
$t_{w(CLK)}$	Pulse duration for CLK	220			ns
$t_{w(DCLK)}$	Pulse duration, DCLK (f_{DCLK} = 64 kHz to 2.048 MHz)	220			ns
	Clock duty cycle, $[t_{w(CLK)}/t_{c(CLK)}]$ for CLK	45%	50%	55%	

† All typical values are at V_{BB} = –5 V, V_{CC} = 5 V, and T_A = 25°C.

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 3)

		MIN	MAX	UNIT
$t_{d(FSX)}$	Frame-sync delay time	100	$t_{c(CLK)} - 100$	ns

receive timing requirements over recommended ranges of supply voltages and operating free-air temperature, fixed-data-rate mode (see Figure 4)

PARAMETER		MIN	MAX	UNIT
$t_{d(FSR)}$	Frame-sync delay time	100	$t_{c(CLK)}-100$	ns

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see Figure 5)

PARAMETER		MIN	MAX	UNIT
$t_{d(TSDX)}$	Delay time, time-slot from DCLKX (see Note 10)	140	$t_{d(DCLKX)}-140$	ns
$t_{d(FSX)}$	Delay time, frame sync	100	$t_{c(CLK)}-100$	ns
$t_{c(DCLKX)}$	Pulse duration, DCLKX	488	15620	ns

NOTE 10: t_{FSLX} minimum requirement overrides the $t_{d(TSDX)}$ maximum requirement for 64-kHz operation.

receive timing requirements over recommended ranges of supply voltages and operating free-air temperature, variable-data-rate mode (see Figure 6)

PARAMETER		MIN	MAX	UNIT
$t_{d(TSDR)}$	Delay time, time slot from DCLKR (see Note 11)	140	$t_{w(DCLKR)}-140$	ns
$t_{d(FSR)}$	Delay time, frame sync $T_{C(CLK)}$	100	$t_{c(CLK)}-100$	ns
$t_{su(PCM\ IN)}$	Setup time before bit 7 falling edge	10		ns
$t_{h(PCM\ IN)}$	Hold time after bit 8 falling edge	60		ns
$t_{w(DCLKR)}$	Pulse duration, DCLKR	488	15620	ns
t_{SER}	Time-slot end receive time	0		ns

NOTE 11: t_{FSLR} minimum requirement overrides the $t_{c(TSDR)}$ maximum requirement for 64-kHz operation.

64-kbit operation timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{FSLX}	Transmit frame sync, minimum down time	FSX = TTL high for remainder of frame	488		ns
t_{FSLR}	Receive frame sync, minimum down time	FSR = TTL high for remainder of frame	1952		ns
$t_{w(DCLK)}$	Pulse duration, data clock			10	μs

switching characteristics

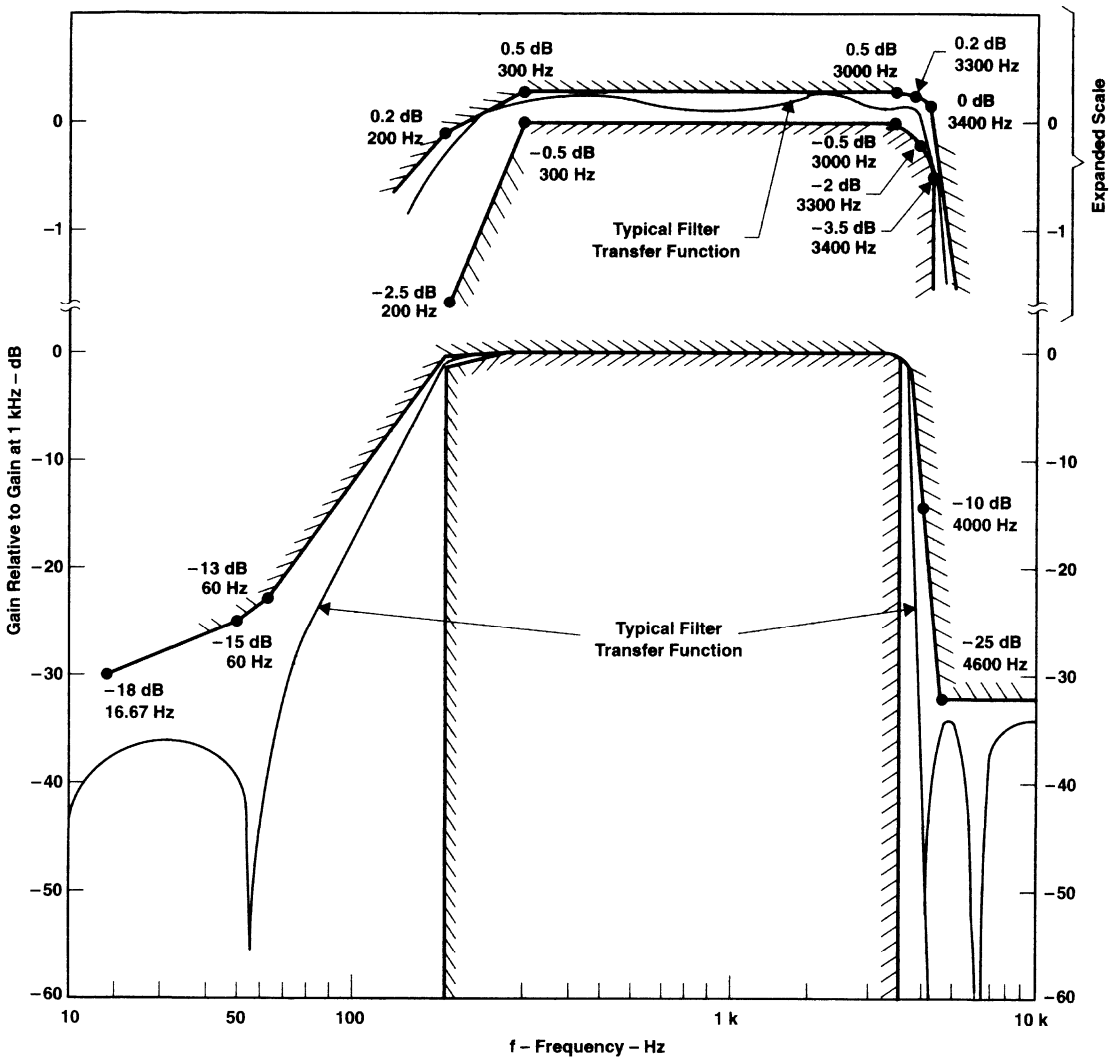
propagation delay times over recommended ranges of operating conditions, fixed-data-rate mode (see timing diagrams)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	From rising edge of transmit clock to bit 1 data valid at PCM OUT (data enable time on time-slot entry)	C_L = 0 to 100 pF	0	145	ns
t_{pd2}	From rising edge of transmit clock bit n to bit n data valid at PCM OUT (data valid time)	C_L = 0 to 100 pF	0	145	ns
t_{pd3}	From falling edge of transmit clock bit 8 to bit 8 Hi-Z at PCM OUT (data float time on time-slot exit)	C_L = 0	60	215	ns
t_{pd4}	From rising edge of transmit clock bit 1 to TSX active (low) (time-slot enable time)	C_L = 0 to 100 pF	0	145	ns
t_{pd5}	From falling edge of transmit clock bit 8 to TSX inactive (high) (time-slot disable time)	C_L = 0	60	190	ns

propagation delay times over recommended ranges of operating conditions, variable-data-rate mode

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd6}	From DCLKX	C_L = 0 to 100 pF	0	100	ns
t_{pd7}	From time-slot enable to PCM OUT		0	50	ns
t_{pd8}	From time-slot disable to PCM OUT		0	80	ns
t_{pd9}	From FSX	$t_{d(TSDX)}$ = 140 ns	0	140	ns

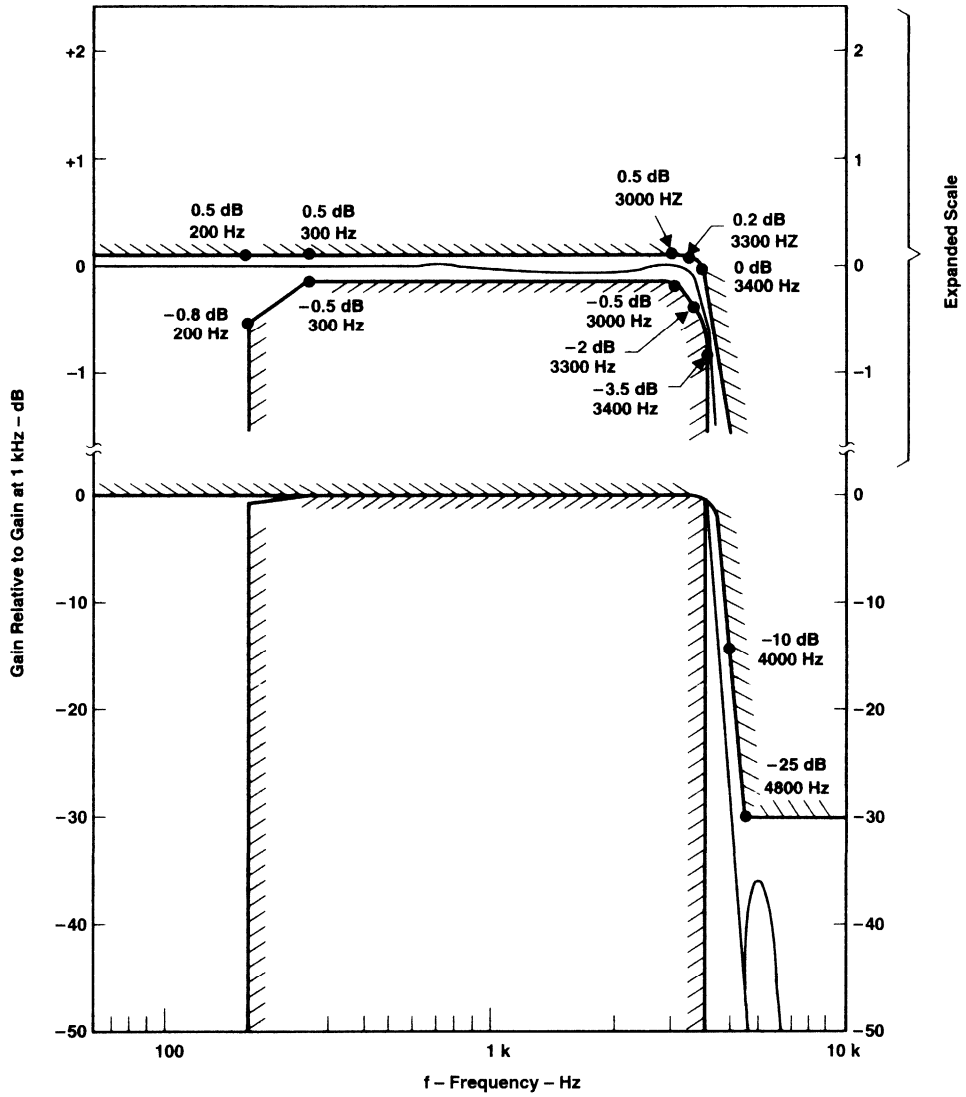
PARAMETER MEASUREMENT INFORMATION



NOTE A: This is a typical transfer function of the receiver filter component.

Figure 1. Transfer Characteristics of the Transmit Filter

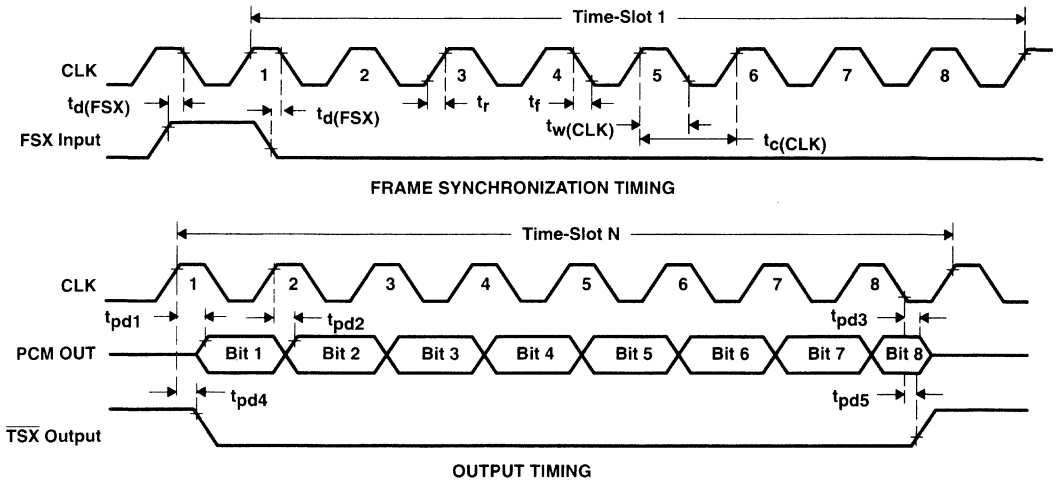
PARAMETER MEASUREMENT INFORMATION



NOTE A: This is a typical transfer function of the receive filter component.

Figure 2. Transfer Characteristics of the Receive Filter

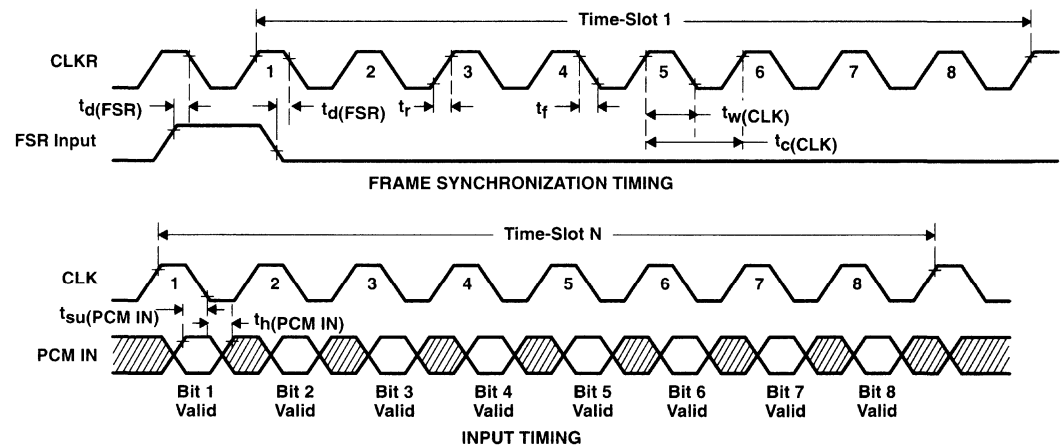
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Inputs are driven from 0.45 V to 2.4 V. Time intervals are referenced to 2 V if the high level is indicated and 0.8 V if the low level is indicated.

B. Bit 1 is the most significant bit (MSB) and is clocked in first on the PCM IN input or is clocked out first on the PCM OUT output. Bit 8 is the least significant bit (LSB) and is clocked in last on the PCM IN input or is clocked out last on the PCM OUT output.

Figure 3. Transmit Timing (Fixed-Data Rate)

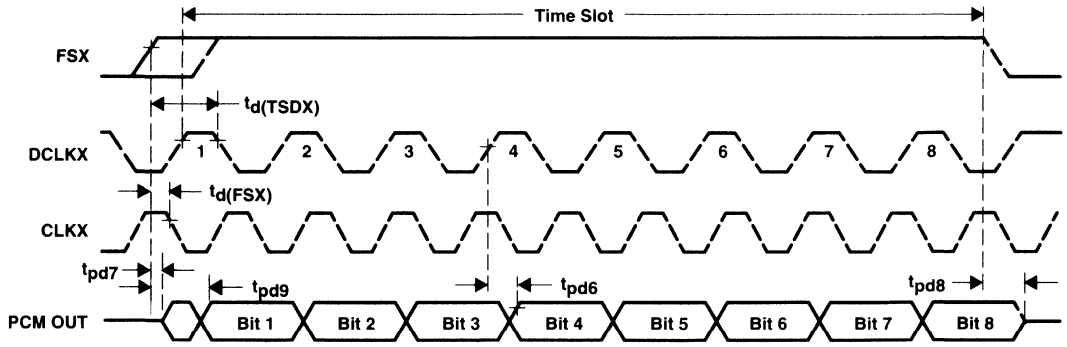


NOTES: A. Inputs are driven from 0.45 V to 2.4 V. Time intervals are referenced to 2 V if the high level is indicated and 0.8 V if the low level is indicated.

B. Bit 1 is the most significant bit (MSB) and is clocked in first on the PCM IN input or is clocked out first on the PCM OUT output. Bit 8 is the least significant bit (LSB) and is clocked in last on the PCM IN input or is clocked out last on the PCM OUT output.

Figure 4. Receive Timing (Fixed-Data Rate)

PARAMETER MEASUREMENT INFORMATION

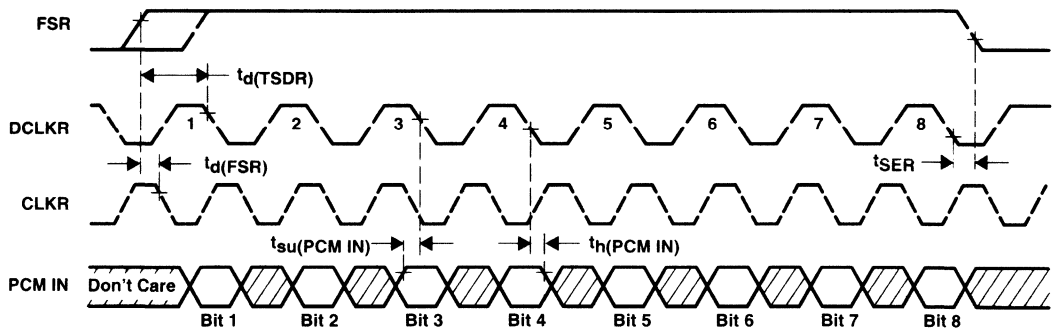


NOTES: A. Inputs are driven from 0.45 V to 2.4 V. Time intervals are referenced to 2 V if the high level is indicated and 0.8 V if the low level is indicated.

B. Bit 1 is the most significant bit (MSB) and is clocked in first on the PCM IN input or is clocked out first on the PCM OUT output. Bit 8 is the least significant bit (LSB) and is clocked in last on the PCM IN input or is clocked out last on the PCM OUT output.

C. All timing parameters referenced to V_{IH} and V_{IL} except t_{pd7} and t_{pd8}, which references the high-impedance state.

Figure 5. Transmit Timing (Variable-Data Rate)



NOTES: A. Inputs are driven from 0.45 V to 2.4 V. Time intervals are referenced to 2 V if the high level is indicated and 0.8 V if the low level is indicated.

B. Bit 1 is the most significant bit (MSB) and is clocked in first on the PCM IN input or is clocked out first on the PCM OUT output. Bit 8 is the least significant bit (LSB) and is clocked in last on the PCM IN input or is clocked out last on the PCM OUT output.

C. All timing parameters referenced to V_{IH} and V_{IL} except t_{pd7} and t_{pd8}, which references the high-impedance state.

Figure 6. Receive Timing (Variable-Data Rate)

PRINCIPLES OF OPERATION

system reliability and design considerations

TCM29C18, TCM29C19, TCM129C18, and TCM129C19 system reliability and design considerations are described in the following paragraphs.

latch-up

Latch-up is possible in all CMOS devices. It is caused by the firing of a parasitic SCR that is present due to the inherent nature of CMOS. When a latch-up occurs, the device draws excessive amounts of current and will continue to draw heavy current until power is removed. Latch-up can result in permanent damage to the device if supply current to the device is not limited.

Even though these devices are heavily protected against latch-up, it is still possible to cause latch-up under certain conditions in which excess current is forced into or out of one or more terminals. Latch-up can occur when the positive supply voltage drops momentarily below ground, when the negative supply voltage rises momentarily above ground, or possibly if a signal is applied to a terminal after power has been applied but before the ground is connected. This can happen if the device is hot-inserted into a card with the power applied, or if the device is mounted on a card that has an edge connector and the card is hot-inserted into a system with the power on.

To help ensure that latch-up does not occur, it is considered good design practice to connect a reverse-biased Schottky diode (with a forward voltage drop of less than or equal to 0.4 V – 1N5711 or equivalent) between the power supply and GND (see Figure 7). If it is possible that a TCM29C18-, TCM29C19-, TCM129C18-, or TCM129C19-equipped card that has an edge connector could be hot-inserted into a powered-up system, it is also important to ensure that the ground edge connector traces are longer than the power and signal traces so that the card ground is always the first to make contact.

device power-up sequence

Latch-up can also occur if a signal source is connected without the device being properly grounded. A signal applied to one terminal could then find a ground through another signal terminal on the device. To ensure proper operation of the device and as a safeguard against this sort of latch-up, it is recommended that the following power-up sequence always be used:

1. Ensure that no signals are applied to the device before the power-up sequence is complete.
2. Connect GND.
3. Apply V_{BB} (most negative voltage).
4. Apply V_{CC} (most positive voltage).
5. Force a power down condition in the device.
6. Connect clocks.
7. Release the power down condition.
8. Apply FS synchronization pulses.
9. Apply the signal inputs.

When powering down the device, this procedure should be followed in the reverse order.

PRINCIPLES OF OPERATION

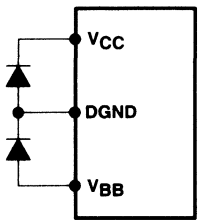


Figure 7. Latch-Up Protection Diode Connection

internal sequencing

On the transmit channel, digital outputs PCM OUT and $\overline{TSX}$ are held in the high-impedance state for approximately four frames (500 µs) after power up or application of V_{BB} or V_{CC}. After this delay, PCM OUT, $\overline{TSX}$, and signaling are functional and occur in the proper time slot. The analog circuits on the transmit side require approximately 60 ms to reach their equilibrium value due to the autozero circuit settling time. Thus valid digital information, such as on/off hook detection, is available almost immediately while analog information is available after some delay.

To further enhance system reliability, PCM OUT and $\overline{TSX}$ are placed in the high-impedance state approximately 20 µs after an interruption of CLKX. These interruptions could possibly occur with some kind of fault condition.

power-down and standby operations

To minimize power consumption, a power-down mode and three standby modes are provided.

For power down, an external low signal is applied to $\overline{PDN}$. In the absence of a signal, $\overline{PDN}$ is internally pulled up to a high logic level and the device remains active. In the power-down mode, the average power consumption is reduced to 5 mW.

Three standby modes give the user the options of placing the entire device on standby, placing only the transmit channel on standby, or placing only the receive channel on standby. To place the entire device on standby, both FSX and FSR are held low. For transmit-only operation (receive channel on standby), FSX is high and FSR is held low. For receive-only operation (transmit section on standby), FSR is high and FSX is held low. When the entire device is in standby mode, power consumption is reduced to 12 mW. See Table 1 for power-down and standby procedures.

Table 1. Power-Down and Standby Procedures

DEVICE STATUS	PROCEDURE	TYPICAL POWER CONSUMPTION	DIGITAL OUTPUT STATUS
Power down	$\overline{PDN}$ = TTL low	5 mW	$\overline{TSX}$ and PCM OUT are in the high-impedance state
Entire device on standby	FSX and FSR are TTL low	12 mW	$\overline{TSX}$ and PCM OUT are in the high-impedance state
Only transmit on standby	FSX is TTL low, FSR is TTL high	70 mW	$\overline{TSX}$ and PCM OUT are placed in the high-impedance state within 300 ns
Only receive on standby	FSR is TTL low, FSX is TTL high	110 mW	

PRINCIPLES OF OPERATION

fixed-data-rate timing (see Figures 3 and 4)

Fixed-data-rate timing is selected by connecting DCLKR to V_{BB} and uses master clock CLK, frame-synchronizer clocks FSX and FSR, and output $\overline{TSX}$. FSX and FSR are 8-kHz inputs that set the sampling frequency. Data is transmitted on PCM OUT on the first eight positive transitions of CLK following the rising edge of FSX. Data is received on PCM IN on the first eight falling edges of CLK following FSX. A digital-to-analog (D/A) conversion is performed on the received digital word and the resulting analog sample is held on an internal sample-and-hold capacitor until transferred to the receive filter.

The TCM29C18 and TCM129C18 operate at 2.048 MHz only. The TCM29C19 and TCM129C19 operate at 1.536 MHz only.

variable-data-rate timing

Variable-data-rate timing is selected by connecting DCLKR to the bit clock for the receive PCM highway rather than to V_{BB}. It uses master clock CLK, bit clocks DCLKX and DCLKR, and frame-synchronization clocks FSX and FSR.

Variable-data-rate timing allows for a flexible data frequency. The frequency of the bit clocks can be varied from 64 kHz to 2.048 MHz. The bit clocks must be asynchronous; however, the master clock is restricted to 2.048 MHz.

When FSX/TSXE is high, PCM data is transmitted from PCM OUT onto the highway on the next eight consecutive positive transitions of DCLKX. Similarly, while the FSR/TSRE input is high, the PCM word is received from the highway by PCM IN on the next eight consecutive negative transitions of DCLKR.

The transmitted PCM word is repeated in all remaining time slots in the 125-μs frame as long as DCLKX is pulsed and FSX is held high. This feature, which allows the PCM word to be transmitted to the PCM highway more than once per frame if desired, is available only with variable-data-rate timing.

asynchronous operation

In either timing mode, the master clock, data clock, and time slot strobe must be synchronized at the beginning of each frame. Specifically, in the variable-rate mode, the falling edge of CLKX must occur within $t_{d(FSX)}$ ns after the rise of FSX, and the falling edge of DCLKX must occur within t_{TSDX} ns after the rise of FSX. CLK and DCLKX are synchronized once per frame but may be of different frequencies. The receive channel operates in a similar manner and is completely independent of the transmit timing (see Figure 6).

PRINCIPLES OF OPERATION

transmit operation

transmit filter

The input section provides gain adjustment in the pass band by means of an on-chip uncommitted operational amplifier. The load impedance to ground (ANLG GND) at the amplifier output (GSX) must be greater than 10 kΩ in parallel with less than 50 pF. The input signal on ANLG IN can be either ac or dc coupled.

A low-pass antialiasing filter section is included on the device. This section provides 35-dB attenuation at the sampling frequency. No external components are required to provide the necessary antialiasing function for the switched-capacitor section of the transmit filter.

The pass band section provides flatness and stopband attenuation that fulfills the AT&T D3/D4 channel bank transmission specification and CCITT recommendation G.712. The device specifications meet or exceed digital class 5 central office switching-systems requirements.

A high-pass section configuration was chosen to reject low-frequency noise from 50- and 60-Hz power lines, 17-Hz European electric railroads, ringing frequencies and their harmonics, and other low-frequency noise. Even with the high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200 Hz. This feature allows the use of low-cost transformer hybrids without external components.

encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample-and-hold capacitor. The encoder performs an analog-to-digital conversion on a switched-capacitor array. Digital date representing the sample is transmitted on the first eight data clock bits of the next frame.

The autozero circuit corrects for dc offset on the input signal to the encoder. The autozero circuit uses the sign bit averaging technique. The sign bit from the encoder output is long-term averaged and subtracted from the input to the encoder. All dc offset is removed from the encoder input waveform.

The analog input is encoded into an 8-bit digital representation by use of the μ-law encoding scheme (CCITT G.711) that equates to 12 bits of resolution for low amplitude signals. Similarly, the decoding section converts 8-bit PCM data into an analog signal with 12 bits of dynamic range. The filter characteristics (band pass) for the encoder and decoder are determined by a single clock input (CLK). The filter roll off (–3 dB) is derived by:

$f_{co} = k \bullet f_{CLK}/256$ for the TCM29C18 and TCM129C18
$f_{co} = k \bullet f_{CLK}/192$ for the TCM29C19 and TCM129C19

where k has a value of 0.44 for the high-frequency roll-off point and a value of 0.019 for the low-frequency roll-off point.

The sampling rate of the ADC is determined by the transmit frame-sync clock (FSX); the sampling rate of the DAC is determined by the receive frame-sync clock (FSR). Once a conversion is initiated by FSX or FSR, data is clocked in or out on the next eight consecutive clock pulses in the fixed-rate-mode. Likewise, data may also be transferred on the next eight consecutive clock pulses of the data clocks (DCLKX and DCLKR) in the variable-data-rate mode. In the variable-data-rate mode, DCLKX and DCLKR are independent but must be in the range from $f_{CLK}/32$ to f_{CLK}.

PRINCIPLES OF OPERATION

receive operation

decoding

The serial PCM word is received at PCM IN on the first eight data clock bits of the frame. Digital-to-analog conversion is performed and the corresponding analog sample is held on an internal sample-and-hold capacitor. This sample is transferred to the receive filter.

receive filter

The receive section of the filter provides pass band flatness and stop band rejection that fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin x)/x response of such decoders.

receive output power amplifiers

A balanced-output amplifier is provided to allow maximum flexibility in output configuration. Either of the two outputs can be used single ended (i.e., referenced to ANLG GND) to drive single-ended loads. Alternatively, the differential output directly drives a bridged load. The output stage is capable of driving loads as low as 300 Ω single ended to a level of 12 dBm or 600 Ω differentially to a level of 15 dBm.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions (i.e., when the digital input at PCM IN is the eight-code sequence specified in CCITT recommendation G.711).

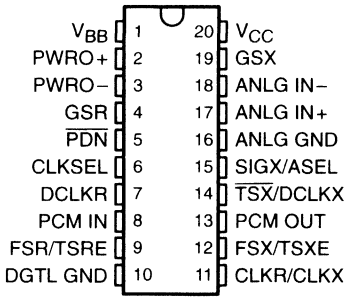
output gain

The devices are internally connected to set PWRO+ and PWRO– to 0 dBm.

SCTS029A – AUGUST 1989 –REVISED JULY 1996

- **Combined ADC, DAC, and Filters**
- **Extended Variable Frequency Operation**
  - **Master Clock Up to 4.096 MHz**
  - **Sample Rates Up to 16 kHz**
  - **Passband Up to 6 kHz**
- **Reliable Silicon-Gate CMOS Technology**
- **Low Power Consumption**
  - **Operating Mode . . . 80 mW Typical**
  - **Power-Down Mode . . . 5 mW Typical**
- **Excellent Power-Supply Rejection Ratio Over Frequency Range of 0 to 50 kHz**
- **No External Components Needed for Sample, Hold, and Autozero Functions**
- **Precision Internal Voltage References**
- **μ-law and A-law Coding**

DW OR N PACKAGE
(TOP VIEW)



description

The TCM29C23 and TCM129C23 are single-chip PCM codecs (pulse-code-modulated encoders and decoders) and PCM lines filters. These devices provide all the functions required to interface a full-duplex (4-wire) voice telephone circuit with a TDM (time-division-multiplexed) system. Primary applications include digital encryption systems, digital voice-band data storage systems, digital signal processing, and mobile telephones.

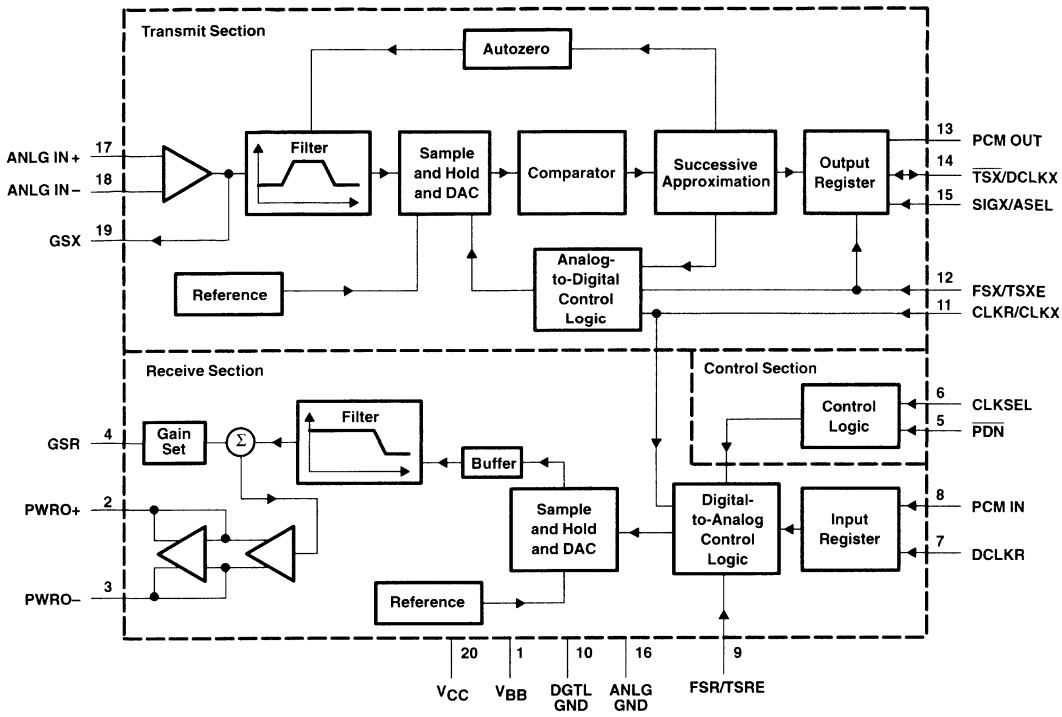
These devices are designed to perform the transmit encoding (A/D conversion) and receive decoding (D/A conversion) as well as the transmit and receive filtering functions in a pulse-code-modulated system. They are intended to be used at the analog termination of a PCM line or trunk.

The TCM29C23 and TCM129C23 provide the band-pass filtering of the analog signals prior to encoding and after decoding. These combination devices perform the encoding and decoding of voice and call progress tones as well as the signaling supervision information.

The TCM29C23 is characterized for operation from 0°C to 70°C. The TCM129C23 is characterized for operation from –40°C to 85°C.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ANLG GND	16		Analog ground return for all internal voice circuits. Not internally connected to DGTL GND.
ANLG IN+	17	I	Noninverting analog input to uncommitted transmit operational amplifier.
ANLG IN–	18	I	Inverting analog input to uncommitted transmit operational amplifier.
CLKR	11	I	Receive master clock and data clock for the fixed-data-rate mode. Receive master clock only for variable-data-rate mode. CLKR and CLKX are internally connected together.
CLKSEL	6	I	Clock frequency selection. Input must be connected to V_{BB}, V_{CC}, or ground to reflect the master clock frequency.
CLKX	11	I	Transmit master clock and data clock for the fixed-data-rate mode. Transmit master clock only for variable-data-rate mode. CLKR and CLKX are internally connected.
DCLKR	7	I	Selects fixed- or variable-data-rate operation. When connected to V_{BB}, the device operates in the fixed-data-rate mode. When DCLKR is not connected to V_{BB}, the device operates in the variable-data-rate mode and DCLKR becomes the receive data clock, which operates at frequencies from 64 kHz to 4.096 MHz.
DGTL GND	10		Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
FSR/TSRE	9	I	Frame-synchronization clock input/time-slot enable for receive channel. In the fixed-data-rate mode, FSR distinguishes between signaling and nonsignaling frames by a double- or single-length pulse, respectively. In the variable-data-rate mode, this signal must remain high for the duration of the slot. The receive channel enters the standby state when FSR is TTL low for 300 ms.
FSX/TSXE	12	I	Frame-synchronization clock input/time-slot enable for the transmit channel. Operates independently of, but in an analogous manner to, FSR/TSRE. The transmit channel enters the standby state when FSX is low for 300 ms.
GSR	4	I	Input to the gain-setting network on the output power amplifier. Transmission level can be adjusted over a 12-dB range depending upon the voltage at GSR.
GSX	19	O	Output terminal of internal uncommitted operational amplifier. Internally, this is the voice signal input to the transmit filter.
PCM IN	8	I	Receive PCM input. PCM data is clocked in on this pin on eight consecutive negative transition of the receive data clock, which is CLKR in fixed-data-rate timing and DCLKR in variable-data-rate timing.
PCM OUT	13	O	Transmit PCM output. PCM data is clocked out of this output on eight consecutive positive transition of the transmit data clock, which is CLKX in fixed-data-rate timing and DCLKX in variable-data-rate timing.
$\overline{PDN}$	5	I	Power-down select. This device is inactive with a TTL low-level input to this terminal and active with a TTL high-level input to this terminal.
PWRO+	2	O	Noninverting output of power amplifier. Can drive transformer hybrids or high-impedance loads directly in either a differential or single-ended configuration.
PWRO–	3	O	Inverting output of power amplifier; functionally identical to but complementary to PWRO+.
SIGX/ASEL	15	I	A-law and μ-law operation select. When connected to V_{BB}, A-law is selected. When connected to V_{CC} or ground, μ-law is selected.
$\overline{TSX}$/DCLKX	12	I/O	Transmit channel time slot strobe (output) or data clock (input) for the transmit channel. In the fixed-data-rate mode, this is an open-drain output to be used as an enable signal for a 3-state output buffer. In the variable-data-rate mode, DCLKX becomes the transmit data clock, which operates at TTL levels from 64 kHz to 2.048 MHz.
V_{BB}	1		Most negative supply voltage; input is –5 V ±5%.
V_{CC}	16		Most positive supply voltage; input is 5 V ±5%.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.3 V to 15 V
Output voltage range, V_O ..... −0.3 V to 15 V
Input voltage range, V_I ..... −0.3 V to 15 V
Digital ground voltage range ..... −0.3 V to 15 V
Operating free-air temperature range, T_A: TCM29C23 ..... 0°C to70°C
TCM129C23 ..... −40°C to 85°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values for maximum ratings are with respect to V_{BB}.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 3)		4.75	5	5.25	V
V_{BB}	Supply voltage		−4.75	−5	−5.25	V
	DGTL GND voltage with respect to ANLG GND			0		V
V_{IH}	High-level input voltage, all inputs except CLKSEL		2.2			V
V_{IL}	Low-level input voltage, all inputs except CLKSEL				0.8	V
	CLKSEL input voltage	For 2.048 MHz	V_{BB}		V_{BB} +0.5	V
		For 1.544 MHz	0		0.5	
		For 1.536 Mhz	V_{CC} −0.5		V_{CC}	
R_L	Load resistance	At GSX	10			kΩ
		At PWRO+ and/or PWRO−	300			Ω
C_L	Load capacitance	At GSX			50	pF
		At PWRO+ and/or PWRO−			100	
T_A	Operating free-air temperature	TCM29C23	0		70	°C
		TCM129C23	−40		85	

NOTES: 2. To avoid possible damage to these CMOS devices and resulting reliability problems, the power-up procedure described in the device power-up sequence paragraphs later in this document should be followed.

3. Voltages at analog inputs and outputs, V_{CC} and V_{BB}, are with respect to ANLG GND. All other voltages are referenced to DGTL GND unless otherwise noted.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

supply current, f_{DCLK} = 4.096 MHz, outputs not loaded

PARAMETER			TEST CONDITIONS	TCM29C23			TCM129C23			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{CC}	Supply current from V_{CC}	Operating			7	9		8	13	mA
		Standby	FSX, or FSR at V_{IL} after 300 ms		0.5	1		0.7	1.5	
		Power down	$\overline{PDN}$ at V_{IL} after 10 µs		0.3	0.8		0.4	1	
I_{BB}	Supply current from V_{BB}	Operating			−7	−9		−8	−13	mA
		Standby	FSX or FSR at V_{IL} after 300 ms		−0.5	−1		−0.7	−1.5	
		Power down	$\overline{PDN}$ at V_{IL} after 10 µs		−0.3	−0.8		−0.4	−1	
P_D	Power dissipation	Operating			70	90		80	130	mW
		Standby	FSX or FSR at V_{IL} after 300 ms		5	10		7	15	
		Power down	$\overline{PDN}$ at V_{IL} after 10 µs		3	8		4	10	

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

digital interface

PARAMETER			TEST CONDITIONS	TMC29C23			TMC129C23			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	PCM OUT	I_{OH} = −9.6 mA	2.4			2.4			V
V_{OL}	Low-level output voltage at PCM OUT, TSX, SIG		I_{OL} = 3.2 mA			0.4			0.5	V
I_{IH}	High-level input current, any digital input		V_I = 2.2 V to V_{CC}			10			12	µA
I_{IL}	Low-level input current, any digital input		V_I = 0 to 0.8 V			10			12	µA
C_i	Input capacitance				5	10		5	10	pF
C_o	Output capacitance				5			5		pF

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

transmit amplifier input

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input current at ANLG IN+, ANLG IN−	V_I = −2.17 V to 2.17 V			±200	nA
Input offset voltage at ANLG IN +, ANLG IN−				±25	mV
Common-mode rejection at ANLG IN+, ANLG IN−		55			dB
Open-loop voltage amplification at GSX		5000			
Open-loop unity-gain bandwidth at GSX			1		MHz
Input resistance at ANLG IN+, ANLG IN−		10			MΩ

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

receive filter output

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output offset voltage at PWRO+, PWRO− (single ended)	Relative to ANLG GND		80		mV
Output resistance at PWRO+, PWRO−			1		Ω

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

gain and dynamic range, V_{CC} = 5 V, V_{BB} = −5 V, T_A = 25°C (unless otherwise noted) (see Notes 4, 5, and 6)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Encoder milliwatt response (transmit gain tolerance)		Signal input = 1.064 Vrms for μ-law		±0.5	±1	dBm0
		Signal input = 1.068 Vrms for A-law				
Encoder milliwatt response (nominal supplies and temperature)		T_A = 0°C to 70°C, Supply voltages = 5 V ±5%			±0.15	dB
Digital milliwatt response (receive tolerance gain) relative to zero-transmission level point		Signal input per CCITT G.711, Output signal = 1 kHz		±0.5	±1	dBm0
Digital milliwatt response variation with temperature and supplies		T_A = 0°C to 70°C, Supply voltages = 5 V ±5%			±0.15	dB
Zero-transmission-level point, transmit channel (0 dBm0)	μ-law	R_L = 600 Ω		2.76		dBm
	A-law			2.79		
	μ-law	R_L = 900 Ω		1		
	A-law			1.03		
Zero-transmission-level point, receive channel (0 dBm0)	μ-law	R_L = 600 Ω		5.76		dBm
	A-law			5.79		
	μ-law	R_L = 900 Ω		4		
	A-law			4.03		

NOTES: 4. Unless otherwise noted, the analog input is a 0-dBm0, 1020-Hz sine wave, where 0 dBm0 is defined as the zero-reference point of the channel under test. This corresponds to an analog signal input of 1.064 Vrms or an output of 1.503 Vrms.

5. The input amplifier is set for noninverting unity gain. The digital input is a PCM bit stream generated by passing a 0-dBm0, 1020-Hz sine wave through an ideal encoder.

6. Receive output is measured single ended in the maximum gain configuration. To set the output amplifier for maximum gain, GSR is connected to PWRO– and the output is taken at PWRO+. All output levels are (sin x)/x corrected.

gain tracking over recommended ranges of supply voltage and operating free-air temperature, reference level = −10 dBm0

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit gain-tracking error, sinusoidal input	3 ≥ input level ≥ −40 dBm0		±0.5	dB
	−40 > input level ≥ −50 dBm0		±1.5	
Receive gain-tracking error, sinusoidal input	3 ≥ input level ≥ −40 dBm0		±0.5	dB
	−40 > input level ≥ −50 dBm0		±1.5	

noise over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise, C-message weighted	ANLG IN+ = ANLG GND, ANLG IN– = GSX		18	dBrnC0
Transmit noise, psophometrically weighted	ANLG IN+ = ANLG GND, ANLG IN– = GSX		−72	dBm0p
Receive noise, C-message-weighted quiet code	PCM IN = 11111111 (μ-law), PCM IN = 10101010 (A-law), Measured at PWRO+		11	dBrnC0
Receive noise, psophometrically weighted	PCM = lowest positive decode level		−79	dBm0p

power-supply rejection and crosstalk attenuation over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{CC} supply-voltage rejection ratio, transmit channel	0 ≤ f < 30 kHz	Idle channel, Supply signal = 200 mV peak to peak, f measured at PCM OUT		−30		dB
	30 ≤ f < 50 kHz			−45		
V_{BB} supply-voltage rejection ratio, transmit channel	0 ≤ f < 30 kHz	Idle channel, Supply signal = 200 mV peak to peak, f measured at PCM OUT		−30		dB
	30 ≤ f < 50 kHz			−55		
V_{CC} supply-voltage rejection ratio, receive channel (single ended)	0 ≤ f < 30 kHz	Idle channel, Supply signal = 200 mV peak to peak, f measured at PWRO+		−20		dB
	30 ≤ f < 50 kHz			−45		
V_{BB} supply-voltage rejection ratio, receive channel (single ended)	0 ≤ f < 30 kHz	Idle channel, Supply signal = 200 mV peak to peak, Narrow-band, f measured at PWRO+		−20		dB
	30 ≤ f < 50 kHz			−45		
Crosstalk attenuation, transmit to receive (single ended)		ANLG IN+ = 0 dBm0, f = 1.02 kHz, Unity gain, PCM IN = lowest decode level, Measured at PWRO+	68			dB
Crosstalk attenuation, receive to transmit (single ended)		PCM IN = 0 dBm0, f = 1.02 kHz, Measured at PCM OUT	68			dB

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

distortion over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit signal-to-distortion ratio, sinusoidal input (CCITT G.712 – Method 2)	0 ≥ ANLG IN+ ≥ −30 dBm0	33			dB
	−30 > ANLG IN+ ≥ −40 dBm0	28			
	−40 > ANLG IN+ ≥ −45 dBm0	23			
Receive signal-to-distortion ratio, sinusoidal input (CCITT G.712 – Method 2)	0 ≥ ANLG IN+ ≥ −30 dBm0	33			dB
	−30 > ANLG IN+ ≥ −40 dBm0	28			
	−40 > ANLG IN+ ≥ −45 dBm0	23			
Transmit single-frequency distortion products	AT&T Advisory #64 (3.8), Input signal = 0 dBm0			−40	dBm0
Receive single-frequency distortion products	AT&T Advisory #64 (3.8), Input signal = 0 dBm0			−46	dBm0

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

transmit filter transfer over recommended ranges of supply voltage and operating free-air temperature, f_{DCLK} = 4.096 MHz, FSX/FSR = 16 kHz (see Figure 1)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	Input amplifier set for unity gain, Noninverting maximum gain output, Input signal at ANLG IN+ is 0 dBm0	50 Hz	−10	0	dB
		200 Hz	−1	0.5	
		300 Hz to 6 kHz	−0.5	0.5	
		6.5 kHz	−4	0.3	
		6.8 kHz	−6	0	
		8 kHz		−12	
		9 kHz and above		−30	

receive filter transfer over recommended ranges of supply voltage and operating free-air temperature (see Figure 2)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	Input signal at PCM IN is 0 dBm0	Below 200 Hz	−2	0.5	dB
		200 Hz	−1	0.5	
		300 Hz to 6 kHz	−0.5	0.5	
		6.6 kHz	−4	0.3	
		6.8 kHz	−6	0	
		8 kHz		−12	
		9.2 kHz and above		−30	

timing requirements

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figure 3)

		MIN	TYP†	MAX	UNIT
$t_{c(CLK)}$	Clock period, for CLKX, CLKR (2.048-MHz systems)	244			ns
t_r, t_f	Rise and fall times for CLKX and CLKR			5	20	ns
$t_{w(CLK)}$	Pulse duration for CLKX and CLKR (see Note 7)	110			ns
$t_{w(DCLK)}$	Pulse duration, DCLK (f_{DCLK} = 64 kHz to 2.048 MHz) (see Note 7)	110			ns
	Clock duty cycle, [$t_{w(CLK)}/t_{c(CLK)}$] for CLKX and CLKR	45%	50%	55%	

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.
NOTE 7: FSX CLK must be phase locked with CLKX. FSR CLK must be phase locked with CLKR.

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 3)

PARAMETER		MIN	MAX	UNIT
$t_{d(FSX)}$	Frame-sync delay time	60	$t_{c(CLK)}-60$	ns

receive timing requirements over recommended ranges of supply voltages and operating free-air temperature, fixed-data-rate mode (see Figure 4)

PARAMETER		MIN	MAX	UNIT
$t_{d(FSR)}$	Frame-sync delay time	60	$t_{c(CLK)}-60$	ns

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see Figure 5)

PARAMETER		MIN	MAX	UNIT
$t_{d(TSDX)}$	Time-slot delay time from DCLKX	60	$t_{d(DCLKX)}-60$	ns
$t_{d(FSX)}$	Frame-sync delay time	60	$t_{c(CLK)}-60$	ns
$t_{c(DCLKX)}$	Clock period for DCLKX	244	15620	ns

receive timing requirements over recommended ranges of supply voltages and operating free-air temperature, variable-data-rate mode (see Figure 6)

PARAMETER		MIN	MAX	UNIT
$t_{d(TSDR)}$	Time-slot delay time from DCLKR	60	$t_{d(DCLKR)}-140$	ns
$t_{d(FSR)}$	Frame-sync delay time	60	$t_{c(CLK)}-60$	ns
$t_{su(PCM\ IN)}$	Setup time before bit 7 falling edge	10		ns
$t_{h(PCM\ IN)}$	Hold time after bit 8 falling edge	60		ns
$t_{c(DCLKR)}$	Data clock frequency	244	15620	ns
t_{SER}	Time-slot end receive time	0		ns

switching characteristics

propagation delay times over recommended ranges of operating conditions, fixed-data-rate mode (see Figure 3)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	From rising edge of transmit clock to bit 1 data valid at PCM OUT (data enable time on time-slot entry) (see Note 8)	C_L = 0 to 100 pF	0	90	ns
t_{pd2}	From rising edge of transmit clock bit n to bit data valid at PCM OUT (data valid time)	C_L = 0 to 100 pF	0	90	ns
t_{pd3}	From falling edge of transmit clock bit 8 to bit 8 Hi-Z at PCM OUT (data float time on time-slot exit) (see Note 8)	C_L = 0	60	215	ns
t_{pd4}	From rising edge of transmit clock bit 1 to TSX active (low) (time slot enable time)	C_L = 0 to 100 pF	0	90	ns
t_{pd5}	From falling edge of transmit clock bit 8 to TSX inactive (high) (time-slot disable time) (see Note 8)	C_L = 0	60	190	ns

NOTE 8: Timing parameters t_{pd1}, t_{pd3}, and t_{pd5} are referenced to the high-impedance state.

propagation delay times over recommended ranges of operating conditions, variable-data-rate mode (see Note 9 and Figure 5)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd7}	Data delay time from DCLKX	C_L = 0 to 100 pF	0	90	ns
t_{pd8}	Data delay from time-slot enable to PCM OUT		0	50	ns
t_{pd9}	Data delay from time-slot disable to PCM OUT		0	80	ns
t_{pd10}	Data delay time from FSX	$t_{d(TSDX)}$ = 80 ns	0	90	ns

NOTE 9: Timing parameters t_{pd8} and t_{pd9} are referenced to the high-impedance state.

PARAMETER MEASUREMENT INFORMATION

CLK, CLKR, and CLKX selection requirements for DSP-based applications

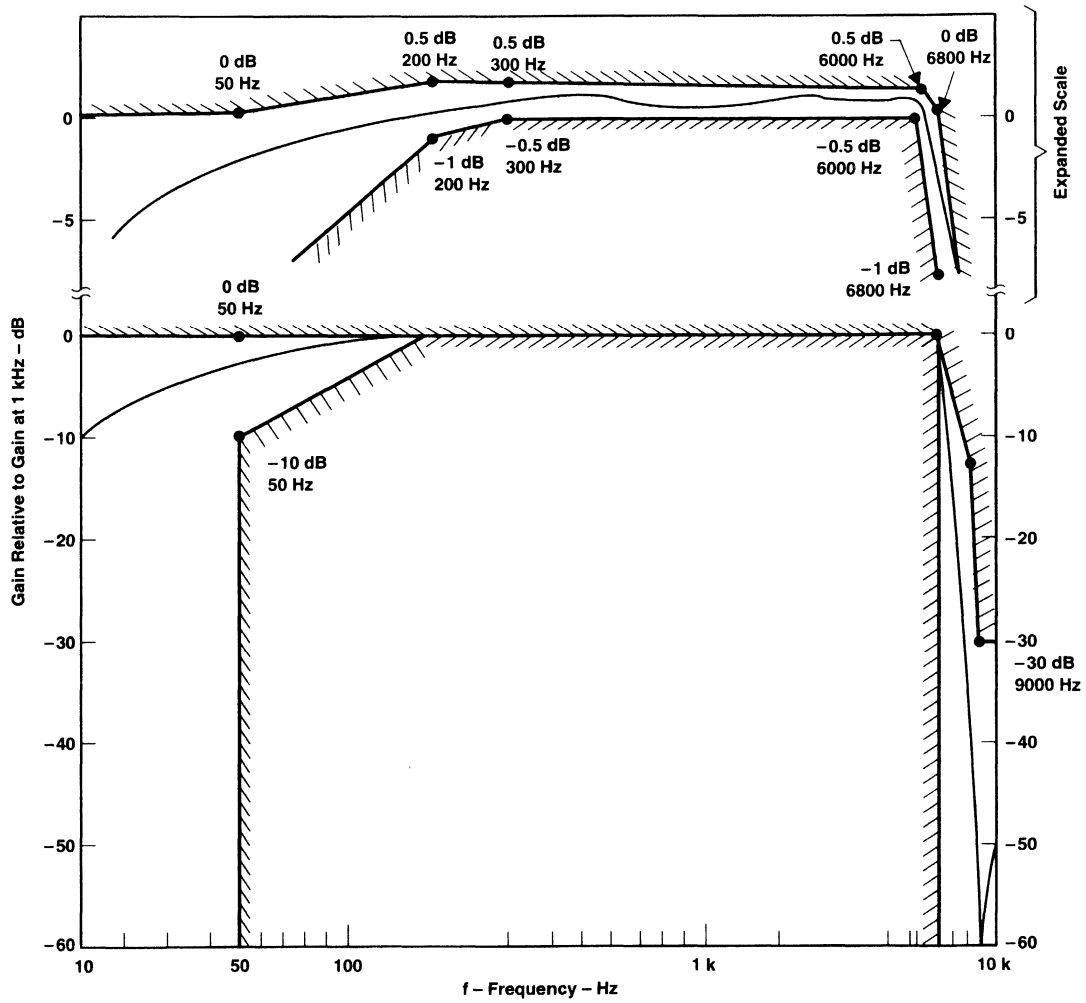
CLK, CLKR, and CLKX must be selected as follows:

CLKSEL PIN	CLK, CLKR, CLKX (BETWEEN 1 MHz to 3 MHz)
–5 V	= (256) × (frame-sync frequency)
0 V	= (193) × (frame-sync frequency)
5 V	= (192) × (frame-sync frequency)

e.g., for frame-sync frequency = 16 kHz

CLKSEL PIN	CLK, CLKR, CLKX (BETWEEN 1 MHz to 3 MHz)
–5 V	= 4.096 MHz
0 V	= 3.088 MHz
5 V	= 3.072 MHz

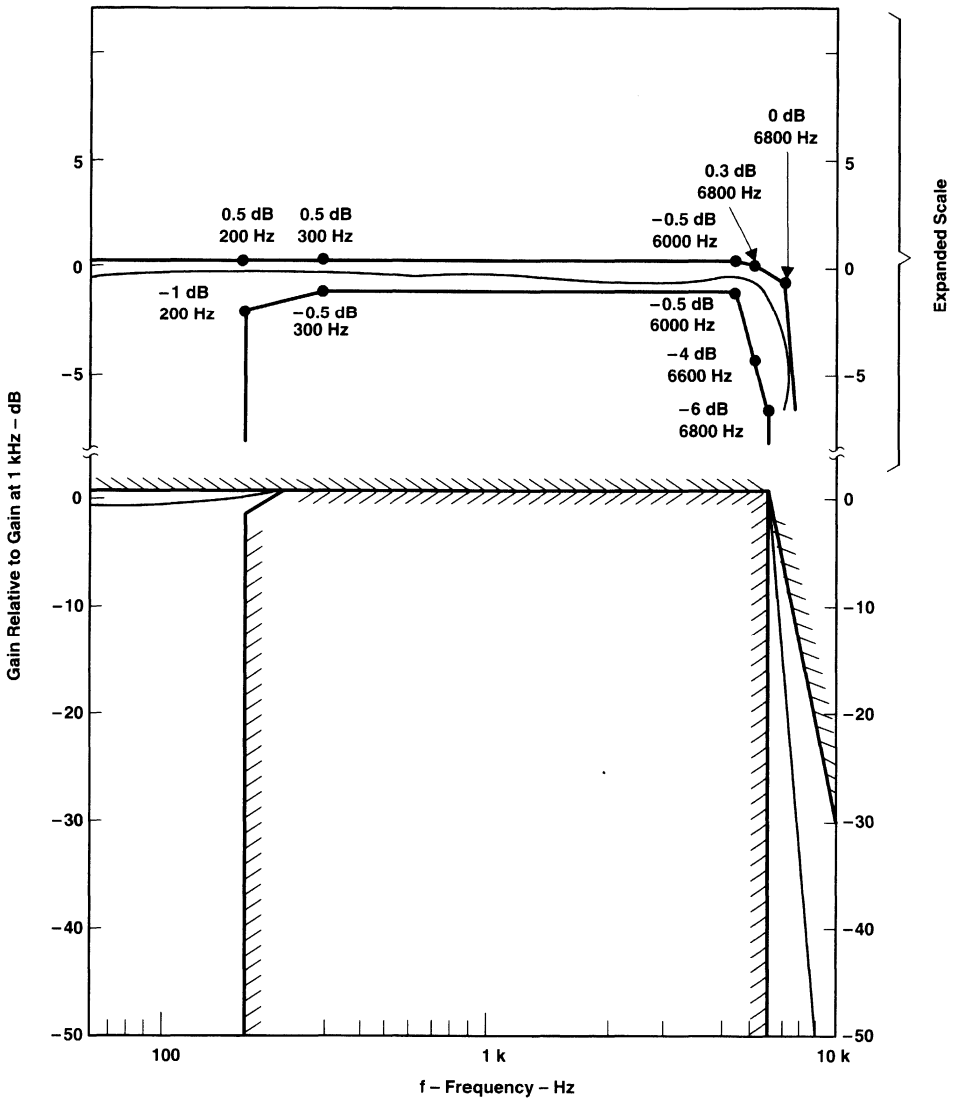
PARAMETER MEASUREMENT INFORMATION



NOTE A: CLKR/CLKX = 4.096 MHz

Figure 1. Transfer Characteristics of the Transmit Filter

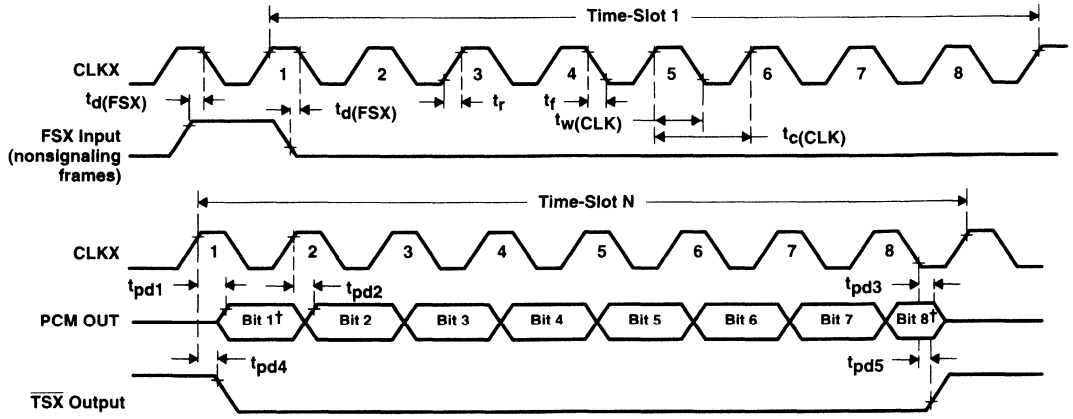
PARAMETER MEASUREMENT INFORMATION



NOTE A: CLKR/CLKX = 4.096 MHz

Figure 2. Transfer Characteristics of the Receive Filter

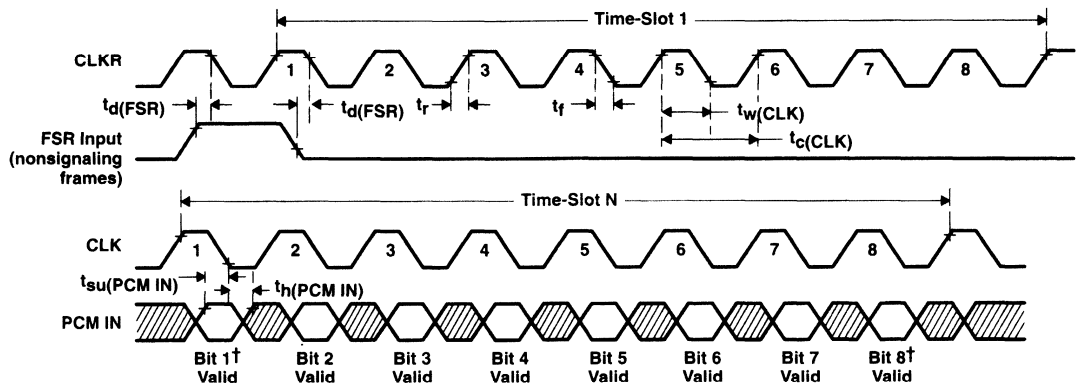
PARAMETER MEASUREMENT INFORMATION



† Bit 1 = MSB = sign bit and locked in first on PCM IN or clocked out first on PCM OUT. Bit 8 = LSB = least significant bit and is clocked in last on PCM IN or is clocked out last on PCM OUT.

NOTE A: Inputs are driven from 0.45 V to 2.4 V. Time intervals are referenced to 2 V if the high level is indicated and 0.8 V if the low level is indicated.

Figure 3. Transmit Timing (Fixed-Data Rate)

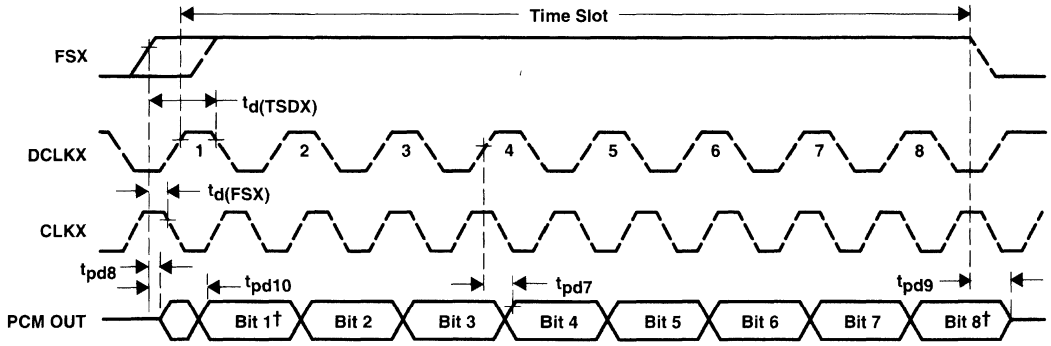


† Bit 1 = MSB = sign bit and locked in first on PCM IN or clocked out first on PCM OUT. Bit 8 = LSB = least significant bit and is clocked in last on PCM IN or is clocked out last on PCM OUT.

NOTE A: Inputs are driven from 0.45 V to 2.4 V. Time intervals are referenced to 2 V if the high level is indicated and 0.8 V if the low level is indicated.

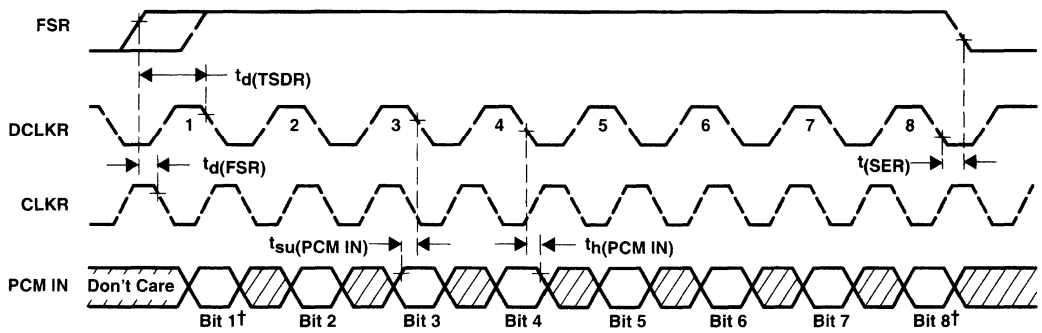
Figure 4. Receive Timing (Fixed-Data Rate)

PARAMETER MEASUREMENT INFORMATION



† Bit 1 = MSB = sign bit and locked in first on the PCM IN or clocked out first on PCM OUT. Bit 8 = LSB = least significant bit and is clocked in last on PCM IN or is clocked out last on PCM OUT.
NOTE A: IAll timing parameters referenced to V_{IH} and V_{IL} except t_{pd7} and t_{pd8}, which reference the high-impedance state.

Figure 5. Transmit Timing (Variable-Data-Rate)



† Bit 1 = MSB = sign bit and locked in first on the PCM IN or clocked out first on PCM OUT. Bit 8 = LSB = least significant bit and is clocked in last on PCM IN or is clocked out last on PCM OUT.
NOTE A: All timing parameters referenced to V_{IH} and V_{IL} except t_{pd7} and t_{pd8}, which reference the high-impedance state.

Figure 6. Receive Timing (Variable-Data-Rate)

PRINCIPLES OF OPERATION

system reliability and design considerations

TCM29C23, TCM129C23 system reliability and design considerations are described in the following paragraphs.

latch-up

Latch-up is possible in all CMOS devices. It is caused by the firing of a parasitic SCR that is present due to the inherent nature of CMOS. When a latch-up occurs, the device draws excessive amounts of current and will continue to draw heavy current until power is removed. Latch-up can result in permanent damage to the device if supply current to the device is not limited.

Even though the TCM29C23 and TCM129C23 are heavily protected against latch-up, it is still possible to cause latch-up under certain conditions in which excess current is forced into or out of one or more terminals. Latch-up can occur when the positive supply voltage drops momentarily below ground, when the negative supply voltage rises momentarily above ground, or possibly if a signal is applied to a terminal after power has been applied but before the ground is connected. This can happen if the device is hot-inserted into a card with the power applied, or if the device is mounted on a card that has an edge connector and the card is hot-inserted into a system with the power on.

To help ensure that latch-up does not occur, it is considered good design practice to connect a reverse-biased Schottky diode (with a forward voltage drop of less than or equal to 0.4 V – 1N5711 or equivalent) between the power supply and GND (see Figure 7). If it is possible that a TCM29C23- or TCM129C23-equipped card that has an edge connector could be hot-inserted into a powered-up system, it is also important to ensure that the ground edge connector traces are longer than the power and signal traces so that the card ground is always the first to make contact.

device power-up sequence

Latch-up can also occur if a signal source is connected without the device being properly grounded. A signal applied to one terminal could then find a ground through another signal terminal on the device. To ensure proper operation of the device and as a safeguard against this sort of latch-up, it is recommended that the following power-up sequence always be used:

1. Ensure that no signals are applied to the device before the power-up sequence is complete.
2. Connect GND.
3. Apply V_{BB} (most negative voltage).
4. Apply V_{CC} (most positive voltage).
5. Force a power down condition in the device.
6. Connect clocks.
7. Release the power down condition.
8. Apply FS synchronization pulses.
9. Apply the signal inputs.

When powering down the device, this procedure should be followed in the reverse order.

PRINCIPLES OF OPERATION

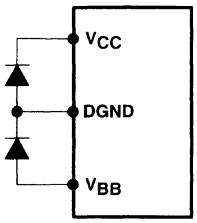


Figure 7. Latch-Up Protection Diode Connection

internal sequencing

On the transmit channel, digital outputs PCM OUT and $\overline{TSX}$ are held in the high-impedance state for approximately four frames (500 µs) after power up or application of V_{BB} or V_{CC}. After this delay, PCM OUT, $\overline{TSX}$, and signaling are functional and occur in the proper time slot. The analog circuits on the transmit side require approximately 60 ms to reach their equilibrium value due to the autozero circuit settling time. Thus valid digital information, such as on/off hook detection, is available almost immediately while analog information is available after some delay. To further enhance system reliability, PCM OUT and $\overline{TSX}$ are placed in the high-impedance state approximately 20 µs after an interruption of CLKX.

power-down and standby operations

To minimize power consumption, a power-down mode and three standby modes are provided.

For power down, an external low signal is applied to $\overline{PDN}$. In the absence of a signal, PDN is interally pulled up to a high logic level and the device remains active. In the power-down mode, the average power consumption is reduced to 5 mW.

Three standby modes give the user the options of placing the entire device on standby, placing only the transmit channel on standby, or placing only the receive channel on standby. to place the entire device on standby, both FSX and FSR are held low. For transmit-only operation (receive channel on standby), FSX is high and FSR is held low. For receive-only operation (transmit section on standby), FSR is high and FSX is held low. When the entire device is in standby mode, power consumption is reduced to an average of 3 mW. See Table 1 for power-down and standby procedures.

Table 1. Power-Down and Standby Procedures

DEVICE STATUS	PROCEDURE	TYPICAL POWER CONSUMPTION	DIGITAL OUTPUT STATUS
Power down	$\overline{PDN}$ low	3 mW	$\overline{TSX}$ and PCM OUT are in the high-impedance state; SIGR goes to low within 10 µs.
Entire device on standby	FSX and FSR are low	3 mW	$\overline{TSX}$ and PCM OUT are in the high-impedance state; SIGR goes to low within 300 ms.
Only transmit on standby	FSX is low, FSR is high	40 mW	$\overline{TSX}$ and PCM OUT are placed in the high-impedance state within 300 ms.
Only receive on standby	FSR is low, FSX is high	30 mW	SIGR is placed in the high-impedance state within 300 ms.

PRINCIPLES OF OPERATION

fixed-data-rate timing

Fixed-data-rate timing is selected by connecting DCLKR to V_{BB}. It uses master clocks CLKX and CLKR, frame-synchronizer clocks FSX and FSR, and output $\overline{TSX}$. FSX and FSR are inputs that set the sampling frequency. Data is transmitted on PCM OUT on the first eight positive transitions of CLKX following the rising edge of FSX. Data is received on PCM IN on the first eight falling edges of CLKR following FSX. A digital-to-analog (D/A) conversion is performed on the received digital word and the resulting analog sample is held on an internal sample-and-hold capacitor until transferred to the receive filter.

variable-data-rate timing

Variable-data-rate timing is selected by connecting DCLKR to the bit clock for the receive PCM highway rather than to V_{BB}. It uses master clocks CLKX and CLKR, bit clocks DCLKX and DCLKR, and frame-synchronization clocks FSX and FSR.

Variable-data-rate timing allows for a flexible data frequency. The frequency of the bit clocks can be varied from 64 kHz to 4.096 MHz. The bit clocks must be asynchronous.

When the FSX/TSXE input is high, PCM data is transmitted from PCM OUT onto the highway on the next eight consecutive positive transitions of DCLKX. Similarly, while the FSR/TSRE input is high, the PCM word is received from the highway by PCM IN on the next eight consecutive negative transitions of DCLKR.

The transmitted PCM word will be repeated in all remaining time slots in the frame as long as DCLKX is pulsed and FSX is held high. This feature, which allows the PCM word to be transmitted to the PCM highway more than once per frame if desired, is available only with variable-data-rate timing. Signaling is allowed only in the fixed-data-rate mode because the variable-data-rate mode provides no means with which to specify a signaling frame.

asynchronous operation

In order to avoid crosstalk problems associated with special interrupt circuits, the design includes separate digital-to-analog converters and voltage references on the transmit and receive sides to allow completely independent operation of the two channels. In either timing mode, the master clock, data clock, and time-slot strobe must be synchronized at the beginning of each frame. Specifically, in the variable-rate mode, the falling edge of CLKX must occur within $t_{d(FSX)}$ ns after the rise of FSX and the falling edge of DCLKX must occur within t_{TSDX} ns after the rise of FSX. CLKX and DCLKX are synchronized once per frame but may be of different frequencies. The receive channel operates in a similar manner and is completely independent of the transmit timing (see Figure 6). This approach requires the provision of two separate master clocks but avoids the use of a synchronizer, which can cause intermittent data conversion errors.

precision voltage references

Voltage references that determine the gain and dynamic range characteristics of the device are generated internally. No external components are required to provide the voltage references. A difference in subsurface charge density between two suitably implanted MOS devices is used to derive a temperature- and bias-stable reference voltage, which are calibrated during the manufacturing process. Separate references are supplied to the transmit and receive sections, and each is calibrated independently. Each reference value is then further trimmed in the gain-setting operational amplifiers to a final precision value. Manufacturing tolerances of typically ±0.04 dB in absolute gain can be achieved for each half channel, providing the user a significant margin to compensate for error in other system components.

PRINCIPLES OF OPERATION

conversion laws

The TCM29C23 and TCM129C23 provide pin-selectable A-law or μ-law operation as specified by the CCITT G.711 recommendation. A-law operation is selected when ASEL is connected to V_{BB}. Signaling is not allowed during A-law operation. μ-law operation is selected by connecting ASEL to V_{CC} or GND.

transmit operation

transmit filter

The input section provides gain adjustment in the pass band by means of an on-chip uncommitted operational amplifier. The load impedance to ground (ANLG GND) at the amplifier output (GSX) must be greater than 10 kΩ in parallel with less than 50 pF. The input signal on ANLG IN+ can be either ac or dc coupled. The input operational amplifier can also be used in the inverting mode or differential amplifier mode.

A low-pass antialiasing section is included on the device. This section provides 35-dB attenuation at the sampling frequency. No external components are required to provide the necessary antialiasing function for the switched-capacitor section of the transmit filter.

encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample-and-hold capacitor. The encoder performs an analog-to-digital conversion on a switched-capacitor array. Digital data representing the sample is transmitted on the first eight data clock bits of the next frame.

The autozero circuit corrects for dc offset on the input signal to the encoder using the sign bit averaging technique. The sign bit from the encoder output is long-term averaged and subtracted from the input to the encoder. All dc offset is removed from the encoder input waveform.

receive operation

decoding

The serial PCM word is received at PCM IN on the first eight data clock bits of the frame. Digital-to-analog conversion is performed, and the corresponding analog sample is held on an internal sample-and-hold capacitor. This sample is transferred to the receive filter.

receive filter

The receive section of the filter provides pass-band flatness and stop-band rejection that fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin x)/x response of such decoders.

receive output power amplifiers

A balanced output amplifier is provided to allow maximum flexibility in output configuration. Either of the two outputs can be used single ended (i.e., referenced to ANLG GND) to drive single-ended loads. Alternatively, the differential output directly drives a bridged load. The output stage is capable of driving loads as low as 300 Ω single ended to a level of 12 dBm or 600 Ω differentially to a level of 15 dBm.

The receive channel transmission level may be adjusted between specified limits by manipulating of the GSR input. GSR is internally connected to an analog gain-setting network. When GSR is connected to PWRO+, the level is minimum. The output transmission level between 0 and –12 dB as GSR is adjusted (with an adjustable resistor) between PWRO+ and PWRO–.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions (i.e., when the digital input at PCM IN is the eight-code sequence specified in CCITT recommendation G.711).

APPLICATION INFORMATION

output gain-set design considerations (see Figure 7)

PWRO+ and PWRO– are low-impedance complementary outputs. The voltages at the nodes are:

V_{O+} at PWRO+
V_{O-} at PWRO–
$V_O = V_{O+} - V_{O-}$ (total differential response)

R1 and R2 are a gain-setting resistor network with the center tap to the GSR input.

A value greater than 10 kΩ and less than 100 kΩ for R1 + R2 is recommended because of the following:

The parallel combination of R1 + R2 and R_L sets the total loading.
The total capacitance at the GSR input and the parallel combination of R1 and R2 define a time constant that has to be minimized to avoid inaccuracies.

V_{AD} represents the maximum available digital milliwatt output response (V_A = 3.06 V rms).

$$V_{OD} = A \cdot V_{AD}$$

$$\text{where } A = \frac{1 + (R1/R2)}{4 + (R1/R2)}$$

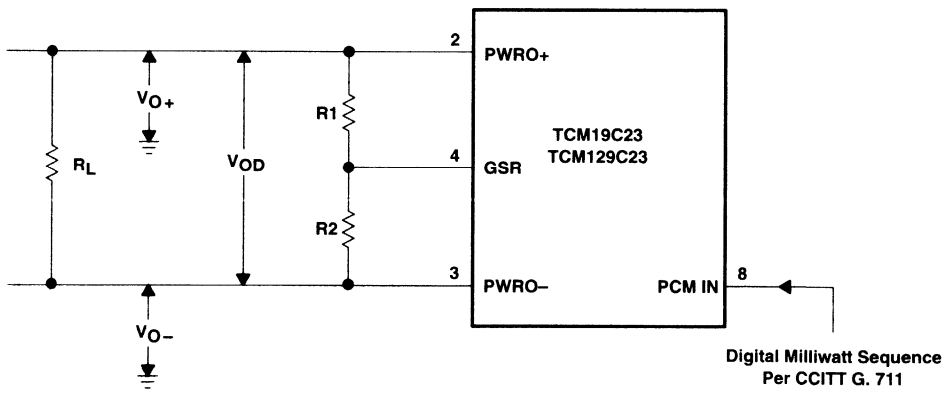


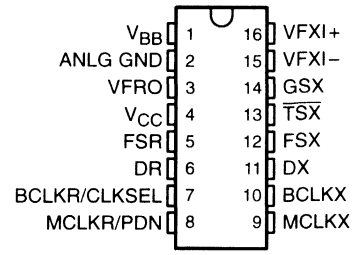
Figure 8. Gain-Setting Configuration

TCM320AC54
MONOLITHIC SERIAL INTERFACE COMBINED PCM CODEC AND FILTER

SCTS043A – NOVEMBER 1994 – REVISED JULY 1996

- **Complete PCM Codec and Filtering System Includes:**
  - **Transmit High-Pass and Low-Pass Filtering**
  - **Receive Low-Pass Filter With (sin x)/x Correction**
  - **Active RC Noise Filters**
  - **μ-Law Compatible Coder and Decoder**
  - **Internal Precision Voltage Reference**
  - **Serial I/O Interface**
  - **Internal Autozero Circuitry**
- **μ-Law Coding**
- **DTAD and DSP Interface Codec**
- **±5-V Operation**
- **Low Operating Power . . . 50 mW Typ**
- **Power-Down Standby Mode . . . 3 mW Typ**
- **Automatic Power Down**
- **TTL- or CMOS-Compatible Digital Interface**
- **Maximizes Line Interface Card Circuit Density**

DW OR N PACKAGE
(TOP VIEW)



description

The TCM320AC54 is comprised of a single-chip PCM codec (pulse-code-modulated encoder and decoder) and PCM line filter. This device provides all the functions required to interface a full-duplex (2-wire) voice telephone circuit with a TDM (time-division-multiplexed) system. Primary applications include:

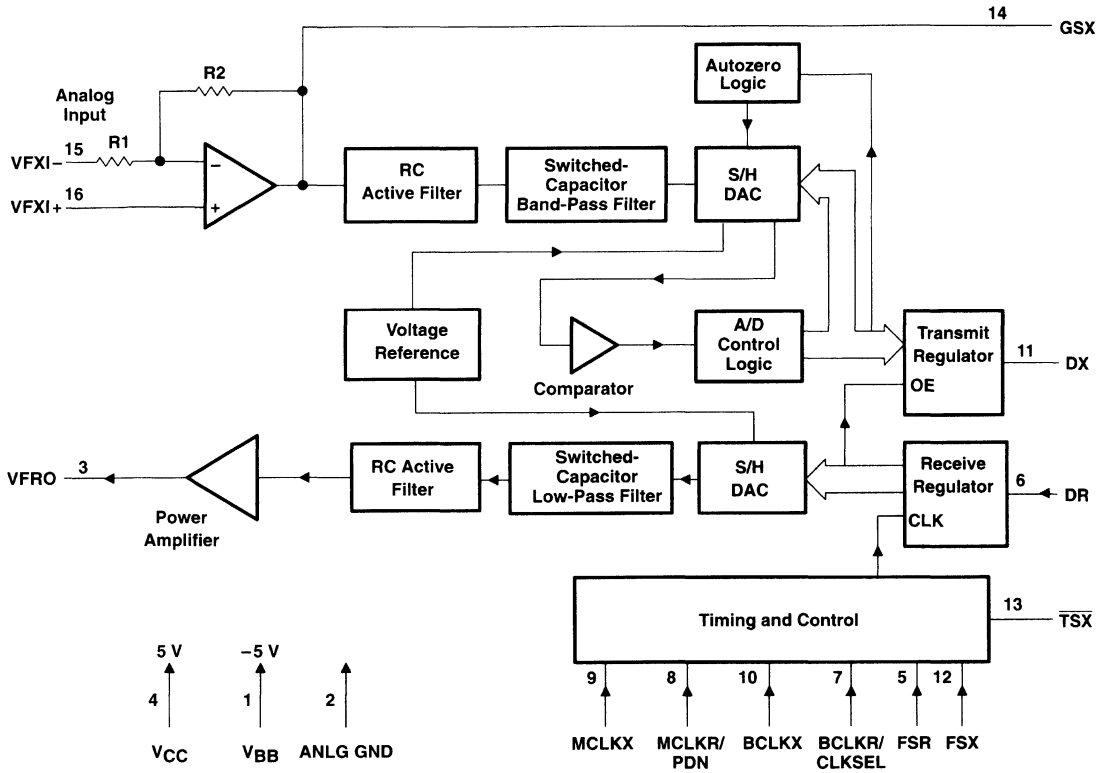
- Line interface for digital transmission and switching of T1 carrier, PABX, and central office telephone systems
- Subscriber line concentrators
- Digital-encryption systems
- Digital signal processing

The device is designed to perform the transmit encoding (A/D conversion) and receive decoding (D/A conversion) as well as the transmit and receive filtering functions in a PCM system. It is intended to be used at the analog termination of a PCM line or trunk. The device requires two transmit and receive master clocks that may be asynchronous (1.536 MHz, 1.544 MHz, or 2.048 MHz), transmit and receive data clocks that are synchronous with the master clock (but can vary from 64 kHz to 2.048 MHz), and transmit and receive frame-sync pulses. The TCM320AC54 provides the band-pass filtering of the analog signals prior to encoding and after decoding of voice and call progress tones.

The TCM320AC54 is characterized for operation from 0°C to 70°C.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the CMOS gates.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
ANLG GND	2	Analog ground. All signals are referenced to ANLG GND.
BCLKR/CLKSEL	7	Receive bit (data) clock/clock select terminal for master clock. BCLKR/CLKSEL shifts data into DR after the FSR leading edge and can vary from 64 kHz to 2.048 MHz. Alternately, BCLKR/CLKSEL can be a logic input that selects either 1.536 MHz/1.544 MHz or 2.048 MHz for the master clock in the synchronous mode. BCLKX is used for both transmit and receive directions (see Table 1).
BCLKX	10	Transmit bit (data) clock. BCLKX shifts out the PCM data on DX and can vary from 64 kHz to 2.048 MHz, but must be synchronous with MCLKX.
DR	6	Receive data input. PCM data is shifted into DR following the FSR leading edge.
DX	11	The 3-state PCM data output that is enabled by FSX
FSR	5	Frame sync clock input for receive channel. FSR is an 8-kHz pulse train that enables BCLKR to shift PCM data in DR (see Figures 1 and 2 for timing details).
FSX	12	Frame sync clock input for transmit channel. FSX is an 8-kHz pulse train that enables BCLKX to shift out the PCM data on DX (see Figures 1 and 2 for timing details).
GSX	14	Analog output of the transmit input amplifier. GSX is used to externally set gain.
$\overline{\text{MCLKR}}$/PDN	8	Receive master clock (must be 1.536 MHz, 1.544 MHz, or 2.048 MHz). $\overline{\text{MCLKR}}$/PDN may be synchronous with MCLKX but should be synchronous with MCLKX for best performance. When the input is continuously low, MCLKX is selected for all internal timing. When the input is continuously high, the device is powered down.
MCLKX	9	Transmit master clock (must be 1.536 MHz, 1.544 MHz, or 2.048 MHz). MCLKX may be asynchronous with MCLKR.
$\overline{\text{TSX}}$	13	Transmit time-slot strobe. $\overline{\text{TSX}}$ is an open-drain output that pulses low during the encoder time slot.
V_{BB}	1	Negative power supply. $V_{BB} = -5\ V \pm 10\%$
V_{CC}	4	Positive power supply. $V_{CC} = 5\ V \pm 10\%$
VFRO	3	Analog output of the receive filter
VFXI+	16	Noninverting input of the transmit input amplifier
VFXI–	15	Inverting input of the transmit input amplifier

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Supply voltage, V_{BB} (see Note 1) . . . . . −7 V
Voltage range at any analog input or output . . . . . V_{CC} +0.3 V to V_{BB} −0.3 V
Voltage range at any digital input or output . . . . . V_{CC} +0.3 V to ANLG GND −0.3 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions (see Note 2)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Supply voltage, V_{BB}	−4.5	−5	−5.5	V
High-level input voltage, V_{IH}	2.2			V
Low-level input voltage, V_{IL}			0.6	V
Common-mode input voltage range, V_{ICR}‡			±2.5	V
Load resistance, GSX, R_L	10			kΩ
Load capacitance, GSX, C_L			50	pF
Operating free-air temperature, T_A	0		70	°C

‡ Measured with CMRR > 60 dB.

NOTE 2: To avoid possible damage to these CMOS devices and resulting reliability problems, the power-up procedure described in the device power-up sequence paragraphs later in this document should be followed.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

supply current

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current from V_{CC}	Power down	No load		0.5	3	mA
		Active			6	11	
I_{BB}	Supply current from V_{BB}	Power down	No load		0.5	3	mA
		Active			6	11	

electrical characteristics at V_{CC} = 5 V ±5%, V_{BB} = −5 V ±5%, GND at 0 V, T_A = 25°C (unless otherwise noted)

digital interface

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	DX	I_H = −3.2 mA	2.4		V
V_{OL}	Low-level output voltage	DX	I_L = 3.2 mA		0.4	V
		$\overline{TSX}$	I_L = 3.2 mA, Drain open		0.4	
I_{IH}	High-level input current		$V_I = V_{IH}$ to V_{CC}		±15	µA
I_{IL}	Low-level input current	All digital inputs	V_I = GND to V_{IL}		±15	µA
V_{OL}	Output current in high-impedance state	DX	V_O = GND to V_{CC}		±15	µA

analog interface with transmit amplifier input

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_I	Input current	VFXI+ or VFXI−	V_I = −2.5 V to 2.5 V			±200	nA
r_i	Input resistance	VFXI+ or VFXI−	V_I = −2.5 V to 2.5 V	10			MΩ
r_o	Output resistance		Closed loop		1	3	Ω
	Output dynamic range	GSX	$R_L \geq$ 10 kΩ			±2.8	V
A_V	Open-loop voltage amplification	VFXI+ to GSX		5000			
B_I	Unity-gain bandwidth	GSX		1	2		MHz
V_{IO}	Input offset voltage	VFXI+ or VFXI−				±20	mV
CMRR	Common-mode rejection ratio			60			dB
K_{SVR}	Supply-voltage rejection ratio			60			dB

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.

analog interface with receive filter

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output resistance	VFRO			1	3	Ω
Load resistance		VFRO = ±2.5 V	600			Ω
Load capacitance	VFRO to GND				500	pF
Output dc offset voltage	VFRO to GND				±200	mV

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.

operating characteristics, V_{CC} = 5 V ±5%, V_{BB} = −5 V ±5%, GND at 0 V, V_I = 1.2276 V, f = 1.02 kHz, T_A = 0°C to 70°C, transmit input amplifier connected for unity gain, noninverting (unless otherwise noted)

timing requirements

			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$f_{clock(M)}$	Frequency of master clock (see Table 1)	MCLKX and MCLKR	Depends on BCLKX/CLKSEL		1.536 1.544 2.048		MHz
$f_{clock(B)}$	Frequency of bit clock, transmit	BCLKX		64		2.048	kHz
t_{w1}	Pulse duration, MCLKX and MCLKR high			160			ns
t_{w2}	Pulse duration, MCLKX and MCLKR low			160			ns
t_{r1}	Rise time of master clock	MCLKX and MCLKR	Measured from 20% to 80%			50	ns
t_{f1}	Fall time of master clock	MCLKX and MCLKR				50	ns
t_{r2}	Rise time of bit clock, transmit	BCLKX	Measured from 20% to 80%			50	ns
t_{f2}	Fall time of bit clock, transmit	BCLKX				50	ns
t_{su1}	Setup time, BCLKX high (and FSX in long-frame sync mode) before MCLKX↓		First bit clock after the leading edge of FSX	100			ns
t_{w3}	Pulse duration, BCLKX and BCLKR high		V_{IH} = 2.2 V	160			ns
t_{w4}	Pulse duration, BCLKX and BCLKR low		V_{IL} = 0.6 V	160			ns
t_{h1}	Hold time, frame sync low after bit clock low (long frame only)			0			ns
t_{h2}	Hold time, BCLKX high after frame sync↑ (short frame only)			0			ns
t_{su2}	Setup time, frame sync high before bit clock↓ (long frame only)			80			ns
t_{d1}	Delay time, BCLKX high to data valid		Load = 150 pF plus 2 LSTTL loads‡	0		140	ns
t_{d2}	Delay time, BCLKX high to $\overline{TSX}$ low		Load = 150 pF plus 2 LSTTL loads‡			140	ns
t_{d3}	Delay time, BCLKX (or 8 clock FSX in long frame only) low to data output disabled			50		165	ns
t_{d4}	Delay time, FSX or BCLKX high to data valid (long frame only)		C_L = 0 pF to 150 pF	20		165	ns
t_{su3}	Setup time, DR valid before BCLKR↓			50			ns
t_{h3}	Hold time, DR valid after BCLKR or BCLKX↓			50			ns
t_{su4}	Setup time, FSR or FSX high before BCLKR or BCLKR↓		Short-frame sync pulse (1 or 2 bit clock periods long) (see Note 3)	50			ns
t_{h4}	Hold time, FSX or FSR high after BCLKX or BCLKR↓		Short-frame sync pulse (1 or 2 bit clock periods long) (see Note 3)	100			ns
t_{h5}	Hold time, frame sync high after bit clock↓		Long-frame sync pulse (from 3 to 8 bit clock periods long)	100			ns
t_{w5}	Minimum pulse duration of the frame sync pulse (low level)		64-kbps operating mode	160			ns

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.
‡ Nominal input value for an-LSTTL load is 18 kΩ.
NOTE 3: For short-frame sync timing, FSR and FSX must go high while their respective bit clocks are high.

filter gains and tracking errors

PARAMETER	TEST CONDITIONS‡	MIN	TYP†	MAX	UNIT
Maximum peak transmit overload level	3.17 dBm0		2.501		V
Transmit filter gain, absolute (at 0 dBm0)	T_A = 25°C	−1.5		1.5	dB
Transmit filter gain, relative to absolute	f = 16 Hz			−35	dB
	f = 50 Hz			−25	
	f = 60 Hz			−21	
	f = 200 Hz	−2		0.5	
	f = 300 Hz to 3000 Hz	−0.5		0.5	
	f = 3300 Hz	−0.55		0.5	
	f = 3400 Hz	−1.5		1.5	
	f = 4000 Hz			−10	
	f ≥ 4600 Hz (measure response from 0 Hz to 4000 Hz)			−25	
Absolute transmit gain variation with temperature and supply voltage	Relative to absolute transmit gain	−0.1		0.1	dB
Transmit gain tracking error with level	Sinusoidal test method, Reference level = −10 dBm0				dB
	3 dBm0 ≥ input level ≥ −40 dBm0			±0.4	
	−40 dBm0 > input level ≥ −50 dBm0			±0.8	
Receive filter gain, absolute (at 0 dBm0)	Input is digital code sequence for 0 dBm0 signal, T_A = 25°C	−1.5		1.5	dB
Receive filter gain, relative to absolute	f = 0 Hz to 3000 Hz, T_A = 25°C	−0.5		0.5	dB
	f = 3300 Hz	−0.55		0.5	
	f = 3400 Hz	−1.5		1.5	
	f = 4000 Hz			−10	
Absolute receive gain variation with temperature and supply voltage		−0.1		0.1	dB
Receive gain tracking error with level	Sinusoidal test method; reference input PCM code corresponds to an ideally encoded −10 dBm0 signal				dB
	3 dBm0 ≥ input level ≥ −40 dBm0			±0.4	
	−40 dBm0 > input level ≥ −50 dBm0			±0.8	
Receive output drive voltage	R_L = 10 kΩ			±2.5	V

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.
‡ Absolute rms signal levels are defined as follows: V_I = 1.2276 V = 0 dBm0 = 4 dBm at f = 1.02 kHz with R_L = 600 Ω.

envelope delay distortion with frequency

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transmit delay, absolute (at 0 dBm0)	f = 1600 Hz		290	315	µs
Transmit delay, relative to absolute	f = 500 Hz to 600 Hz		195	220	µs
	f = 600 Hz to 800 Hz		120	145	
	f = 800 Hz to 1000 Hz		50	75	
	f = 1000 Hz to 1600 Hz		20	40	
	f = 1600 Hz to 2600 Hz		55	75	
	f = 2600 Hz to 2800 Hz		80	105	
	f = 2800 Hz to 3000 Hz		130	155	
Receive delay, absolute (at 0 dBm0)	f = 1600 Hz		180	200	µs
Receive delay, relative to absolute	f = 500 Hz to 1000 Hz	–40	–25		µs
	f = 1000 Hz to 1600 Hz	–30	–20		
	f = 1600 Hz to 2600 Hz		70	90	
	f = 2600 Hz to 2800 Hz		100	125	
	f = 2800 Hz to 3000 Hz		140	175	

noise

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit noise, C-message weighted	VFXI = 0 V		5	19	dBrnC0
Receive noise, C-message weighted	PCM code equals alternating positive and negative zero		2	10	dBrnC0
Noise, single frequency	VFXI+ = 0 V, f = 0 kHz to 100 kHz, Loop-around measurement			–53	dBm0

† All typical values are at V_{CC} = 5 V, V_{BB} = –5 V, and T_A = 25°C.

power-supply rejection

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Positive power-supply rejection, transmit	V_{CC} = 5 V + 100 mVrms, f = 0 kHz to 50 kHz	VFXI+ = –50 dBm0,	25		dBC‡
Negative power-supply rejection, transmit	V_{BB} = 5 V + 100 mVrms, f = 0 kHz to 50 kHz	VFXI+ = –50 dBm0,	25		dBC‡
Positive power-supply rejection, receive	PCM code equals positive zero, V_{CC} = 5 V + 100 mVrms	f = 0 Hz to 50 kHz	25		dBC‡
Negative supply-voltage rejection, receive	PCM code equals positive zero, V_{BB} = –5 V + 100 mVrms	f = 0 Hz to 50 kHz	25		dBC‡
Spurious out-of-band signals at the channel output (VFRO)	0 dBm0, 300-Hz to 3400-Hz input applied to DR (measure individual image signals at VFRO)			–25	dB
	f = 4600 Hz to 7600 Hz			–28	dB
	f = 7600 Hz to 100 Hz			–35	

‡ The unit dBC applies to C-message weighting.

distortion

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Signal-to-distortion ratio, transmit or receive half-channel‡	Level = 3 dBm0		28		dBC†
	Level = 0 dBm0 to −30 dBm0		30		
	Level = −40 dBm0	Transmit	25		
		Receive	25		
Single-frequency distortion products, transmit				−41	dB
Single-frequency distortion products, receive				−41	dB
Intermodulation distortion	Loop-around measurement, VFXI+ = −4 dBm0 to −21 dBm0, Two frequencies in the range of 300 Hz to 3400 Hz			−35	dB

† The unit dBC applies to C-message weighting.
‡ Sinusoidal test method. The TCM320A54 is measured using a C-message weighted filter.

crosstalk

PARAMETER	TEST CONDITIONS		MIN	TYP§	MAX	UNIT
Crosstalk, transmit-to-receive	f = 300 Hz to 3000 Hz,	DR at steady PCM code		−90	−75	dB
Crosstalk, receive-to-transmit (see Note 4)	VFXI = 0 V,	f = 300 Hz to 3000 Hz		−90	−75	dB

§ All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.
NOTE 4: Receive-to-transmit crosstalk is measured with a – 50-dBm0 activation signal applied at VFXI+.

PARAMETER MEASUREMENT INFORMATION

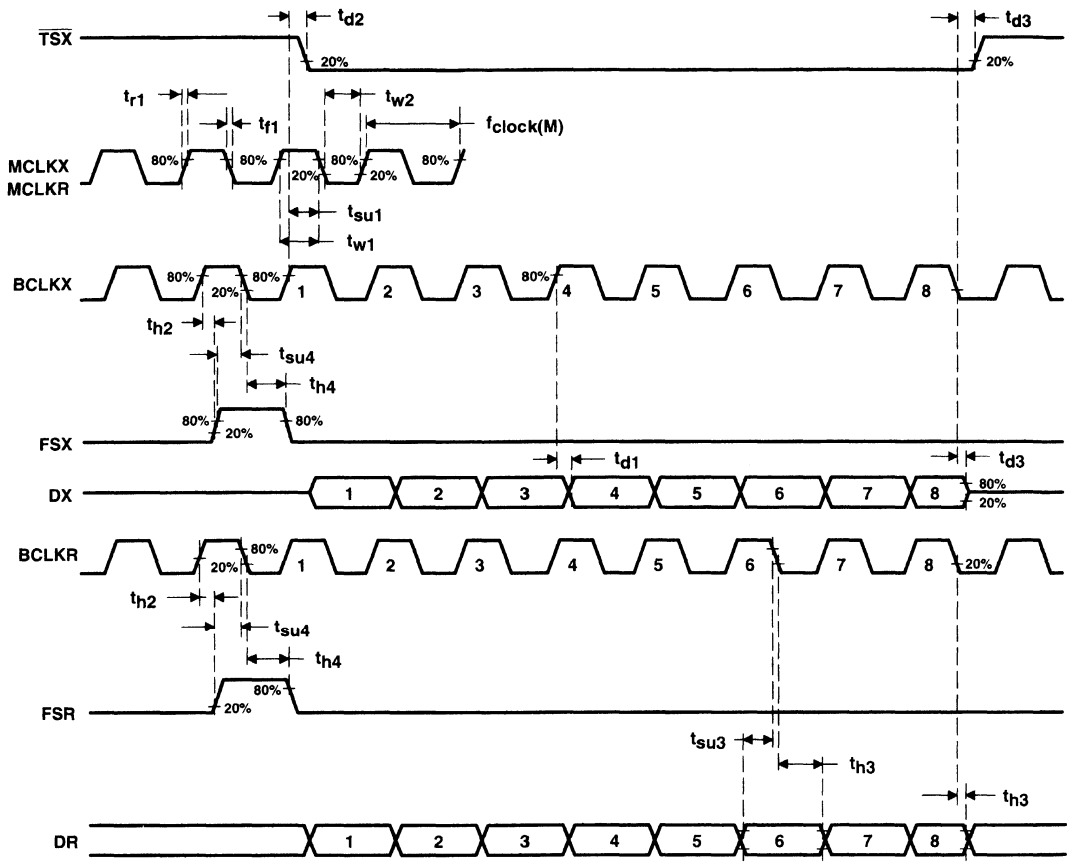


Figure 1. Short-Frame Sync Timing

PARAMETER MEASUREMENT INFORMATION

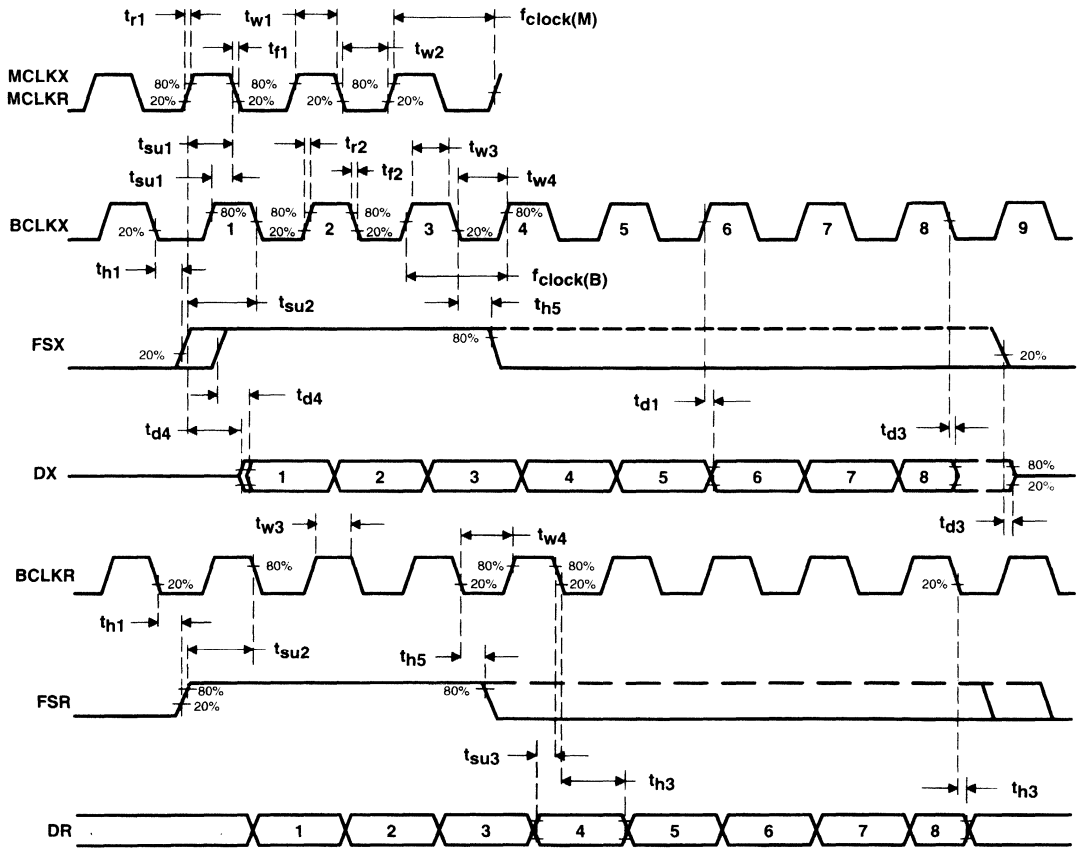


Figure 2. Long-Frame Sync Timing

PRINCIPLES OF OPERATION

system reliability and design considerations

TCM320AC54 system reliability and design considerations are described in the following paragraphs.

Latch-up is possible in all CMOS devices. It is caused by the firing of a parasitic SCR that is present due to the inherent nature of CMOS. When a latch-up occurs, the device draws excessive amounts of current and will continue to draw heavy current until power is removed. Latch-up can result in permanent damage to the device if supply current to the device is not limited.

Even though the TCM320AC54 is heavily protected against latch-up, it is still possible to cause latch-up under certain conditions in which excess current is forced into or out of one or more terminals. Latch-up can occur when the positive supply voltage drops momentarily below ground, when the negative supply voltage rises momentarily above ground, or possibly if a signal is applied to a terminal after power has been applied but before the ground is connected. This can happen if the device is hot-inserted into a card with the power applied, or if the device is mounted on a card that has an edge connector and the card is hot-inserted into a system with the power on.

To help ensure that latch-up does not occur, it is considered good design practice to connect a reverse-biased Schottky diode (with a forward voltage drop of less than or equal to 0.4 V – 1N5711 or equivalent) between the power supply and GND (see Figure 3). If it is possible that a TCM320AC54-equipped card that has an edge connector could be hot-inserted into a powered-up system, it is also important to ensure that the ground edge connector traces are longer than the power and signal traces so that the card ground is always the first to make contact.

device power-up sequence

Latch-up can also occur if a signal source is connected without the device being properly grounded. A signal applied to one terminal could then find a ground through another signal terminal on the device. To ensure proper operation of the device and as a safeguard against this sort of latch-up, it is recommended that the following power-up sequence always be used:

1. Ensure that no signals are applied to the device before the power-up sequence is complete.
2. Connect GND.
3. Apply V_{BB} (most negative voltage).
4. Apply V_{CC} (most positive voltage).
5. Force a power down condition in the device.
6. Connect clocks.
7. Release the power down condition.
8. Apply FS synchronization pulses.
9. Apply the signal inputs.

When powering down the device, this procedure should be followed in the reverse order.

PRINCIPLES OF OPERATION

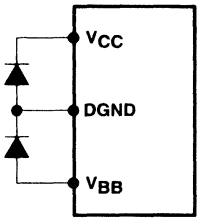


Figure 3. Latch-Up Protection Diode Connection

internal sequencing

Power-on reset circuitry initializes the TCM320AC54 when power is first applied, placing it into the power-down mode. DX and VFRO outputs go into high-impedance states and all nonessential circuitry is disabled. A low level or clock applied to MCLKR/PDN powers up the device and activates all circuits. DX, a 3-state PCM data output, remains in the high-impedance state until the arrival of the second FSX pulse.

synchronous operation

For synchronous operation, a clock is applied to MCLKX. MCLKR/PDN is used as a power-down control. A low level on MCLKR/PDN powers up the device and a high level powers it down. In either case, MCLKX is selected as the master clock for both receive and transmit direction. BCLKX must also have a bit clock applied to it. The selection of the proper internal divider for a master-clock frequency of 1.536 MHz, 1.544 MHz, or 2.048 MHz can be done via BCLKR/CLKSEL. The device automatically compensates for the 193rd clock pulse of each frame.

A fixed level on BCLKR/CLKSEL selects BCLKX as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation that can be selected depending on the state of BCLKR/CLKSEL. In the synchronous mode, BCLKX can be in the range from 64 kHz to 2.048 MHz but must be synchronous with MCLKX.

Table 1. Selection of Master-Clock Frequencies

BCLKR/CLKSEL	MASTER-CLOCK FREQUENCY SELECTED
Clock input	1.536 MHz or 1.544 MHz
Logic input L (sync mode only)	2.048 MHz
Logic input H (open) (sync mode only)	1.536 MHz or 1.544 MHz

The encoding cycle begins with each FSX pulse, and the PCM data from the previous cycle is shifted out of the enabled DX output on the rising edge of BCLKX. After eight bit-clock periods, the 3-state DX output is returned to the high-impedance state. With an FSR pulse, PCM data is latched via DR on the falling edge of BCLKX (or BCLKR, if running). FSX and FSR must be synchronous with MCLKX and MCLKR.

PRINCIPLES OF OPERATION

asynchronous operation

For asynchronous operation, separate transmit and receive clocks can be applied. MCLKX and MCLKR must be 1.536 MHz or 1.544 MHz and need not be synchronous. For best performance, however, MCLKR should be synchronous with MCLKX. This is easily achieved by applying only static logic levels to MCLKR/PDN. This connects MCLKX to all internal MCLKR functions. For 1.544-MHz operation, the device compensates for the 193rd clock pulse of each frame. Each encoding cycle is started with FSX and FSX must be synchronous with MCLKX and BCLKX. Each decoding cycle is started with FSR and FSR must be synchronous with BCLKR. The logic levels shown in Table 1 are not valid in the asynchronous mode. BCLKX and BCLKR can operate from 64 kHz to 2.048 MHz.

short-frame sync operation

The device can operate with either a short- or a long-frame sync pulse. On power up, the device automatically goes into the short-frame mode where both FSX and FSR must be one bit-clock period long with timing relationships specified in Figure 1. With FSX high during a falling edge of BCLKX, the next rising edge of BCLKX enables the 3-state output buffer, DX, which outputs the sign bit. The remaining seven bits are clocked out on the following seven rising edges and the next falling edge disables DX. With FSR high during a falling edge of BCLKR (BCLKX in synchronous mode), the next falling edge of BCLKR latches in the sign bit. The following seven falling edges latch in the seven remaining bits. The short-frame sync pulse can be utilized in either the synchronous or asynchronous mode.

long-frame sync operation

Both FSX and FSR must be three or more bit-clock periods long to use the long-frame sync mode with timing relationships as shown in Figure 2. Using the transmit frame sync (FSX), the device detects whether a short- or long-frame sync pulse is being used. For 64-kHz operation, the frame-sync pulse must be kept low for a minimum of 160 ns. The rising edge of FSX or BCLKX, whichever occurs later, enables the DX 3-state output buffer. The first bit clocked out is the sign bit. The next seven rising edges of BCLKX edges clock out the remaining seven bits. The falling edge of BCLKX following the eighth rising edge or FSX going low, whichever occurs later, disables DX. A rising edge on FSR, the receive-frame sync pulse, causes the PCM data at DR to be latched in on the next eight falling edges of BCLKR (BCLKX in synchronous mode). The long-frame sync pulse can be utilized in either the synchronous or asynchronous mode.

transmit section

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors. The low-noise and wide-bandwidth characteristics of this device provide gain in excess of 20 dB across the audio passband. The operational amplifier drives a unity-gain filter consisting of an RC active prefilter followed by an eighth-order switched-capacitor band-pass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. As per μ-law coding conventions, the ADC is a companding type. A precision voltage reference provides a nominal input overload of 2.5 V peak. The sampling of the filter output is controlled by the FSX frame-sync pulse. Then, the successive-approximation encoding cycle begins. The 8-bit code is loaded into a buffer and shifted out through DX at the next FSX pulse. The total encoding delay is approximately 290 μs. Any offset voltage due to the filters or comparator is cancelled by sign-bit integration.

PRINCIPLES OF OPERATION

receive section

The receive section consists of an expanding DAC that drives a fifth-order low-pass filter clocked at 256 kHz. The decoder and the fifth-order low-pass filter corrects for the (sin x)/x attenuation caused by the 8-kHz sample-and-hold circuit. The filter is followed by a second-order RC active post-filter/power amplifier capable of driving a 600-Ω load to a level of 7.2 dBm. The receive section is unity gain. At FSR, the data at DR is clocked in on the falling edge of the next eight BCLKR (BCLKX) periods. At the end of the decoder time slot, the decoding cycle begins and 10 μs later, the decoder DAC output is updated. The decoder delay is about 10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (1/2 frame), or a total of approximately 180 μs.

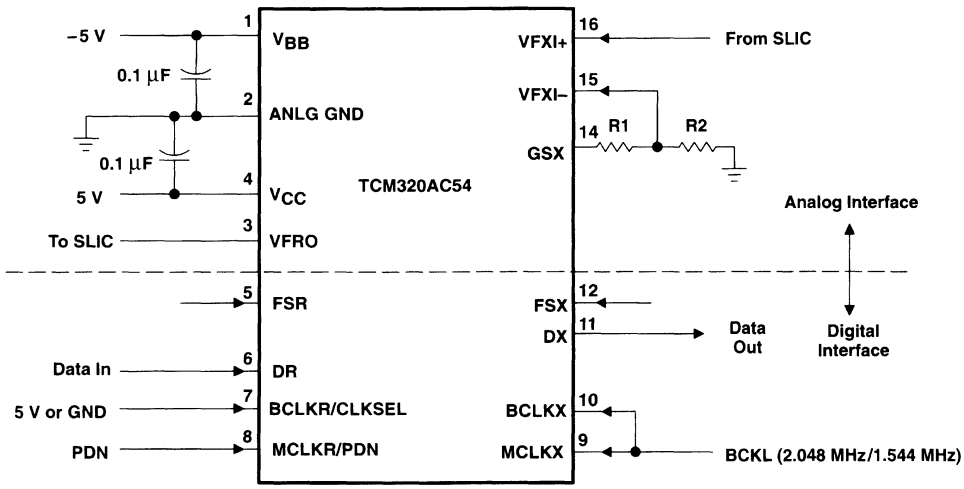
APPLICATION INFORMATION

power supplies

While the terminals of the TCM320AC54 are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications in which the printed-circuit board can be plugged into a hot socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to ANLG GND. This minimizes the interaction of ground return currents flowing through a common bus impedance. V_{CC} and V_{BB} supplies should be decoupled by connecting 0.1-µF decoupling capacitors to this common point. These bypass capacitors must be connected as close as possible to V_{CC} and V_{BB}.

For best performance, the ground point of each codec/filter on a card should be connected to a common card ground in star formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10-µF capacitors.



NOTE A: Transmit gain = 20 log $\left(\frac{R1 + R2}{R2}\right)$, $(R1 + R2) \geq 10\ k\Omega$

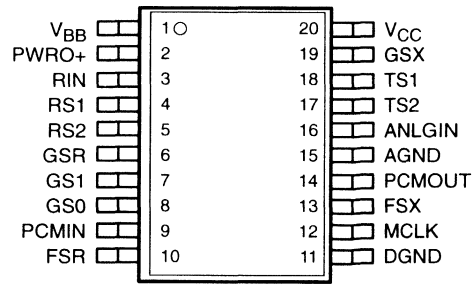
Figure 4. Typical Synchronous Application

TCM37C13, TCM37C14, TCM37C15
PCM COMBO WITH PROGRAMMABLE GAIN CONTROL

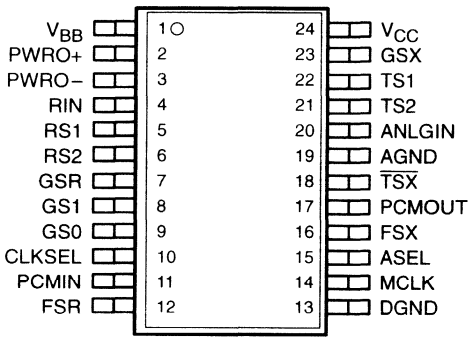
SLWS018 – JUNE 1996

- **Meets CCITT/(D3/D4) Channel Bank Recommendations for Input Signals Greater than –55 dBm0**
- **Programmable Transmit and Receive Gain Control with Pin-Selectable Gain/Attenuation Levels**
- **Includes Differential Output on the TCM37C14**
- **Precision Switched-Capacitor Filters and Converters**
- **Improved Version TCM29C13 Series COMBOs (CODEC and Filters)**
- **Low Power CMOS**
  - **Operating Mode . . . . 80 mW Typical**
  - **Power-Down Mode . . . 5 mW Typical**
- **Internal Sample-and-Hold and Autozero Functions**
- **Precision Internal Voltage References**
- **TCM37C14 Features Pin-Selectable μ-Law or A-Law Companding, TCM37C13 is μ-Law only, and TCM37C15 is A-Law Only.**
- **Pin-Selectable Master Clock Rate (1.536 MHz, 1.544 MHz, and 2.048 MHz Available) on the TCM37C14**

TCM37C13, TCM37C15 . . . DW OR N PACKAGE
(TOP VIEW)



TCM37C14 . . . DW PACKAGE
(TOP VIEW)



description

The TCM37C13, TCM37C14, and TCM37C15 devices are single-chip PCM combos (pulse-code-modulated CODECs with voice-band filtering). They are designed to perform transmit encoding (A/D conversion) and receive decoding (D/A conversion), as well as the transmit and receive filtering functions required to meet CCITT/(D3/D4) G.711 and G.714 specifications in a PCM system. Each device provides all the functions required to interface a full-duplex, 4-line voice telephone circuit with a TDM (time-division-multiplexed) system, and also perform the encoding and decoding of call progress tones. The TCM37C13, TCM37C14, and TCM37C15 are based on the proven TI TCM29C13 core, and have the added feature of programmable transmit and receive gain.

Primary applications include line interface for digital transmission and switching of T1 carrier (PABX [private branch automatic exchange] and central office telephone systems), subscriber line concentrators, digital encryption systems, and digital signal processing. They are intended to be used at the analog termination of a PCM line or trunk to the POTS (plain old telephone system) local-loop line.

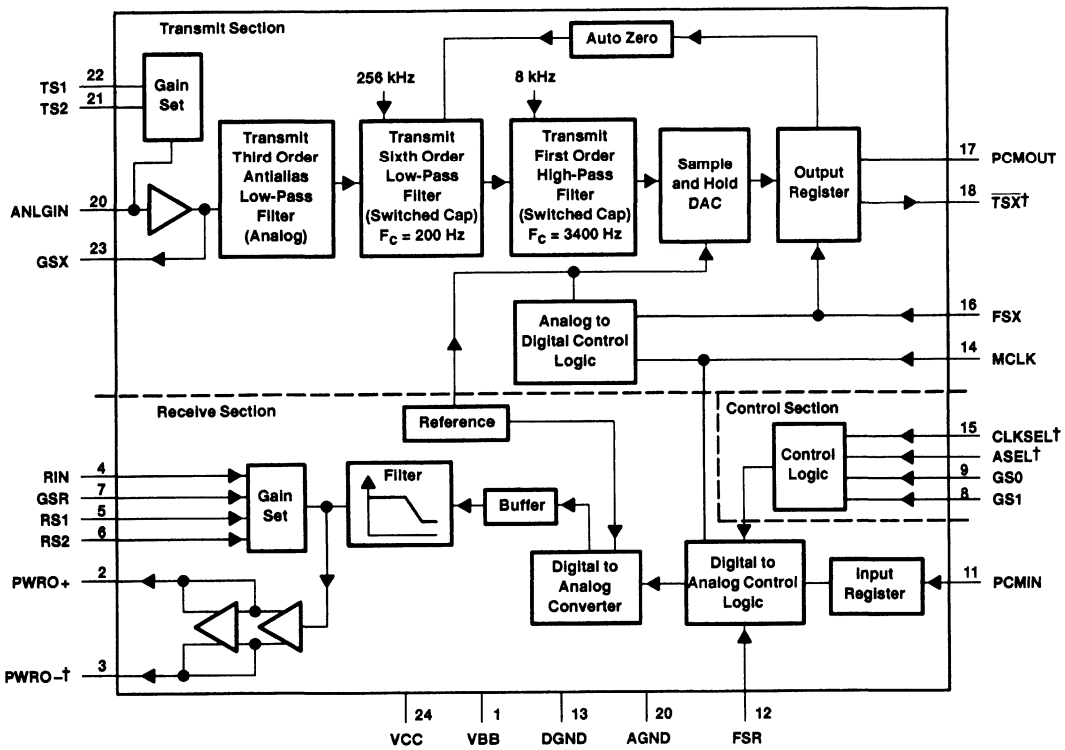
ADVANCE INFORMATION

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

description (continued)

The TCM37C13 and TCM37C15 are available in 20-pin DW SOIC (small-outline IC) or 20-pin N PDIP (plastic dual inline package) packages, and the TCM37C14 is available in a 24-pin DW SOIC package and includes differential output. All are characterized for operation from 0°C to 70°C.

functional block diagram



† TCM37C14 only.

NOTE A: Terminal numbers shown are for the TCM37C14.

ADVANCE INFORMATION

Terminal Functions

TERMINAL NAME	TERMINAL '37C13 '37C15	TERMINAL '37C14	I/O	DESCRIPTION
AGND	15	19		Analog ground return for all internal voice circuits. AGND is not connected internally to DGND.
ANLGIN	16	20	I	Analog input to transmit operational amplifier.
ASEL		15	I	Selection between A-law and μ-law operation. When ASEL is connected to V_{BB}, A-law is selected. When ASEL is connected to V_{CC} or ground, μ-law is selected.
CLKSEL		10	I	Clock frequency selection. Input must be connected to V_{BB}, V_{CC}, or ground to select the master clock frequency. When tied to V_{BB}, MCLK is 2.048 MHz. When tied to ground, MCLK is at 1.544 MHz. When tied to V_{CC}, MCLK is 1.536 MHz.
DGND	11	13		Digital ground for all internal logic circuits. DGND is not internally connected to AGND.
FSR	10	12	I	Frame synchronization clock input/time slot enable for receive channel. The receive channel enters the standby state when FSR is held low for 300 ms.
FSX	13	16	I	Frame synchronization clock input/time slot enable for transmit.
GS0	8	9	I	Input for first bit of the programmable gain control circuitry. This terminal works in combination with GS1 to simultaneously control transmit and receive gain, and controls power down instruction. See Table 1 and 2 for control logic information.
GS1	7	8	I	Input for second bit of the programmable gain control circuitry. This terminal works in combination with GS0 to simultaneously control transmit and receive gain, and controls power down instruction. See Table 1 and 2 for control logic information.
GSR	6	7	I	Input to gain-setting network of the output power amplifier. Gain is set by external resistors with three levels of programmable gain or attenuation control. See Figure 6 and Figure 7 for recommended configuration.
GSX	19	23	O	Output terminal of internal uncommitted operational amplifier. Internally, this is the voice signal input to the transmit filter.
MCLK	12	14	I	Master clock (input). For the TCM37C14, the master clock frequency can be either 2.048 MHz, 1.544 MHz, or 1.536 MHz, and is selected by the CLKSEL pin. MCLK for the TCM37C13 and the TCM37C15 is 2.048 MHz.
PCMIN	9	11	I	Receive PCM input. PCM data is clocked in on this pin on eight consecutive negative transitions of the receive data clock, (MCLK).
PCMOUT	14	17	O	Transmit PCM output. PCM data is clocked out on this output on eight consecutive positive transitions of the transmit data clock, (MCLK).
PWRO+	2	2	O	Noninverting output of power amplifier. PWRO+ can drive transformer hybrids or high-impedance loads directly in a differential or a single-ended configuration.
PWRO–		3	O	Inverting output of power amplifier. PWRO– is functionally identical with and complementary to PWRO+.
RIN	3	4	I	Input to receive section amplifiers. See Figure 6 and Figure 7 for recommended circuitry.
RS1	4	5		Terminal for first gain-control resistor on the receive section. Selected through closure of the first gain control switch. See Figure 6 and Figure 7 for recommended circuitry.
RS2	5	6		Terminal for second gain control resistor on the receive section. Selected through closure of the second gain control switch. See Figure 6 and Figure 7 for recommended configuration.
TS1	18	22		Terminal for gain-control resistor on input of transmit section. Selected through closure of the first gain-control switch. See Figure 6 and Figure 7 for recommended configuration.
TS2	17	21		Terminal for gain-control resistor on input of transmit section. Selected through closure of the second gain-control switch. See Figure 6 and Figure 7 for recommended configuration.
$\overline{TSX}$		18	O	Transmit channel time slot strobe for the transmit channel (active low).
V_{BB}	1	1		Most negative voltage supply voltage. Input is –5 V ± 5%.
V_{CC}	20	24		Most positive supply voltage. Input is 5 V ± 5%.

ADVANCE INFORMATION

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . −0.3 V to 15 V
Input voltage, V_I . . . . . −0.3 V to 15 V
Digital ground voltage . . . . . −0.3 V to 15 V
Continuous total dissipation at (or below) 25°C free-air temperature . . . . . 1375 mW
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to V_{BB}.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see Notes 2 and 3)		4.75	5	5.25	V
Supply voltage, V_{BB}		−4.75	−5	−5.25	V
DGND voltage with respect to AGND			0		V
High-level input voltage, V_{IH}		2.2			V
Low-level input voltage, V_{IL}				0.8	V
Load resistance, R_L	At GSX	10			kΩ
	At PWRO+ and/or PWRO−	300			Ω
Load capacitance, C_L	At GSX			50	pF
	At PWRO+ and/or PWRO−			100	
Operating free-air temperature, T_A		0		70	°C

NOTES: 2. To avoid possible damage to these CMOS devices and resulting reliability problems, the power-up procedure described in the device power-up sequence paragraphs later in this document should be followed.
3. Voltages at analog inputs and outputs, V_{CC} and V_{BB} terminals, are with respect to the AGND terminal. All other voltages are referenced to the DGND terminal unless otherwise noted.

ADVANCE INFORMATION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (outputs not loaded) (unless otherwise noted)

supply current

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current from V_{CC}	Operating			7	9	mA
		Standby	FSX or FSR at V_{IL} (after 300 ms)		0.5	1	
		Power-down	PDN = V_{IL} (after 300 ms)		0.3	0.9	
I_{BB}	Supply current from V_{BB}	Operating			−7	−9	mA
		Standby	FSX or FSR at V_{IL} (after 300 ms)		−0.5	−1	
		Power-down	PDN = V_{IL} (after 300 ms)		−0.3	−0.9	
	Power dissipation	Operating			70	90	mW
		Standby	FSX or FSR at V_{IL} (after 300 ms)		5	10	
		Power-down	PDN = V_{IL} (after 300 ms)		3	8	

digital interface

PARAMETER			TEST CONDITION	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	PCMOUT	I_{OH} = −9.6 mA	2.4			V
V_{OL}	Low-level output voltage at PCMOUT, $\overline{TSX}$		I_{OL} = 3.2 mA			0.4	V
I_{IH}	High-level input current, any digital input		V_I = 2.2 V to V_{CC}			10	μA
I_{IL}	Low-level input current, any digital input		V_I = 0 to 0.8 V			10	μA
C_i	Input capacitance				5	10	pF
C_o	Output capacitance				5		pF

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C

transmit amplifier input

PARAMETER	TEST CONDITION	MIN	TYP†	MAX	UNIT
Input current at ANLGIN	V_I = −2.17 V to 2.17 V			±100	nA
Input offset voltage at ANLGIN	V_I = −2.17 V to 2.17 V			±25	mV
Common-mode rejection at ANLGIN	V_I = −2.17 V to 2.17 V	55			dB
Open-loop voltage amplification at GSX		5000			
Open-loop unity-gain bandwidth at GSX			1		MHz
Input resistance at ANLGIN		10			MΩ

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C

receive filter output‡

PARAMETER	TEST CONDITION	MIN	TYP†	MAX	UNIT
Output offset voltage PWRO+, PWRO− (single-ended), Relative to AGND			80		mV
Output resistance at PWRO+, PWRO−			1		Ω

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C
‡ PWRO− on TCM37C14 only.

ADVANCE INFORMATION

ADVANCE INFORMATION

gain and dynamic range, V_{CC} = 5 V, V_{BB} = −5 V, T_A = 25°C (see Notes 4, 5, and 6) (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Encoder milliwatt response (transmit gain tolerance)		Signal input = 1.064 Vrms for μ-law Signal input = 1.068 Vrms for A-law		±0.04	±0.2	dBm0
Encoder milliwatt response (nominal supplies and temperature)		T_A = 0°C – 70°C, supplies = ±5%			±0.08	dB
Encoder milliwatt response (receive tolerance gain) relative to zero-transmission level point		Signal input per CCITT G.711, output signal = 1 kHz		±0.04	±0.2	dBm0
Digital milliwatt response variation with temperature and supplies		T_A = 0°C – 70°C, supplies = ±5%			±0.08	dB
Zero-transmission-level point, transmit channel (0 dBm0)	μ-law	R_L = 600 Ω		2.76		dBm
	A-law			2.79		
	μ-law	R_L = 900 Ω		1		
	A-law			1.03		
Zero-transmission-level point, receive channel (0 dBm0)	μ-law	R_L = 600		5.76		dBm
	A-law			5.79		
	μ-law	R_L = 900 Ω		4		
	A-law			4.03		

NOTES: 4. Unless otherwise noted, the analog input is a 0-dBm0, 1020-Hz sine wave, where 0 dBm0 is defined as the zero-reference point of the channel under test with unity gain set on the amplifier. This corresponds to an analog signal input of 1.064 Vrms, or an output of 1.503 Vrms.

5. The input amplifier is set for unity gain, noninverting. The digital input is a PCM bit stream generated by passing a 0-dBm0, 1020-Hz sine wave through an ideal encoder.

6. Receive output is measured single-ended with the output amplifier in the unity gain configuration. All output levels are (sin x)/x corrected.

gain tracking, reference level = −10 dBm0

PARAMETER	TEST CONDITION	MIN	MAX	UNIT
Transmit gain tracking error, sinusoidal input	3 > input level ≥ −40 dBm0		±0.25	dB
	−40 > input level ≥ −50dBm0		±0.5	
	−50 > input level ≥ −55 dBm0		±1.2	
Receive gain tracking error, sinusoidal input	3 > input level ≥ −40 dBm0		±0.25	dB
	−40 > input level		±0.5	
	−50 > input level ≥ −55 dBm0		±1.2	

noise

PARAMETER	TEST CONDITION	MIN	TYP†	MAX	UNIT
Transmit noise, C-message weighted	ANLGIN = AGND		1	7	dBrnC0
Transmit noise, psophometrically weighted	ANLGIN = AGND		−82	−80	dBm0p
Receive noise, C-message-weighted quiet code at PWRO+	PCMIN = 11111111 (μ-law), PCMIN = 10101010 (A-law)		2	5	dBrnC0
Receive noise, psophometrically weighted	PCM = lowest positive decode level			−81	dBm0p

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C

power supply rejection and crosstalk attenuation

PARAMETER		TEST CONDITION	MIN	TYP†	MAX	UNIT
V_{CC} supply voltage rejection ratio, transmit channel	0 < f < 30 kHz	Idle channel, supply signal = 200 mVpp, f measured at PCMOUT				dB
	30 < f < 50 kHz			–45		
V_{BB} supply voltage rejection ratio, transmit channel	0 < f < 30 kHz	Idle channel, supply signal = 200 mVpp, f measured at PCMOUT		–35		dB
	30 < f < 50 kHz	Idle channel,		–55		
V_{CC} supply voltage rejection ratio, receive channel (single-ended)	0 < f < 30 kHz	Idle channel, supply signal = 200 mVpp, narrow-band, f measured at PWRO+		–40		dB
	30 < f < 50 kHz			–45		
V_{BB} supply voltage rejection ratio, receive channel (single-ended)	0 < f < 30 kHz	Idle channel, supply signal = 200 mVpp, narrow-band, f measured at PWRO+		–40		dB
	30 < f < 50 kHz			–45		
Crosstalk attenuation, transmit-to-receive at PWRO+ (single-ended)		ANLGIN = 0 dBm0, f = 1.02 kHz, unity gain, PCMIN = lowest decode level	75			dB
Crosstalk attenuation, receive-to-transmit at PWRO+ (single-ended)		PCMIN = 0 dBm0, f = 1.02 kHz	75			dB

† All typical values are at V_{BB} = –5 V, V_{CC} = 5 V, and T_A = 25°C

distortion

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Transmit signal to distortion ratio, sinusoidal input (CCITT G.712 – Method 2)	0 > ANLGIN ≥ –30 dBm0	36			dB
	–30 > ANLGIN ≥ –40 dBm0	30			
	–40 > ANLGIN	25			
Receive signal to distortion ratio, sinusoidal input (CCITT G.712 – Method 2)	0 > ANLGIN ≥ –30 dBm0	36			dB
	–30 > ANLGIN ≥ –40 dBm0	30			
	–40 > ANLGIN ≥ –45 dBm0	25			
Transmit single-frequency distortion products	AT&T advisory #64 (3.8), Input signal = 0 dBm0			–46	dBm0
Receive single-frequency distortion products	AT&T advisory #64 (3.8), Input signal = 0 dBm0			–46	dBm0
Intermodulation distortion, end-to-end Spurious out-of-band signals, end-to-end	CCITT G.712 (7.1)			–35	dBm0
	CCITT G.712 (7.2)			–49	
	CCITT G.712 (6.1)			–25	
	CCITT G.712 (9)			–40	

ADVANCE INFORMATION

transmit filter transfer function (see Figure 1)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Transmit absolute delay time to PCMOUT	Fixed data rate, Input to ANLGIN 1.02 kHz at 0 dBm0	f_{MCLK} = 2.048 MHz,		245		µS
Transmit differential envelope delay time relative to transmit absolute delay time	f = 500 Hz to 600 Hz			170		µS
	f = 600 Hz to 1000 Hz			95		
	f = 1000 Hz to 2600 Hz			45		
	f = 2600 Hz to 2800 Hz			105		
Receive absolute delay time to PWRO+	Fixed data rate, Digital input is DMW codes	f_{MCLK} = 2.048 MHz,		190		µS
Receive differential envelope delay time relative to transmit absolute delay time	f = 500 Hz to 600 Hz			45		µS
	f = 600 Hz to 1000 Hz			35		
	f = 1000 Hz to 2600 Hz			85		
	f = 2600 Hz to 2800 Hz			110		
Gain (voltage amplification) relative to gain at 1.02 kHz	Input amplifier set for unity gain, noninverting maximum gain output, input signal at ANLGIN is 0 dBm0	16.67 Hz			−30	dB
		50 Hz			−25	
		60 Hz			−23	
		200 Hz	−1.8		−0.125	
		300 Hz to 3 kHz	−0.15		0.15	
		3.3 kHz	−0.35		0.15	
		3.4 kHz	−1		−0.1	
		4 kHz			−14	

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C

receive filter transfer function (see Figure 2)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain (voltage amplification) relative to gain at 1.02 kHz	Input signal at PCMIN is 0 dBm0	Below 3 kHz	−0.15	0.15	dB
		3.3 kHz	−0.35	0.15	
		3.4 kHz	−1	−0.1	
		4 kHz		−14	
		4.6 kHz and above		−30	

timing requirments

clock timing (see Figure 3)

		MIN	TYP	MAX	UNIT
$t_{c(MCLK)}$	Clock period for MCLK (2.048 MHz systems)	488			ns
t_r	Rise time for MCLK	5		30	ns
t_f	Fall time for MCLK	5		30	ns
$t_{w(MCLK)}$	Pulse duration for MCLK (see Note 7)	220			ns
	Clock duty cycle [$t_{w(CLK)}/t_{c(CLK)}$] for MCLK	45%	50%	55%	

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C
NOTE 7: FSX CLK and FSR CLK must be phase-locked with MCLK.

transmit timing (see Figure 3)

		MIN	MAX	UNIT
$t_{d(FSX)}$	Delay time (frame sync), FSR high or low before MCLK ↓	100	$t_{c(MCLK)}$ −100	ns

receive timing (see Figure 4)

PARAMETER		MIN	MAX	UNIT
$t_{d(FSR)}$	Delay time, frame sync high or low before MCLK ↓	100	$t_{c(MCLK)}$ –100	ns
$t_{su(PCMIN)}$	Setup time, PCMIN high before MCLK ↓	50		ns
$t_{h(PCMIN)}$	Hold time, after PCMIN ↓	60		ns

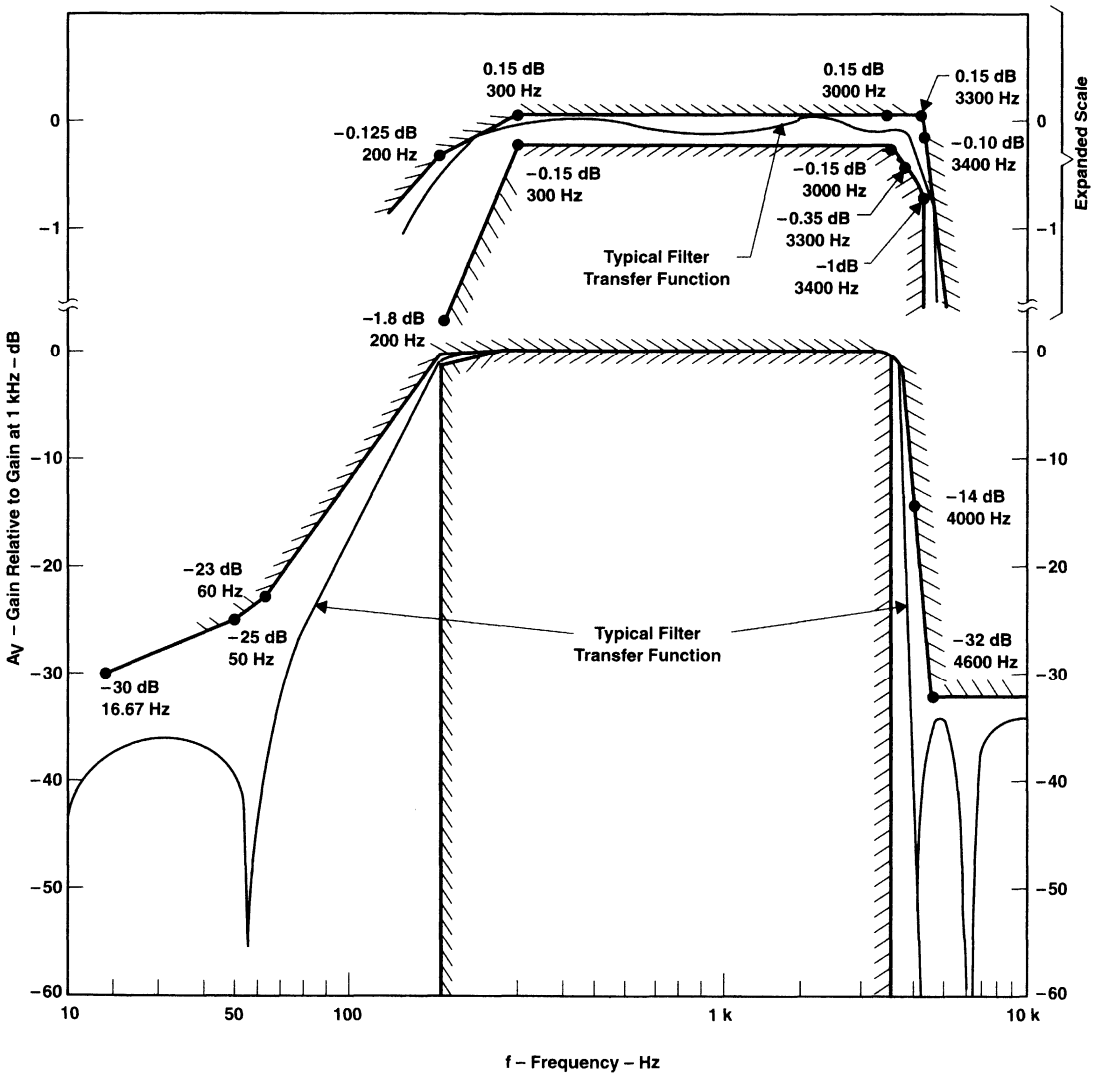
switching characteristics

propagation delay times (see Figure 3 and 4)

PARAMETER		TEST CONDITION	MIN	MAX	UNIT
t_{pd1}	Propagation delay times, MCLK ↑ to bit 1 data valid at PCMOUT (data enable time on time slot entry) (see Note 8)	CL = 0 pF to 100 pF	0	145	ns
t_{pd2}	Propagation delay times, MCLK ↑ bit n to bit n data valid at PCMOUT (data valid time)	CL = 0 pF to 100 pF	0	145	ns
t_{pd3}	Propagation delay times, MCLK ↓ low bit 8 to bit 8 Hi-Z at PCMOUT (data float time on time slot exit) (see Note 8)	CL = 0 pF	60	215	ns
t_{pd4}	Propagation delay times, MCLK ↑ bit 1 to $\overline{TSX}$ active (low) (time slot enable time)	CL = 0 pF to 100 pF	0	145	ns
t_{pd5}	Propagation delay times, MCLK ↓ to bit 8 to $\overline{TSX}$ inactive (high) (timeslot disable time) (see Note 8)	CL = 0 pF	60	190	ns

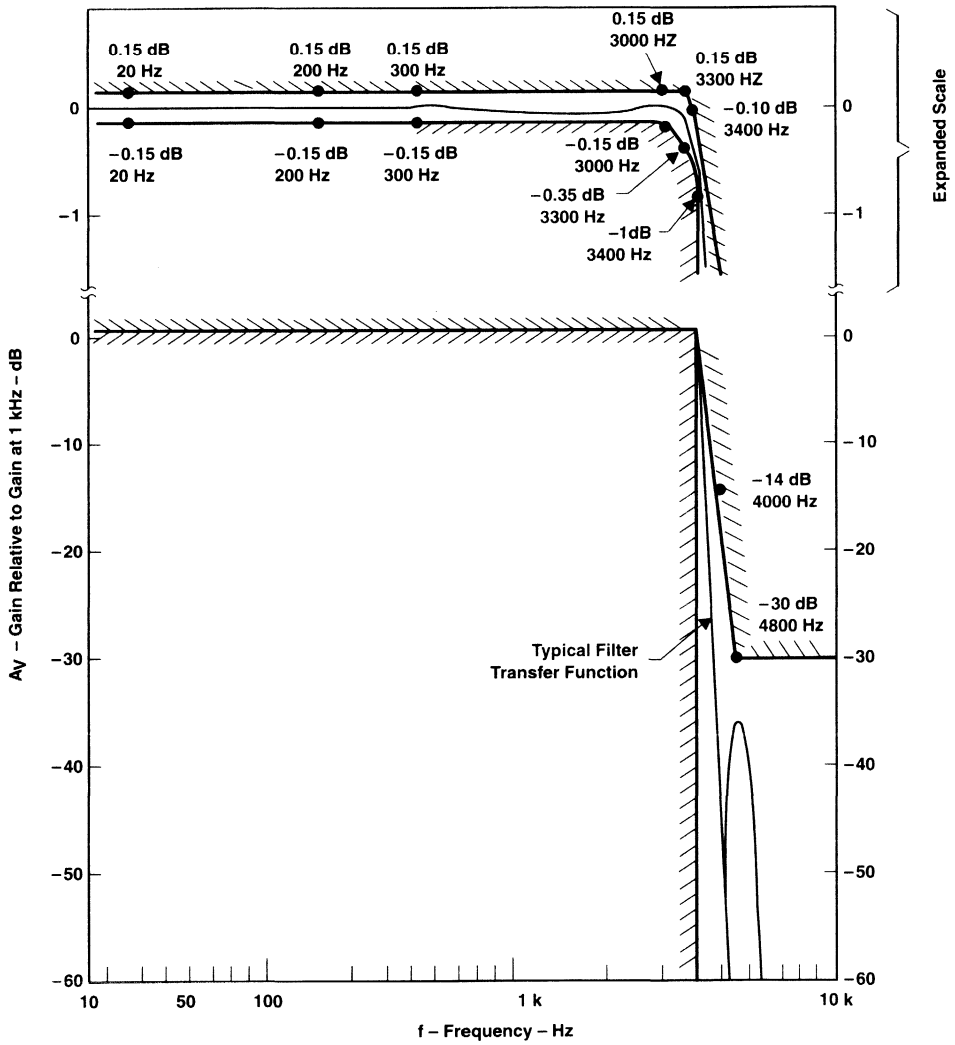
NOTE 8: Timing parameters t_{pd1}, t_{pd3}, and t_{pd5} are referenced to the high-impedance state.

ADVANCE INFORMATION



NOTE A: For this figure, gain (voltage amplification) is defined as gain relative to gain at 1 kHz in dB.

Figure 1. Transmit Filter Transfer Characteristics



NOTE A: For this figure, gain (voltage amplification) is defined as gain relative to gain at 1 kHz in dB.

Figure 2. Receive Filter Transfer Characteristics

ADVANCE INFORMATION

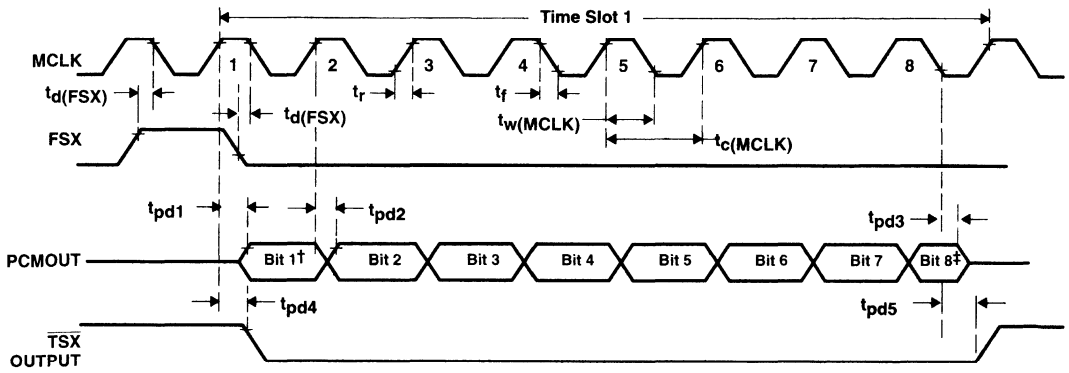
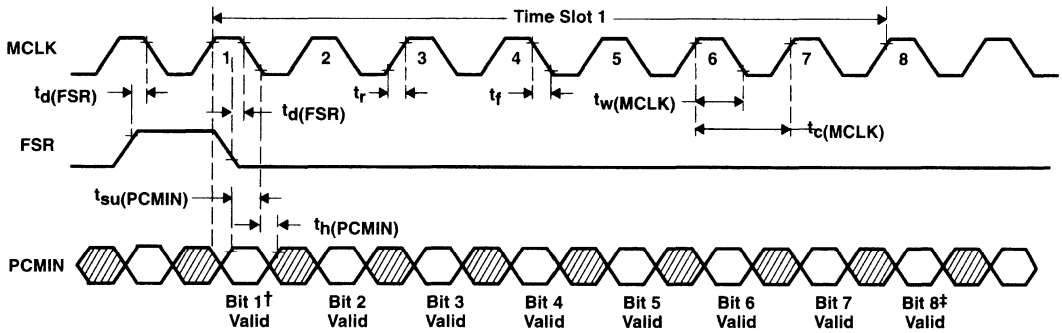


Figure 3. Transmit Timing



† Bit 1 = MSB = most significant bit (sign bit) and is clocked in first on the PCMIN pin or clocked out first on the PCMOUT terminal.
‡ BIT 8 = LSB = least significant bit and is clocked in last on the PCMIN or is clocked out last on the PCMOUT terminal.
NOTE A: Inputs are driven from 0.45 V to 2.4 V. Time intervals are referenced to 2 V when the high level is indicated and 0.8 V when the low level is indicated.

Figure 4. Receive Timing

ADVANCE INFORMATION

PRINCIPLES OF OPERATION

system reliability and design considerations

General TCM37C13, TCM37C14, and TCM37C15 system reliability and design considerations are described in the following paragraphs.

latch-up

Latch-up is possible in all CMOS devices. It is caused by the firing of a parasitic SCR that is present due to the inherent nature of CMOS. When a latch-up occurs, the device draws excessive amounts of current and will continue to draw heavy current until power is removed. Latch-up can result in permanent damage to the device if supply current to the device is not limited.

Even though the TCM37C13, '14, and '15 are heavily protected against latch-up, it is still possible to cause latch-up under certain conditions in which excess current is forced into or out of one or more terminals.Latch-up can occur when the positive supply voltage drops momentarily below ground, when the negative supply voltage rises momentarily above ground, or possibly if a signal is applied to a terminal after power has been applied but before the ground is connected. This can happen if the device is hot-inserted into a card with the power applied, or if the device is mounted on a card that has an edge connector, and the card is hot-inserted into a system with the power on.

To help ensure that latch-up does not occur, it is considered good design practice to connect a reverse-biased Schottky diode (with a forward voltage drop of less than or equal to 0.4 V — 1N5711 or equivalent), between each power supply and GND (see Figure 5). If it is possible that a TCM37C13-, '14-, or '15-equipped card that has an edge connector could be hot-inserted into a powered-up system, it is also important to ensure that the ground edge connector traces are longer than the power and signal traces so that the card ground is always the first to make contact.

device power-up sequence

Latch-up can also occur if a signal source is connected without the device being properly grounded. A signal applied to one terminal could then find a ground through another signal terminal on the device. To ensure proper operation of the device and as a safeguard against this sort of latch-up, it is recommended that the following power-up sequence always be used:

1. Ensure no signals are applied to the device before the power-up sequence is complete.
2. Connect GND.
3. Apply V_{BB} (most negative voltage).
4. Apply V_{CC} (most positive voltage).
5. Force a power down condition in the device.
6. Connect the master clock.
7. Release the power-down condition.
8. Apply FSX and/or FXR synchronization pulses.
9. Apply signal inputs.

When powering down the device, this procedure should be followed in the reverse order.

ADVANCE INFORMATION

PRINCIPLES OF OPERATION

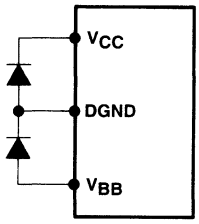


Figure 5. Latch-Up Protection Diode Connection

internal sequencing

On the transmit channel, digital outputs PCMOUT and $\overline{\text{TSX}}$† are held in the high-impedance state for approximately four frames (500 µs) after power up or application of V_{BB} or V_{CC}. After this delay, PCMOUT and $\overline{\text{TSX}}$† are functional and occur in the proper timeslot. The analog circuits on the transmit side require approximately 60 ms to reach their equilibrium value due to the autozero circuit settling time. Thus, valid digital information, such as for on/off hook detection, is available almost immediately, while analog information is available after some delay.

To further enhance system reliability, PCMOUT and $\overline{\text{TSX}}$† are placed in a high-impedance state approximately 20 µs after an interruption of MCLK. This interruption could possibly occur with some kind of fault condition elsewhere in the system.

† TCM37C14 only.

ADVANCE INFORMATION

PRINCIPLES OF OPERATION

miscellaneous functions

Miscellaneous functions of the TCM37C13, TCM37C14, and TCM37C15 are described in the following paragraphs.

gain/attenuation control

On-chip logic is included on the TCM37C13, '14, and '15 to control the channel gain or attenuation, and power-down functions with minimum terminal allocation. The operational amplifiers in the receive and transmit sections can be configured to either attenuate or amplify the signal depending on how external resistors are connected to the device.

Two control input terminals (GS0 and GS1) select one of three levels of gain or attenuation in the transmit and receive path, and power-down. Note that the gain for both the transmit and receive sides are set together and that the device enters the power-down mode when both GS0 and GS1 are held low

gain adjustment

If gain is used on the receive side, the input PCM data levels must be properly limited to prevent saturation of the output amplifier. Refer to the gain and dynamic range table in the electrical characteristics section of this document.

The gain of the transmit and receive amplifiers is set by external resistors connected to the device as shown in Figure 6 and can be adjusted using internal switching elements as shown in Table 1.

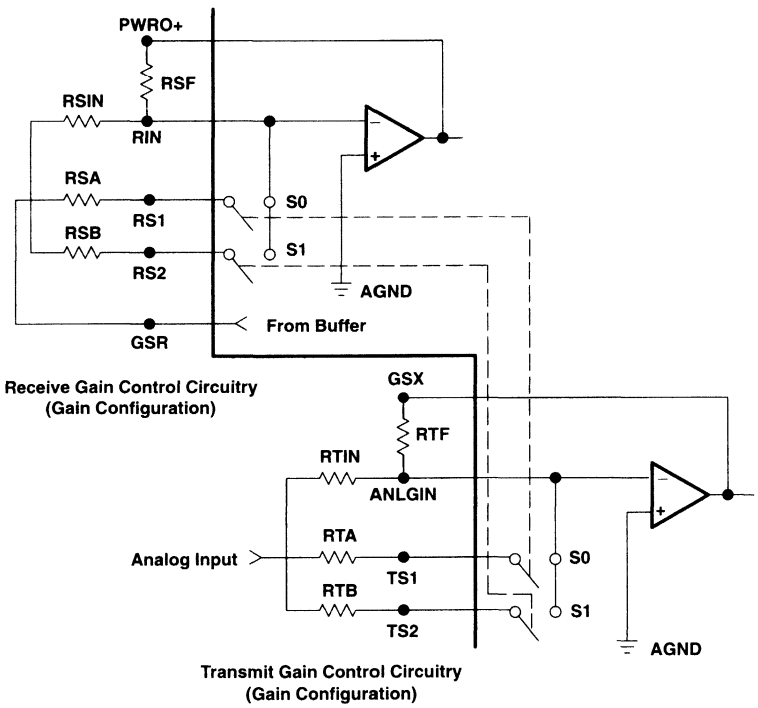


Figure 6. Gain Control Circuitry

ADVANCE INFORMATION

PRINCIPLES OF OPERATION

Table 1. Logic Table for Programmable Gain Control

CONTROL TERMINALS		INTERNAL SWITCH POSITION				TRANSFER FUNCTION (GAIN)	
GS0	GS1	TS1	TS2	RS1	RS2	RECEIVE	TRANSMIT
LOW	LOW	POWER DOWN					
LOW	HI	OPEN	OPEN	OPEN	OPEN	– RSF/RSIN	– RTF/RTIN
HI	LOW	CLOSED	OPEN	CLOSED	OPEN	– RSF/RSIN ‖ RSA	– RTF/RTIN ‖ RTA
HI	HI	OPEN	CLOSED	OPEN	CLOSED	– RSF/RSIN ‖ RSB	– RTF/RTIN ‖ RTB

attenuation adjust

The attenuation of the transmit and receive amplifiers is set by external resistors connected to the device as shown in Figure 7 and can be adjusted using internal switching elements as shown in Table 2.

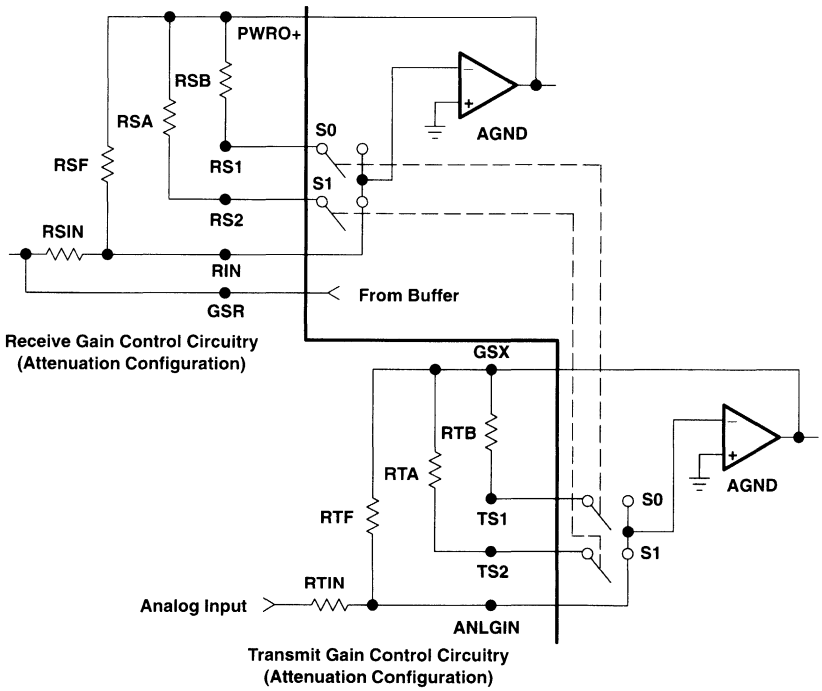


Figure 7. Attenuation Control Circuitry

PRINCIPLES OF OPERATION

Table 2. Logic Table for Programmable Attenuation Control

CONTROL TERMINALS		INTERNAL SWITCH POSITION				TRANSFER FUNCTION (ATTENUATION)	
GS0	GS1	TS1	TS2	RS1	RS2	RECEIVE	TRANSMIT
LOW	LOW	POWER DOWN					
LOW	HI	OPEN	OPEN	OPEN	OPEN	–RSF/RSIN	–RTF/RTIN
HI	LOW	CLOSED	OPEN	CLOSED	OPEN	– RSF ‖ RSB/RSIN	– RTF ‖ RTB/RTIN
HI	HI	OPEN	CLOSED	OPEN	CLOSED	– RSF ‖ RSA/RSIN	– RTF ‖ RTA/RTIN

power-down and standby operations

To minimize power consumption, a power-down mode and three standby modes are provided. For power-down, low signals are applied to terminals GS0 and GS1. It is not sufficient to remove the high signal from GS0 and GS1. In the absence of a signal, the pins float to high and the device remains active. In the power-down mode, the average power consumption is reduced to an average of 5 mW.

The standby modes give the options of placing the entire device on standby, placing only the transmit channel on standby, or placing only the receive channel on standby. To place the entire device on standby, both FSX and FSR are held low. For transmit-only operation, FSX is high and FSR is held low. For receive-only operation, FSR is high and FSX is low. See Table 3 for power-down and standby procedures.

Table 3. Power-Down And Standby Procedures

DEVICE STATUS	PROCEDURE	TYPICAL POWER CONSUMPTION	DIGITAL OUTPUT STATUS
Power down	GS0 and GS1 are low	3 mW	$\overline{TSX}$ and PCMOUT are in a high-impedance state
Entire device on standby	FSX and FSR are low	3 mW	$\overline{TSX}$ and PCMOUT are in a high-impedance state
Only transmit on standby	FSX is low FSR is high	40 mW	$\overline{TSX}$ and PCMOUT are placed in a high-impedance state within 300 ms.
Only receive on standby	FSR is low FSX is high	30 mW	

fixed-data-rate timing

Fixed-data-rate timing uses master clock MCLK, frame synchronizer clocks FSX and FSR, and outputs $\overline{TSX}$ (TCM37C14 only). An 8-kHz clock signal should be applied to the FSX and FSR inputs to set the sampling frequency. Data is transmitted on the PCMOUT terminal on the first eight positive transitions of MCLK following the rising edge of FSX. Data is received on the PCMIN terminal on the first eight falling edges of MCLK following FSR. A D/A conversion is performed on the received digital word and the resulting analog sample voltage is held on an internal sample-and-hold capacitor until transferred to the receive filter.

The TCM37C14 operates with MCLK frequencies of 1.536 MHz, 1.544 MHz, or 2.048 MHz, while the TCM37C13 and TCM37C15 operate at 2.048 MHz.

precision voltage references

Voltage references that determine the gain and dynamic range characteristics of the device are generated internally and require no external components to operate. A difference in subsurface charge density between two suitably implanted MOS devices is used to derive a temperature- and bias-stable reference voltage. These references are calibrated during the manufacturing process. Separate references are supplied to the transmit and receive sections, and each is calibrated independently. Each reference value is then further trimmed by the gain-setting operational amplifiers to a final precision value. Manufacturing tolerances of typically ± 0.04 dB in absolute gain for each half channel can be achieved, providing a significant margin to compensate for error in other board components.

PRINCIPLES OF OPERATION

conversion laws

The TCM37C14 provides pin-selectable μ-law or A-law operation as specified by the CCITT G.711 recommendation. A-law operation is selected when the ASEL terminal is connected to V_{BB} and μ-law operation is selected when the ASEL terminal is connected to V_{CC} or to GND.

The TCM37C13 provides μ-law operation only, and the TCM37C15 provides A-law operation only.

transmit operation

The transmit operation is described in the following paragraphs.

transmit filter

The input section provides gain adjustment in the passband by means of an on-chip uncommitted operational amplifier. The load impedance to ground (AGND) at the amplifier output must be greater than 10 kΩ in parallel with less than 50 pF.

A low-pass antialiasing section is included on the device. This section provides 35-dB attenuation at the sampling frequency. No external components are required to provide the necessary antialiasing function for the switched capacitor section of the transmit filter.

The band–pass section provides passband flatness and stopband attenuation that fulfills the AT&T D3/D4 channel bank transmission specification and CCITT recommendation G.712. Device specifications meet or exceed digital class-5 central office switching systems requirements for input signals greater than –55 dBm0.

A high-pass section configuration was chosen to reject low-frequency noise from 50- and 60-Hz power lines, 17-Hz European electric railroads, ringing frequencies and their harmonics, and other low-frequency noise. Even with the high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200 Hz. This feature allows the use of low-cost transformer hybrids without external components to be used in systems.

encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample-and-hold capacitor. The encoder performs an A/D conversion on a switched-capacitor array. Digital data representing the sample is then transmitted on the first eight data clocks bits of the next frame.

The autozero circuit corrects for dc offset on the input signal to the encoder, using the sign bit averaging technique. The sign bit from the encoder output is long-term averaged and subtracted from the input to the encoder, removing all dc offset from the encoder input waveform.

receive operation

The receive operation is described in the following paragraphs.

decoding

The serial PCM word is received at the PCMIN terminal on the first eight data clock bits of the frame. D/A conversion is performed and the corresponding analog sample is held on an internal sample-and-hold capacitor. The sample voltage is then transferred to the receive filter.

receive filter

The receive filter provides passband flatness and stopband rejection that fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin x)/x response of such decoders.

PRINCIPLES OF OPERATION

receive output power amplifiers

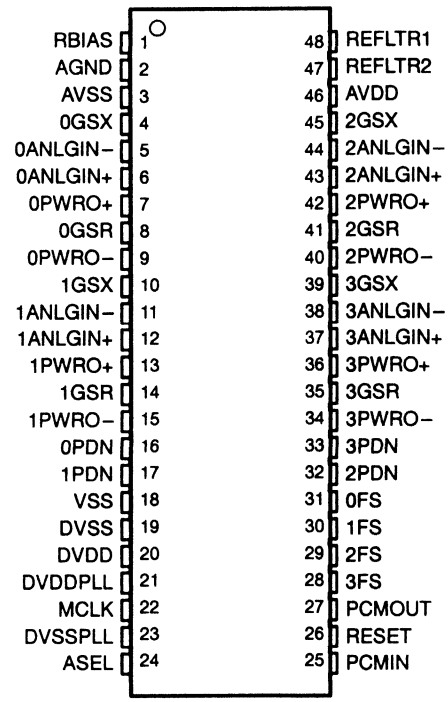
A balanced-output amplifier is provided to allow maximum flexibility in output configuration. Either of the two outputs can be used to drive single-ended loads (i.e. referenced to AGND) . Alternatively, the differential output can directly drive a bridged load. The output stage is capable of driving resistive loads as low as 300 Ω to a single-ended level of 12 dBm, or as low as 600 Ω in the differential mode to a level of 15 dBm.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions (i.e. when the digital input at PCMIN is the 8-code sequence specified in CCITT recommendation G.711).

SLWS040 – JUNE 1996

- **Single 5-V Supply**
- **Replaces Four TCM29C13 Combos (CODEC and Filters)**
- **Reliable Submicron Silicon-Gate CMOS Technology**
- **Low Power Consumption (per Channel)**
  - **Operating Mode . . . 40 mW Typical**
  - **Power-Down Mode . . . 1 mW Typical**
- **Meets CCITT/(D3/D4) G.711 and G.714 Channel Bank Specifications**
- **Differential Signal Processing Architecture for Low Idle-Channel Noise and Good Power Supply Rejection**
- **Single PCM I/O for Simplified PCM Interface**
- **Advanced Switched-Capacitor Filters and Sigma-Delta A/D and D/A Converter Technology**

DGG PACKAGE
(TOP VIEW)



description

The TCM38C17 QCombo is a 4-channel single-chip PCM combo (pulse-code-modulated CODEC with voice-band filtering) device. It performs the transmit encoding (A/D conversion) and receive decoding (D/A conversion), as well as the transmit and receive filtering functions required to meet CCITT G.711 and G.714 specifications in a PCM system. Each channel provides all the functions required to interface a full-duplex, 4-line voice telephone circuit with a TDM (time-division-multiplexed) system. The TCM38C17 is specifically designed for fixed-data-rate applications and is intended to replace four TCM29C13 devices.

Primary applications include digital transmission and switching of T1 carrier PABX (private automatic branch exchange) and central office telephone systems and subscriber line concentrators. The device serves as the analog termination of a PCM line or trunk to the POTS (plain old telephone system) local-loop line.

Other applications include any PCM digital-audio interface such as voice-band data storage systems and many digital signal processing applications that can benefit from the reduced footprint of a quad codec configuration and single-rail operation. Dynamic range and excellent idle-channel noise performance are maintained using the TI advanced 4Vt process technologies.

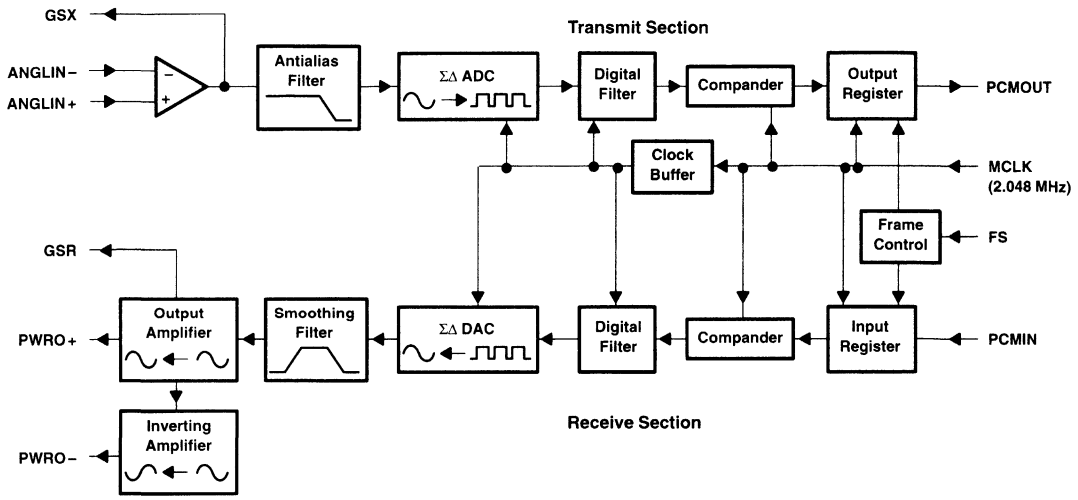
The TCM38C17 is available in a 48-pin plastic DGG TSSOP (thin shrink small-outline package) and is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TI and QCombo are registered trademarks of Texas Instruments, Inc.

functional block diagram



NOTE A: One of four identical channels is depicted.

PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	2		Analog ground (mid supply). An external decoupling capacitor (0.1 μF) should be connected from AGND to AVSS for filtering purposes.
0ANLGIN+	6	I	Noninverting analog input to uncommitted transmit operational amplifier for channel 0.
0ANLGIN–	5	I	Inverting analog input to uncommitted transmit operational amplifier for channel 0.
1ANLGIN+	12	I	Noninverting analog input to uncommitted transmit operational amplifier for channel 1.
1ANLGIN–	11	I	Inverting analog input to uncommitted transmit operational amplifier for channel 1.
2ANLGIN+	43	I	Noninverting analog input to uncommitted transmit operational amplifier for channel 2.
2ANLGIN–	44	I	Inverting analog input to uncommitted transmit operational amplifier for channel 2.
3ANLGIN+	37	I	Noninverting analog input to uncommitted transmit operational amplifier for channel 3.
3ANLGIN–	38	I	Inverting analog input to uncommitted transmit operational amplifier for channel 3.
ASEL	24	I	A-law and μ-law operation select. When ASEL is connected to ground, A-law is selected. When ASEL is connected to VDD, μ-law is selected (digital).
AVDD	46		Analog supply voltage, 5 V, ±10%.
AVSS	3		Analog ground return for AVDD supply.
DVDD	20		Digital supply voltage, 5 V, ±10%.
DVDDPLL	21		Phase-locked loop digital supply voltage, 5 V ±10%.
DVSSPLL	23		Digital ground return for DVDD supply.
DVSS	19		Phase-locked loop ground return for DVDDPLL supply.
0FS	31	I	Frame synchronization clock input/time slot enable for channel 0 (digital).
1FS	30	I	Frame synchronization clock input/time slot enable for channel 1 (digital).
2FS	29	I	Frame synchronization clock input/time slot enable for channel 2 (digital).
3FS	28	I	Frame synchronization clock input/time slot enable for channel 3 (digital).
0GSR	8	I	Receive amplifier gain-set input (channel 0). The ratio of an external voltage divider network connected to 0PWRO– and 0PWRO+ determines the receive amplifier gain. Maximum gain occurs when 0GSR is connected to 0PWRO–, and minimum gain occurs when it is connected to 0PWRO+ (analog).
1GSR	14	I	Receive amplifier gain-set input (channel 1). The ratio of an external voltage divider network connected to 1PWRO– and 1PWRO+ determines the receive amplifier gain. Maximum gain occurs when 1GSR is connected to 1PWRO–, and minimum gain occurs when it is connected to 1PWRO+ (analog).
2GSR	41	I	Receive amplifier gain-set input (channel 2). The ratio of an external voltage divider network connected to 2PWRO– and 2PWRO+ determines the receive amplifier gain. Maximum gain occurs when 2GSR is connected to 2PWRO–, and minimum gain occurs when it is connected to 2PWRO+ (analog).
3GSR	35	I	Receive amplifier gain-set input (channel 3). The ratio of an external voltage divider network connected to 3PWRO– and 3PWRO+ determines the receive amplifier gain. Maximum gain occurs when 3GSR is connected to 3PWRO–, and minimum gain occurs when it is connected to 3PWRO+ (analog).
0GSX	4	O	Output terminal of internal uncommitted transmit operational amplifier for channel 0 (analog).
1GSX	10	O	Output terminal of internal uncommitted transmit operational amplifier for channel 1. (analog)
2GSX	45	O	Output terminal of internal uncommitted transmit operational amplifier for channel 2. (analog)
3GSX	39	O	Output terminal of internal uncommitted transmit operational amplifier for channel 3 (analog).
MCLK	22	I	Master clock input (2.048 MHz) (digital).
PCMIN	25	I	Transmit PCM input (digital).
PCMOUT	27	O	Transmit PCM output (digital).
0PDN	16	I	Power-down select for channel 0. This channel of the device is inactive with a CMOS low-level input to 0PDN and active with a CMOS high-level input to the terminal (digital).
1PDN	17	I	Power-down select for channel 1. This channel of the device is inactive with a CMOS low-level input to 1PDN and active with a CMOS high-level input to the terminal (digital).
2PDN	32	I	Power-down select for channel 2. This channel of the device is inactive with a CMOS low-level input to 2PDN and active with a CMOS high-level input to the terminal (digital).

PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
3PDN	33	I	Power-down select for channel 3. This channel of the device is inactive with a CMOS low-level input to 3PND and active with a CMOS high-level input to the terminal (digital).
0PWRO+	7	O	Noninverting output of channel 0 power amplifier, able to drive 600 Ω ‖ 100 pF load (analog).
0PWRO–	9	O	Inverting output of channel 0 power amplifier, able to drive 600 Ω ‖ 100 pF load (analog).
1PWRO+	13	O	Noninverting output of channel 1 power amplifier, able to drive 600 Ω ‖ 100 pF load (analog).
1PWRO–	15	O	Inverting output of channel 1 power amplifier, able to drive 600 Ω ‖ 100 pF load (analog).
2PWRO+	42	O	Noninverting output of channel 2 power amplifier, able to drive 600 Ω ‖ 100 pF load (analog).
2PWRO–	40	O	Inverting output of channel 2 power amplifier, able to drive 600 Ω ‖ 100 pF load (analog).
3PWRO+	36	O	Noninverting output of channel 3 power amplifier, able to drive 600 Ω ‖ 100 pF load (analog).
3PWRO–	34	O	Inverting output of channel 3 power amplifier, able to drive 600 Ω ‖ 100 pF load (analog).
RBIAS	1		Bias current setting resistor. A 100 kΩ, ± 5% resistor should be connected between terminals RBIAS and AVSS to set the bias current of the device.
REFLTR1	48		Voltage reference. A 1-μF external decoupling capacitor should be connected from REFLTR1 to AVSS for filtering purposes.
REFLTR2	47		Voltage reference. A 1-μF external decoupling capacitor should be connected from REFLTR2 to AVSS for filtering purposes
RESET	26		Reset. Reset for all internal registers is initiated when RESET is brought high and held high for eight clock cycles (digital).
VSS	18		Substrate bias. This terminal should be externally connected to AVSS.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) ..... −0.3 V to 7 V
Input voltage range, V_I ..... −0.3 V to 7 V
Digital ground voltage range, V_O ..... −0.3 V to 7 V
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to AVSS.

recommended operating conditions (see Notes 2 and 3)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.5	5	5.5	V
High-level input voltage, V_{IH}	$0.8 \times V_{DD}$			V
Low-level input voltage, V_{IL}			$0.2 \times V_{DD}$	V
Load resistance between PWRO+and AVSS (single ended), R_L	600			Ω
Load capacitance between PWRO+ and AVSS, (single ended) C_L			100	pF
Operating free-air temperature, T_A	−40		85	°C

NOTES: 2. To avoid possible damage to these CMOS devices and resulting reliability problems, the power-up procedure described in the device power-up sequence paragraphs later in this document should be followed.

3. Voltages at analog inputs, outputs and the AVDD terminal are with respect to the AGND terminal. All other voltages are referenced to the DVSS terminal unless otherwise noted.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

supply current, total device, MCLK = 2.048 MHz, outputs not loaded, V_{DD} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply current from V_{DD}	Operating			35		mA
		Power down	PDN (all channels)		1		mA

digital interface

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	PCMOUT	I_{OH} = −3.2 mA		4.6		V
V_{OL}	Low-level output voltage	PCMOUT	I_{OL} = 3.2 mA		0.2	0.4	V
I_{IH}	High-level input current, any digital input		$V_I = 0.8 \times V_{DD}$			10	μA
I_{IL}	Low-level input current, any digital input		$V_I = 0.2 \times V_{DD}$			10	μA
C_i	Input capacitance				5		pF
C_o	Output capacitance				5	50	pF

transmit amplifier input (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Input current at ANLGIN+ and ANLGIN−	Internal gain control set to 0 dB			±100	nA
Input offset voltage at ANLGIN+ and ANLGIN−				±20	mV
Common-mode rejection at ANLGIN+ and ANLGIN−		55			dB
Open-loop voltage amplification at ANLGIN+ and ANLGIN−		5000			
Open-loop unity-gain bandwidth at ANLGIN+ and ANLGIN−			1		MHz
Input resistance at ANLGIN+ and ANLGIN−		10			MΩ

receive filter output

PARAMETER	TEST CONDITION	MIN	TYP†	MAX	UNIT
Output offset voltage PWRO+	Relative to AGND			80	mV
Output resistance at PWRO+			1		Ω

† All typical values are at V_{DD} = 5 V, and T_A = 25°C

transmit and receive gain and dynamic range, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Encoder milliwatt response (transmit gain tolerance)	Signal input = 0.75 Vrms		±0.04	±0.18	dBm0
Encoder milliwatt response (nominal supplies and temperature)	T_A = 0°C to 70°C, Supplies = ±5%			±0.08	dB
Digital milliwatt response (receive tolerance gain) relative to zero-transmission-level point	Signal input per CCITT G.711, Output signal = 1 kHz		±0.04	+0.18	dBm0
Digital milliwatt response variation with temperature and power supplies	T_A = 0°C to 70°C, Supplies = ±5%			±0.08	dB
Transmit overload signal level (3 dB), peak-to-peak centered at AGND	Input buffer is configured in unity gain			3	Vpp
Receive reference-signal level at PWRO, 0 dB level (3 dB is full scale)	R_L = 600 Ω @ maximum gain (Load resistance is connected between PWRO+ and PWRO−)		2		Vrms
Overload-signal level, (3 dB level) fully differential (see Note 4)	R_L = 600 Ω @ maximum gain (Load resistance is connected between PWRO+ and PWRO−)		8		Vpp

NOTE 4: Maximum voltage swing (single-ended) is 3.5 V when V_{DD} is 4.5 V.

PRODUCT PREVIEW

transmit and receive gain tracking over recommended ranges of supply voltage and operating free-air temperature, reference level = –10 dBm0

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Transmit gain tracking error, sinusoidal input	3 > input level > –40 dBm0			±0.25	dB
	–40 > input level > –50 dBm0			±0.5	
	–50 > input level > –55 dBm0			±1.2	
Receive gain tracking error, sinusoidal input	3 > input level > –40 dBm0			±0.25	dB
	–40 > input level > –50dBm0			±0.5	
	–50 > input level > –55 dBm0			±1.2	

noise over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Transmit noise, C-message weighted	ANLGIN+ = AGND			12	dBrnC0
Transmit noise, psophometrically weighted	ANLGIN+ = AGND			–75	dBm0p
Receive noise, C-message-weighted quiet code	PCMIN = 10101010 (A-law) measured at PWR0+			12	dBrnC0
Receive noise, psophometrically weighted	PCM = lowest positive decode level			–79	dBm0p

power supply rejection and crosstalk attenuation over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITION	MIN	TYP†	MAX	UNIT
V_{DD} supply voltage rejection, transmit channel	0 < f < 30 kHz	Idle channel, supply signal = 200 mVpp, f measured at PCMOUT		–40		dB
	30 < f < 50 kHz			–45		
V_{DD} supply voltage rejection, receive channel (single-ended)	0 < f < 30 kHz	Idle channel, supply signal = 200 mVpp, narrow-band, f measured at PWRO+		–40		dB
	30 < f< 50 kHz			–45		
Crosstalk (same channel) attenuation, transmit-to-receive (single-ended)		ANLGIN+ = 0 dBm0, f = 1.02 kHz, unity gain, PCMIN = lowest decode level, measured at PWRO	75			dB
Crosstalk (same channel) attenuation, receive-to-transmit (single-ended)		PCMIN = 0 dBm0, f = 1.02 kHz, measured at PCMOUT	75			dB
Crosstalk (between channels) attenuation	transmit to transmit	0 dBm0, 300 Hz – 3400 Hz	76			dB
	transmit to receive		78			
	receive to transmit		76			
	receive to receive		78			

† All typical values are at V_{DD} = 5 V, and T_A = 25°C

PRODUCT PREVIEW

distortion over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Transmit signal to distortion ratio, sinusoidal input (CCITT G.712 - Method 2)	0 > ANLGIN > −30 dBm0	36			dB
	−30 > ANLGIN > −40 dBm0	30			
	−40 > ANLGIN > −45 dBm0	25			
Receive signal to distortion ratio, sinusoidal input (CCITT G.712 - Method 2)	0 > ANLGIN > −30 dBm0	36			dB
	−30 > ANLGIN > −40 dBm0	30			
	−40 > ANLGIN > −45 dBm0	25			
Transmit single-frequency distortion products	AT&T Advisory #64 (3.8), Input signal = 0 dBm0			−46	dBm0
Receive single-frequency distortion products	AT&T Advisory #64 (3.8), Input signal = 0 dBm0			−46	dBm0
Intermodulation distortion, end-to-end Spurious out-of-band signals, end-to-end	CCITT G.712 (7.1)			−35	dBm0
	CCITT G.712 (7.2)			−49	
	CCITT G.712 (6.1)			−25	
	CCITT G.712 (9)			−40	

transmit filter transfer over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

PARAMETER	TEST CONDITION		MIN	MAX	UNIT
Gain (voltage amplification) relative to gain at 1.02 kHz	Input amplifier set for unity gain, Noninverting maximum gain output, Input signal at ANLGIN is 0 dBm0	16.67 Hz		−30	dB
		50 Hz		−25	
		60 Hz		−23	
		200 Hz	−1.8	−0.125	
		300 Hz to 3 kHz	−0.15	0.15	
		3.3 kHz	−0.35	0.15	
		3.4 kHz	−1	−0.1	
		4 kHz		−14	

receive filter transfer over recommended ranges of supply voltage and operating free-air temperature (see Figure 2)

PARAMETER	TEST CONDITION		MIN	MAX	UNIT
Gain (voltage amplification) relative to gain at 1.02 kHz	Input signal at PCMIN is 0 dBm0	Below 20 Hz	−0.15	0.15	dB
		20 Hz	−0.15	0.15	
		200 Hz	−0.15	0.15	
		300 Hz to 3 kHz	−0.15	0.15	
		3.3 kHz	−0.35	0.15	
		3.4 kHz	−1	−0.1	
		4 kHz		−14	
		4.6 kHz and above		−30	

PRODUCT PREVIEW

timing requirements

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 3 and 4)

		MIN	NOM†	MAX	UNIT
$t_{c(MCLK)}$	Clock period for MCLK 2.048 MHz systems	488			ns
t_r	Rise time for MCLK		5	30	ns
t_f	Fall time for MCLK		5	30	ns
$t_{w(MCLK)}$	Pulse duration for MCLK (see Note 5)	220			ns
	Clock duty cycle [$t_{w(MCLK)}/t_{c(MCLK)}$] for MCLK	45%	50%	55%	

† All nominal values are at V_{DD} = 5 V, and T_A = 25°C.
NOTE 5: FS clock must be phase-locked with MCLK

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 3)

		MIN	MAX	UNIT
$t_{d(FSX)}$	Delay time, frame sync	100	t_c (MCLK) –100	ns

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 4)

		MIN	MAX	UNIT
$t_{d(FSR)}$	Delay time, frame sync	100	t_c (MCLK) –100	ns
$t_{su(PCMIN)}$	Setup time, receive data	10		ns
$t_{h(PCMIN)}$	Hold time, receive data	60		ns

switching characteristics

propagation delay times over recommended ranges of operating conditions, fixed-data-rate mode (see Figure 3)

PARAMETER		TEST CONDITION	MIN	MAX	UNIT
t_{pd1}	Transmit clock↑ to bit 1 data valid at PCMOUT (data enable time on time slot entry) (see Note 5)	C_L = 0 to 100 pF	0	145	ns
t_{pd2}	Transmit clock↑ bit n to bit n data valid at PCMOUT (data valid time)	C_L = 0 to 100 pF	0	145	ns
t_{pd3}	Transmit clock↓ bit 8 to bit 8 hi-Z at PCMOUT (data float time on time slot exit) (see Note 6)	C_L = 0 pF	60	215	ns

NOTE 6: Timing parameters tpd1, tpd3, and tpd5 are referenced to the high-impedance state.

PRODUCT PREVIEW

absolute and relative delay times over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITION	MIN	TYP†	MAX	UNIT
Transmit absolute delay time to PCMOUT	Fixed data rate, MCLK = 2.048 MHz, Input to ANLGIN 1.02 kHz at 0 dBm0		500		µS
Transmit differential envelope delay time relative to transmit absolute delay time	f = 500 Hz – 600 Hz		170		µS
	f = 600 Hz – 1000 Hz		95		
	f = 1000 Hz – 2600 Hz		45		
	f = 2600 Hz – 2800 Hz		105		
Receive absolute delay time to PWRO	Fixed data rate, MCLK = 2.048 MHz, Digital input is DMW codes		190		µS
Receive differential envelope delay time relative to transmit absolute delay time	f = 500 Hz – 600 Hz		45		µS
	f = 600 Hz – 1000 Hz		35		
	f = 1000 Hz – 2600 Hz		85		
	f = 2600 Hz – 2800 Hz		110		

† All typical values are at V_{DD} = 5 V, and T_A = 25°C

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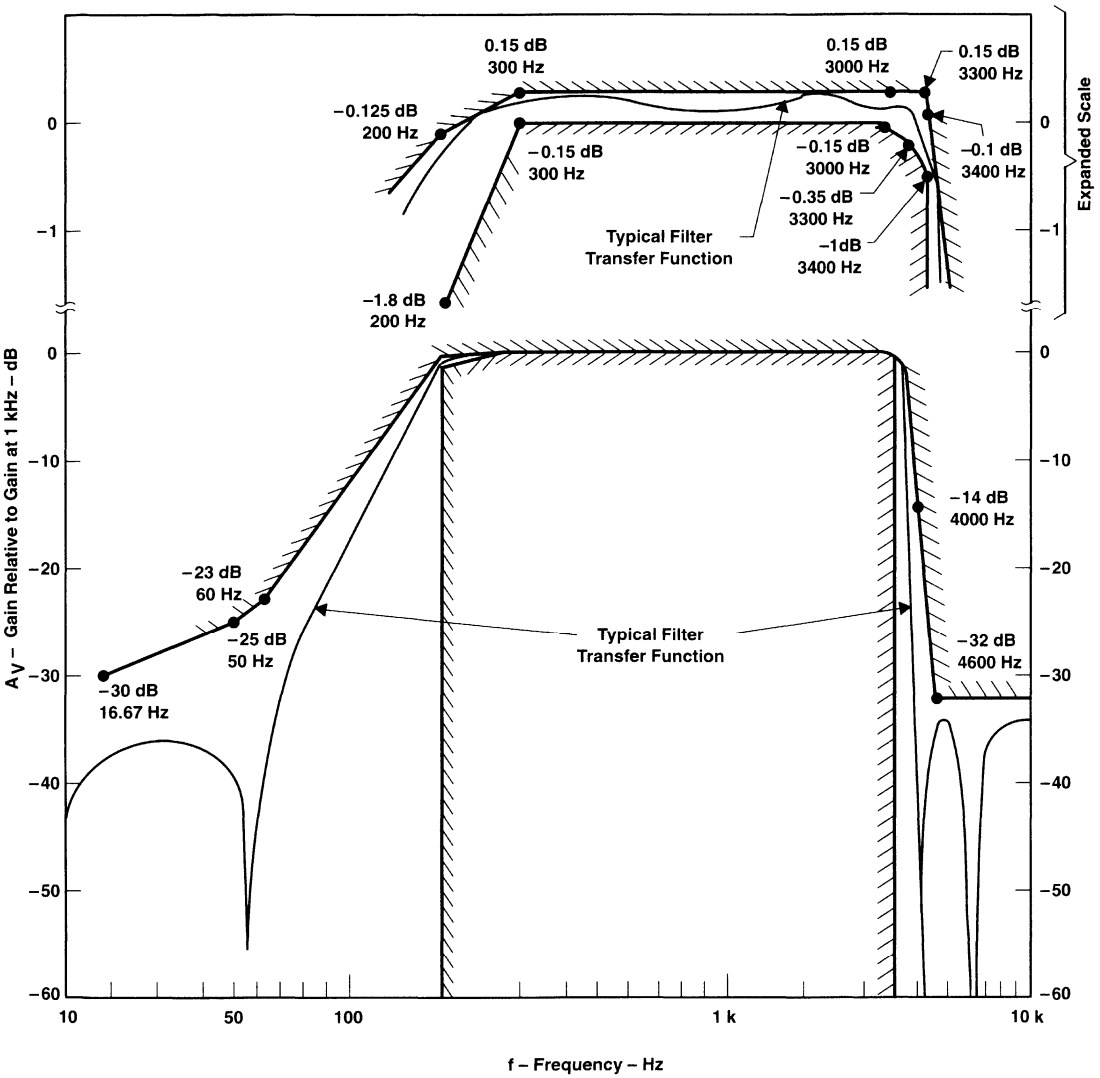
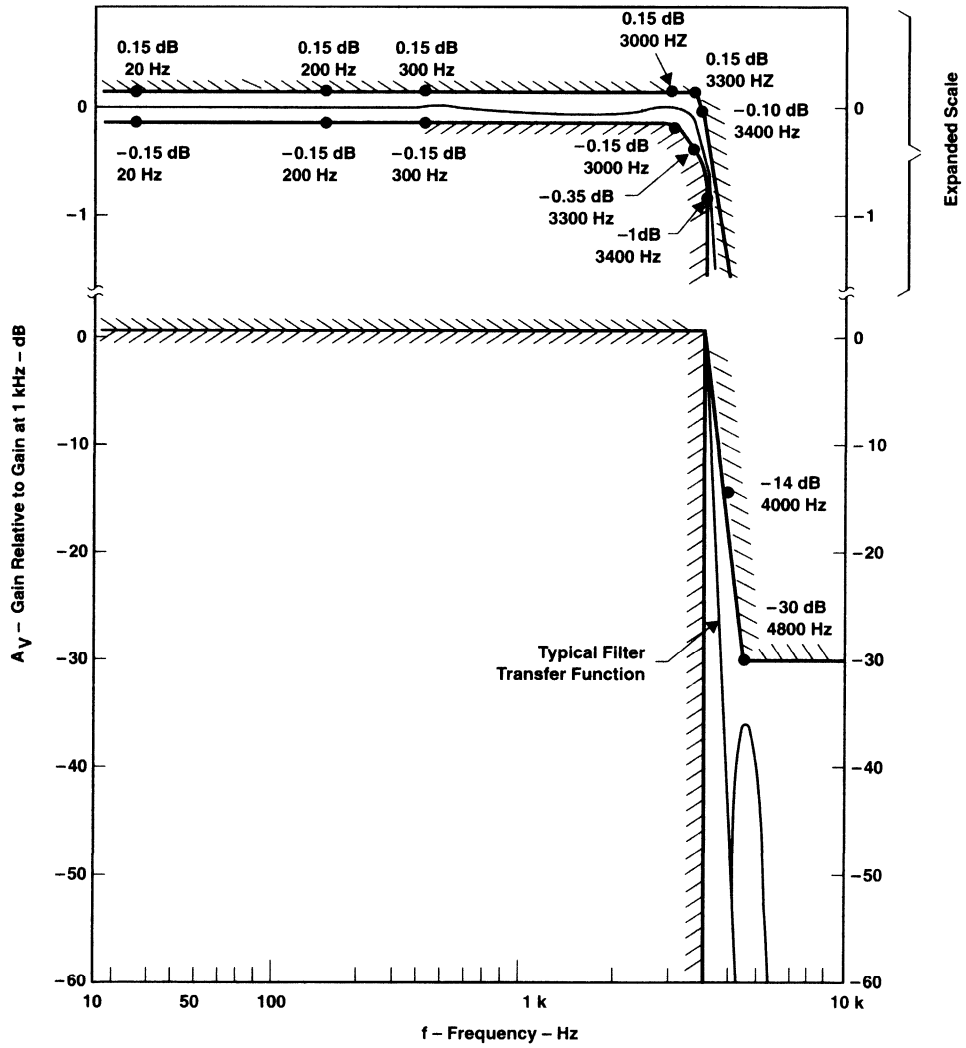
PARAMETER MEASUREMENT INFORMATION



NOTE B: For this figure, gain (voltage amplification) is defined as gain relative to gain at 1 kHz –dB

Figure 1. Transmit-Filter Transfer Characteristics

PARAMETER MEASUREMENT INFORMATION

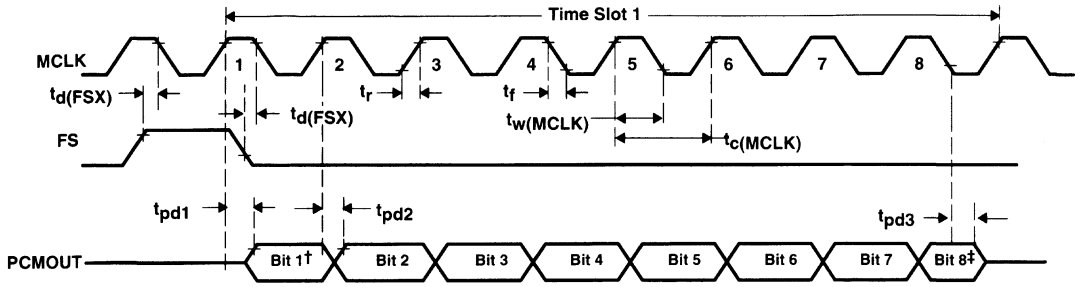


NOTE A: For this figure, gain (voltage amplification) is defined as gain relative to gain at 1 kHz –dB

Figure 2. Receive-Filter Transfer Characteristics

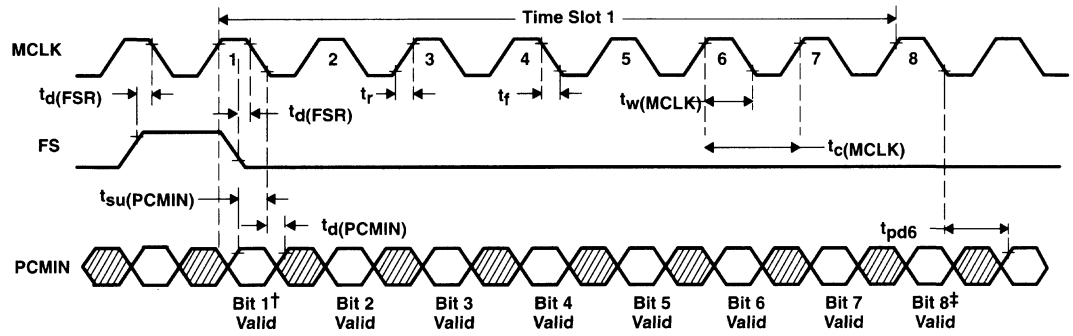
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



† Bit 1 = MSB = most significant bit and is clocked in first on the PCMIN terminal or is clocked out first on the PCMOUT terminal.
‡ Bit 8 = LSB = least significant bit and is clocked in last on the PCMIN terminal or is clocked out last on the PCMOUT terminal.
NOTE A: Inputs are driven from 0.45 V to 2.4 V. Time intervals are referenced to 2 V when the high level is indicated and 0.8 V if the low level is indicated.

Figure 3. PCM Transmit Timing



† Bit 1 = MSB = most significant bit and is clocked in first on the PCMIN terminal or is clocked out first on the PCMOUT terminal.
‡ Bit 8 = LSB = least significant bit and is clocked in last on the PCMIN terminal or is clocked out last on the PCMOUT terminal.
NOTE A: Inputs are driven from 0.45 V to 2.4 V. Time intervals are referenced to 2 V when the high level is indicated and 0.8 V if the low level is indicated.

Figure 4. PCM Receive Timing

PRODUCT PREVIEW

PRINCIPALS OF OPERATION

system reliability and design considerations

TCM38C17 system reliability and design considerations are described in the following paragraphs.

latch-up

Latch-up is possible in all CMOS devices. It is caused by the firing of a parasitic SCR that is present due to the inherent nature of CMOS. When a latch-up occurs, the device draws excessive amounts of current and will continue to draw heavy current until power is removed. Latch-up can result in permanent damage to the device if supply current to the device is not limited.

Even though the QCombo is heavily protected against latch-up, it is still possible to cause latch-up under certain conditions in which excess current is forced into or out of one or more terminals. Latch-up can occur when the supply voltage drops momentarily below ground or possibly if a signal is applied to a terminal after power has been applied but before the ground is connected. This can happen if the device is hot-inserted into a card with the power applied, or if the device is mounted on a card that has an edge connector and the card is hot-inserted into a system with the power on.

To help ensure that latch-up does not occur, it is considered good design practice to connect a reverse-biased Schottky diode (with a forward voltage drop of less than or equal to 0.4 V — 1N5711 or equivalent) between the power supply and GND (see Figure 5). If it is possible that a QCombo-equipped card that has an edge connector could be hot-inserted into a powered-up system, it is also important to ensure that the ground edge connector traces are longer than the power and signal traces so that the card ground is always the first to make contact.

device power-up sequence

Latch-up can also occur if a signal source is connected without the device being properly grounded. A signal applied to one terminal could then find a ground through another signal terminal on the device. To ensure proper operation of the device and as a safeguard against this sort of latch-up, it is recommended that the following power-up sequence always be used:

1. Ensure that no signals are applied to the device before the power-up sequence is complete.
2. Connect GND.
3. Apply power.
4. Force a power down condition in the device.
5. Connect the master clock.
6. Release the power down condition.
7. Apply FS synchronization pulses.
8. Apply the signal inputs.

When powering down the device, this procedure should be followed in the reverse order.

PRINCIPLES OF OPERATION

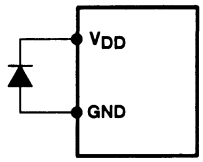


Figure 5. Latch-Up Protection Diode Connection

internal sequencing

On the transmit channel, digital output PCMOUT is held in the high-impedance state for approximately four frames (500 μs) after power up or application of V_{DD}. After this delay, PCMOUT is functional and occurs in the proper timeslot. Valid digital information, such as for on/off hook detection, is available almost immediately.

To further enhance system reliability, PCMOUT is placed in a high-impedance state approximately 20 μs after an interruption of MCLK. This interruption could possibly occur with some kind of fault condition elsewhere in the system.

power-down operation

To minimize power consumption, a power-down mode is provided for each channel. To power down a channel, an external logic low signal is applied to the corresponding PDN terminal. It is not sufficient to remove the logic high to PDN; in the absence of a signal, the PDN terminal floats to logic high and the device remains active. In the power-down mode, the average power consumption is reduced to an average of 1 mW/channel.

miscellaneous

TCM38C17 timing and voltage references are described in the following paragraphs.

data timing

The TCM38C17 operates at 2.048 MHz using fixed-data-rate timing. An 8-kHz clock signal should be applied to the FS terminal to set the sampling frequency. Data is transmitted on the PCMOUT terminal on the first eight positive transitions of MCLK following the rising edge of FS. Data is received on the PCMIN terminal on the first eight falling edges of MCLK following FS.

precision voltage references

It is recommended that an external capacitor of 1-μF value be connected between REFLTR1 and AVSS and between REFLTR2 and AVSS to ensure clean voltage references. Voltage references that determine the gain and dynamic range characteristics of the device are generated internally. A band-gap mechanism is used to derive a temperature-independent and bias-stable reference voltage. These references are calibrated during the manufacturing process. Separate references are supplied to the transmit and receive sections, and each is calibrated independently. Each reference value is then further trimmed in the gain-setting operational amplifiers to a final precision value. Manufacturing tolerances of typically ±0.04 dB in absolute gain (voltage amplification) can be achieved for each half channel, providing the user a significant margin to compensate for error in other board components.

PRINCIPALS OF OPERATION

transmit operation

TCM38C17 transmit operation is described in the following paragraphs.

transmit input amplifier

The input section provides gain adjustment in the passband by means of an on-chip uncommitted operational amplifier. Gain for the amplifier is set using external input and feedback resistors as shown in Figure 6. This allows maximum flexibility in presetting volume levels. Unity gain can be achieved by assigning R_I and R_F equal values. The feedback impedance between GSX and ANLGIN– should be greater than 10 kΩ in parallel with less than 50 pF. GSX also provides a means of sampling the amplified signal.

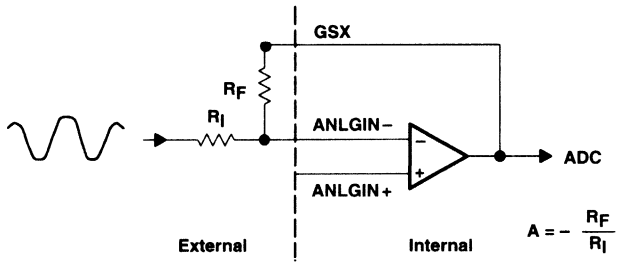


Figure 6. Transmit Path Gain Setting Circuitry

transmit filter

The transmit section filters provide passband flatness and stopband attenuation that fulfills the AT&T D3/D4 channel bank transmission specification and CCITT recommendation G.712. The device specifications meet or exceed digital class 5 central office switching systems requirements.

A high-pass section configuration was chosen to reject low-frequency noise from 50- and 60-Hz power lines, 17-Hz European electric railroads, ringing frequencies and their harmonics, and other low-frequency noise. Even with the high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200 Hz. This feature allows the use of low-cost transformer hybrids without external components.

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PRINCIPALS OF OPERATION

receive operation

TCM38C17 receive operation is described in the following paragraphs.

receive filter

The receive section filters provide pass-band flatness and stopband rejection that fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin x)/x response of such decoders.

output amplifier

The QCombo incorporates a versatile analog output power amplifier than can drive transformer hybrids or low-impedance loads directly in either a single-ended or differential configuration. The QCombo output stage allows for volume control (in the differential mode) by connection of a resistor chain to the output terminals of the device. The inverting operational amplifier can drive a 600 Ω load in parallel with 100 pF. Figure 7 is a representation of the internal structure of the output amplifier.

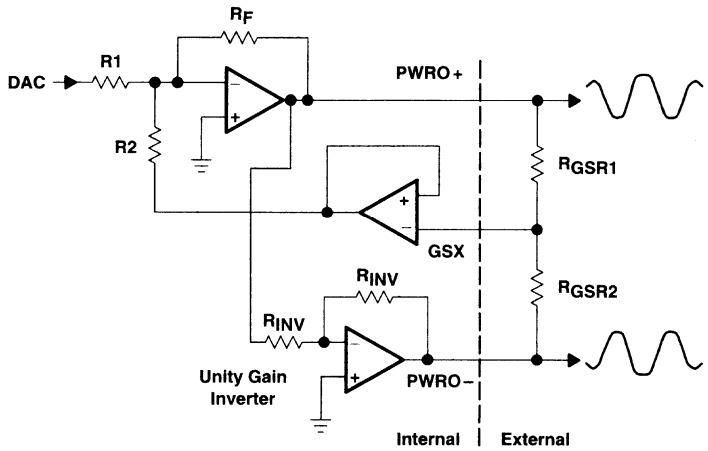


Figure 7. Output Amplifier Architecture

APPLICATIONS INFORMATION

Various TCM38C17 output configurations are detailed in the following paragraphs.

differential configuration

For connection to a transformer, the fully differential configuration is recommended to provide maximum possible output, or voltage swing, to the primary of an attached transformer. Figure 8 shows the QCombo in a fully differential mode.

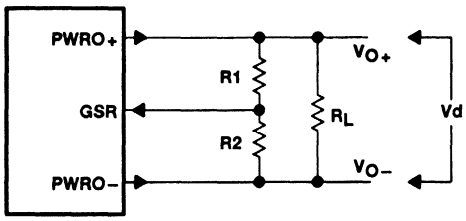


Figure 8. Fully Differential Gain-Setting Configuration

PWRO+ and PWRO– are low-impedance complementary outputs. The total output available for the output load (R_L) is then $V_D = V_{O+} - V_{O-}$. R1 and R2 form a gain-setting resistor network with a center tap connected to the GSR input.

R1 + R2 should be greater than 10 kΩ and less than 100 kΩ because the parallel combination R1 + R2 and R_L sets the total loading. The total parasitic capacitance of the GSR input, along with the parallel combination of R1 and R2, define a time constant that must be minimized to avoid inaccuracies in the gain calculations.

The resistor gain control actually consists of attenuating the full differential output voltage. The equation to determine the value of the attenuation constant is given in equation 1.

$$A = \frac{1 + (R1 \div R2)}{4 + (R1 \div R2)} \quad (1)$$

which can also be expressed as shown in equation 2.

$$A = \frac{R1 + R2}{4(R2 + R1 \div 4)} \quad (2)$$

where A = attenuation constant

Depending on the values of gain setting resistors R1 and R2, the attenuation constant (A) can have a value of 0.25 to unity (1), or approximately 12 dB of voltage adjustment.

APPLICATIONS INFORMATION

differential configuration (continued)

Maximum output (A = 1) can be obtained by maximizing R1 and minimizing R2. This can be done by letting R1 = infinity and R2 = 0 Ω (common GSR and PWRO–), as shown in Figure 9. Referring to the transmit and receive gain and dynamic range specifications, a maximum output of approximately 8 Vpp can be expected in this configuration. See the maximum analog output section for more detail on the digital input required for maximum analog output.

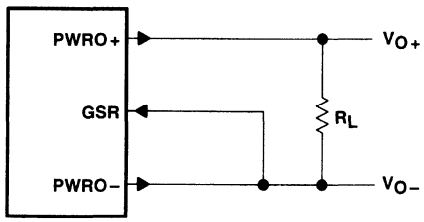


Figure 9. Fully Differential Maximum Gain-Setting Configuration (A = 1)

Figure 10 illustrates the QCombo with the resistor gain-control setting for an attenuation of A = 0.625.

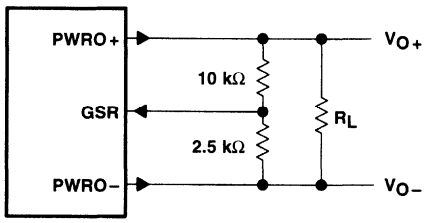


Figure 10. Fully Differential Mid-Gain-Setting Configuration (A = 0.625)

Shown in Figure 11, a minimum output (A = 0.25 dB) can be obtained by letting R1 = 0 Ω (common GSR and PWRO+), and R2 = infinity.

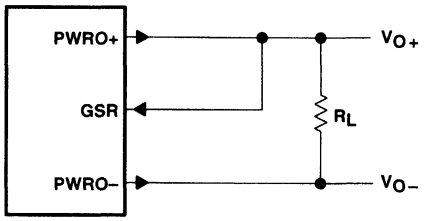


Figure 11. Fully Differential Minimum-Gain-Setting Configuration (A = 0.25)

PRODUCT PREVIEW

APPLICATIONS INFORMATION

single-ended configuration

Figure 12 illustrates the QCombo in a typical single-ended configuration. Either of the outputs can be connected through the load to analog ground (AGND), achieving an output voltage swing that is one half of the fully differential output voltage swing. Gain is set by manipulating the resistor network in the same way as detailed for the differential mode. The single-ended mode is most commonly used when interfacing to a succeeding stage that is referenced to analog ground.

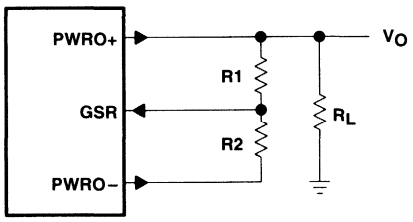


Figure 12. Single-Ended Configuration

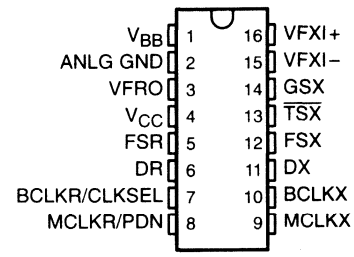
- **Complete PCM Codec and Filtering Systems Include:**
  - **Transmit High-Pass and Low-Pass Filtering**
  - **Receive Low-Pass Filter With (sin x)/x Correction**
  - **Active RC Noise Filters**
  - **μ-Law or A-Law Compatible Coder and Decoder**
  - **Internal Precision Voltage Reference**
  - **Serial I/O Interface**
  - **Internal Autozero Circuitry**
- **μ-Law . . . TP3054A and TP13054A**
- **A-Law . . . TP3057A and TP13057A**
- **±5-V Operation**
- **Low Operating Power . . . 50 mW Typ**
- **Power-Down Standby Mode . . . 3 mW Typ**
- **Automatic Power Down**
- **TTL- or CMOS-Compatible Digital Interface**
- **Maximizes Line Interface Card Circuit Density**
- **Improved Versions of National Semiconductor TP3054, TP3057, TP3054-X, TP3057-X**

description

The TP3054A, TP3057A, TP13054A, and TP13057A are comprised of a single-chip PCM codec (pulse code-modulated encoder and decoder) and PCM line filter. These devices provide all the functions required to interface a full-duplex (2-wire) voice telephone circuit with a TDM (time-division-multiplexed) system. These devices are pin-for-pin compatible with the National Semiconductor TP3054A and TP3057A, respectively. Primary applications include:

- Line interface for digital transmission and switching of T1 carrier, PABX, and central office telephone systems
- Subscriber line concentrators
- Digital-encryption systems
- Digital voice-band data-storage systems
- Digital signal processing

DW OR N PACKAGE
(TOP VIEW)

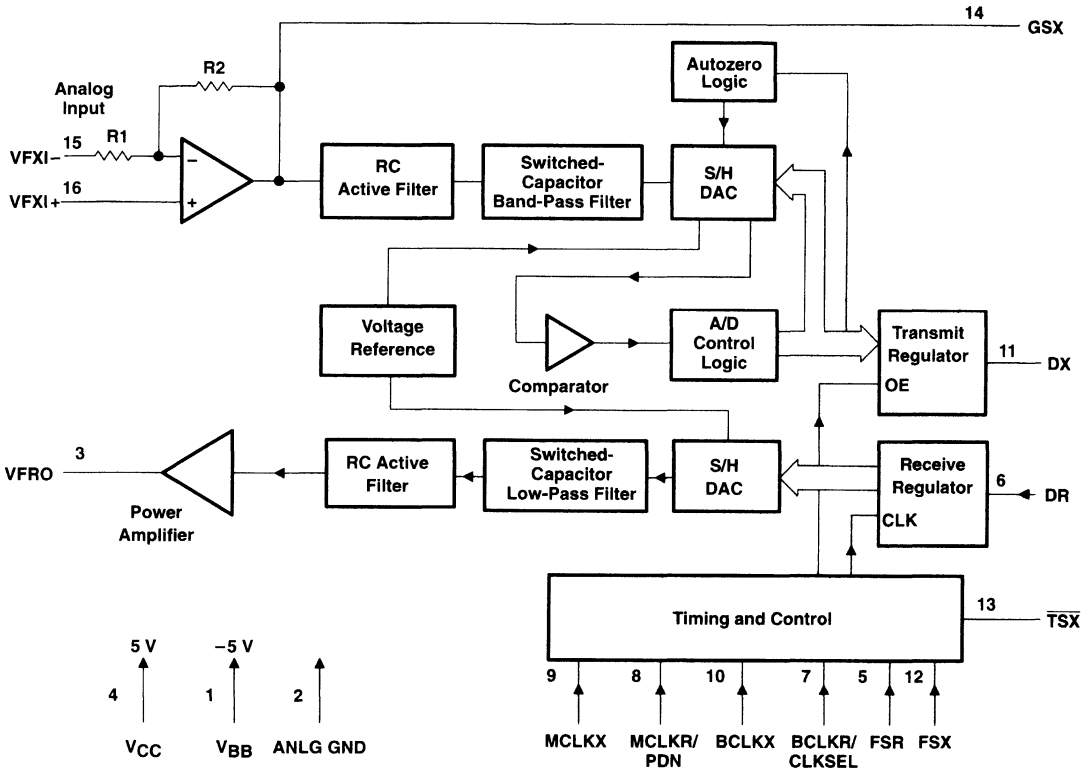


These devices are designed to perform the transmit encoding (A/D conversion) and receive decoding (D/A conversion) as well as the transmit and receive filtering functions in a PCM system. They are intended to be used at the analog termination of a PCM line or trunk. The devices require two transmit and receive master clocks that may be asynchronous (1.536 MHz, 1.544 MHz, or 2.048 MHz), transmit and receive data clocks that are synchronous with the master clock (but can vary from 64 kHz to 2.048 MHz), and transmit and receive frame-sync pulses. The TP3054A, TP3057A, TP13054A, and TP13057A provide the band-pass filtering of the analog signals prior to encoding and after decoding of voice and call progress tones. The TP3057A and TP13057A contain patented circuitry to achieve low transmit channel idle noise and are not recommended for applications in which the composite signals on the transmit side are below −55 dBm0.

The TP3054A and TP3057A are characterized for operation from 0°C to 70°C. The TP13054A and TP13057A are characterized for operation from −40°C to 85°C.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

functional block diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
ANLG GND	2	Analog ground. All signals are referenced to ANLG GND.
BCLKR/CLKSEL	7	The bit clock that shifts data into DR after the FSR leading edge. May vary from 64 kHz to 2.048 MHz. Alternately, BCLKR/CLKSEL can be a logic input that selects either 1.536 MHz/1.544 MHz or 2.048 MHz for the master clock in the synchronous mode. BCLKX is used for both transmit and receive directions (see Table 1).
BCLKX	10	The bit clock that shifts out the PCM data on DX. May vary from 64 kHz to 2.048 MHz, but must be synchronous with MCLKX.
DR	6	Receive data input. PCM data is shifted into DR following the FSR leading edge.
DX	11	The 3-state PCM data output that is enabled by FSX.
FSR	5	Receive-frame sync pulse input that enables BCLKR to shift PCM data in DR. FSR is an 8-kHz pulse train (see Figures 1 and 2 for timing details).
FSX	12	Transmit-frame sync pulse that enables BCLKX to shift out the PCM data on DX. FSX is an 8-kHz pulse train (see Figures 1 and 2 for timing details).
GSX	14	Analog output of the transmit input amplifier. GSX is used to externally set gain.
MCLKR/PDN	8	Receive master clock (must be 1.536 MHz, 1.544 MHz, or 2.048 MHz). May be synchronous with MCLKX, but should be synchronous with MCLKX for best performance. When MCLKR is connected continuously low, MCLKX is selected for all internal timing. When MCLKR is connected continuously high, the device is powered down.
MCLKX	9	Transmit master clock (must be 1.536 MHz, 1.544 MHz, or 2.048 MHz). May be asynchronous with MCLKR
$\overline{TSX}$	13	Open-drain output that pulses low during the encoder time slot
V_{BB}	1	Negative power supply. $V_{BB} = -5$ V ±5%
V_{CC}	4	Positive power supply. $V_{CC} = 5$ V ±5%
VFRO	3	Analog output of the receive filter
VFXI+	16	Noninverting input of the transmit input amplifier
VFXI−	15	Inverting input of the transmit input amplifier

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Supply voltage, V_{BB} (see Note 1) ..... −7 V
Voltage range at any analog input or output ..... V_{CC} +0.3 V to V_{BB} −0.3 V
Voltage range at any digital input or output ..... V_{CC} +0.3 V to ANLG GND −0.3 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: TP3054A, TP3057A ..... 0°C to 70°C
TP13054A, TP13057A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Supply voltage, V_{BB}		−4.75	−5	−5.25	V
High-level input voltage, V_{IH}		2.2			V
Low-level input voltage, V_{IL}				0.6	V
Common-mode input voltage range, V_{ICR}‡				±2.5	V
Load resistance, GSX, R_L		10			kΩ
Load capacitance, GSX, C_L				50	pF
Operating free-air temperature, T_A	TP3054A, TP3057A	0		70	°C
	TP13054A, TP13057A	−40		85	

‡ Measured with CMRR > 60 dB.

NOTE 2: To avoid possible damage to these CMOS devices and resulting reliability problems, the power-up procedure described in the device power-up sequence paragraphs later in this document should be followed.

electrical characteristics over recommended ranges of supply voltage operating free-air temperature range (unless otherwise noted)

supply current

PARAMETER			TEST CONDITIONS	TP305xA			TP1305xA			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
I_{CC}	Supply current from V_{CC}	Power down	No load		0.5	1		0.5	1.2	mA
		Active			6	9		6	10	
I_{BB}	Supply current from V_{BB}	Power down	No load		0.5	1		0.5	1.2	mA
		Active			6	9		6	10	

electrical characteristics at V_{CC} = 5 V ±5%, V_{BB} = −5 V ±5%, GND at 0 V, T_A = 25°C (unless otherwise noted)

digital interface

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	DX	I_H = -3.2 mA	2.4		V
V_{OL}	Low-level output voltage	DX	I_L = 3.2 mA		0.4	V
		$\overline{TSX}$	I_L = 3.2 mA, Drain open		0.4	
I_{IH}	High-level input current		$V_I = V_{IH}$ to V_{CC}		±10	µA
I_{IL}	Low-level input current	All digital inputs	V_I = GND to V_{IL}		±10	µA
I_{OZ}	Output current in high-impedance state	DX	V_O = GND to V_{CC}		±10	µA

analog interface with transmit amplifier input

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_I	Input current	VFXI+ or VFXI−	V_I = −2.5 V to 2.5 V			±200	nA
r_i	Input resistance	VFXI+ or VFXI−	V_I = −2.5 V to 2.5 V	10			MΩ
r_o	Output resistance		Closed loop, Unity gain		1	3	Ω
	Output dynamic range	GSX	$R_L \geq 10$ kΩ			±2.8	V
A_V	Open-loop voltage amplification	VFXI+ to GSX		5000			
B_I	Unity-gain bandwidth	GSX		1	2		MHz
V_{IO}	Input offset voltage	VFXI+ or VFXI−				±20	mV
CMRR	Common-mode rejection ratio			60			dB
K_{SVR}	Supply-voltage rejection ratio			60			dB

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.

analog interface with receive filter

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output resistance	VFRO			1	3	Ω
Load resistance		VFRO = ±2.5 V	600			Ω
Load capacitance	VFRO to GND				500	pF
Output dc offset voltage	VFRO to GND				±200	mV

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.

timing requirements

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$f_{clock(M)}$	Frequency of master clock	MCLKX and MCLKR	Depends on the device used and BCLKX/CLKSEL		1.536 1.544 2.048		MHz
$f_{clock(B)}$	Frequency of bit clock, transmit	BCLKX		64		2048	kHz
t_{w1}	Pulse duration, MCLKX and MCLKR high			160			ns
t_{w2}	Pulse duration, MCLKX and MCLKR low			160			ns
t_{r1}	Rise time of master clock	MCLKX and MCLKR	Measured from 20% to 80%			50	ns
t_{f1}	Fall time of master clock	MCLKX and MCLKR				50	ns
t_{r2}	Rise time of bit clock, transmit	BCLKX	Measured from 20% to 80%			50	ns
t_{f2}	Fall time of bit clock, transmit	BCLKX				50	ns
t_{su1}	Setup time, BCLKX high (and FSX in long-frame sync mode) before MCLKX↓		First bit clock after the leading edge of FSX	100			ns
t_{w3}	Pulse duration, BCLKX and BCLKR high		V_{IH} = 2.2 V	160			ns
t_{w4}	Pulse duration, BCLKX and BCLKR low		V_{IL} = 0.6 V	160			ns
t_{h1}	Hold time, frame sync low after bit clock low (long frame only)			0			ns
t_{h2}	Hold time, BCLKX high after frame sync↑ (short frame only)			0			ns
t_{su2}	Setup time, frame sync high before bit clock↓ (long frame only)			80			ns
t_{d1}	Delay time, BCLKX high to data valid		Load = 150 pF plus 2 LSTTL loads‡	0		140	ns
t_{d2}	Delay time, BCLKX high to $\overline{TSX}$ low		Load = 150 pF plus 2 LSTTL loads‡			140	ns
t_{d3}	Delay time, BCLKX (or 8 clock FSX in long frame only) low to data output disabled			50		165	ns
t_{d4}	Delay time, FSX or BCLKX high to data valid (long frame only)		C_L = 0 pF to 150 pF	20		165	ns
t_{su3}	Setup time, DR valid before BCLKR↓			50			ns
t_{h3}	Hold time, DR valid after BCLKR or BCLKX↓			50			ns
t_{su4}	Setup time, FSR or FSX high before BCLKR or BCLKR↓		Short-frame sync pulse (1 or 2 bit clock periods long) (see Note 3)	50			ns
t_{h4}	Hold time, FSX or FSR high after BCLKX or BCLKR↓		Short-frame sync pulse (1 or 2 bit clock periods long) (see Note 3)	100			ns
t_{h5}	Hold time, frame sync high after bit clock↓		Long-frame sync pulse (from 3 to 8 bit clock periods long)	100			ns
t_{w5}	Minimum pulse duration of the frame sync pulse (low level)		64 kbps operating mode	160			ns

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.
‡ Nominal input value for an LSTTL load is 18 kΩ.
NOTE 3: For short-frame sync timing, FSR and FSX must go high while their respective bit clocks are high.

operating characteristics, over operating free-air temperature range, V_{CC} = 5 V ±5%, V_{BB} = −5 V ±5%, GND at 0 V, V_I = 1.2276 V, f = 1.02 kHz, transmit input amplifier connected for unity gain, noninverting (unless otherwise noted)

filter gains and tracking errors

PARAMETER		TEST CONDITIONS‡	MIN	TYP†	MAX	UNIT
Maximum peak transmit overload level	TP3054A, TP13054A	3.17 dBm0		2.501		V
	TP3057A, TP13057A	3.14 dBm0		2.492		
Transmit filter gain, absolute (at 0 dBm0)		T_A = 25°C	−0.15		0.15	dB
Transmit filter gain, relative to absolute		f = 16 Hz			−40	dB
		f = 50 Hz			−30	
		f = 60 Hz			−26	
		f = 200 Hz	−1.8		−0.1	
		f = 300 Hz to 3000 Hz	−0.15		0.15	
		f = 3300 Hz	−0.35		0.05	
		f = 3400 Hz	−0.8		0	
		f = 4000 Hz			−14	
		f ≥ 4600 Hz (measure response from 0 Hz to 4000 Hz)			−32	
Absolute transmit gain variation with temperature and supply voltage		Relative to absolute transmit gain	−0.1		0.1	dB
Transmit gain tracking error with level		Sinusoidal test method, Reference level = −10 dBm0				dB
		3 dBm0 ≥ input level ≥ −40 dBm0			±0.2	
		−40 dBm0 > input level ≥ −50 dBm0			±0.4	
		−50 dBm0 > input level ≥ −55 dBm0			±0.8	
Receive filter gain, absolute (at 0 dBm0)		Input is digital code sequence for 0-dBm0 signal, T_A = 25°C	−0.15		0.15	dB
Receive filter gain, relative to absolute		f = 0 H_Z to 3000 Hz, T_A = 25°C	−0.15		0.15	dB
		f = 3300 Hz	−0.35		0.05	
		f = 3400 Hz	−0.8		0	
		f = 4000 Hz			−14	
Absolute receive gain variation with temperature and supply voltage		T_A = full range, See Note 4	−0.1		0.1	dB
Receive gain tracking error with level		Sinusoidal test method; reference input PCM code corresponds to an ideally encoded −10 dBm0 signal				
		3 dBm0 ≥ input level ≥ −40 dBm0			±0.2	
		−40 dBm0 > input level ≥ −50 dBm0			±0.4	
		−50 dBm0 > input level ≥ −55 dBm0			±0.8	
Receive output drive voltage		R_L = 10 kΩ			±2.5	V
Transmit and receive gain tracking error with level (A-law, CCITT C 712)		Pseudo-noise test method; reference input PCM code corresponds to an ideally encoded −10 dBm0 signal				dB
		3 dBm0 ≥ input level ≥ −40 dBm0			±0.25	
		−40 dBm0 > input level ≥ −50 dBm0			±0.3	
		−50 dBm0 > input level ≥ −55 dBm0			±0.45	

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.
‡ Absolute rms signal levels are defined as follows: V_I = 1.2276 V = 0 dBm0 = 4 dBm at f = 1.02 kHz with R_L = 600 Ω.
NOTE 4: Full range for the TP3054A and TP3057A is 0°C to 70°C. Full range for the TP13054A and TP13057A is −40°C to 85°C.

envelope delay distortion with frequency

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit delay, absolute (at 0 dBm0)	f = 1600 Hz		290	315	µs
Transmit delay, relative to absolute	f = 500 Hz to 600 Hz		195	220	µs
	f = 600 Hz to 800 Hz		120	145	
	f = 800 Hz to 1000 Hz		50	75	
	f = 1000 Hz to 1600 Hz		20	40	
	f = 1600 Hz to 2600 Hz		55	75	
	f = 2600 Hz to 2800 Hz		80	105	
	f = 2800 Hz to 3000 Hz		130	155	
Receive delay, absolute (at 0 dBm0)	f = 1600 Hz		180	200	µs
Receive delay, relative to absolute	f = 500 Hz to 1000 Hz	−40	−25		µs
	f = 1000 Hz to 1600 Hz	−30	−20		
	f = 1600 Hz to 2600 Hz		70	90	
	f = 2600 Hz to 2800 Hz		100	125	
	f = 2800 Hz to 3000 Hz		140	175	

noise

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit noise, C-message weighted	TP3054A, TP13054A	VFXI = 0 V		9	14	dBrnC0
Transmit noise, psophometric weighted (see Note 5)	TP3057A, TP13057A	VFXI = 0 V		−78	−75	dBm0p
Receive noise, C-message weighted	TP3054A, TP13054A	PCM code equals alternating positive and negative zero		2	4	dBrnC0
Receive noise, psophometric weighted	TP3057A, TP13057A	PCM code equals positive zero		−86	−83	dBm0p
Noise, single frequency		VFXI+ = 0 V, f = 0 kHz to 100 kHz, Loop-around measurement			−53	dBm0

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.

NOTE 5: Measured by extrapolation from the distortion test result. This parameter is achieved through use of patented circuitry and is not recommended for applications in which the composite signals on the transmit side are below −55 dBm0.

power supply rejection

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
Positive power-supply rejection, transmit	V_{CC} = 5 V + 100 mVrms, VFXI+ = −50 dBm0	f = 0 Hz to 4 kHz	A-law	38		dB
			μ-law	38		dBC†
		f = 4 kHz to 50 kHz		40		dB
Negative power-supply rejection, transmit	V_{BB} = −5 V + 100 mVrms, VFXI+ = −50 dBm0	f = 0 Hz to 4 kHz	A-law	35		dB
			μ-law	35		dBC†
		f = 4 kHz to 50 kHz		40		dB
Positive power-supply rejection, receive	PCM code equals positive zero, V_{CC} = 5 V + 100 mVrms	f = 0 Hz to 4 kHz	A-law	40		dB
			μ-law	40		dBC†
		f = 4 kHz to 50 kHz		40		dB
Negative power-supply rejection, receive	PCM code equals positive zero, V_{BB} = −5 V + 100 mVrms	f = 0 Hz to 4 kHz	A-law	38		dB
			μ-law	38		dBC†
		f = 4 kHz to 50 kHz		40		dB
Spurious out-of-band signals at the channel output (VFRO)	0 dBm0, 300-Hz to 3400-Hz input applied to DR (measure individual image signals at VFRO)				−30	dB
	f = 4600 Hz to 7600 Hz				−33	dB
	f = 7600 Hz to 8400 Hz				−40	
	f = 8400 Hz to 100 kHz				−40	

distortion

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Signal-to-distortion ratio, transmit or receive half-channel‡	Level = 3 dBm0		33		dBC†
	Level = 0 dBm0 to -30 dBm0		36		
	Level = −40 dBm0	Transmit	29		
		Receive	30		
	Level = −55 dBm0	Transmit	14		
		Receive	15		
Single-frequency distortion products, transmit				−46	dB
Single-frequency distortion products, receive				−46	dB
Intermodulation distortion	Loop-around measurement, VFXI+ = −4 dBm0 to −21 dBm0, Two frequencies in the range of 300 Hz to 3400 Hz			−41	dB
Signal-to-distortion ratio, transmit half-channel (A-law) (CCITT G.714)§	Level = −3 dBm0		33		dB
	Level = −6 dBm0 to −27 dBm0		36		
	Level = −34 dBm0		33.5		
	Level = −40 dBm0		28.5		
	Level = −55 dBm0		13.5		
Signal-to-distortion ratio, receive half-channel (A-law) (CCITT G.714)§	Level = −3 dBm0		33		dB
	Level = −6 dBm0 to −27 dBm0		36		
	Level = −34 dBm0		34.2		
	Level = −40 dBm0		30		
	Level = −55 dBm0		15		

† The unit dBC applies to C-message weighting.
‡ Sinusoidal test method (see Note 6)
§ Pseudo-noise test method
NOTE 6: The TP3054A and TP13054A are measured using a C-message weighted filter. The TP3057A and TP13057A are measured using a psophometric weighted filter.

crosstalk

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Crosstalk, transmit to receive	f = 300 Hz to 3000 Hz,	DR at steady PCM code		−90	−75	dB
Crosstalk, receive to transmit (see Note 7)	VFXI = 0 V,	f = 300 Hz to 3000 Hz		−90	−75	dB

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.
NOTE 7: Receive-to-transmit crosstalk is measured with a – 50 dBm0 activation signal applied at VFXI+.

PARAMETER MEASUREMENT INFORMATION

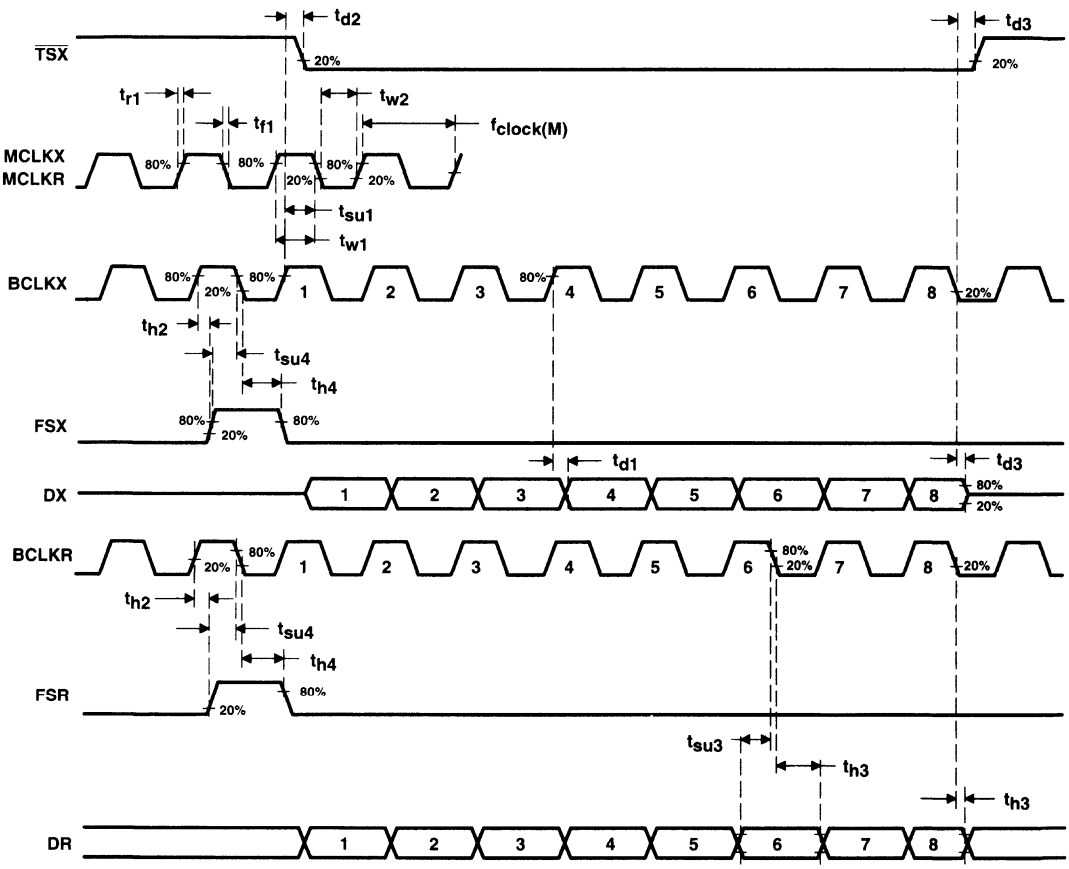


Figure 1. Short-Frame Sync Timing

PARAMETER MEASUREMENT INFORMATION

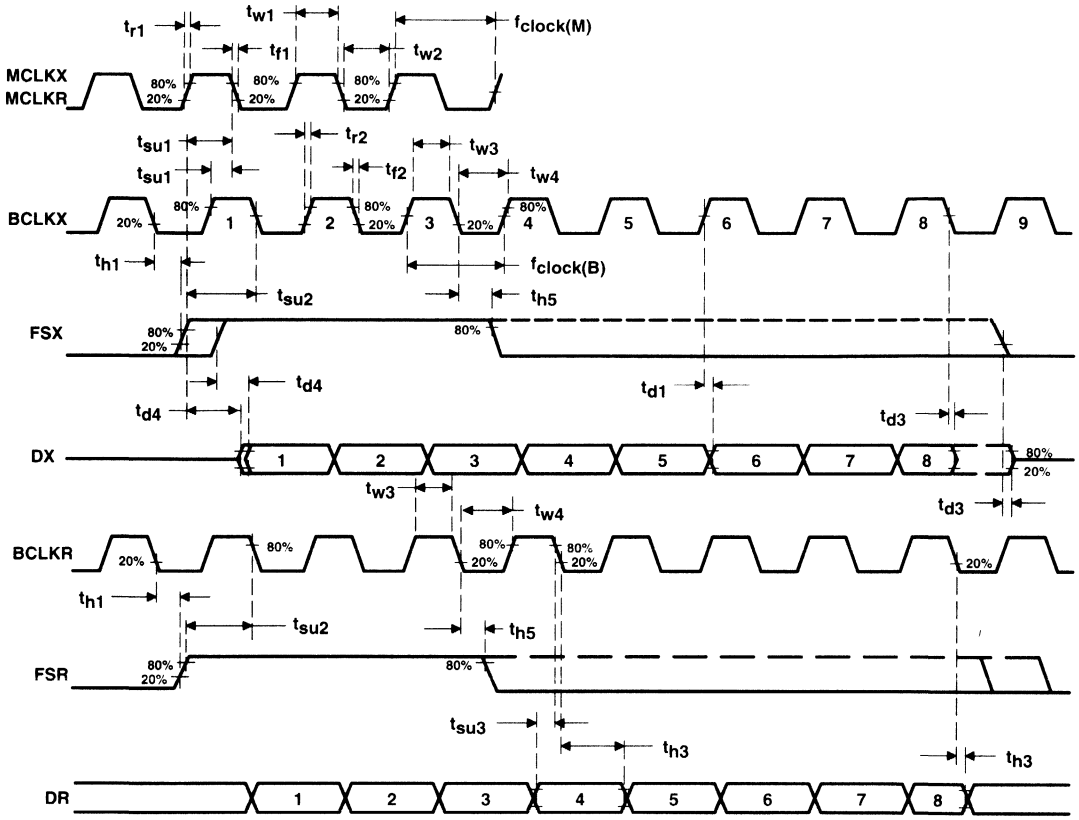


Figure 2. Long-Frame Sync Timing

PRINCIPLES OF OPERATION

system reliability and design considerations

TP305xA, TP1305xA system reliability and design considerations are described in the following paragraphs.

latch-up

Latch-up is possible in all CMOS devices. It is caused by the firing of a parasitic SCR that is present due to the inherent nature of CMOS. When a latch-up occurs, the device draws excessive amounts of current and will continue to draw heavy current until power is removed. Latch-up can result in permanent damage to the device if supply current to the device is not limited.

Even though the TP305xA and TP1305xA are heavily protected against latch-up, it is still possible to cause latch-up under certain conditions in which excess current is forced into or out of one or more terminals. Latch-up can occur when the positive supply voltage drops momentarily below ground, when the negative supply voltage rises momentarily above ground, or possibly if a signal is applied to a terminal after power has been applied but before the ground is connected. This can happen if the device is hot-inserted into a card with the power applied, or if the device is mounted on a card that has an edge connector and the card is hot-inserted into a system with the power on.

To help ensure that latch-up does not occur, it is considered good design practice to connect a reverse-biased Schottky diode (with a forward voltage drop of less than or equal to 0.4 V – 1N5711 or equivalent) between the power supply and GND (see Figure 3). If it is possible that a TP305xA- or TP1305xA-equipped card that has an edge connector could be hot-inserted into a powered-up system, it is also important to ensure that the ground edge connector traces are longer than the power and signal traces so that the card ground is always the first to make contact.

device power-up sequence

Latch-up can also occur if a signal source is connected without the device being properly grounded. A signal applied to one terminal could then find a ground through another signal terminal on the device. To ensure proper operation of the device and as a safeguard against this sort of latch-up, it is recommended that the following power-up sequence always be used:

1. Ensure that no signals are applied to the device before the power-up sequence is complete.
2. Connect GND.
3. Apply V_{BB} (most negative voltage).
4. Apply V_{CC} (most positive voltage).
5. Force a power down condition in the device.
6. Connect clocks.
7. Release the power down condition.
8. Apply FS synchronization pulses.
9. Apply the signal inputs.

When powering down the device, this procedure should be followed in the reverse order.

PRINCIPLES OF OPERATION

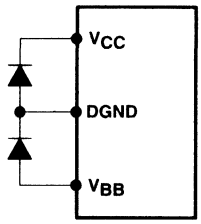


Figure 3. Latch-Up Protection Diode Connection

internal sequencing

Power-on reset circuitry initializes the TP3054A, TP3057A, TP13054A, and TP13057A devices when power is first applied, placing it into the power-down mode. DX and VFRO outputs go into high-impedance states and all nonessential circuitry is disabled. A low level or clock applied to MCLKR/PDN powers up the device and activates all circuits. DX, a 3-state PCM data output, remains in the high-impedance state until the arrival of the second FSX pulse.

synchronous operation

For synchronous operation, a clock is applied to MCLKX. MCLKR/PDN is used as a power-down control. A low level on MCLKR powers up the device and a high level powers it down. In either case, MCLKX is selected as the master clock for both receive and transmit direction. BCLKX must also have a bit clock applied to it. The selection of the proper internal divider for a master-clock frequency of 1.536 MHz, 1.544 MHz, or 2.048 MHz can be done via BCLKR/CLKSEL. The device automatically compensates for the 193rd clock pulse of each frame.

A fixed level on BCLKR/CLKSEL selects BCLKX as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation that can be selected depending on the state of BCLKR/CLKSEL. In the synchronous mode, BCLKX may be in the range from 64 kHz to 2.048 MHz but must be synchronous with MCLKX.

Table 1. Selection of Master-Clock Frequencies

BCLKR/CLKSEL	MASTER-CLOCK FREQUENCY SELECTED	
	TP13054A, TP3054A	TP13057A, TP3057A
Clock Input	1.536 MHz or 1.544 MHz	2.048 MHz
Logic Input L (sync mode only)	2.048 MHz	1.536 MHz or 1.544 MHz
Logic Input H (open) (sync mode only)	1.536 MHz or 1.544 MHz	2.048 MHz

The encoding cycle begins with each FSX pulse and the PCM data from the previous cycle is shifted out of the enabled DX output on the rising edge of BCLKX. After eight bit-clock periods, the 3-state DX output is returned to the high-impedance state. With an FSR pulse, PCM data is latched via DR on the falling edge of BCLKX (or BCLKR, if running). FSX and FSR must be synchronous with MCLKX and MCLKR.

PRINCIPLES OF OPERATION

asynchronous operation

For asynchronous operation, separate transmit and receive clocks can be applied. MCLKX and MCLKR must be 2.048 MHz for the TP3057A and TP13057A, 1.536 MHz or 1.544 MHz for the TP3054A and TP13054A and need not be synchronous. However, for best performance, MCLKR should be synchronous with MCLKX. This is easily achieved by applying only static logic levels to MCLKR/PDN. This connects MCLKX to all internal MCLKR functions. For 1.544-MHz operation, the device compensates for the 193rd clock pulse of each frame. Each encoding cycle is started with FSX and FSX must be synchronous with MCLKX and BCLKX. Each decoding cycle is started with FSR and FSR must be synchronous with BCLKR. The logic levels shown in Table 1 are not valid in the asynchronous mode. BCLKX and BCLKR can operate from 64 kHz to 2.048 MHz.

short-frame sync operation

The device can operate with either a short- or a long-frame sync pulse. On power up, the device automatically goes into the short-frame mode where both FSX and FSR must be one bit-clock period long with timing relationships specified in Figure 1. With FSX high during a falling edge of BCLKX, the next rising edge of BCLKX enables the 3-state output buffer, DX, which outputs the sign bit. The remaining seven bits are clocked out on the following seven rising edges, and the next falling edge disables DX. With FSR high during a falling edge of BCLKR (BCLKX in synchronous mode), the next falling edge of BCLKR latches in the sign bit. The following seven falling edges latch in the seven remaining bits. The short-frame sync pulse may be utilized in either the synchronous or asynchronous mode.

long-frame sync operation

Both FSX and FSR must be three or more bit-clock periods long to use the long-frame sync mode with timing relationships as shown in Figure 2. Using the transmit frame sync (FSX), the device detects whether a short- or long-frame sync pulse is being used. For 64-kHz operation, the frame-sync pulse must be kept low for a minimum of 160 ns. The rising edge of FSX or BCLKX, whichever occurs later, enables the DX 3-state output buffer. The first bit clocked out is the sign bit. The next seven rising edges of BCLKX edges clock out the remaining seven bits. The falling edge of BCLKX following the eighth rising edge or FSX going low, whichever occurs later, disables DX. A rising edge on FSR, the receive-frame sync pulse, causes the PCM data at DR to be latched in on the next eight falling edges of BCLKR (BCLKX in synchronous mode). The long-frame sync pulse can be utilized in either the synchronous or asynchronous mode.

transmit section

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors. The low noise and wide bandwidth characteristics of these devices provide gains in excess of 20 dB across the audio passband. The operational amplifier drives a unity-gain filter consisting of an RC active prefilter followed by an eighth-order switched-capacitor band-pass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. As per μ-law (TP3054A and TP13054A) or A-law (TP3057A and TP13057A) coding conventions, the ADC is a companding type. A precision voltage reference provides a nominal input overload ($t_{[max]}$) of nominally 2.5 V peak. The sampling of the filter output is controlled by the FSX frame-sync pulse. Then the successive-approximation encoding cycle begins. The 8-bit code is loaded into a buffer and shifted out through DX at the next FSX pulse. The total encoding delay is approximately 290 μs. Any offset voltage due to the filters or comparator is cancelled by sign-bit integration.

PRINCIPLES OF OPERATION

receive section

The receive section consists of an expanding DAC that drives a fifth-order low-pass filter clocked at 256 kHz. The decoder is μ-law (TP3054A and TP13054A) or A-law (TP3057A and TP13057A) and the fifth-order low-pass filter corrects for the (sin x)/x attenuation caused by the 8-kHz sample/hold. The filter is followed by a second-order RC active post-filter/power amplifier capable of driving a 600-Ω load to a level of 7.2 dBm. The receive section is unity gain. At FSR, the data at DR is clocked in on the falling edge of the next eight BCLKR (BCLKX) periods. At the end of the decoder time slot, the decoding cycle begins and 10 μs later, the decoder DAC output is updated. The decoder delay is about 10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (1/2 frame), or a total of approximately 180 μs.

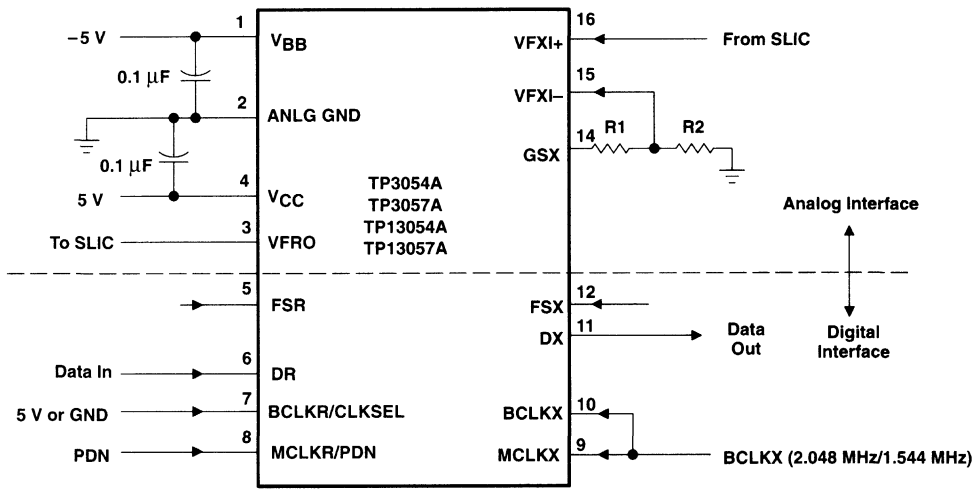
APPLICATION INFORMATION

power supplies

While the pins of the TP1305xA and TP305xA families are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed ensuring that ground is connected to the device before any other connections are made. In applications where the printed-circuit board can be plugged into a hot socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to ANLG GND. This minimizes the interaction of ground return currents flowing through a common bus impedance. V_{CC} and V_{BB} supplies should be decoupled by connecting 0.1-µF decoupling capacitors to this common point. These bypass capacitors must be connected as close as possible to V_{CC} and V_{BB}.

For best performance, the ground point of each codec/filter on a card should be connected to a common card ground in star formation rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10-µF capacitors.



NOTE A: Transmit gain = 20 log $\left(\frac{R1 + R2}{R2}\right)$, (R1 + R2) ≥ 10 kΩ

Figure 4. Typical Synchronous Application

TP3054B, TP3057B, TP13054B, TP13057B
MONOLITHIC SERIAL INTERFACE COMBINED PCM CODEC AND FILTER

SCTS042A – MAY 1990 – REVISED JULY 1996

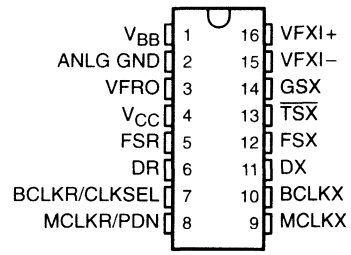
- **Complete PCM Codec and Filtering Systems Includes:**
  - **Transmit High-Pass and Low-Pass Filtering**
  - **Receive Low-Pass Filter With (sin x)/x Correction**
  - **Active RC Noise Filters**
  - **μ-Law or A-Law Compatible Coder and Decoder**
  - **Internal Precision Voltage Reference**
  - **Serial I/O Interface**
  - **Internal Autozero Circuitry**
- **μ-Law – TP3054B and TP13054B**
- **A-Law – TP3057B and TP13057B**
- **±5-V Operation**
- **Low Operating Power . . . 50 mW Typ**
- **Power-Down Standby Mode . . . 3 mW Typ**
- **Automatic Power Down**
- **TTL- or CMOS-Compatible Digital Interface**
- **Maximizes Line Interface Card Circuit Density**
- **Improved Versions of National Semiconductor TP3054, TP3057, TP3054-X, TP3057-X**

description

The TP3054B, TP3057B, TP13054B, and TP13057B are comprised of a single-chip PCM codec (pulse-code-modulated encoder and decoder) and PCM line filter. These devices provide all the functions required to interface a full-duplex (2-wire) voice telephone circuit with a TDM (time-division-multiplexed) system. These devices are pin-for-pin compatible with the National Semiconductor TP3054B and TP3057B, respectively. Primary applications include:

- Line interface for digital transmission and switching of T1 carrier, PABX, and central office telephone systems
- Subscriber line concentrators
- Digital-encryption systems
- Digital voice-band data-storage systems
- Digital signal processing

DW OR N PACKAGE
(TOP VIEW)

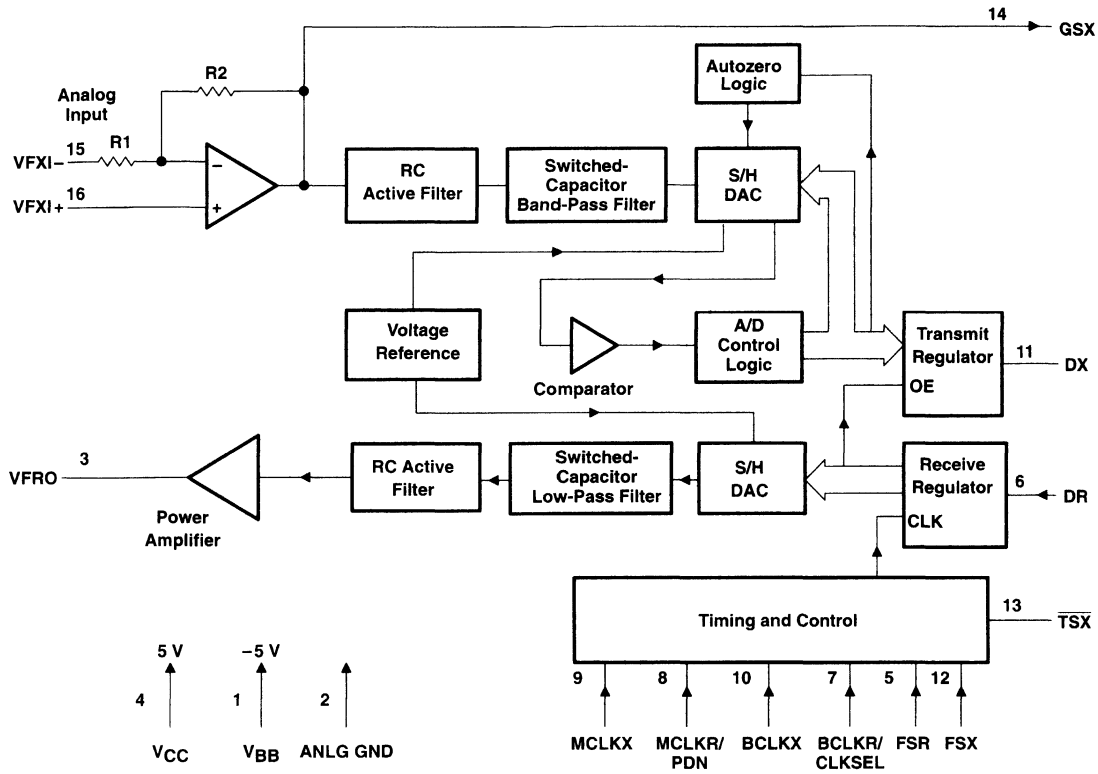


These devices are designed to perform the transmit encoding (A/D conversion) and receive decoding (D/A conversion) as well as the transmit and receive filtering functions in a PCM system. They are intended to be used at the analog termination of a PCM line or trunk. The devices require two transmit and receive master clocks that may be asynchronous (1.536 MHz, 1.544 MHz, or 2.048 MHz), transmit and receive data clocks that are synchronous with the master clock (but can vary from 64 kHz to 2.048 MHz), and transmit and receive frame-sync pulses. The TP3054B, TP3057B, TP13054B, and TP13057B provide the band-pass filtering of the analog signals prior to encoding and after decoding of voice and call progress tones. The TP3054B and TP13054B contain patented circuitry to achieve low transmit channel idle noise and are not recommended for applications in which the composite signals on the transmit side are below –55 dBm0.

The TP3054B and TP3057B are characterized for operation from 0°C to 70°C. The TP13054B and TP13057B are characterized for operation from –40°C to 85°C.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the CMOS gates.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
ANLG GND	2	Analog ground. All signals are referenced to ANLG GND.
BCLKR/CLKSEL	7	The bit clock that shifts data into DR after the FSR leading edge. May vary from 64 kHz to 2.048 MHz. Alternately, BCLKR/CLKSEL can be a logic input that selects either 1.536 MHz/1.544 MHz or 2.048 MHz for the master clock in the synchronous mode. BCLKX is used for both transmit and receive directions (see Table 1).
BCLKX	10	The bit clock that shifts out the PCM data on DX. BCLKX can vary from 64 kHz to 2.048 MHz, but must be synchronous with MCLKX.
DR	6	Receive data input. PCM data is shifted into DR following the FSR leading edge.
DX	11	The 3-state PCM data output that in enabled by FSX
FSR	5	Receive frame-sync pulse input that enables BCLKR to shift PCM data in DR. FSR is an 8-kHz pulse train (see Figures 1 and 2 for timing details).
FSX	12	Transmit frame-sync pulse that enables BCLKX to shift out the PCM data on DX. FSX is an 8-kHz pulse train (see Figures 1 and 2 for timing details).
GSX	14	Analog output of the transmit input amplifier. GSX is used to externally set gain.
MCLKR/PDN	8	Receive master clock (must be 1.536 MHz, 1.544 MHz, or 2.048 MHz). May be synchronous with MCLKX, but should be synchronous with MCLKX for best performance. When MCLKR is connected continuously low, MCLKX is selected for all internal timing. When MCLKR is connected continuously high, the device is powered down.
MCLKX	9	Transmit master clock (must be 1.536 MHz, 1.544 MHz, or 2.048 MHz). May be asynchronous with MCLKR.
$\overline{TSX}$	13	Open-drain output that pulses low during the encoder time slot
V_{BB}	1	Negative power supply pin. $V_{BB} = -5\ V \pm 5\%$
V_{CC}	4	Positive power supply pin. $V_{CC} = 5\ V \pm 5\%$
VFRO	3	Analog output of the receive filter
VFXI+	16	Noninverting input of the transmit input amplifier
VFXI–	15	Inverting input of the transmit input amplifier

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Supply voltage, V_{BB} (see Note 1) . . . . . −7 V
Voltage range at any analog input or output . . . . . V_{CC} +0.3 V to V_{BB} −0.3 V
Voltage range at any digital input or output . . . . . V_{CC} +0.3 V to ANLG GND −0.3 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: TP3054B, TP3057B . . . . . 0°C to 70°C
TP13054B, TP13057B . . . . . −40°C to 85°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Supply voltage, V_{BB}		−4.75	−5	−5.25	V
High-level input voltage, V_{IH}		2.2			V
Low-level input voltage, V_{IL}				0.6	V
Common-mode input voltage range, V_{ICR}‡				±2.5	V
Load resistance, GSX, R_L		10			kΩ
Load capacitance, GSX, C_L				50	pF
Operating free-air temperature, T_A	TP3054B, TP3057B	0		70	°C
	TP13054B, TP13057B	−40		85	

‡ Measured with CMRR > 60 dB.

NOTE 2: To avoid possible damage to these CMOS devices and resulting reliability problems, the power-up procedure described in the device power-up sequence paragraphs later in this document should be followed.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

supply current

PARAMETER			TEST CONDITIONS	TP305xB			TP1305xB			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current from V_{CC}	Power down	No load		0.5	1		0.5	1.2	mA
		Active			6	9		6	10	
I_{BB}	Supply current from V_{BB}	Power down	No load		0.5	1		0.5	1.2	mA
		Active			6	9		6	10	

electrical characteristics at V_{CC} = 5 V ±5%, V_{BB} = −5 V ±5%, GND at 0 V, T_A = 25°C (unless otherwise noted)

digital interface

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	DX	I_H = −3.2 mA	2.4		V
V_{OL}	Low-level output voltage	DX	I_L = 3.2 mA		0.4	V
		$\overline{TSX}$	I_L = 3.2 mA, Drain open		0.4	
I_{IH}	High-level input current		$V_I = V_{IH}$ to V_{CC}		±10	µA
I_{IL}	Low-level input current	All digital inputs	V_I = GND to V_{IL}		±10	µA
V_{OL}	Output current in high-impedance state	DX	V_O = GND to V_{CC}		±10	µA

analog interface with transmit amplifier input

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_I	Input current	VFXI+ or VFXI −	V_I = −2.5 V to 2.5 V			±200	nA
r_i	Input resistance	VFXI+ or VFXI −	V_I = −2.5 V to 2.5 V	10			MΩ
r_o	Output resistance		Closed loop, Unity gain		1	3	Ω
	Output dynamic range	GSX	$R_L \geq 10$ kΩ			±2.8	V
A_V	Open-loop voltage amplification	VFXI+ to GSX		5000			
B_I	Unity-gain bandwidth	GSX		1	2		MHz
V_{IO}	Input offset voltage	VFXI+ or VFXI −				±20	mV
CMRR	Common-mode rejection ratio			60			dB
K_{SVR}	Supply-voltage rejection ratio			60			dB

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.

analog interface with receive filter

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output resistance	VFRO			1	3	Ω
Load resistance		VFRO = ±2.5 V	600			Ω
Load capacitance	VFRO to GND				500	pF
Output dc offset voltage	VFRO to GND				±200	mV

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.

operating characteristics, over operating free-air temperature range, V_{CC} = 5 V ±5%, V_{BB} = −5 V ±5%, GND at 0 V, V_I = 1.2276 V, f = 1.02 kHz, transmit input amplifier connected for unity gain, noninverting (unless otherwise noted)

timing requirements

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$f_{clock(M)}$	Frequency of master clock	MCLKX and MCLKR	Depends on the device used and BCLKX/CLKSEL		1.536 1.544 2.048		MHz
$f_{clock(B)}$	Frequency of bit clock, transmit	BCLKX		64		2.048	kHz
t_{w1}	Pulse duration, MCLKX and MCLKR high			160			ns
t_{w2}	Pulse duration, MCLKX and MCLKR low			160			ns
t_{r1}	Rise time of master clock	MCLKX and MCLKR	Measured from 20% to 80%			50	ns
t_{f1}	Fall time of master clock	MCLKX and MCLKR	Measured from 20% to 80%			50	ns
t_{r2}	Rise time of bit clock, transmit	BCLKX	Measured from 20% to 80%			50	ns
t_{f2}	Fall time of bit clock, transmit	BCLKX	Measured from 20% to 80%			50	ns
t_{su1}	Setup time, BCLKX high (and FSX in long-frame sync mode) before MCLKX↓		First bit clock after the leading edge of FSX	100			ns
t_{w3}	Pulse duration, BCLKX and BCLKR high		V_{IH} = 2.2 V	160			ns
t_{w4}	Pulse duration, BCLKX and BCLKR low		V_{IL} = 0.6 V	160			ns
t_{h1}	Hold time, frame sync low after bit clock low (long frame only)			0			ns
t_{h2}	Hold time, BCLKX high after frame sync↑ (short frame only)			0			ns
t_{su2}	Setup time, frame sync high before bit clock↓ (long frame only)			80			ns
t_{d1}	Delay time, BCLKX high to data valid		Load = 150 pF plus 2 LSTTL loads‡	0		140	ns
t_{d2}	Delay time, BCLKX high to $\overline{TSX}$ low		Load = 150 pF plus 2 LSTTL loads‡			140	ns
t_{d3}	Delay time, BCLKX (or 8 clock FSX in long frame only) low to data output disabled			50		165	ns
t_{d4}	Delay time, FSX or BCLKX high to data valid (long frame only)		C_L = 0 pF to 150 pF	20		165	ns
t_{su3}	Setup time, DR valid before BCLKR↓			50			ns
t_{h3}	Hold time, DR valid after BCLKR or BCLKX↓			50			ns
t_{su4}	Setup time, FSR or FSX high before BCLKR or BCLKR↓		Short-frame sync pulse (1 or 2 bit clock periods long) (see Note 3)	50			ns
t_{h4}	Hold time, FSX or FSR high after BCLKX or BCLKR↓		Short-frame sync pulse (1 or 2 bit clock periods long) (see Note 3)	100			ns
t_{h5}	Hold time, frame sync high after bit clock↓		Long-frame sync pulse (from 3 to 8 bit clock periods long)	100			ns
t_{w5}	Minimum pulse duration of the frame sync pulse (low level)		64 kbps operating mode	160			ns

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.
‡ Nominal input value for an LSTTL lead is 18 kΩ.
NOTE 3: For short-frame sync timing, FSR and FSX must go high while their respective bit clocks are high.

filter gains and tracking errors

PARAMETER		TEST CONDITIONS‡	MIN	TYP†	MAX	UNIT
Maximum peak transmit overload level	TP3054B, TP13054B	3.17 dBm0		2.501		V
	TP3057B, TP13057B	3.14 dBm0		2.492		
Transmit filter gain, absolute (at 0 dBm0)		T_A = 25°C	−0.15		0.15	dB
Transmit filter gain, relative to absolute		f = 16 Hz			−40	dB
		f = 50 Hz			−30	
		f = 60 Hz			−26	
		f = 200 Hz	−1.8		−0.1	
		f = 300 Hz to 3000 Hz	−0.15		0.15	
		f = 3300 Hz	−0.35		0.05	
		f = 3400 Hz	−0.8		0	
		f = 4000 Hz			−14	
		f ≥ 4600 Hz (measure response from 0 Hz to 4000 Hz)			−32	
Absolute transmit gain variation with temperature and supply voltage		Relative to absolute transmit gain See Note 4	−0.1		0.1	dB
Transmit gain tracking error with level		Sinusoidal test method, Reference level = −10 dBm0				dB
		3 dBm0 ≥ input level ≥ −40 dBm0			±0.2	
		−40 dBm0 > input level ≥ −50 dBm0			±0.4	
		−50 dBm0 > input level ≥ −55 dBm0			±0.8	
Receive filter gain, absolute (at 0 dBm0)		Input is digital code sequence for 0 dBm0 signal, T_A = 25°C	−0.15		0.15	dB
Receive filter gain, relative to absolute		f = 0 Hz to 3000 Hz, T_A = 25°C	−0.15		0.15	dB
		f = 3300 Hz	−0.35		0.05	
		f = 3400 Hz	−0.8		0	
		f = 4000 Hz			−14	
Absolute receive gain variation with temperature and supply voltage		T_A = full range, See Note 4	−0.1		0.1	dB
Receive gain tracking error with level		Sinusoidal test method; reference input PCM code corresponds to an ideally encoded −10 dBm0 signal				dB
		3 dBm0 ≥ input level ≥ −40 dBm0			±0.2	
		−40 dBm0 > input level ≥ −50 dBm0			±0.4	
		−50 dBm0 > input level ≥ −55 dBm0			±0.8	
Receive output drive voltage		R_L = 10 kΩ			±2.5	V
Transmit and receive gain tracking error with level (A-law, CCITT C 712)		Pseudo noise test method; reference input PCM code corresponds to an ideally encoded −10 dBm0 signal				dB
		3 dBm0 ≥ input level ≥ −40 dBm0			±0.25	
		−40 dBm0 > input level ≥ −50 dBm0			±0.3	
		−50 dBm0 > input level ≥ −55 dBm0			±0.45	

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.
‡ Absolute rms signal levels are defined as follows: V_I = 1.2276 V = 0 dBm0 = 4 dBm at f = 1.02 kHz with R_L = 600 Ω.
NOTE 4: Full range for the TP3054B and TP3057B is 0°C to 70°C. Full range for the TP13054B and TP13057B is −40°C to 85°C.

envelope delay distortion with frequency

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit delay, absolute (at 0 dBm0)	f = 1600 Hz		290	315	µs
Transmit delay, relative to absolute	f = 500 Hz to 600 Hz		195	220	µs
	f = 600 Hz to 800 Hz		120	145	
	f = 800 Hz to 1000 Hz		50	75	
	f = 1000 Hz to 1600 Hz		20	40	
	f = 1600 Hz to 2600 Hz		55	75	
	f = 2600 Hz to 2800 Hz		80	105	
	f = 2800 Hz to 3000 Hz		130	155	
Receive delay, absolute (at 0 dBm0)	f = 1600 Hz		180	200	µs
Receive delay, relative to absolute	f = 500 Hz to 1000 Hz	−40	−25		µs
	f = 1000 Hz to 1600 Hz	−30	−20		
	f = 1600 Hz to 2600 Hz		70	90	
	f = 2600 Hz to 2800 Hz		100	125	
	f = 2800 Hz to 3000 Hz		140	175	

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.

noise

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit noise, C-message weighted‡	TP3054B, TP13054B	VFXI = 0 V		5	9	dBrnC0
Transmit noise, psophometric weighted (see Note 5)	TP3057B, TP13057B	VFXI = 0 V		−74	−69	dBm0p
Receive noise, C-message weighted	TP3054B, TP13054B	PCM code equals alternating positive and negative zero		2	4	dBrnC0
Receive noise, psophometric weighted	TP3057B, TP13057B	PCM code equals positive zero		−86	−83	dBm0p
Noise, single frequency		VFXI+ = 0 V, f = 0 kHz to 100 kHz, Loop-around measurement			−53	dBm0

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.
‡ This parameter is achieved through use of patented circuitry and is not recommended for applications in which the composite signals on the transmit side are below −55 dBm0.
NOTE 5: Measured by extrapolation from the distortion test result.

power supply rejection

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
Positive power-supply rejection, transmit	V_{CC} = 5 V + 100 mVrms, VFXI+ = −50 dBm0	f = 0 Hz to 4 kHz	A-law	38		dB
			μ-law	38		dBC†
		f = 4 kHz to 50 kHz		40		dB
Negative power-supply rejection, transmit	V_{BB} = −5 V + 100 mVrms, VFXI+ = −50 dBm0	f = 0 Hz to 4 kHz	A-law	35		dB
			μ-law	35		dBC†
		f = 4 kHz to 50 kHz		40		dB
Positive power-supply rejection, receive	PCM code equals positive zero, V_{CC} = 5 V + 100 mVrms	f = 0 Hz to 4 kHz	A-law	40		dB
			μ-law	40		dBC†
		f = 4 kHz to 50 kHz		40		dB
Negative power-supply rejection, receive	PCM code equals positive zero, V_{BB} = −5 V + 100 mVrms	f = 0 Hz to 4 kHz	A-law	38		dB
			μ-law	38		dBC†
		f = 4 kHz to 50 kHz		40		dB
Spurious out-of-band signals at the channel output (VFRO)	0 dBm0, 300-Hz to 3400-Hz input applied to DR (measure individual image signals at VFRO)				−30	dB
	f = 4600 Hz to 7600 Hz				−33	dB
	f = 7600 Hz to 100 kHz				−40	

† The unit dBC applies to C-message weighting.

distortion

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Signal-to-distortion ratio, transmit or receive half-channel‡	Level = 3 dBm0		33		dBC†
	Level = 0 dBm0 to −30 dBm0		36		
	Level = −40 dBm0	Transmit	29		
		Receive	30		
	Level = −55 dBm0	Transmit	14		
		Receive	15		
Single-frequency distortion products, transmit				−46	dB
Single-frequency distortion products, receive				−46	dB
Intermodulation distortion	Loop-around measurement, VFXI+ = −4 dBm0 to −21 dBm0, Two frequencies in the range of 300 Hz to 3400 Hz			−41	dB
Signal-to-distortion ratio, transmit half-channel (A-law) (CCITT G.714)§	Level = −3 dBm0		33		dB
	Level = −6 dBm0 to −27 dBm0		36		
	Level = −34 dBm0		33.5		
	Level = −40 dBm0		28.5		
	Level = −55 dBm0		13.5		
Signal-to-distortion ratio, receive half-channel (A-law) (CCITT G.714)§	Level = −3 dBm0		33		dB
	Level = −6 dBm0 to −27 dBm0		36		
	Level = −34 dBm0		34.2		
	Level = −40 dBm0		30		
	Level = −55 dBm0		15		

† The unit dBC applies to C-message weighting.
‡ Sinusoidal test method (see Note 6)
§ Pseudo-noise test method
NOTE 6: The TP3054B and TP13054B are measured using a C-message filter. The TP3057B and the TP13057B are measured using a psophometric weighted filter.

crosstalk

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Crosstalk, transmit-to-receive	f = 300 Hz to 3000 Hz,	DR at steady PCM code		−90	−75	dB
Crosstalk, receive-to-transmit (see Note 7)	VFXI = 0 V,	f = 300 Hz to 3000 Hz		−90	−75	dB

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.
NOTE 7: Receive-to-transmit crosstalk is measured with a – 50 dBm0 activation signal applied at VFXI+.

PARAMETER MEASUREMENT INFORMATION

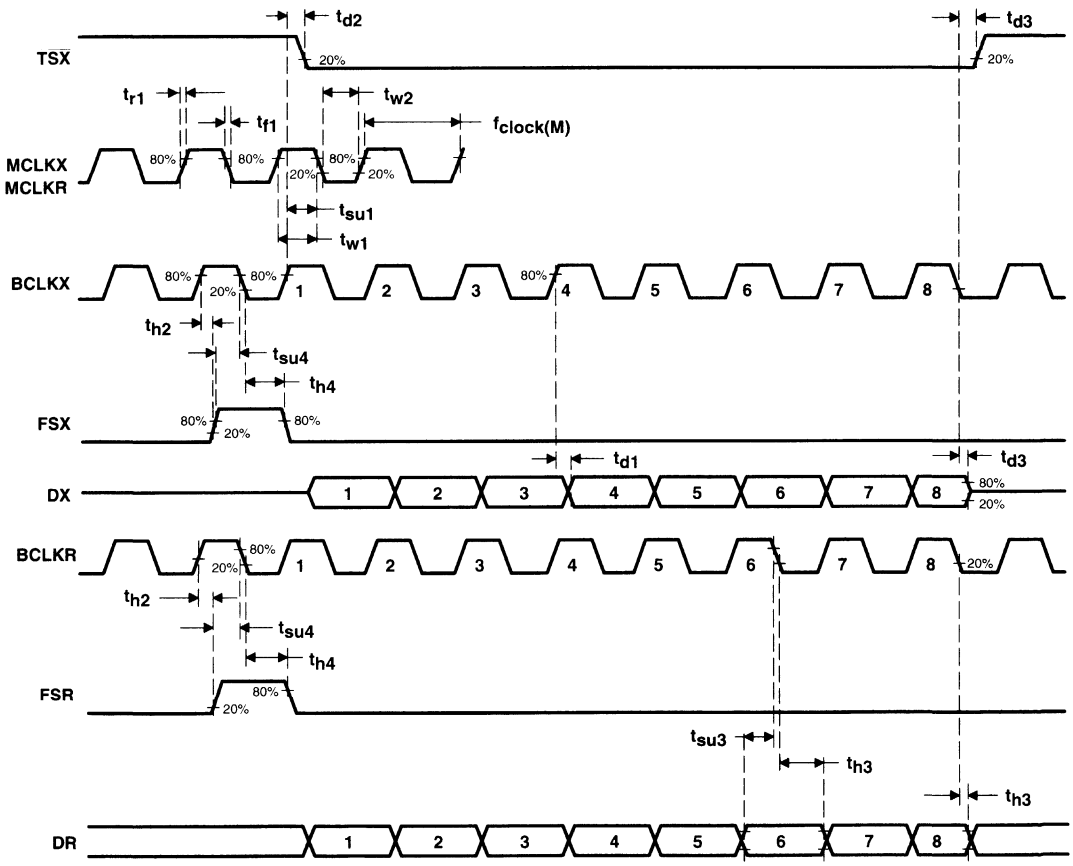


Figure 1. Short-Frame Sync Timing

PARAMETER MEASUREMENT INFORMATION

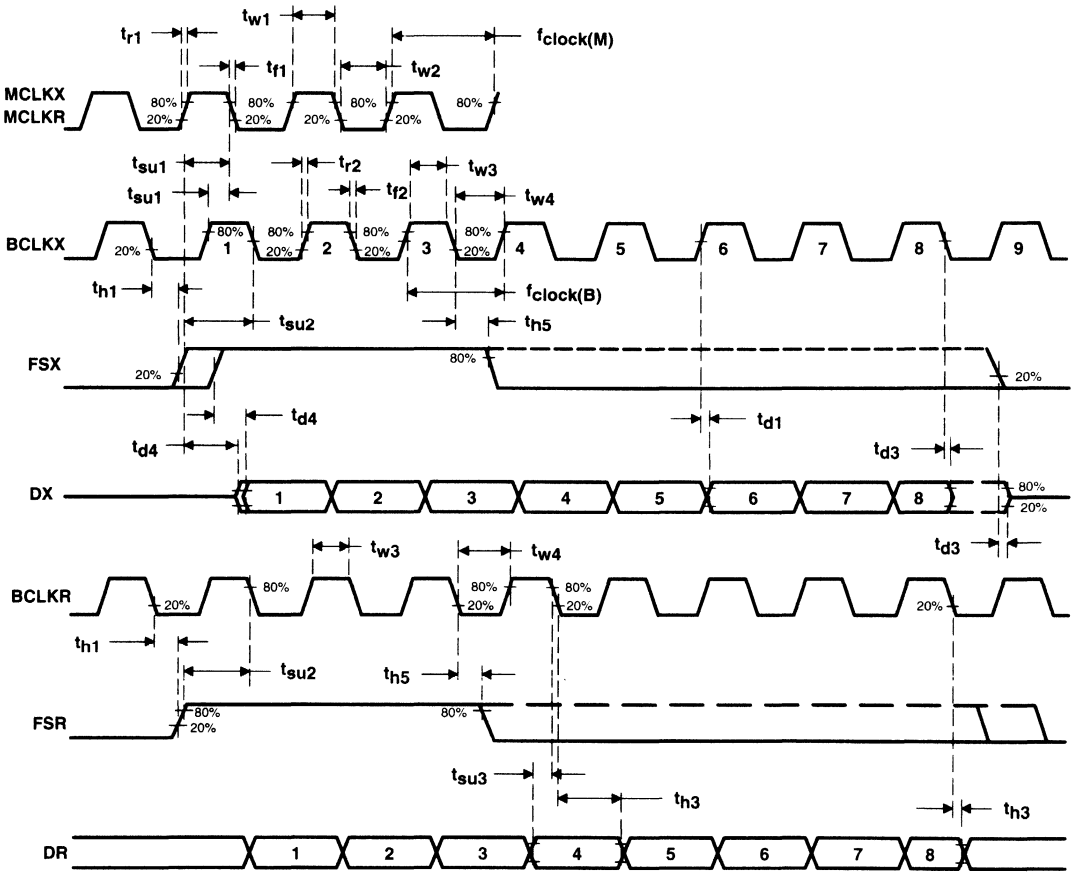


Figure 2. Long-Frame Sync Timing

PRINCIPLES OF OPERATION

system reliability and design considerations

TP305xB, TP1305xB system reliability and design considerations are described in the following paragraphs.

latch-up

Latch-up is possible in all CMOS devices. It is caused by the firing of a parasitic SCR that is present due to the inherent nature of CMOS. When a latch-up occurs, the device draws excessive amounts of current and will continue to draw heavy current until power is removed. Latch-up can result in permanent damage to the device if supply current to the device is not limited.

Even though the TP305xB and TP1305xB devices are heavily protected against latch-up, it is still possible to cause latch-up under certain conditions in which excess current is forced into or out of one or more terminals. Latch-up can occur when the positive supply voltage drops momentarily below ground, when the negative supply voltage rises momentarily above ground, or possibly if a signal is applied to a terminal after power has been applied but before the ground is connected. This can happen if the device is hot-inserted into a card with the power applied, or if the device is mounted on a card that has an edge connector and the card is hot-inserted into a system with the power on.

To help ensure that latch-up does not occur, it is considered good design practice to connect a reverse-biased Schottky diode (with a forward voltage drop of less than or equal to 0.4 V – 1N5711 or equivalent) between the power supply and GND (see Figure 3). If it is possible that a TP305xB- or TP1305xB-equipped card that has an edge connector could be hot-inserted into a powered-up system, it is also important to ensure that the ground edge connector traces are longer than the power and signal traces so that the card ground is always the first to make contact.

device power-up sequence

Latch-up can also occur if a signal source is connected without the device being properly grounded. A signal applied to one terminal could then find a ground through another signal terminal on the device. To ensure proper operation of the device and as a safeguard against this sort of latch-up, it is recommended that the following power-up sequence always be used:

1. Ensure that no signals are applied to the device before the power-up sequence is complete.
2. Connect GND.
3. Apply V_{BB} (most negative voltage).
4. Apply V_{CC} (most positive voltage).
5. Force a power down condition in the device.
6. Connect clocks.
7. Release the power down condition.
8. Apply FS synchronization pulses.
9. Apply the signal inputs.

When powering down the device, this procedure should be followed in the reverse order.

PRINCIPLES OF OPERATION

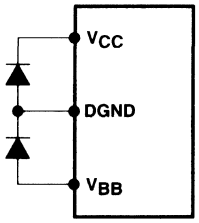


Figure 3. Latch-Up Protection Diode Connection

internal sequencing

Power-on reset circuitry initializes the TP3054B, TP3057B, TP13054B, and TP13057B devices when power is first applied, placing it into the power-down mode. DX and VFRO outputs go into high-impedance states and all nonessential circuitry is disabled. A low level or clock applied to MCLKR/PDN powers up the device and activates all circuits. DX, a 3-state PCM data output, remains in the high-impedance state until the arrival of the second FSX pulse.

synchronous operation

For synchronous operation, a clock is applied to MCLKX. MCLKR/PDN is used as a power-down control. A low level on MCLKR powers up the device and a high level powers it down. In either case, MCLKX is selected as the master clock for both receive and transmit direction. BCLKX must also have a bit clock applied to it. The selection of the proper internal divider for a master-clock frequency of 1.536 MHz, 1.544 MHz, or 2.048 MHz can be done via BCLKR/CLKSEL. The device automatically compensates for the 193rd clock pulse of each frame.

A fixed level on BCLKR/CLKSEL selects BCLKX as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation that can be selected depending on the state of BCLKR/CLKSEL. In the synchronous mode, BCLKX may be in the range from 64 kHz to 2.048 MHz but must be synchronous with MCLKX.

Table 1. Selection of Master-Clock Frequencies

BCLKR/CLKSEL	MASTER-CLOCK FREQUENCY SELECTED	
	TP13054B, TP3054B	TP13057B, TP3057B
Clock Input	1.536 MHz or 1.544 MHz	2.048 MHz
Logic Input L (sync mode only)	2.048 MHz	1.536 MHz or 1.544 MHz
Logic Input H (open) (sync mode only)	1.536 MHz or 1.544 MHz	2.048 MHz

The encoding cycle begins with each FSX pulse, and the PCM data from the previous cycle is shifted out of the enabled DX output on the rising edge of BCLKX. After eight bit-clock periods, the 3-state DX output is returned to the high-impedance state. With an FSR pulse, PCM data is latched via DR on the falling edge of BCLKX (or BCLKR, if running). FSX and FSR must be synchronous with MCLKX and MCLKR.

PRINCIPLES OF OPERATION

asynchronous operation

For asynchronous operation, separate transmit and receive clocks can be applied. MCLKX and MCLKR must be 2.048 MHz for the TP3057B and TP13057B, 1.536 MHz or 1.544 MHz for the TP3054B and TP13054B and need not be synchronous. However, for best performance, MCLKR should be synchronous with MCLKX. This is easily achieved by applying only static logic levels to MCLKR/PDN. This connects MCLKX to all internal MCLKR functions. For 1.544-MHz operation, the device compensates for the 193rd clock pulse of each frame. Each encoding cycle is started with FSX and FSX must be synchronous with MCLKX and BCLKX. Each decoding cycle is started with FSR and FSR must be synchronous with BCLKR. The logic levels shown in Table 1 are not valid in the asynchronous mode. BCLKX and BCLKR can operate from 64 kHz to 2.048 MHz.

short-frame sync operation

The device can operate with either a short- or a long-frame sync pulse. On power up, the device automatically goes into the short-frame mode where both FSX and FSR must be one bit-clock period long with timing relationships specified in Figure 1. With FSX high during a falling edge of BCLKX, the next rising edge of BCLKX enables the 3-state output buffer, DX, which outputs the sign bits. The remaining seven bits are clocked out on the following seven rising edges and the next falling edge disables DX. With FSR high during a falling edge of BCLKR (BCLKX in synchronous mode), the next falling edge of BCLKR latches in the sign bit. The following seven falling edges latch in the seven remaining bits. The short-frame sync pulse may be utilized in either the synchronous or asynchronous mode.

long-frame sync operation

Both FSX and FSR must be three or more bit-clock periods long to use the long-frame sync mode with timing relationships as shown in Figure 2. Using the transmit frame sync (FSX), the device detects whether a short- or long-frame sync pulse is being used. For 64-kHz operation, the frame-sync pulse must be kept low for a minimum of 160 ns. The rising edge of FSX or BCLKX, which ever occurs later, enables the DX 3-state output buffer. The first bit clocked out is the sign bit. The next seven rising edges of BCLKX edges clock out the remaining seven bits. The falling edge of BCLKX following the eighth rising edge or FSX going low, whichever occurs later, disables DX. A rising edge on FSR, the receive-frame sync pulse, causes the PCM data at DR to be latched in on the next eight falling edges of BCLKR (BCLKX in synchronous mode). The long-frame sync pulse can be utilized in either the synchronous or asynchronous mode.

transmit section

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors. The low noise and wide bandwidth characteristics of these devices provide gains in excess of 20 dB across the audio passband. The operational amplifier drives a unity-gain filter consisting of an RC active prefilter followed by an eighth-order switched-capacitor band-pass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. As per μ-law (TP3054B and TP13054B) or A-law (TP3057B and TP13057B) coding conventions, the ADC is a companding type. A precision voltage reference provides a nominal input overload of 2.5 V peak. The sampling of the filter output is controlled by the FSX frame-sync pulse. Then the successive-approximation encoding cycle begins. The 8-bit code is loaded into a buffer and shifted out through DX at the next FSX pulse. The total encoding delay is approximately 290 μs. Any offset voltage due to the filters or comparator is cancelled by sign-bit integration.

PRINCIPLES OF OPERATION

receive section

The receive section consists of an expanding DAC that drives a fifth-order low-pass filter clocked at 256 kHz. The decoder is μ-law (TP3054B and TP13054B) or A-law (TP3057B and TP13057B) and the fifth-order low-pass filter corrects for the (sin x)/x attenuation caused by the 8-kHz sample/hold. The filter is followed by a second-order RC active post-filter/power amplifier capable of driving a 600-Ω load to a level of 7.2 dBm. The receive section is unity gain. At FSR, the data at DR is clocked in on the falling edge of the next eight BCLKR (BCLKX) periods. At the end of the decoder time slot, the decoding cycle begins and 10 μs later, the decoder DAC output is updated. The decoder delay is about 10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (1/2 frame), or a total of approximately 180 μs.

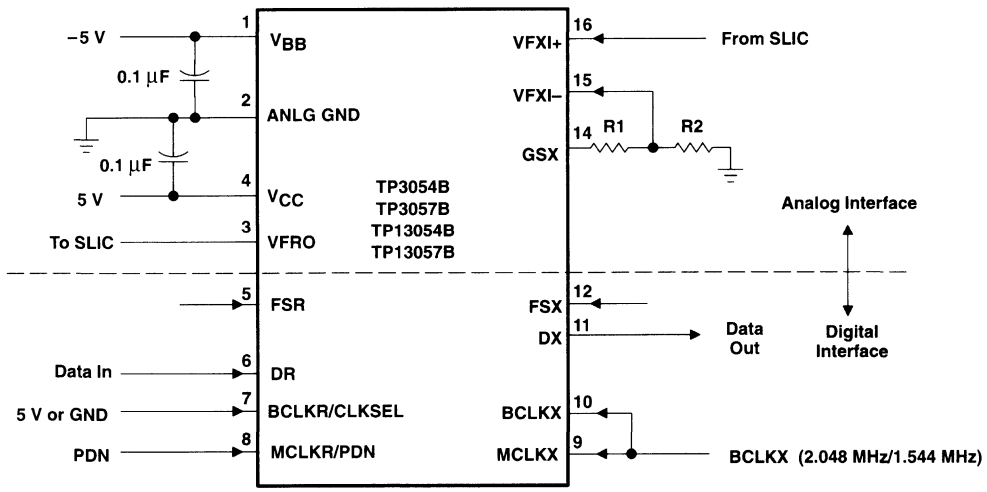
APPLICATION INFORMATION

power supplies

While the pins of the TP1305xB and TP305xB families are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed-circuit board can be plugged into a hot socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to ANLG GND. This minimizes the interaction of ground return currents flowing through a common bus impedance. V_{CC} and V_{BB} supplies should be decoupled by connecting 0.1-µF decoupling capacitors to this common point. These bypass capacitors must be connected as close as possible to V_{CC} and V_{BB}.

For best performance, the ground point of each codec/filter on a card should be connected to a common card ground in star formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10-µF capacitors.



NOTE A: Transmit gain = 20 log $\left(\frac{R1 + R2}{R2}\right)$, $(R1 + R2) \geq 10\ k\Omega$

Figure 4. Typical Synchronous Application

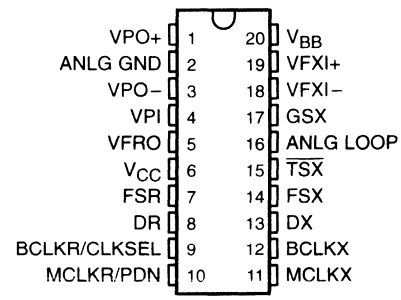
- **Complete PCM Codec and Filtering Systems Include:**
  - **Transmit High-Pass and Low-Pass Filtering**
  - **Receive Low-Pass Filter With (sin x)/x Correction**
  - **Active RC Noise Filters**
  - **μ-Law or A-Law Compatible Coder and Decoder**
  - **Internal Precision Voltage Reference**
  - **Serial I/O Interface**
  - **Internal Autozero Circuitry**
- **μ-Law – TP3064B and TP13064B**
- **A-Law – TP3067B and TP13067B**
- **±5-V Operation**
- **Low Operating Power . . . 70 mW Typ**
- **Power-Down Standby Mode . . . 3 mW Typ**
- **Automatic Power Down**
- **TTL- or CMOS-Compatible Digital Interface**
- **Maximizes Line Interface Card Circuit Density**
- **Improved Versions of National Semiconductor TP3064, TP3067, TP3064-X, TP3067-X**

description

The TP3064A, TP3067A, TP13064A, and TP13067A are comprised of a single-chip PCM codec (pulse-code-modulated encoder and decoder) and PCM line filter. These devices provide all the functions required to interface a full-duplex (2-wire) voice telephone circuit with a TDM (time-division-multiplexed) system. These devices are pin-for-pin compatible with the National Semiconductor TP3064A and TP3067A, respectively. Primary applications include:

- Line interface for digital transmission and switching of T1 carrier, PABX, and central office telephone systems
- Subscriber line concentrators
- Digital-encryption systems
- Digital voice-band data-storage systems
- Digital signal processing

DW OR N PACKAGE
(TOP VIEW)

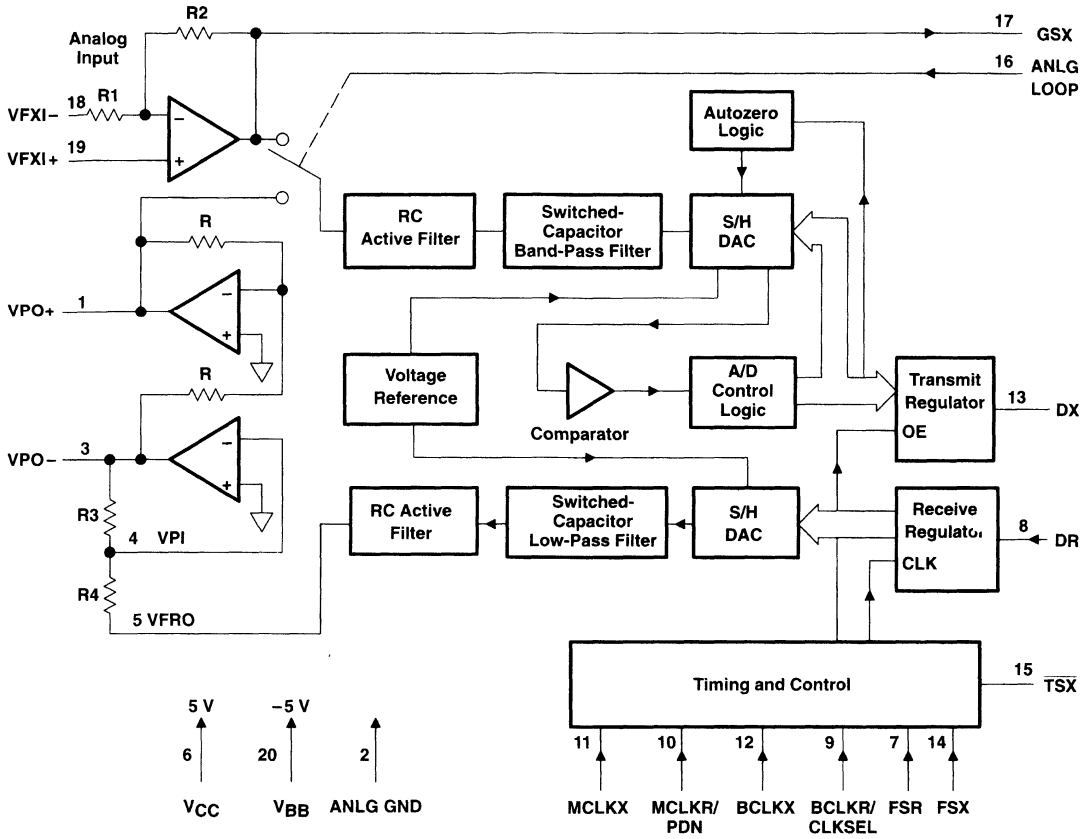


These devices are designed to perform the transmit encoding (A/D conversion) and receive decoding (D/A conversion) as well as the transmit and receive filtering functions in a PCM system. They are intended to be used at the analog termination of a PCM line or trunk. The devices require two transmit and receive master clocks that may be asynchronous (1.536 MHz, 1.544 MHz, or 2.048 MHz), transmit and receive data clocks that are synchronous with the master clock (but can vary from 64 kHz to 2.048 MHz), and transmit and receive frame-sync pulses. The TP3064A, TP3067A, TP13064A, and TP13067A provide the band-pass filtering of the analog signals prior to encoding and after decoding of voice and call progress tones. The TP3067A and TP13067A contain patented circuitry to achieve low transmit channel idle noise and are not recommended for applications in which the composite signals on the transmit side are below –55 dBm0.

The TP3064A and TP3067A are characterized for operation from 0°C to 70°C. The TP13064A and TP13067A are characterized for operation from –40°C to 85°C.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the CMOS gates.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
ANLG GND	2	Analog ground. All signals are referenced to ANLG GND.
ANLG LOOP	16	Analog loopback control input. Must be set to logic low for normal operation. When pulled to logic high, the transmit filter input is disconnected from the output of the transmit preamplifier and connected to VPO+ of the receive power amplifier.
BCLKR/CLKSEL	9	The bit clock that shifts data into DR after the FSR leading edge. May vary from 64 kHz to 2.048 MHz. Alternately, can be a logic input that selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode. BCLKX is used for both transmit and receive directions (see Table 1).
BCLKX	12	The bit clock that shifts out the PCM data on DX. BCLKX can vary from 64 kHz to 2.048 MHz, but must be synchronous with MCLKX.
DR	8	Receive data input. PCM data is shifted into DR following the FSR leading edge.
DX	13	The 3-state PCM data output that is enabled by FSX.
FSR	7	Receive frame sync pulse input that enables BCLKR to shift PCM data in DR. FSR is an 8-kHz pulse train (see Figures 1 and 2 for timing details).
FSX	14	Transmit frame sync pulse that enables BCLKX to shift out the PCM data on DX. FSX is an 8-kHz pulse train (see Figures 1 and 2 for timing details).
GSX	17	Analog output of the transmit input amplifier. GSX is used to externally set gain.
MCLKR/PDN	10	Receive master clock (must be 1.536 MHz, 1.544 MHz, or 2.048 MHz). May be synchronous with MCLKX, but should be synchronous for best performance. When MCLKR is connected continuously low, MCLKX is selected for all internal timing. When MCLKR is connected continuously high, the device is powered down.
MCLKX	11	Transmit master clock (must be 1.536 MHz, 1.544 MHz, or 2.048 MHz). May be asynchronous with MCLKR
$\overline{TSX}$	15	Open-drain output that pulses low during the encoder time slot
V_{BB}	20	Negative power supply. $V_{BB} = -5\ V \pm 5\%$
V_{CC}	6	Positive power supply. $V_{CC} = 5\ V \pm 5\%$
VFRO	5	Analog output of the receive filter
VFXI+	19	Noninverting input of the transmit input amplifier
VFXI–	18	Inverting input of the transmit input amplifier
VPI	4	Inverting input to the receive power amplifier. Also powers down both amplifiers when connected to V_{BB}
VPO+	1	The noninverted output of the receive power amplifier
VPO–	3	The inverted output of the receive power amplifier

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Supply voltage, V_{BB} (see Note 1) ..... −7 V
Voltage range at any analog input or output ..... V_{CC} + 0.3 V to V_{BB} − 0.3 V
Voltage range at any digital input or output ..... V_{CC} + 0.3 V to GND − 0.3 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: TP3064A, TP3067A ..... 0°C to 70°C
TP13064A, TP13067A ..... −40°C to 85°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Supply voltage, V_{BB}		−4.75	−5	−5.25	V
High-level input voltage, V_{IH}		2.2			V
Low-level input voltage, V_{IL}				0.6	V
Common-mode input voltage range, V_{ICR}‡				±2.5	V
Load resistance at GSX, R_L		10			kΩ
Load capacitance at GSX, C_L				50	pF
Operating free-air temperature, T_A	TP3064A, TP3067A	0		70	°C
	TP13064A, TP13067A	−40		85	

‡ Measure with CMRR > 60 dB.

NOTE 2: To avoid possible damage to these CMOS devices and resulting reliability problems, the power-up procedure described in the device power-up sequence paragraphs later in this document should be followed.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

supply current

PARAMETER			TEST CONDITIONS	TP306xA			TP1306xA			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{CC}	Supply current from V_{CC}	Power down	No load		0.5	1		0.5	1.2	mA
		Active			6	10		6	11	
I_{BB}	Supply current from V_{BB}	Power down	No load		0.5	1		0.5	1.2	mA
		Active			6	10		6	11	

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.

electrical characteristics at V_{CC} = 5 V ± 5%, V_{BB} = −5 V ± 5%, GND at 0 V, T_A = 25°C (unless otherwise noted)

digital interface

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	DX	I_H = −3.2 mA	2.4		V
V_{OL}	Low-level output voltage	DX	I_L = 3.2 mA		0.4	V
		$\overline{TSX}$	I_L = 3.2 mA, Drain open		0.4	
I_{IH}	High-level input current		$V_I = V_{IH}$ to V_{CC}		±10	µA
I_{IL}	Low-level input current	All digital inputs	V_I = GND to V_{IL}		±10	µA
I_{OZ}	Output current in high-impedance state	DX	V_O = GND to V_{CC}		±10	µA

analog interface with transmit amplifier input

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_I	Input current	VFXI+ or VFXI−	V_I = −2.5 V to 2.5 V			+200	nA
r_i	Input resistance	VFXI+ or VFXI−	V_I = −2.5 V to 2.5 V	10			MΩ
r_o	Output resistance		Closed loop, Unit gain		1	3	Ω
	Output dynamic range	GSX	$R_L \geq 10$ kΩ			±2.8	V
A_V	Open-loop voltage amplification	VFXI+ to GSX		5000			
B_I	Unity-gain bandwidth	GSX			1	2	MHz
V_{IO}	Input offset voltage	VFXI+ or VFXI−				±20	mV
CMRR	Common-mode rejection ratio			60			dB
k_{SVR}	Supply-voltage rejection ratio			60			dB

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.

analog interface with receive filter

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output resistance	VFRO			1	3	Ω
Load resistance		VFRO = ±2.5 V	600			Ω
Load capacitance	VFRO to GND				500	pF
Output dc offset voltage	VFRO to GND				±200	mV

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.

analog interface with power amplifiers

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_I	Input current		VPI = –1 V to 1 V				±100	nA
r_i	Input resistance		VPI = –1 V to 1 V		10			MΩ
r_o	Output resistance	VPO+ or VPO–	Inverting unity gain			1		Ω
A_V	Voltage amplification	VPO– or VPO+	VPO– = 1.77 Vrms, R_L = 600 Ω			–1		
B_I	Unity-gain bandwidth	VPO–	Open loop			400		kHz
V_{IO}	Input offset voltage						±25	mV
k_{SVR}	Supply-voltage rejection ratio of V_{CC} or V_{BB}		VPO– connected to VPI	0 kHz to 4 kHz	60			dB
				4 kHz to 50 kHz	36			
R_L	Load resistance		Connected from VPO+ to VPO–		600			Ω
C_L	Load capacitance						100	pF

† All typical values are at V_{CC} = 5 V, V_{BB} = –5 V, and T_A = 25°C.

operating characteristics, over operating free-air temperature range V_{CC} = 5 V ± 5%, V_{BB} = −5 V ± 5%, GND at 0 V, V_I = 1.2276 V, f = 1.02 kHz, transmit input amplifier connected for unity gain, noninverting (unless otherwise noted)

timing requirements

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$f_{clock(M)}$	Frequency of master clock	MCLX and MCLKR	Depends on the device used and BCLKX/CLKSEL		1.536 1.544 2.048		MHz
$f_{clock(B)}$	Frequency of bit clock, transmit	BCLKX		64		2.048	MHz
t_{r1}	Rise time of master clock	MCLKX and MCLKR	Measured from 20% to 80%			50	ns
t_{f1}	Fall time of master clock	MCLKX and MCLKR	Measured from 20% to 80%			50	ns
t_{r2}	Rise time of bit clock, transmit	BCLKX	Measured from 20% to 80%			50	ns
t_{f2}	Fall time of bit clock, transmit	BCLKX	Measured from 20% to 80%			50	ns
t_{w1}	Pulse duration, MCLKX and MCLKR high			160			ns
t_{w2}	Pulse duration, MCLKX and MCLKR low			160			ns
t_{su1}	Setup time, BCLKX high (and FSX in long-frame sync mode) before MCLKX↓		First bit clock after the leading edge of FSX	100			ns
t_{w3}	Pulse duration, BCLKX and BCLKR high		V_{IH} = 2.2 V	160			ns
t_{w4}	Pulse duration, BCLKX and BCLKR low		V_{IL} = 0.6 V	160			ns
t_{h1}	Hold time, frame sync low after bit clock low (long frame only)			0			ns
t_{h2}	Hold time, BCLKX high after frame sync↑ (short frame only)			0			ns
t_{su2}	Setup time, frame sync high before bit clock↓ (long frame only)			80			ns
t_{d1}	Delay time, BCLKX high to data valid		Load = 150 pF plus 2 LSTTL loads‡	0		140	ns
t_{d2}	Delay time, BCLKX high to $\overline{TSX}$ low		Load = 150 pF plus 2 LSTTL loads‡			140	ns
t_{d3}	Delay time, BCLKX (or 8 clock FSX in long frame only) low to data output disabled			50		165	ns
t_{d4}	Delay time, FSX or BCLKX high to data valid (long frame only)		C_L = 0 pF to 150 pF	20		165	ns
t_{su3}	Setup time, DR valid before BCLKR↓			50			ns
t_{h3}	Hold time, DR valid after BCLKR or BCLKX↓			50			ns
t_{su4}	Setup time, FSR or FSX high before BCLKR or BCLKX↓		Short-frame sync pulse (1- or 2-bit clock periods long) (see Note 3)	50			ns
t_{h4}	Hold time, FSX or FSR high after BCLKX or BCLKR↓		Short-frame sync pulse (1- or 2-bit clock periods long) (see Note 3)	100			ns
t_{h5}	Hold time, frame sync high after bit clock↓		Long-frame sync pulse (from 3- to 8-bit clock periods long)	100			ns
t_{w5}	Pulse duration of the frame sync pulse (low level)		64 kbps operating mode	160			ns

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.
‡ Nominal input value for an LSTTL load is 18 kΩ.
NOTE 3: For short-frame sync timing, FSR and FSX must go high while their respective bit clocks are high.

filter gains and tracking errors

PARAMETER		TEST CONDITIONS‡	MIN	TYP†	MAX	UNIT
Maximum peak transmit overload level	TP3064A, TP13064A	3.17 dBm0		2.501		V
	TP3067A, TP13067A	3.14 dBm0		2.492		
Transmit filter gain, absolute (at 0 dBm0)		T_A = 25°C	−0.15		0.15	dB
Transmit filter gain, relative to absolute		f = 16 Hz			−40	dB
		f = 50 Hz			−30	
		f = 60 Hz			−26	
		f = 200 Hz	−1.8		−0.1	
		f = 300 Hz to 3000 Hz	−0.15		0.15	
		f = 3300 Hz	−0.35		0.05	
		f = 3400 Hz	−0.8		0	
		f = 4000 Hz			−14	
		f ≥ 4600 Hz (measure response from 0 Hz to 4000 Hz)			−32	
Absolute transmit gain variation with temperature and supply voltage		Relative to absolute transmit gain	−0.1		0.1	dB
Transmit gain tracking error with level		Sinusoidal test method; Reference level = −10 dBm0				dB
		3 dBm0 ≥ input level ≥ −40 dBm0			±0.2	
		−40 dBm0 > input level ≥ −50 dBm0			±0.4	
		−50 dBm0 > input level ≥ −55 dBm0			±0.8	
Receive filter gain, absolute (at 0 dBm0)		Input is digital code sequence for 0 dBm0 signal, T_A = 25°C	−0.15		0.15	dB
Receive filter gain, relative to absolute		f = 0 Hz to 3000 Hz, T_A = 25°C	−0.15		0.15	dB
		f = 3300 Hz	−0.35		0.05	
		f = 3400 Hz	−0.8		0	
		f = 4000 Hz			−14	
Absolute receive gain variation with temperature and supply voltage		T_A = full range, See Note 4	−0.1		0.1	dB
Receive gain tracking error with level		Sinusoidal test method; reference input PCM code corresponds to an ideally encoded −10 dBm0 signal				dB
		3 dBm0 ≥ input level ≥ −40 dBm0			±0.2	
		−40 dBm0 > input level ≥ −50 dBm0			±0.4	
		−50 dBm0 > input level ≥ −55 dBm0			±0.8	
Receive output drive voltage		R_L = 10 kΩ			±2.5	V
Transmit and receive gain tracking error with level (A-law, CCITT C712)		Pseudo-noise-test method; reference input PCM code corresponds to an ideally encoded −10 dBm0 signal				dB
		3 dBm0 ≥ input level ≥ −40 dBm0			±0.25	
		−40 dBm0 > input level ≥ −50 dBm0			±0.3	
		−50 dBm0 > input level ≥ −55 dBm0			±0.45	

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.
‡ Absolute rms signal levels are defined as follows: V_I = 1.2276 V = 0 dBm0 = 4 dBm at f = 1.02 kHz with R_L = 600 Ω.
NOTE 4: Full range for the TP3064A and TP3067A is 0°C to 70°C. Full range for the TP13064A and TP13067A is −40°C to 85°C.

envelope delay distortion with frequency

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit delay, absolute (at 0 dBm0)	f = 1600 Hz		290	315	µs
Transmit filter gain, relative to absolute	f = 500 Hz to 600 Hz		195	220	µs
	f = 600 Hz to 800 Hz		120	145	
	f = 800 Hz to 1000 Hz		50	75	
	f = 1000 Hz to 1600 Hz		20	40	
	f = 1600 Hz to 2600 Hz		55	75	
	f = 2600 Hz to 2800 Hz		80	105	
	f = 2800 Hz to 3000 Hz		130	155	
Receive delay, absolute (at 0 dBm0)	f = 1600 Hz		180	200	µs
Receive delay, relative to absolute	f = 500 Hz to 1000 Hz	–40	–25		µs
	f = 1000 Hz to 1600 Hz	–30	–20		
	f = 1600 Hz to 2600 Hz		70	90	
	f = 2600 Hz to 2800 Hz		100	125	
	f = 2800 Hz to 3000 Hz		140	175	

† All typical values are at V_{CC} = 5 V, V_{BB} = –5 V, and T_A = 25°C.

noise

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit noise, C-message weighted	TP3064A, TP13064A	V_{FXI} = 0 V		9	14	dBrnC0
Transmit noise, psophometric weighted (see Note 5)	TP3067A, TP13067A	V_{FXI} = 0 V		–78	–75	dBm0p
Receive noise, C-message weighted	TP3064A, TP13064A	PCM code equals alternating positive and negative zero		2	4	dBrnC0
Receive noise, psophometric weighted	TP3067A, TP13067A	PCM code equals positive zero		–86	–83	dBm0p
Noise, single frequency		VFXI+ = 0 V, f = 0 kHz to 100 kHz, Loop-around measurement			–53	dBm0

† All typical values are at V_{CC} = 5 V, V_{BB} = –5 V, and T_A = 25°C.

NOTE 5: Measured by extrapolation from the distortion test result. This parameter is achieved through use of patented circuitry and is not recommended for applications in which the composite signals on the transmit side are below –55 dBm0.

power supply rejection

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
Positive power-supply rejection, transmit	V_{CC} = 5 V + 100 mVrms, VFXI+ = −50 dBm0	f = 0 Hz to 4 kHz	A-law	38		dB
			μ-law	38		dBC†
		f = 4 kHz to 50 kHz		40		dB
Negative power-supply rejection, transmit	V_{BB} = −5 V + 100 mVrms, VFXI+ = −50 dBm0	f = 0 Hz to 4 kHz	A-law	35		dB
			μ-law	35		dBC†
		f = 4 kHz to 50 kHz		40		dB
Positive power-supply rejection, receive	PCM code equals positive zero, V_{CC} = 5 V + 100 mVrms	f = 0 Hz to 4 kHz	A-law	40		dB
			μ-law	40		dBC†
		f = 4 kHz to 50 kHz		40		dB
Negative power-supply rejection, receive	PCM code equals positive zero, V_{BB} = −5 V + 100 mVrms	f = 0 Hz to 4 kHz	A-law	38		dB
			μ-law	38		dBC†
		f = 4 kHz to 50 kHz		40		dB
Spurious out-of-band signals at the channel output (VFRO)	0 dBm0, 300-Hz to 3400-Hz input applied to DR (measure individual image signals at VFRO)				−30	dB
	f = 4600 Hz to 7600 Hz				−33	dB
	f = 7600 Hz to 100 kHz				−40	

† The unit dBC applies to C-message weighting.

distortion

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Signal-to-distortion ratio, transmit or receive half-channel‡	Level = 3 dBm0		33		dBC†
	Level = 0 dBm0 to −30 dBm0		36		
	Level = −40 dBm0	Transmit	29		
		Receive	30		
	Level = −55 dBm0	Transmit	14		
		Receive	15		
Single-frequency distortion products, transmit				−46	dB
Single-frequency distortion products, receive				−46	dB
Intermodulation distortion	Loop-around measurement, VFXI+ = −4 dBm0 to −21 dBm0, Two frequencies in the range of 300 Hz to 3400 Hz			−41	dB
Signal-to-distortion ratio, transmit half-channel (A-Law) (CCITT G.714)§	Pseudo noise test method				
	Level = −3 dBm0		33		dB
	Level = −6 dBm0 to −27 dBm0		36		
	Level = −34 dBm0		33.5		
	Level = −40 dBm0		28.5		
	Level = −55 dBm0		13.5		
Signal-to-distortion ratio, receive half-channel (A-law) (CCITT G.714)§	Level = −3 dBm0		33		dB
	Level = −6 dBm0 to −27 dBm0		36		
	Level = −34 dBm0		34.2		
	Level = −40 dBm0		30		
	Level = −55 dBm0		15		

† The unit dBC applies to C-message weighting.
‡ Sinusoidal test method (see Note 6)
§ Pseudo-noise test method
NOTE 6: The TP13064A and TP3064A are measured using a C-message filter. The TP13067A and TP3067A are measured using a psophometric weighted filter.

crosstalk

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Crosstalk, transmit to receive	f = 300 Hz to 3000 Hz, DR at steady PCM code		–90	–75	dB
Crosstalk, receive to transmit (see Note 7)	VFXI = 0 V, f = 300 Hz to 3000 Hz		–90	–72	dB

† All typical values are at V_{CC} = 5 V, V_{BB} = –5 V, and T_A = 25°C.
NOTE 7: Receive-to-transmit crosstalk is measured with a –50 dBm0 activation signal applied to VFXI+.

power amplifiers

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Maximum 0 dBm0 rms level for better than ±0.1 dB linearity over the range if –10 dBm0 to 3 dBm0	Balanced load, R_L connected between VPO+ and VPO –			
	R_L = 600 Ω	3.3		V_{rms}
	R_L = 1200 Ω	3.5		
	R_L = 30 kΩ	4		
Signal/distortion	R_L = 600 Ω	50		dB

PARAMETER MEASUREMENT INFORMATION

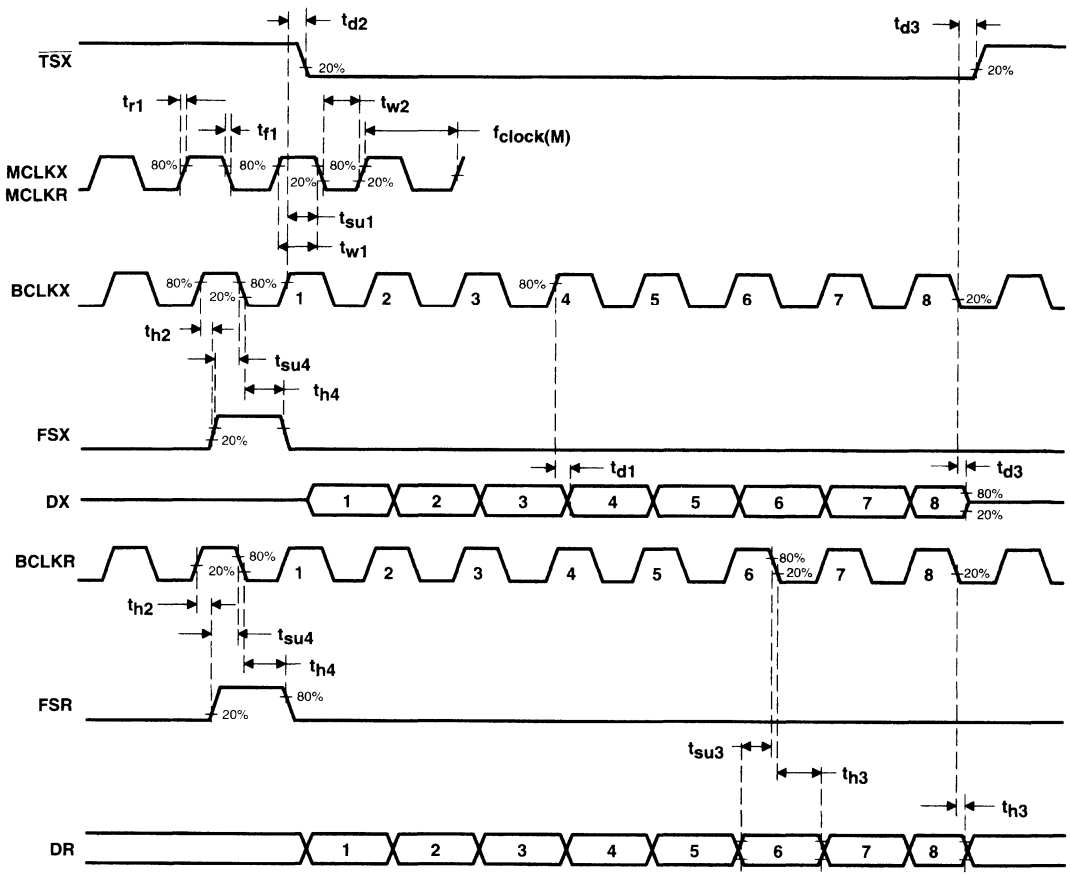


Figure 1. Short-Frame Sync Timing

PARAMETER MEASUREMENT INFORMATION

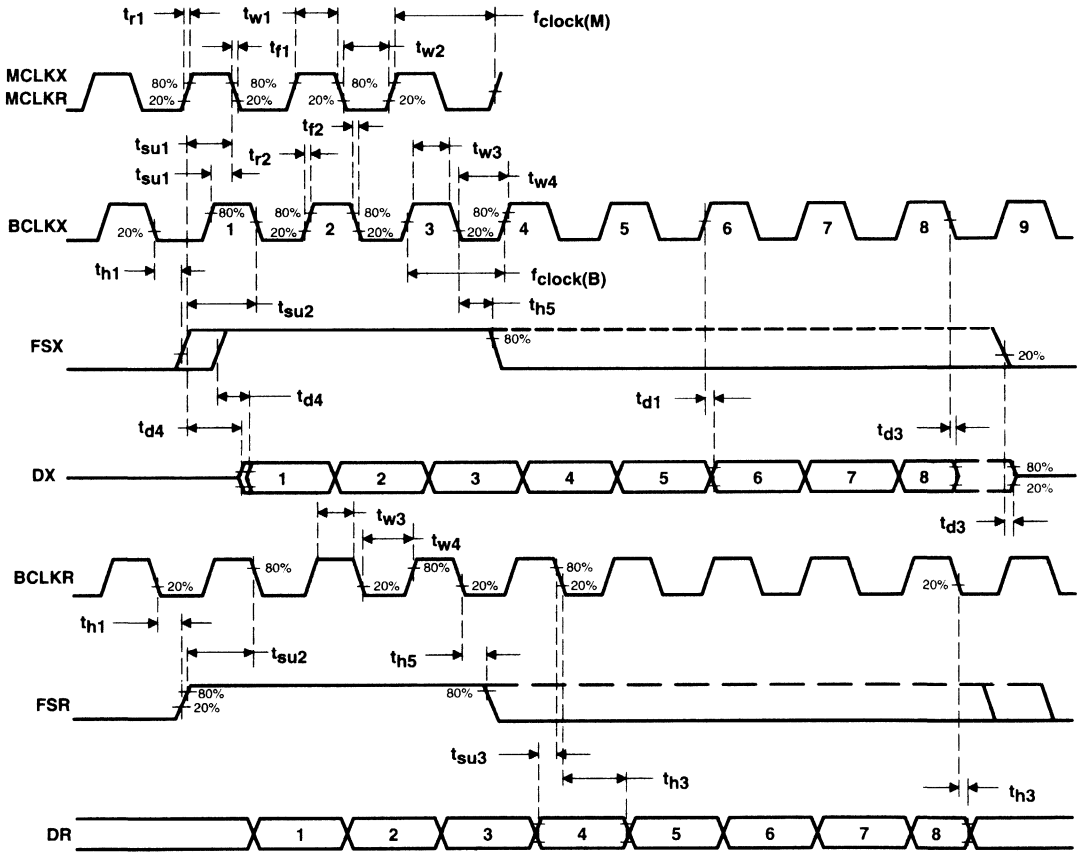


Figure 2. Long-Frame Sync Timing

PRINCIPLES OF OPERATION

system reliability and design considerations

TP306xA, TP1306xA system reliability and design considerations are described in the following paragraphs.

latch-up

Latch-up is possible in all CMOS devices. It is caused by the firing of a parasitic SCR that is present due to the inherent nature of CMOS. When a latch-up occurs, the device draws excessive amounts of current and will continue to draw heavy current until power is removed. Latch-up can result in permanent damage to the device if supply current to the device is not limited.

Even though the TP306xA and TP1306xA devices are heavily protected against latch-up, it is still possible to cause latch-up under certain conditions in which excess current is forced into or out of one or more terminals. Latch-up can occur when the positive supply voltage drops momentarily below ground, when the negative supply voltage rises momentarily above ground, or possibly if a signal is applied to a terminal after power has been applied but before the ground is connected. This can happen if the device is hot-inserted into a card with the power applied, or if the device is mounted on a card that has an edge connector and the card is hot-inserted into a system with the power on.

To help ensure that latch-up does not occur, it is considered good design practice to connect a reverse-biased Schottky diode (with a forward voltage drop of less than or equal to 0.4 V – 1N5711 or equivalent) between the power supply and GND (see Figure 3). If it is possible that a TP306xA- or TP1306xA-equipped card that has an edge connector could be hot-inserted into a powered-up system, it is also important to ensure that the ground edge connector traces are longer than the power and signal traces so that the card ground is always the first to make contact.

device power-up sequence

Latch-up can also occur if a signal source is connected without the device being properly grounded. A signal applied to one terminal could then find a ground through another signal terminal on the device. To ensure proper operation of the device and as a safeguard against this sort of latch-up, it is recommended that the following power-up sequence always be used:

1. Ensure that no signals are applied to the device before the power-up sequence is complete.
2. Connect GND.
3. Apply V_{BB} (most negative voltage).
4. Apply V_{CC} (most positive voltage).
5. Force a power down condition in the device.
6. Connect clocks.
7. Release the power down condition.
8. Apply FS synchronization pulses.
9. Apply the signal inputs.

When powering down the device, this procedure should be followed in the reverse order.

PRINCIPLES OF OPERATION

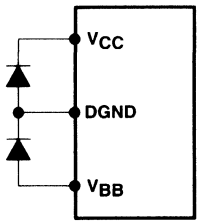


Figure 3. Latch-Up Protection Diode Connection

internal sequencing

Power-on reset circuitry initializes the TP3064A, TP3067A, TP13064A, and TP13067A devices when power is first applied, placing it into the power-down mode. DX and VFRO outputs go into high-impedance states and all nonessential circuitry is disabled. A low level or clock applied to MCLKR/PDN powers up the device and activates all circuits. DX, a 3-state PCM data output, remains in the high-impedance state until the arrival of the second FSX pulse.

synchronous operation

For synchronous operation, a clock is applied to MCLKX. MCLKR/PDN is used as a power-down control. A low level on MCLKR powers up the device and a high level powers it down. In either case, MCLKX is selected as the master clock for both receive and transmit direction. BCLKX must also have a bit clock applied to it. The selection of the proper internal divider for a master-clock frequency of 1.536 MHz, 1.544 MHz, or 2.048 MHz can be done via BCLKR/CLKSEL. The device automatically compensates for the 193rd clock pulse of each frame.

A fixed level on BCLKR/CLKSEL selects BCLKX as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation that can be selected depending on the state of BCLKR/CLKSEL. In the synchronous mode, BCLKX may be in the range from 64 kHz to 2.048 MHz but must be synchronous with MCLKX.

Table 1. Selection of Master-Clock Frequencies

BCLKR/CLKSEL	MASTER-CLOCK FREQUENCY SELECTED	
	TP3064A, TP13064A	TP3067A, TP13067A
Clock Input	1.536 MHz or 1.544 MHz	2.048 MHz
Logic Input L (sync mode only)	2.048 MHz	1.536 MHz or 1.544 MHz
Logic Input H (open) (sync mode only)	1.536 MHz or 1.544 MHz	2.048 MHz

The encoding cycle begins with each FSX pulse, and the PCM data from the previous cycle is shifted out of the enabled DX output on the rising edge of BCLKX. After eight bit-clock periods, the 3-state DX output is returned to the high-impedance state. With an FSR pulse, PCM data is latched via DR on the falling edge of BCLKX (or BCLKR, if running). FSX and FSR must be synchronous with MCLKX and MCLKR.

PRINCIPLES OF OPERATION

asynchronous operation

For asynchronous operation, separate transmit and receive clocks can be applied. MCLKX and MCLKR must be 2.048 MHz for the TP3064A and TP13064A, 1.536 MHz or 1.544 MHz for the TP3067A and TP13067A and need not be synchronous. However, for best performance, MCLKR should be synchronous with MCLKX. This is easily achieved by applying only static logic levels to MCLKR/PDN. This connects MCLKX to all internal MCLKR functions. For 1.544-MHz operation, the device compensates for the 193rd clock pulse of each frame. Each encoding cycle is started with FSX, and FSX must be synchronous with MCLKX and BCLKX. Each decoding cycle is started with FSR, and FSR must be synchronous with BCLKR. The logic levels shown in Table 1 are not valid in the asynchronous mode. BCLKX and BCLKR can operate from 64 kHz to 2.048 MHz.

short-frame sync operation

The device can operate with either a short- or a long-frame sync pulse. On power up, the device automatically goes into the short-frame mode where both FSX and FSR must be one bit-clock period long with timing relationships specified in Figure 1. With FSX high during a falling edge of BCKLX, the next rising edge of BCLKX enables the 3-state output buffer, DX, which outputs the sign bit. The remaining seven bits are clocked out on the following seven rising edges, and the next falling edge disables DX. With FSR high during a falling edge of BCLKR (BCLKX in synchronous mode), the next falling edge of BCLKR latches in the sign bit. The following seven falling edges latch in the remaining bits. The short-frame sync pulse can be utilized in either the synchronous or asynchronous mode.

long-frame sync operation

Both FSX and FSR must be three or more bit-clock periods long to use the long-frame sync mode with timing relationships, as shown in Figure 2. Using the transmit frame sync (FSX), the device detects whether a short- or long-frame sync pulse is being used. For 64-kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The rising edge of FSX or BCLKX, which ever occurs later, enables the DX 3-state output buffer. The first bit clocked out is the sign bit. The next seven rising edges of BCLKX edges clock out the remaining seven bits. The falling edge of BCLKX following the eighth rising edge or FSX going low, whichever occurs later, disables DX. A rising edge on FSR, the receive frame sync pulse, causes the PCM data at DR to be latched in on the next eight falling edges of BCLKR (BCLKX in synchronous mode). The long-frame sync pulse may be used in either the synchronous or asynchronous mode.

PRINCIPLES OF OPERATION

transmit section

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors. The low noise and wide bandwidth characteristics of these devices provide gains in excess of 20 dB across the audio passband. The operational amplifier drives a unity-gain filter consisting of an RC active prefilter followed by an eight-order switched-capacitor band-pass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. As per μ-law (TP3064A and TP13064A) or A-law (TP3067A and TP13067A) coding conventions, the ADC is a companding type. A precision voltage reference provides an input overload of nominally 2.5-V peak. The sampling of the filter output is controlled by the FSX frame sync pulse. Then the successive-approximation encoding cycle begins. The 8-bit code is loaded into a buffer and shifted out through DX at the next FSX pulse. The total encoding delay is approximately 290 μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration (see Table 2).

Table 2. Encoding Format at DX Output

	TP3064A, TP13064A μ-Law	TP3067A, TP13067A A-Law (INCLUDES EVEN-BIT INVERSION)
V_I = + Full scale	1 0 0 0 0 0 0 0	1 0 1 0 1 0 1 0
V_I = 0	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
V_I = – Full scale	0 0 0 0 0 0 0 0	0 0 1 0 1 0 1 0

receive section

The receive section consists of an expanding DAC that drives a fifth-order low-pass filter clocked at 256 kHz. The decoder is μ-law (TP3064A and TP13064A) or A-law (TP3067A and TP13067A), and the fifth-order low-pass filter corrects for the (sin x)/x attenuation caused by the 8-kHz sample/hold. The filter is followed by a second-order RC active post filter with its output at VFRO. The receive section is unity gain, but gain can be added by using the power amplifiers. At FSR, the data at DR is clocked in on the falling edge of the next eight BCLKR (BCLKX) periods. At the end of the decoder time slot, the decoding cycle begins and 10-μs later the decoder DAC output is updated. The decoder delay is about 10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (1/2 frame), or a total of approximately180 μs.

receive power amplifiers

Two inverting-mode power amplifiers are provided for directly driving a match-line interface transformer. The gain of the first power amplifier can be adjusted to boost the ±2.5-V peak output signal from the receive filter up to the ±3.3-V peak into an unbalanced 300-Ω load, or ±4 V into an unbalanced 15-kΩ load. The second power amplifier is internally connected in the unity-gain inverting mode to give 6 dB of signal gain for balanced loads.

Maximum power transfer to a 600-Ω subscriber line termination is obtained by differentially driving a balanced transformer with $\sqrt{2}$:1 turns ratio, as shown in Figure 3. A total peak power of 15.6 dBm can be delivered to the load plus termination.

APPLICATION INFORMATION

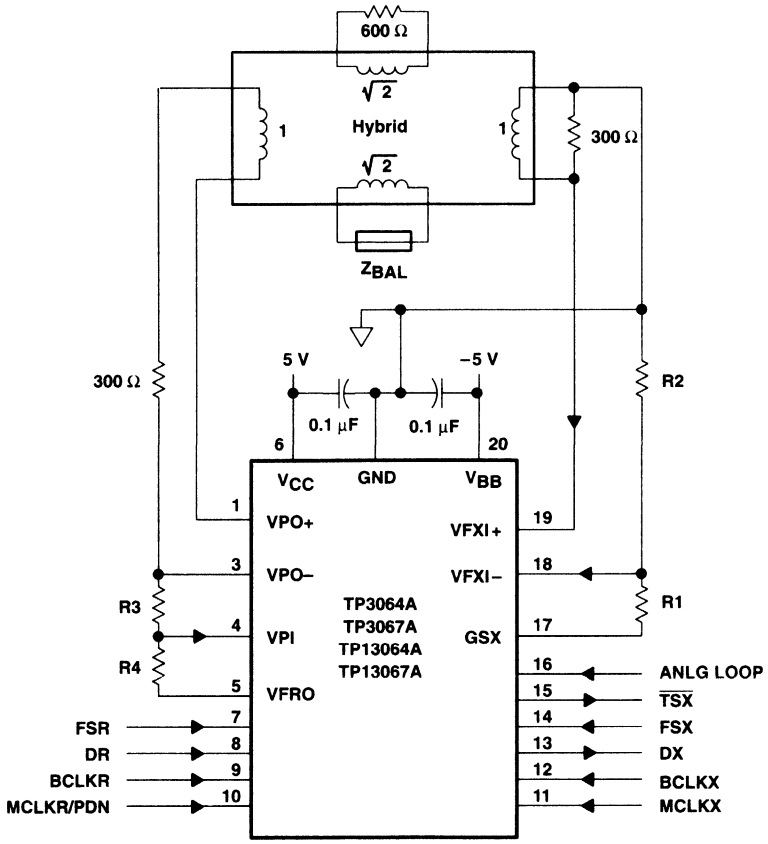
power supplies

While the pins of the TP1306xA and TP306xA families are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed ensuring that ground is connected to the device before any other connections are made. In applications where the printed-circuit board can be plugged into a hot socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to ANLG GND. This minimizes the interaction of ground return currents flowing through a common bus impedance. V_{CC} and V_{BB} supplies should be decoupled by connecting 0.1-μF decoupling capacitors to this common point. These bypass capacitors must be connected as close as possible to V_{CC} and V_{BB}.

For best performance, the ground point of each codec/filter on a card should be connected to a common card ground in star formation rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10-μF capacitors.

APPLICATION INFORMATION



NOTES: A. Transmit gain = 20 y log $\left(\frac{R1 + R2}{R2}\right)$, (R1 + R2) ≥ 10 kΩ

B. Receive gain = 20 y log $\left(\frac{2 \times R3}{R4}\right)$, R4 ≥ 10 kΩ

Figure 4. Typical Synchronous Application

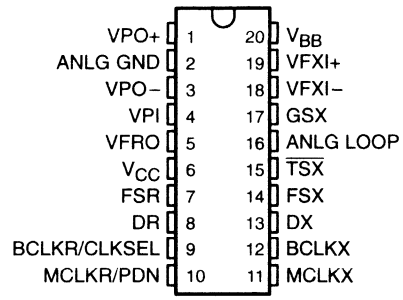
- **Complete PCM Codec and Filtering Systems Include:**
  - **Transmit High-Pass and Low-Pass Filtering**
  - **Receive Low-Pass Filter With (sin x)/x Correction**
  - **Active RC Noise Filters**
  - **μ-Law or A-Law Compatible Coder and Decoder**
  - **Internal Precision Voltage Reference**
  - **Serial I/O Interface**
  - **Internal Autozero Circuitry**
- **μ-Law – TP13064B and TP3064B**
- **A-Law – TP13067B and TP3067B**
- **±5-V Operation**
- **Low Operating Power . . . 70 mW Typ**
- **Power-Down Standby Mode . . . 3 mW Typ**
- **Automatic Power Down**
- **TTL- or CMOS-Compatible Digital Interface**
- **Maximizes Line Interface Card Circuit Density**
- **Improved Versions of National Semiconductor TP3064, TP3067, TP3064-X, and TP3067-X**

description

The TP3064B, TP3067B, TP13064B, and TP13067B each comprise a single-chip pulse-code-modulation encoder and decoder (PCM codec), and PCM line filter. They also provide band-pass filtering of the analog signals prior to the encoding, and low-pass filtering after the decoding of voice signals and call-progress tones. All the functions required to interface a full-duplex (2-wire) voice telephone circuit with a time-division-multiplexed (TDM) system are included on-chip. These devices are pin-for-pin compatible with the National Semiconductor TP3064 and TP3067. Primary applications include:

- Line interface for digital transmission and switching of T1 carrier, PABX (private automated branch exchange), and central office telephone systems
- Subscriber line concentrators
- Digital-encryption systems
- Digital voice-band data-storage systems
- Digital signal processing

DW OR N PACKAGE
(TOP VIEW)

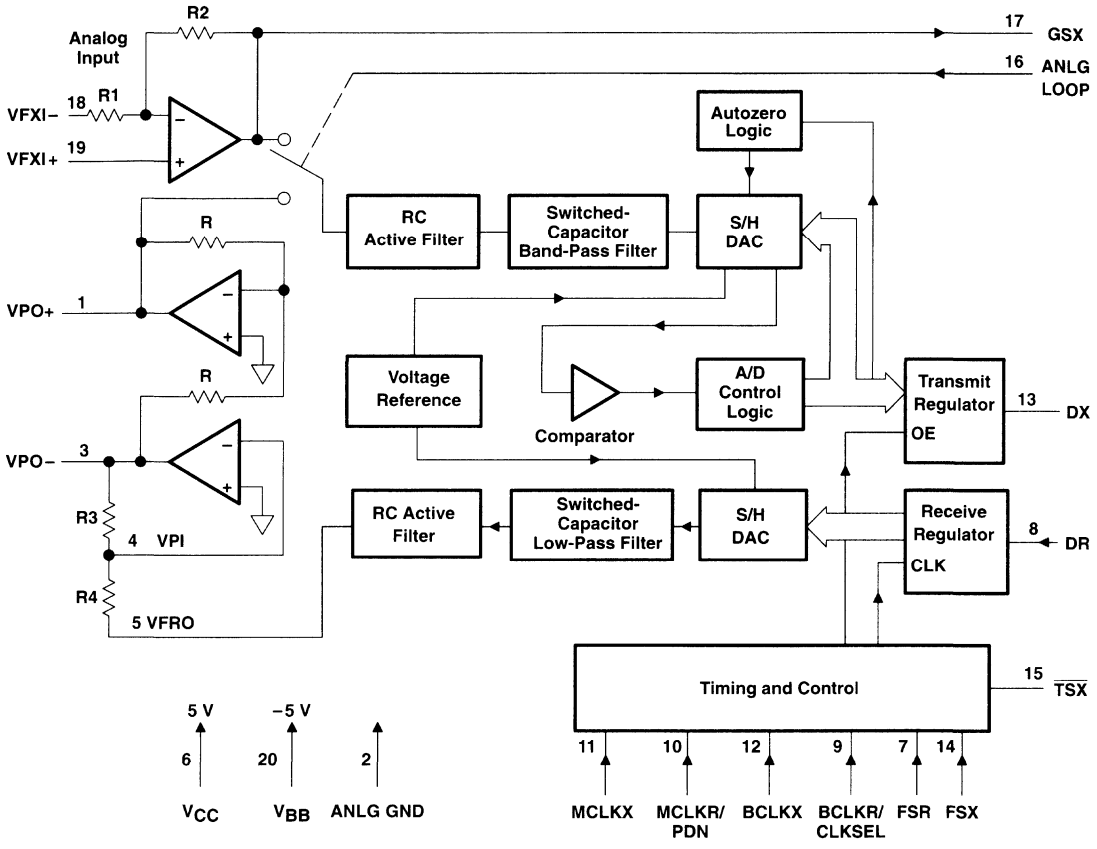


These devices are designed to perform the transmit encoding (A/D conversion) and receive decoding (D/A conversion) as well as the transmit and receive filtering functions in a PCM system, and are intended to be used at the analog termination of a PCM line or trunk. They require a transmit master clock and a receive master clock that may be asynchronous (1.536 MHz, 1.544 MHz, or 2.048 MHz), transmit and receive data clocks that are synchronous with the master clock (but can vary from 64 kHz to 2.048 MHz), and transmit and receive frame-sync pulses. The TP3064B and TP13064B contain patented circuitry to achieve low transmit channel idle noise and are not recommended for applications in which the composite signals on the transmit side are below −55 dBm0.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the CMOS gates.

The TP3064B and TP3067B are characterized for operation from 0°C to 70°C. The TP13064B and TP13067B are characterized for operation from −40°C to 85°C.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
ANLG GND	2	Analog ground. All signals are referenced to ANLG GND.
ANLG LOOP	16	Analog loopback control input. Must be set to logic low for normal operation. When pulled to logic high, the transmit filter input is disconnected from the output of the transmit preamplifier and connected to the VPO+ output of the receive power amplifier.
BCLKR/CLKSEL	9	The bit clock that shifts data into DR after the FSR leading edge. May vary from 64 kHz to 2.048 MHz. Alternately, can be a logic input that selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode. BCLKX is used for both transmit and receive directions (see Table 1).
BCLKX	12	The bit clock that shifts out the PCM data on DX. May vary from 64 kHz to 2.048 MHz, but must be synchronous with MCLKX
DR	8	Receive data input. PCM data is shifted into DR following the FSR leading edge.
DX	13	The 3-state PCM data output that is enabled by FSX
FSR	7	Receive frame-sync pulse input that enables BCLKR to shift PCM data in DR. FSR is an 8-kHz pulse train (see Figures 1 and 2 for timing details).
FSX	14	Transmit frame-sync pulse that enables BCLKX to shift out the PCM data on DX. FSX is an 8-kHz pulse train (see Figures 1 and 2 for timing details).
GSX	17	Analog output of the transmit input amplifier. GSX is used to externally set gain.
MCLKR/PDN	10	Receive master clock (must be 1.536 MHz, 1.544 MHz, or 2.048 MHz). May be synchronous with MCLKX, but should be synchronous for best performance. When MCLKR is connected continuously low, MCLKX is selected for all internal timing. When MCLKR is connected continuously high, the device is powered down.
MCLKX	11	Transmit master clock (must be 1.536 MHz, 1.544 MHz, or 2.048 MHz). May be asynchronous with MCLKR
$\overline{TSX}$	15	Open-drain output that pulses low during the encoder time slot
V_{BB}	20	Negative power supply. $V_{BB} = -5\ V \pm 5\%$
V_{CC}	6	Positive power supply. $V_{CC} = 5\ V \pm 5\%$
VFRO	5	Analog output of the receive filter
VFXI+	19	Noninverting input of the transmit input amplifier
VFXI–	18	Inverting input of the transmit input amplifier
VPI	4	Inverting input to the receive power amplifier. Also powers down both amplifiers when connected to V_{BB}.
VPO+	1	The noninverted output of the receive power amplifier
VPO–	3	The inverted output of the receive power amplifier

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Supply voltage, V_{BB} (see Note 1) . . . . . −7 V
Voltage range at any analog input or output . . . . . V_{CC} + 0.3 V to V_{BB} − 0.3 V
Voltage range at any digital input or output . . . . . V_{CC} + 0.3 V to GND − 0.3 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: TP3064B, TP3067B . . . . . 0°C to 70°C
TP13064B, TP13067B . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Supply voltage, V_{BB}		−4.75	−5	−5.25	V
High-level input voltage, V_{IH}		2.2			V
Low-level input voltage, V_{IL}				0.6	V
Common-mode input voltage range, V_{ICR}†				±2.5	V
Load resistance at GSX, R_L		10			kΩ
Load capacitance at GSX, C_L				50	pF
Operating free-air temperature, T_A	TP3064B, TP3067B	0		70	°C
	TP13064B, TP13067B	−40		85	

† Measure with CMRR > 60 dB.

NOTE 2: To avoid possible damage to these CMOS devices and resulting reliability problems, the power-up procedure described in the device power-up sequence paragraphs later in this document should be followed.

electrical characteristics over power supply variations and recommended free-air temperature range (unless otherwise noted)

supply current

PARAMETER			TEST CONDITIONS	TP306xB			TP1306xB			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{CC}	Supply current from V_{CC}	Power down	No load		0.5	1		0.5	1.2	mA
		Active			6	10		6	11	
I_{BB}	Supply current from V_{BB}	Power down	No load		0.5	1		0.5	1.2	mA
		Active			6	10		6	11	

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.

electrical characteristics at V_{CC} = 5 V ± 5%, V_{BB} = −5 V ± 5%, GND at 0 V, T_A = 25°C (unless otherwise noted)

digital interface

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	DX	I_H = −3.2 mA	2.4		V
V_{OL}	Low-level output voltage	DX	I_L = 3.2 mA		0.4	V
		$\overline{TSX}$	I_L = 3.2 mA, Drain open		0.4	
I_{IH}	High-level input current		$V_I = V_{IH}$ to V_{CC}		±10	μA
I_{IL}	Low-level input current	All digital inputs	V_I = GND to V_{IL}		±10	μA
I_{OZ}	Output current in high-impedance state	DX	V_O = GND to V_{CC}		±10	μA

analog interface with transmit amplifier input

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_I	Input current	VFXI+ or VFXI–	V_I = −2.5 V to 2.5 V			±200	nA
r_i	Input resistance	VFXI+ or VFXI–	V_I = −2.5 V to 2.5 V	10			MΩ
r_o	Output resistance		Closed loop, Unit gain		1	3	Ω
	Output dynamic range	GSX	$R_L \geq 10$ kΩ			±2.8	V
A_V	Open-loop voltage amplification	VFXI+ to GSX		5000			
B_I	Unity-gain bandwidth	GSX		1	2		MHz
V_{IO}	Input offset voltage	VFXI+ or VFXI–				±20	mV
CMRR	Common-mode rejection ratio			60			dB
k_{SVR}	Supply-voltage rejection ratio			60			dB

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.

analog interface with receive filter

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output resistance	VFRO			1	3	Ω
Load resistance		VFRO = ±2.5 V	600			Ω
Load capacitance	VFRO to GND				500	pF
Output dc offset voltage	VFRO to GND				±200	mV

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.

analog interface with power amplifiers

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_I	Input current		VPI = –1 V to 1 V				±100	nA
r_i	Input resistance		VPI = –1 V to 1 V		10			MΩ
r_o	Output resistance	VPO+ or VPO–	Inverting unity gain			1		Ω
A_V	Voltage amplification	VPO– or VPO+	VPO– = 1.77 Vrms, R_L = 600 Ω			–1		
B_I	Unity-gain bandwidth	VPO–	Open loop			400		kHz
V_{IO}	Input offset voltage						±25	mV
k_{SVR}	Supply-voltage rejection ratio of V_{CC} or V_{BB}		VPO– connected to VPI	0 kHz to 4 kHz	60			dB
				4 kHz to 50 kHz	36			
R_L	Load resistance		Connected from VPO+ to VPO–		600			Ω
C_L	Load capacitance						100	pF

† All typical values are at V_{CC} = 5 V, V_{BB} = –5 V, and T_A = 25°C.

timing requirements

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$f_{clock(M)}$	Frequency of master clock	MCLX and MCLKR	Depends on the device used and BCLKX/CLKSEL		1.536 1.544 2.048		MHz
$f_{clock(B)}$	Frequency of bit clock, transmit	BCLKX		64		2.048	MHz
t_{r1}	Rise time of master clock	MCLKX and MCLKR	Measured from 20% to 80%			50	ns
t_{f1}	Fall time of master clock	MCLKX and MCLKR	Measured from 20% to 80%			50	ns
t_{r2}	Rise time of bit clock, transmit	BCLKX	Measured from 20% to 80%			50	ns
t_{f2}	Fall time of bit clock, transmit	BCLKX	Measured from 20% to 80%			50	ns
t_{w1}	Pulse duration, MCLKX and MCLKR high			160			ns
t_{w2}	Pulse duration, MCLKX and MCLKR low			160			ns
t_{su1}	Setup time, BCLKX high (and FSX in long-frame sync mode) before MCLKX↓		First bit clock after the leading edge of FSX	100			ns
t_{w3}	Pulse duration, BCLKX and BCLKR high		V_{IH} = 2.2 V	160			ns
t_{w4}	Pulse duration, BCLKX and BCLKR low		V_{IL} = 0.6 V	160			ns
t_{h1}	Hold time, frame sync low after bit clock low (long frame only)			0			ns
t_{h2}	Hold time, BCLKX high after frame sync↑ (short frame only)			0			ns
t_{su2}	Setup time, frame sync high before bit clock↓ (long frame only)			80			ns
t_{d1}	Delay time, BCLKX high to data valid		Load = 150 pF plus 2 LSTTL loads‡	0		140	ns
t_{d2}	Delay time, BCLKX high to $\overline{TSX}$ low		Load = 150 pF plus 2 LSTTL loads‡			140	ns
t_{d3}	Delay time, BCLKX (or 8 clock FSX in long frame only) low to data output disabled			50		165	ns
t_{d4}	Delay time, FSX or BCLKX high to data valid (long frame only)		C_L = 0 pF to 150 pF	20		165	ns
t_{su3}	Setup time, DR valid before BCLKR↓			50			ns
t_{h3}	Hold time, DR valid after BCLKR or BCLKX↓			50			ns
t_{su4}	Setup time, FSR or FSX high before BCLKR or BCLKX↓		Short-frame sync pulse (1- or 2-bit clock periods long) (see Note 3)	50			ns
t_{h4}	Hold time, FSX or FSR high after BCLKX or BCLKR↓		Short-frame sync pulse (1- or 2-bit clock periods long) (see Note 3)	100			ns
t_{h5}	Hold time, frame sync high after bit clock↓		Long-frame sync pulse (from 3- to 8-bit clock periods long)	100			ns
t_{w5}	Pulse duration of the frame sync pulse (low level)		64 kbps operating mode	160			ns

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.
‡ Nominal input value for an LSTTL load is 18 kΩ.
NOTE 3: For short-frame sync timing, FSR and FSX must go high while their respective bit clocks are high.

operating characteristics over operating free-air temperature range, V_{CC} = 5 V ± 5%, V_{BB} = −5 V ± 5%, GND at 0 V, V_I = 1.2276 V, f = 1.02 kHz, transmit input amplifier connected for unity gain, noninverting (unless otherwise noted)

filter gains and tracking errors

PARAMETER		TEST CONDITIONS‡	MIN	TYP†	MAX	UNIT
Maximum peak transmit overload level	TP3064B, TP13064B	3.17 dBm0		2.501		V
	TP3067B, TP13067B	3.14 dBm0		2.492		
Transmit filter gain, absolute (at 0 dBm0)		T_A = 25°C	−0.15		0.15	dB
Transmit filter gain, relative to absolute		f = 16 Hz			−40	dB
		f = 50 Hz			−30	
		f = 60 Hz			−26	
		f = 200 Hz	−1.8		−0.1	
		f = 300 Hz to 3000 Hz	−0.15		0.15	
		f = 3300 Hz	−0.35		0.05	
		f = 3400 Hz	−0.8		0	
		f = 4000 Hz			−14	
		f ≥ 4600 Hz (measure response from 0 Hz to 4000 Hz)			−32	
Absolute transmit gain variation with temperature and supply voltage		Relative to absolute transmit gain	−0.1		0.1	dB
Transmit gain tracking error with level		Sinusoidal test method; Reference level = −10 dBm0				dB
		3 dBm0 ≥ input level ≥ −40 dBm0			±0.2	
		−40 dBm0 > input level ≥ −50 dBm0			±0.4	
		−50 dBm0 > input level ≥ −55 dBm0			±0.8	
Receive filter gain, absolute (at 0 dBm0)		Input is digital code sequence for 0 dBm0 signal, T_A = 25°C	−0.15		0.15	dB
Receive filter gain, relative to absolute		f = 0 Hz to 3000 Hz, T_A = 25°C	−0.15		0.15	dB
		f = 3300 Hz	−0.35		0.05	
		f = 3400 Hz	−0.8		0	
		f = 4000 Hz			−14	
Absolute receive gain variation with temperature and supply voltage		T_A = full range, See Note 4	−0.1		0.1	dB
Receive gain tracking error with level		Sinusoidal test method; reference input PCM code corresponds to an ideally encoded −10 dBm0 signal				dB
		3 dBm0 ≥ input level ≥ −40 dBm0			±0.2	
		−40 dBm0 > input level ≥ −50 dBm0			±0.4	
		−50 dBm0 > input level ≥ −55 dBm0			±0.8	
Receive output drive voltage		R_L = 10 kΩ			±2.5	V
Transmit and receive gain tracking error with level (A-law, CCITT C712)		Pseudo-noise test method; reference input PCM code corresponds to an ideally encoded −10 dBm0 signal				dB
		3 dBm0 ≥ input level ≥ −40 dBm0			±0.25	
		−40 dBm0 > input level ≥ −50 dBm0			±0.3	
		−50 dBm0 > input level ≥ −55 dBm0			±0.45	

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.
‡ Absolute rms signal levels are defined as follows: V_I = 1.2276 V = 0 dBm0 = 4 dBm at f = 1.02 kHz with R_L = 600 Ω.
NOTE 4: Full range for the TP3064B and TP3067B is 0°C to 70°C. Full range for the TP13064B and TP13067B is −40°C to 85°C.

envelope delay distortion with frequency

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit delay, absolute (at 0 dBm0)	f = 1600 Hz		290	315	μs
Transmit filter gain, relative to absolute	f = 500 Hz to 600 Hz		195	220	μs
	f = 600 Hz to 800 Hz		120	145	
	f = 800 Hz to 1000 Hz		50	75	
	f = 1000 Hz to 1600 Hz		20	40	
	f = 1600 Hz to 2600 Hz		55	75	
	f = 2600 Hz to 2800 Hz		80	105	
	f = 2800 Hz to 3000 Hz		130	155	
Receive delay, absolute (at 0 dBm0)	f = 1600 Hz		180	200	μs
Receive delay, relative to absolute	f = 500 Hz to 1000 Hz	−40	−25		μs
	f = 1000 Hz to 1600 Hz	−30	−20		
	f = 1600 Hz to 2600 Hz		70	90	
	f = 2600 Hz to 2800 Hz		100	125	
	f = 2800 Hz to 3000 Hz		140	175	

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.

noise

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit noise, C-message weighted‡	TP3064B, TP13064B	VFXI = 0 V		5	9	dBrnC0
Transmit noise, psophometric weighted (see Note 5)	TP3067B, TP13067B	VFXI = 0 V		−74	−69	dBm0p
Receive noise, C-message weighted	TP3064B, TP13064B	PCM code equals alternating positive and negative zero		2	4	dBrnC0
Receive noise, psophometric weighted	TP3067B, TP13067B	PCM code equals positive zero		−86	−83	dBm0p
Noise, single frequency		VFXI+ = 0 V, f = 0 kHz to 100 kHz, Loop-around measurement			−53	dBm0

† All typical values are at V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.
‡ This parameter is achieved through use of patented circuitry and is not recommended for applications in which the composite signals on the transmit side are below −55 dBm0.
NOTE 5: Measured by extrapolation from the distortion test result

power supply rejection

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
Positive power-supply rejection, transmit	V_{CC} = 5 V + 100 mVrms, VFXI+ = −50 dBm0	f = 0 Hz to 4 kHz	A-law	38		dB
			μ-law	38		dBC†
		f = 4 kHz to 50 kHz		40		dB
Negative power-supply rejection, transmit	V_{BB} = −5 V + 100 mVrms, VFXI+ = −50 dBm0	f = 0 Hz to 4 kHz	A-law	35		dB
			μ-law	35		dBC†
		f = 4 kHz to 50 kHz		40		dB
Positive power-supply rejection, receive	PCM code equals positive zero, V_{CC} = 5 V + 100 mVrms	f = 0 Hz to 4 kHz	A-law	40		dB
			μ-law	40		dBC†
		f = 4 kHz to 50 kHz		40		dB
Negative power-supply rejection, receive	PCM code equals positive zero, V_{BB} = −5 V + 100 mVrms	f = 0 Hz to 4 kHz	A-law	38		dB
			μ-law	38		dBC†
		f = 4 kHz to 50 kHz		40		dB
Spurious out-of-band signals at the channel output (VFRO)	0 dBm0, 300-Hz to 3400-Hz input applied to DR (measure individual image signals at VFRO)				−30	dB
	f = 4600 Hz to 7600 Hz				−33	dB
	f = 7600 Hz to 8400 Hz				−40	
	f = 8400 Hz to 100 kHz				−40	

† The unit dBC applies to C-message weighting.

distortion

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Signal-to-distortion ratio, transmit or receive half-channel‡	Level = 3 dBm0		33		dBC†
	Level = 0 dBm0 to −30 dBm0		36		
	Level = −40 dBm0	Transmit	29		
		Receive	30		
	Level = −55 dBm0	Transmit	14		
		Receive	15		
Single-frequency distortion products, transmit				−46	dB
Single-frequency distortion products, receive				−46	dB
Intermodulation distortion	Loop-around measurement, VFXI+ = −4 dBm0 to −21 dBm0, Two frequencies in the range of 300 Hz to 3400 Hz			−41	dB
Signal-to-distortion ratio, transmit half-channel (A-law) (CCITT G.714)§	Level = −3 dBm0		33		dB
	Level = −6 dBm0 to −27 dBm0		36		
	Level = −34 dBm0		33.5		
	Level = −40 dBm0		28.5		
	Level = −55 dBm0		13.5		
Signal-to-distortion ratio, receive half-channel (A-law) (CCITT G.714)§	Level = −3 dBm0		33		dB
	Level = −6 dBm0 to −27 dBm0		36		
	Level = −34 dBm0		34.2		
	Level = −40 dBm0		30		
	Level = −55 dBm0		15		

† The unit dBC applies to C-message weighting.
‡ Sinusoidal test method (see Note 6).
§ Pseudo-noise test method
NOTE 6: The TP13064A and TP3064A are measured using a C-message filter. The TP13067A and TP3067A are measured using a psophometric weighted filter.

crosstalk

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Crosstalk, transmit to receive	f = 300 Hz to 3000 Hz,	DR at steady PCM code		–90	–75	dB
Crosstalk, receive to transmit (see Note 7)	VFXI = 0 V,	f = 300 Hz to 3000 Hz		–90	–72	dB

† All typical values are at V_{CC} = 5 V, V_{BB} = –5 V, and T_A = 25°C.
NOTE 7: Receive-to-transmit crosstalk is measured with a –50 dBm0 activation signal applied to VFXI+.

power amplifiers

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Maximum 0 dBm0 rms level for better than ±0.1 dB linearity over the range if –10 dBm0 to 3 dBm0	Balanced load, R_L, connected between VPO+ and VPO–			
	R_L = 600 Ω	3.3		V_{RMS}
	R_L = 1200 Ω	3.5		
	R_L = 30 kΩ	4		
Signal/distortion	R_L = 600 Ω	50		dB

PARAMETER MEASUREMENT INFORMATION

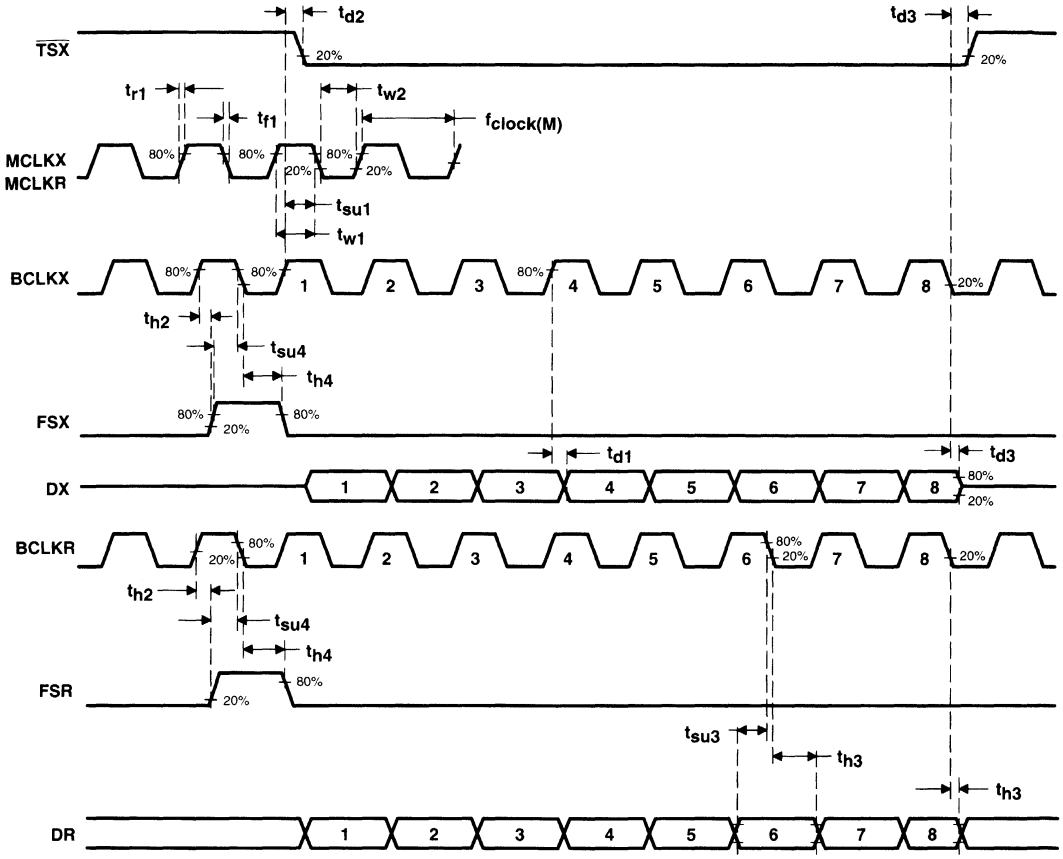


Figure 1. Short-Frame Sync Timing

PARAMETER MEASUREMENT INFORMATION

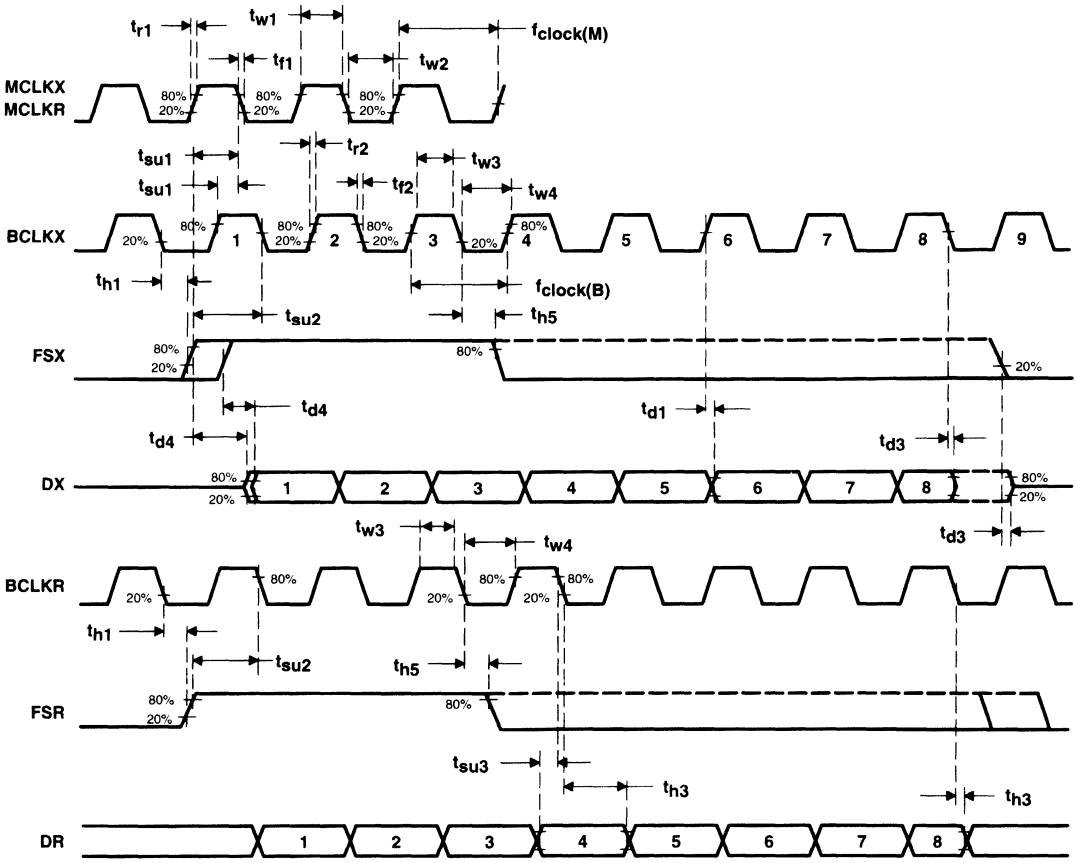


Figure 2. Long-Frame Sync Timing

PRINCIPLES OF OPERATION

system reliability and design considerations

TP306xB, TP1306xB system reliability and design considerations are detailed in the following paragraphs.

latch-up

Latch-up is possible in all CMOS devices. It is caused by the firing of a parasitic SCR that is present due to the inherent nature of CMOS. When a latch-up occurs, the device draws excessive amounts of current and will continue to draw heavy current until power is removed. Latch-up can result in permanent damage to the device if supply current to the device is not limited.

Even though the TP306xB and TP1306xB devices are heavily protected against latch-up, it is still possible to cause latch-up under certain conditions in which excess current is forced into or out of one or more terminals. Latch-up can occur when the positive supply voltage drops momentarily below ground, when the negative supply voltage rises momentarily above ground, or possibly if a signal is applied to a terminal after power has been applied but before the ground is connected. This can happen if the device is hot-inserted into a card with the power applied, or if the device is mounted on a card with an edge connector, and the card is hot-inserted into a system with the power on.

To help ensure that latch-up does not occur, it is considered good design practice to connect a reversed biased Schottky diode (with a forward voltage drop of less than or equal to 0.4 V — 1N5711 or equivalent), between each power supply and GND (see Figure 3). If it is possible that a TP306xB- or TP1306xB-equipped card that has an edge connector could be hot-inserted into a powered-up system, it is also important to ensure that the ground edge connector traces are longer than the power and signal traces so that the card ground is always the first to make contact.

device power-up sequence

Latch-up can also occur if a signal source is connected without the device being properly grounded. A signal applied to one terminal could then find a ground through another signal terminal on the device. To ensure proper operation of the device and as a safeguard against this sort of latch-up, it is recommended the following power-up sequence always be used:

1. Ensure no signals are applied to the device before the power-up sequence is complete.
2. Connect GND.
3. Apply V_{BB} (most negative voltage).
4. Apply V_{CC} (most positive voltage).
5. Force a power down condition in the device.
6. Connect clocks.
7. Release power down condition.
8. Apply FSX and/or FXR synchronization pulses.
9. Apply signal inputs.

When powering down the device, this procedure should be followed in the reverse order.

PRINCIPALS OF OPERATION

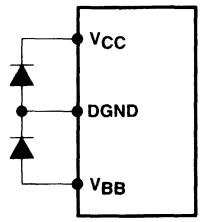


Figure 3. Diode Configuration for Latch-Up Protection Circuitry

internal sequencing

Power-on reset circuitry initializes the TP3064B, TP3067B, TP13064B, and TP13067B devices when power is first applied, placing it into the power-down mode. DX and VFRO outputs go into high-impedance states and all nonessential circuitry is disabled. A low level or clock applied to MCLKR/PDN powers up the device and activates all circuits. DX, a 3-state PCM data output, remains in the high-impedance state until the arrival of the second FSX pulse.

power supplies

All ground connections to each device should meet at a common point as close as possible to ANLG–GND. This minimizes the interaction of ground return currents flowing through a common bus impedance. V_{CC} and V_{BB} supplies should be decoupled by connecting 0.1-µF decoupling capacitors between each power rail and this common point. These bypass capacitors must be connected as close as possible to V_{CC} and V_{BB}.

For best performance, the ground point of each codec/filter on a card should be connected to a common card ground in star formation rather than through a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10-µF capacitors.

synchronous operation

For synchronous operation, a clock is applied to MCLKX. MCLKR/PDN is used as a power-down control. A logic 0 applied to MCLKR powers-up the device and a high level powers it down. In either case, MCLKX is selected as the master clock for both receive and transmit direction. BCLKX must also have a bit clock applied to it. The selection of the proper internal divider for a master-clock frequency of 1.536 MHz, 1.544 MHz, or 2.048 MHz can be done using BCLKR/CLKSEL. The device automatically compensates for the 193rd clock pulse of each frame.

A fixed level on BCLKR/CLKSEL selects BCLKX as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation that can be selected depending on the state of BCLKR/CLKSEL. In the synchronous mode, BCLKX may be in the range from 64 kHz to 2.048 MHz but must be synchronous with MCLKX.

The encoding cycle begins with each FSX pulse, and the PCM data from the previous cycle is shifted out of the enabled DX output on the rising edge of BCLKX. After eight-bit clock periods, the 3-state DX output is returned to the high-impedance state. With an FSR pulse, PCM data is latched via DR on the falling edge of BCLKX (or BCLKR, if running). FSX and FSR must be synchronous with MCLKX and MCLKR.

PRINCIPALS OF OPERATION

asynchronous operation

For asynchronous operation, separate transmit and receive clocks can be applied. MCLKX and MCLKR must be 2.048 MHz for the TP3064B and TP13064B, 1.536 MHz or 1.544 MHz for the TP3067B and TP13067B and need not be synchronous. However, for best performance, MCLKR should be synchronous with MCLKX. This is easily achieved by applying only static logic levels to MCLKR/PDN. This connects MCLKX to all internal MCLKR functions. For 1.544-MHz operation, the device compensates for the 193rd clock pulse of each frame. Each encoding cycle is started with FSX, and FSX must be synchronous with MCLKX and BCLKX. Each decoding cycle is started with FSR, and FSR must be synchronous with BCLKR. The logic levels shown in Table 1 are not valid in the asynchronous mode. BCLKX and BCLKR can operate from 64 kHz to 2.048 MHz.

short-frame sync operation

The device can operate with either a short- or a long-frame sync pulse. On power up, the device automatically goes into the short-frame mode where both FSX and FSR must be one bit-clock period long, with timing relationships specified in Figure 1. With FSX high during a falling edge of BCKLX, the next rising edge of BCLKX enables the 3-state output buffer, DX, which outputs the sign bit. The remaining seven bits are clocked out on the following seven rising edges, and the next falling edge disables DX. With FSR high during a falling edge of BCLKR (BCLKX in synchronous mode), the next falling edge of BCLKR latches in the sign bit. The following seven falling edges latch in the seven remaining bits. The short-frame sync pulse may be utilized in either the synchronous or asynchronous mode.

Table 1. Selection of Master-Clock Frequencies

BCLKR/CLKSEL	MASTER-CLOCK FREQUENCY SELECTED	
	TP3064B, TP13064B	TP3067B, TP13067B
Clock Input	1.536 MHz or 1.544 MHz	2.048 MHz
Logic Input L (sync mode only)	2.048 MHz	1.536 MHz or 1.544 MHz
Logic Input H (open) (sync mode only)	1.536 MHz or 1.544 MHz	2.048 MHz

long-frame sync operation

Both FSX and FSR must be three or more bit-clock periods long to use the long-frame sync mode with timing relationships as shown in Figure 2. Using the transmit frame sync (FSX), the device detects whether a short- or long-frame sync pulse is being used. For 64-kHz operation, the frame-sync pulse must be kept low for a minimum of 160 ns. The rising edge of FSX or BCLKX, which ever occurs later, enables the DX 3-state output buffer. The first bit clocked out is the sign bit. The next seven rising edges of BCLKX edges clock out the remaining seven bits. The falling edge of BCLKX following the eighth rising edge or FSX going low, whichever occurs later, disables DX. A rising edge on FSR, the receive frame sync pulse, causes the PCM data at DR to be latched in on the next eight falling edges of BCLKR (BCLKX in synchronous mode). The long-frame sync pulse can be used in either the synchronous or asynchronous mode.

PRINCIPALS OF OPERATION

transmit section

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors. Gains in excess of 20 dB across the audio pass band are possible via low noise and wide bandwidth. The operational amplifier drives a unity-gain filter consisting of an RC active prefilter followed by an eight-order switched-capacitor band-pass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. As per μ-law (TP3064B and TP13064B) or A-law (TP3067B and TP13067B) coding conventions, the ADC is a companding type. A precision voltage reference provides a input overload of nominally 2.5-V peak. The sampling of the filter output is controlled by the FSX frame-sync pulse. Then the successive-approximation encoding cycle begins. The 8-bit code is loaded into a buffer and shifted out through DX at the next FSX pulse. The total encoding delay is approximately 290 μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration (see Table 2).

Table 2. Encoding Format at DX Output

	TP3064B, TP13064B μ-LAW	TP3067B, TP13067B A-LAW (INCLUDES EVEN-BIT INVERSION)
V_I = + Full scale	1 0 0 0 0 0 0 0	1 0 1 0 1 0 1 0
V_I = 0	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
V_I = – Full scale	0 0 0 0 0 0 0 0	0 0 1 0 1 0 1 0

receive section

The receive section consists of an expanding DAC that drives a fifth-order low-pass filter clocked at 256 kHz. The decoder is μ-law (TP3064B and TP13064B) or A-law (TP3067B and TP13067B) and the fifth-order low-pass filter corrects for the (sin x)/x attenuation caused by the 8-kHz sample/hold. The filter is followed by a second-order RC active post-filter with its output at VFRO. The receive section is unity-gain but gain can be added by using the power amplifiers. At FSR, the data at DR is clocked in on the falling edge of the next eight BCLKR (BCLKX) periods. At the end of the decoder time slot, the decoding cycle begins and 10 μs later the decoder DAC output is updated. The decoder delay is about 10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (1/2 frame), or a total of approximately180 μs.

receive power amplifiers

Two inverting-mode power amplifiers are provided for directly driving a match-line interface transformer. The gain of the first power amplifier can be adjusted to boost the ±2.5-V peak output signal from the receive filter up to the ±3.3-V peak into an unbalanced 300-Ω load, or ±4 V into an unbalanced 15-kΩ load. The second power amplifier is internally connected in unity-gain inverting mode to give 6-dB signal gain for balanced loads.

Maximum power transfer to a 600-Ω subscriber line termination is obtained by differentially driving a balanced transformer with $\sqrt{2}$:1 turns ratio, as shown in Figure 3. A total peak power of 15.6 dBm can be delivered to the load plus termination.

APPLICATION INFORMATION

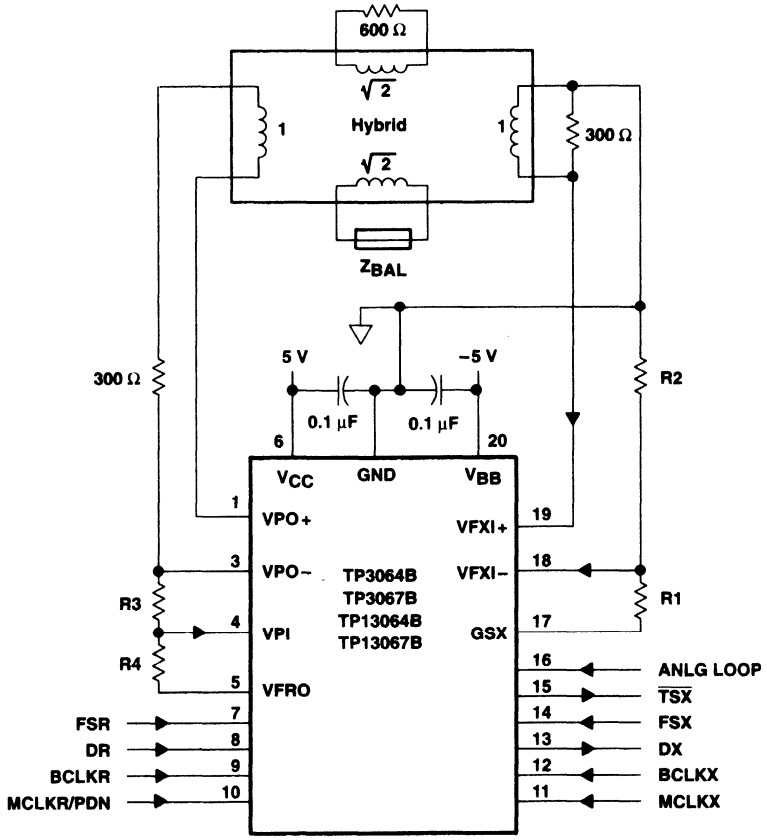
power supplies

While the pins of the TP1306xB and TP306xB families are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed ensuring that ground is connected to the device before any other connections are made. In applications where the printed-circuit board can be plugged into a hot socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to ANLG GND. This minimizes the interaction of ground return currents flowing through a common bus impedance. V_{CC} and V_{BB} supplies should be decoupled by connecting 0.1-μF decoupling capacitors to this common point. These bypass capacitors must be connected as close as possible to V_{CC} and V_{BB}.

For best performance, the ground point of each codec/filter on a card should be connected to a common card ground in star formation rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10-μF capacitors.

APPLICATION INFORMATION

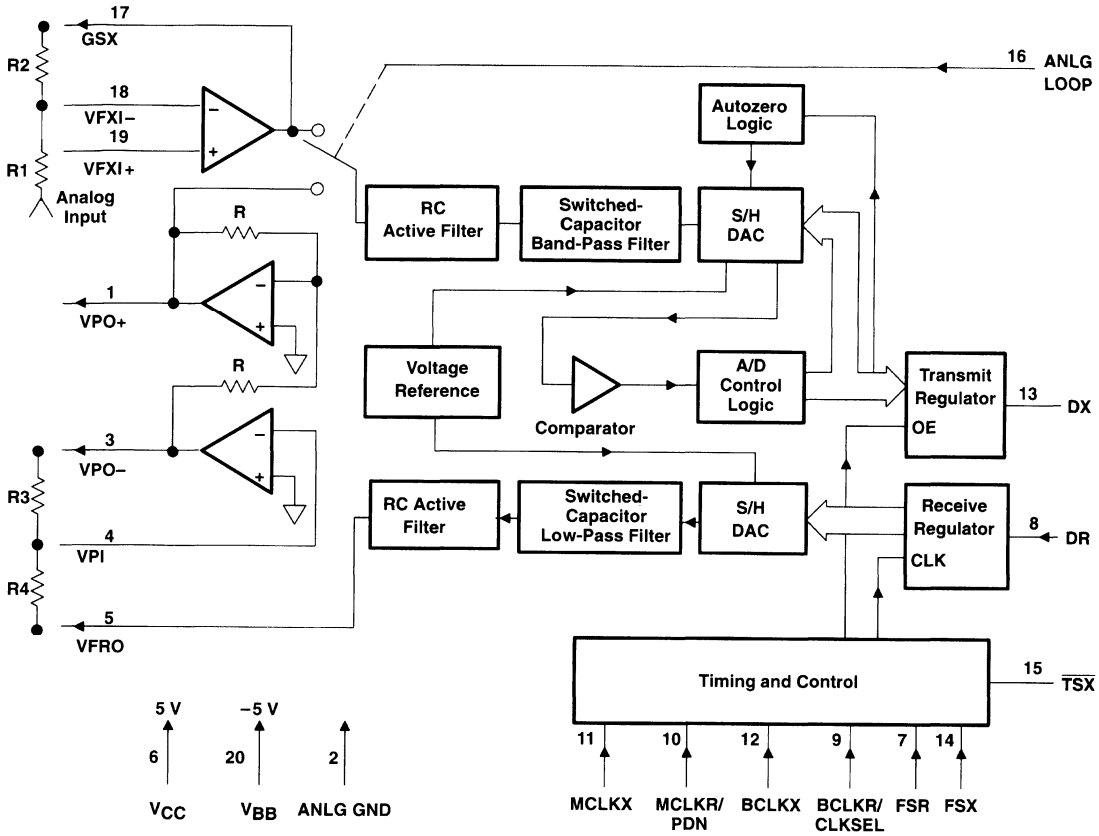


NOTES: A. Transmit gain = 20 log $\left(\frac{R1 + R2}{R2}\right)$, (R1 + R2) ≥ 10 kΩ

B. Receive gain = 20 log $\left(\frac{2 \times R3}{R4}\right)$, R4 ≥ 10 kΩ

Figure 4. Typical Synchronous Application

APPLICATION INFORMATION



Transient Voltage Suppressors

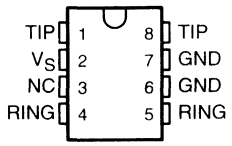
SCTS040A – JUNE 1989 – REVISED MAY 1996

- **Meet or Exceed Bell Standard LSSGR Requirements**
- **Externally-Controlled Negative Firing Voltage . . . –70 V Max**
- **Accurately Controlled, Wide Negative Firing Voltage Range . . . –5 V to –65 V**
- **Surge Current (see Note 1):**

	TCM1030	TCM1060
10/1000	16 A	30 A
10/160	25 A	45 A
2/10	35 A	50 A

- **High Holding Current**
  - **TCM1030 . . . 100 mA Min**
  - **TCM1060 . . . 150 mA Min**

D OR P PACKAGE
(TOP VIEW)



NC – No internal connection
The D package is available taped and reeled. Add R suffix (i.e., TCM1030DR).

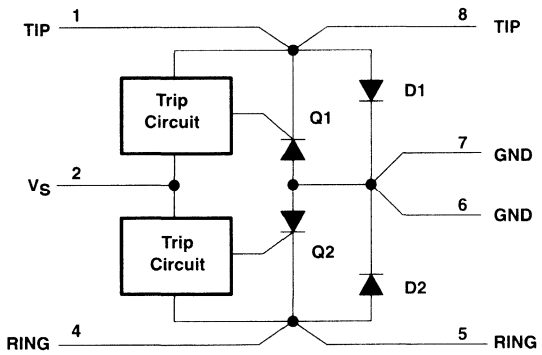
description

The TCM1030 and TCM1060 dual transient-voltage suppressors are designed specifically for telephone line-card protection against lightning and transients (voltage transients) induced by ac lines. One of the TIP terminals (pin 1 or 8) and one of the RING terminals (pin 4 or 5) are connected to the tip and ring circuits of a SLIC (subscriber-line interface circuit). The battery feed connections between the SLIC and the subscriber line are from the remaining TIP (pin 1 or 8) and RING (pin 4 or 5) through the TCM1030 or the TCM1060 to the tip and ring lines. Transients are suppressed between tip and ground, and ring and ground.

Positive transients are clamped by diodes D1 and D2. Negative transients that are more negative than V_S cause the SCRs, Q1 and Q2, to crowbar. The high holding current of the SCRs prevent dc latchup as the transient subsides.

The TCM1030 and TCM1060 are characterized for operation from –40°C to 85°C.

functional block diagram



NOTE 1: The notation 10/1000 refers to a waveshape having t_r = 10 μs and t_w = 1000 μs ending at 50% of the peak value. The notation 10/160 is t_r = 10 μs and t_w = 160 μs. The notation 2/10 is t_r = 2 μs and t_w = 10 μs.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

TCM1030 nonrepetitive peak surge current (see Note 1): 10/1000 ..... ±16 A
10/160 ..... ±25 A
2/10 ..... ±35 A
TCM1060 nonrepetitive peak surge current (see Note 1): 10/1000 ..... ±30 A
10/160 ..... ±45 A
2/10 ..... ±50 A
Nonrepetitive peak surge current, t_w = 10 ms, half sinewave (see Note 2) ..... 5 A
Continuous 60-Hz sinewave at 1 A ..... 2 s
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range, T_{stg} ..... −40°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1 The notation 10/1000 refers to a waveshape having t_r = 10 μs and t_w = 1000 μs ending at 50% of the peak value. The notation 10/160 is t_r = 10 μs and t_w = 160 μs. The notation 2/10 is t_r = 2 μs and t_w = 10 μs.

2. This value applies when the case temperature is at or below 85°C. The surge current may be repeated after the device has returned to thermal equilibrium.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	377 mW
P	1000 mW	8.0 mW/°C	520 mW

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TCM1030			TCM1060			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{CF}	Forward clamping voltage (diode forward voltage) (see Note 3)	I_{FM} = 1-A transient		1.2	2		1.2	2	V
		I_{FM} = 10-A transient		2.5	4		2	4	
		I_{FM} = 16-A transient		4	5		2.5	5	
		I_{FM} = 30-A transient					3.1	5	
$V_{C(R)}$	Reverse clamping voltage (SCR on-state voltage) (see Note 3)	I_{TM} = 1-A transient		1.2	2		1.2	2	V
		I_{TM} = 10-A transient		2.5	4		2.5	4	
		I_{TM} = 16-A transient		4	5		3	5	
		I_{TM} = 30-A transient					4.8	7	
$I_{I(trip)}$	Trip current (see Note 4)	V_S = −50 V	−100		−325	−100		−325	mA
I_H	Holding current	V_S = −50 V	−100			−150			mA
$V_{I(trip)}$	Trip voltage	V_S = −50 V, I = trip current	−50		−55	−50		−55	V
		V_S = −65 V, I = trip current	−65		−70	−65		−70	
$I_{I(stby)}$	Standby current	TIP and RING at −85 V or GND, V_S = −85 V			±5			±5	μA
	Transient overshoot voltage	V_S = −50 V, t_r = 10 ns		2.5			2.5		V
C_{off}	Off-state (high impedance) capacitance	TIP and RING at −50 V		25			25		pF
		TIP and RING at GND		50			50		
dv/dt	Critical rate of rise of off-state voltage (see Note 5)	V_S open, V_S = −50 V		−1			−1		kV/μs

† All typical values are at T_A = 25°C.

NOTES: 3. The current flows through one TIP (or RING) terminal and one of the GND terminals. The voltage is measured between the other TIP (or RING) terminal and the other GND terminal. Measurement time ≤ 1 ms.

4. The negative value of trip current refers to the current flowing out of TIP or RING on the line side that is sufficient in magnitude to trigger the SCRs. Measurement time ≤ 1 ns.

5. The critical dv/dt is measured using a linear rate of rise with the maximum voltage limited to −50 V with V_S connected to TIP or RING being measured.

TYPICAL CHARACTERISTICS

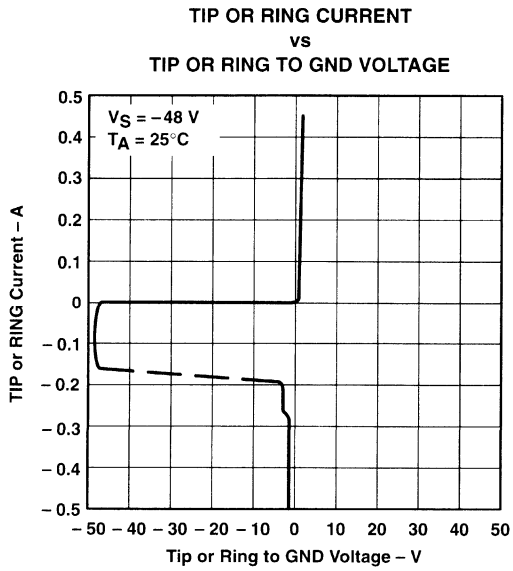


Figure 1

APPLICATION INFORMATION

The trip voltage represents the most negative level of stress applied to the system. Positive transients are clamped by diodes D1 and D2. When a negative transient is applied, current flows from V_S to TIP or RING where the transient voltage is applied. When the current through TIP or RING reaches the pulse-trip current, the SCR turns on and shorts TIP or RING to GND. The majority of the transient energy is dissipated in the external resistor (nominally 100 Ω for the TCM1030 and 50 Ω for the TCM1060). Current into V_S ceases when the SCR turns on. When the energy of the transient has been dissipated so that the current into TIP or RING due to the transient plus the battery feed supply is less than the holding current, the SCR turns off.

To help ensure reliability and consistency in the firing voltage, it is recommended that two capacitors be connected between V_S and GND, as close to the device terminals as possible. One capacitor should be a 0.1 μF, 100 V ceramic unit and the other, a 0.47 μF, 100 V stacked-film (not wound) metalized plastic capacitor. If inductance is present in the line to V_S, these capacitors help prevent overshoot in the firing voltage during fast rise-time transients.

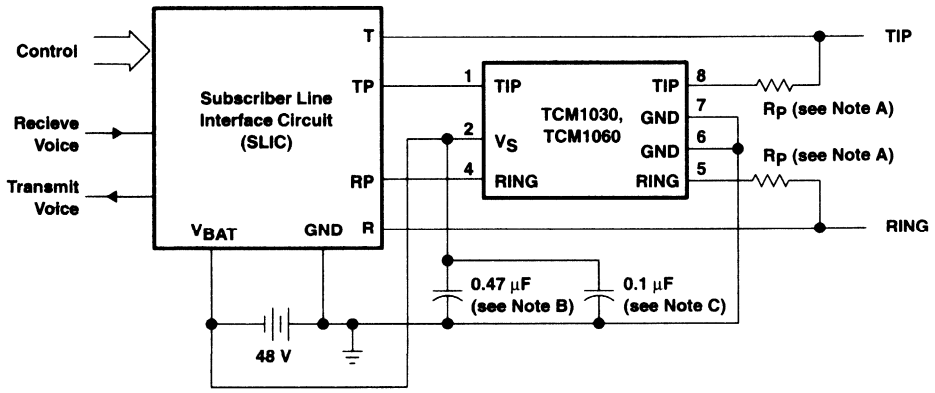
To avoid dc latchup after the SCR has fired, the current must be less than the holding current, I_H. To prevent this from happening, the line feed current must be limited to the following conditions:

$$\frac{V_{TP} - V_{RP}}{R_{line} + 2R_p} < I_H$$

where V_{TP} and V_{RP} are the voltages on TIP and RING, respectively, of the TCM1030 or TCM1060. Induced ac currents into TIP or RING (e.g., power-line inductive coupling) must be less than the trip current to prevent the SCR from firing.

APPLICATION INFORMATION

Line short-circuits to external power sources can damage the suppressor due to excessive power dissipation. Conventional protection techniques, such as fuses or PTC (positive temperature coefficient) thermistors, should be used to eliminate or reduce the fault current.



NOTES: A. RP is 100 Ω minimum for TCM1030 and 50 Ω minimum for TCM1060.
B. 0.47 µF, 100 V stacked film metalized plastic capacitor
C. 0.1 µF, 100 V ceramic capacitor

Figure 2. Typical Line-Card Application Circuit

4 RF for Telemetry and RKE

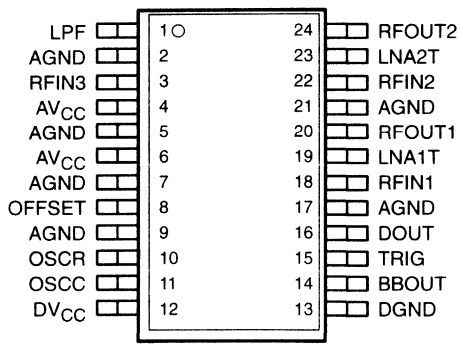
- **Wide VHF/UHF Frequency Range: 200 MHz to 450 MHz for World-Wide Remote Control Frequency Compatibility**
- **High Receiver Sensitivity . . . –103 dBm at 315 MHz**
- **Accepts Baseband Data Rates from 500 Hz to 10 kHz**
- **Manchester Decoded and Raw Baseband Outputs for Easy Interface to TI MARCSTAR™ or Other Serial Data Decoders and Microcontrollers**
- **TRF (Tuned Radio Frequency) Design Eliminates Local Oscillator (No Emissions) and Reduces Many Government Type-Approvals (Including FCC)**
- **No Mixing Products Result in No Image to Reject**
- **Adjustable Internal Sampling Clock Set By External Components**
- **Internal Amplifier and Comparator for Amplification and Shaping of Low-Level Input Signals with Average-Detecting Autobias Adaptive Threshold Circuitry for Improved Sensitivity**
- **Minimum External Component Count and Surface-Mount Packaging for Extremely Small Circuit Footprint – Typically Replaces more than 40 Components in an Equivalent Discrete Solution**
- **No Manual Alignment When Using SAW Filters**
- **Advanced Submicron BiCMOS Process Technology for Minimum Power Consumption**

description

The TRF1400 VHF/UHF RZ ASK Remote Control Receiver is a member of the MARCSTAR (Multichannel Advanced Remote Control Signalling Transmitter and Receiver) family of remote control serial data devices specifically designed for RZ ASK (Return-to-Zero Amplitude-Shift Keyed) communications systems operating in the 200 MHz – 450 MHz band. These devices are targeted for use in automotive and home security systems, garage door openers, remote utility metering, and other low-power remote control and telemetry systems.

A complete RZ ASK receiver solution on a chip, the TRF1400 requires only a minimum of external components for operation. This significantly reduces the complexity and footprint of new designs compared with current discrete receiver designs. The TRF1400 requires no manual alignment when using external SAW (surface acoustic wave) filters. For a lower cost solution, the device is also compatible with external LC components.

DW PACKAGE
(TOP VIEW)



The TRF1400 also includes several on-chip features that would normally require additional circuitry in a receiver system design. These include two low-noise front-end amplifiers, an RF amplifier/comparator for detection and shaping of input signals, and a demodulated RZ ASK baseband TTL-level output that readily interfaces to

ADVANCE INFORMATION

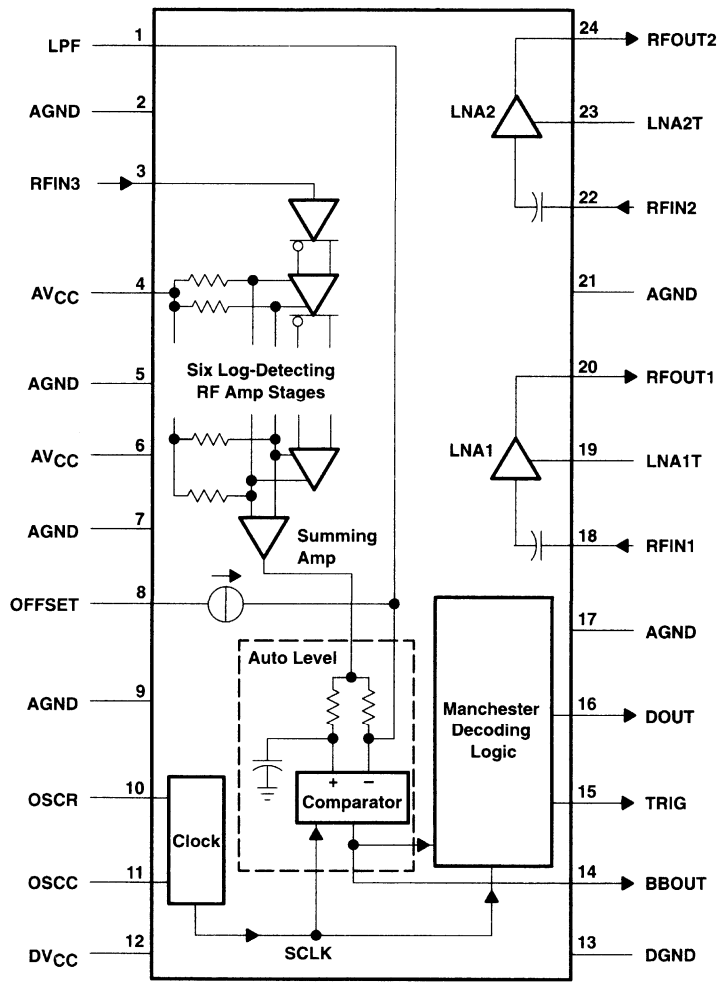
MARCSTAR is a trademark of Texas Instruments Incorporated.

description (continued)

self-synchronizing devices such as the TI rolling-code MARCSTAR decoder (TRC1300/TRC1315). Also included is on-chip Manchester decoding logic that provides a specially formatted TTL data output, synchronized with a trigger output, for easy interface to any microcontroller using Manchester-encoded data.

The TRF1400 VHF/UHF RZ ASK remote control receiver is available in a 24-pin SOIC (DW) package, and is characterized for operation over the temperature range of –40°C to 85°C. The DW package is available taped and reeled. Add R suffix to device type (e.g., TRF1400R).

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	2, 5, 7, 9, 17, 21		Analog ground for all internal analog circuits. AGND is not internally connected to digital ground (DGND). All analog signals are referenced to this terminal.
AV_{CC}	4, 6		Positive power supply voltage for all analog circuits — 4.5 V to 5.5 V.
BBOUT	14	O	Baseband data output. This is the demodulated envelope of the recovered RF signal. BBOUT is active with any received ASK signal coding format.
DGND	13		Digital ground for all internal logic circuits. DGND is not internally connected to analog grounds (AGND).
DOUT	16	O	Data output. This data is a binary, TTL representation of the baseband data, and is only meaningful when Manchester-encoded ASK data is received. DOUT is active high and is internally pulled down.
DV_{CC}	12		Positive power supply voltage for all digital circuits — 4.5 V to 5.5 V. For best noise performance, DV_{CC} should connect to AV_{CC} at the power supply, not at the TRC1400.
LNA1T	19		Low-noise amplifier (LNA) #1 ground termination. LNA1T should be connected to AGND through a parallel resistor-capacitor bias network. If left unconnected, the LNA is disabled.
LNA2T	23		Low-noise amplifier (LNA) #2 ground termination. LNA2T should be connected to AGND through a parallel resistor-capacitor bias network. If left unconnected, the LNA is disabled.
LPF	1		External low-pass capacitor used in the average-detecting adaptive threshold circuitry.
OFFSET	8		Connection to external offset resistor. This resistor (1 MΩ suggested) sets the internal threshold detector offset voltage. Lowering the value of this resistor decreases device sensitivity.
OSCC	11		Internal oscillator frequency-setting capacitor. This capacitor, connected between OSCC and GND, in conjunction with a resistor connected between OSCR and OSCC determines the speed of the internal clock oscillator (SCLK). The SCLK signal is used for processing the demodulated incoming data stream and controls the Manchester decoding and timing recovery logic sections of the device. The internal oscillator must be set to 10× the received Manchester data rate for valid TRIG and DOUT, or to 5× the received baseband data rate.
OSCR	10		Internal oscillator frequency-setting resistor. This resistor, connected between OSCR and OSCC, in conjunction with a capacitor connected between OSCC and GND determines the speed of the internal oscillator (SCLK). The SCLK signal is used for processing the demodulated incoming data stream and controls the Manchester decoding and timing recovery logic sections of the device. The internal oscillator must be set to 10× the received Manchester data rate for valid TRIG and DOUT, or to 5× the received baseband data rate.
RFIN1	18	I	RF input to first low-noise, high-gain amplifier stage.
RFIN2	22	I	RF input to second low-noise, high-gain amplifier stage.
RFIN3	3	I	RF input to the detecting RF amplifier stages. Filtered RF in the form of AM RZ ASK data at frequencies between 200 MHz and 450 MHz, at a baud rate between 500 Hz and 20 kHz can be applied to this terminal for detection and decoding.
RFOUT1	20	O	RF output of the first low-noise, high-gain amplifier.
RFOUT2	24	O	RF output of the second low-noise, high-gain amplifier. Typically, the input of an external SAW or LC filter is connected to this terminal.
TRIG	15	O	Trigger output. TRIG pulses to indicate each new received data cell and is only meaningful when Manchester-encoded ASK data is received. TRIG is active high and is internally pulled down.

ADVANCE INFORMATION

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, AVCC, DVCC (see Note 1) . . . . . −0.6 to 6
Input voltage range, V_I . . . . . −0.6 to 6
Continuous total power dissipation . . . . . 180 mW
Operating free-air temperature range, T_A . . . . . −55°C to 85°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
ESD protection, all terminals: human body model . . . . . 2 kV
machine model . . . . . 200 V
JEDEC latchup . . . . . 150 mA or 11 V

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5		5.5	V
Input frequency, f_{in}	200		450	MHz
Operating free-air temperature, T_A	−40		85	°C
Minimum permissible AM modulation of RF envelope, measured at −102 dBm at RFINPUT		25%		

electrical characteristics as measured in the test circuit detailed in Figures 1 through 6 with f_{in} = 315 MHz over recommended ranges of supply voltage and operating free-air temperature, typical values are at V_{CC} = 5 V and T_A = 25°C (unless otherwise noted)

current consumption

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
I_{CC}	Average supply current from V_{CC}	I/O pins terminated with typical loads		3	mA

digital interface

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	DOUT, TRIG, BBOUT	I_{OH} = 3.2 mA	V_{CC}−0.5		V
V_{OL}	Low-level output voltage		I_{OL} = −3.2 mA		0.5	V

VSWR (voltage standing-wave ratio), ripple rejection

PARAMETER	MIN	TYP	MAX	UNIT
VSWR into 50 Ω (requires external LC matching network), RFIN1, RFOUT1, RFIN2, RFOUT2, RFIN3		2:1		V/V
Ripple rejection, 1 MHz (injected at AV_{CC} and DV_{CC}), measured at BBOUT while maintaining BER = 3/100 with desired carrier at −50 dBm (see Note 2)		6% V_{CC}		

NOTE 2: BER (bit error rate — errors/number of bits) is qualified by integration of logic-level pulses (>50% high = 1, <50% low = 0).

RF sensitivity/overload

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
RF input (average) at test board RF input required for BER 3/100 (see Note 2) at 5 kHz baseband data rate, 2.5 kHz Manachester data rate	V_{CC} = 5 V, T_A = 25°C, f_{in} = 315 MHz, external SAW preselector bandpass filter (see Note 3)			−103	dBm
Overload signal at fc with BER 3/100 at 5 kHz (see Note 2) baseband data rate, 2.5 kHz Manchester data rate	V_{CC} = 5 V, T_A = 25°C, f_{in} = 315 MHz		−20		dBm

NOTES: 2. BER (bit error rate = errors/number of bits) is qualified by integration of logic-level pulses (>50% high = 1, <50% low = 0).
3. The SAW bandpass filter must have a rejection level greater than or equal to 50 dB at ±0.5 fc, insertion loss of less than or equal to 3 dB, and a −3 dB passband width of 0.2% fc.

oscillator (internal clock)

PARAMETER	MIN	MAX	UNIT
Sample clock frequency, SCLK (5× baseband data rate, 10× Manchester data rate)	2.5	50	kHz
Frequency spread (process variation, temperature, V_{CC}), not including external component tolerance		±5%	

timing requirements

RF input data (see Figure 7)

		MIN	MAX	UNIT
t_r	Rise time, RF input data		0.1 t_{c1}	µs
t_f	Fall time, RF input data		0.1 t_{c1}	µs

received data

		MIN	MAX	UNIT
	Baseband data frequency AM RZ ASK	0.5	10	kHz
	Manchester data frequency AM RZ ASK	0.25	5	kHz
	Pulse period tolerance for synchronization, valid TRIG and DOUT data		±8%	
	Pulse duty cycle for synchronization, valid TRIG and DOUT data	49%	51%	
t_x	Dead time between wakeup time and frame start time (for synchronization valid, TRIG and DOUT data) (see Figure 8)	38 ÷ SCLK	317 ÷ SCLK	ms
t_{w3}	Duration, modulated RF carrier (see Figure 9)	100	2000	µs

switching characteristics

device latency, for BBOUT, TRIG, DOUT (see Figure 9)

	PARAMETER	MIN	TYP	MAX	UNIT
	Delay time between power applied and output signal at BBOUT		10		ms
	Demodulation delay time across device (RFINPUT to BBOUT)		10		µs
t_{d1}	Delay time between BBOUT ↑ and TRIG ↑	1.9 ÷ SCLK	2.5 ÷ SCLK	3.2 ÷ SCLK	µs
t_{d2}	Delay time between DOUT ↑ and TRIG ↑		0.5 ÷ SCLK		µs

RF carrier (see Figure 9)

	PARAMETER	MIN	TYP	MAX	UNIT
t_{w0}	Duration, logic 0 data cell		2 t_{w3}		µs
t_{w1}	Duration, logic 1 data cell		2 t_{w3}		µs
t_{w2}	Duration, trigger pulse		0.5 ÷ SCLK		µs

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TRF1400 electrical characteristics were measured with the device connected in the circuit shown in Figure 1.

As with any RF design, the successful integration of the device into a circuit board relies heavily on the layout of the board and the quality of the external components. Figure 2 through Figure 6 show layout artwork for the production of the circuit board used to obtain the TRF1400 electrical characteristics. Table 1 lists the parts required to complete the test circuit, which demonstrates TRF1400 performance at 315 MHz. Specified component tolerances and where applicable, Q, should be observed during the selection of parts.

A complete set of Gerber photoplotter files for the circuit board can be obtained from any TI Field Sales Office.

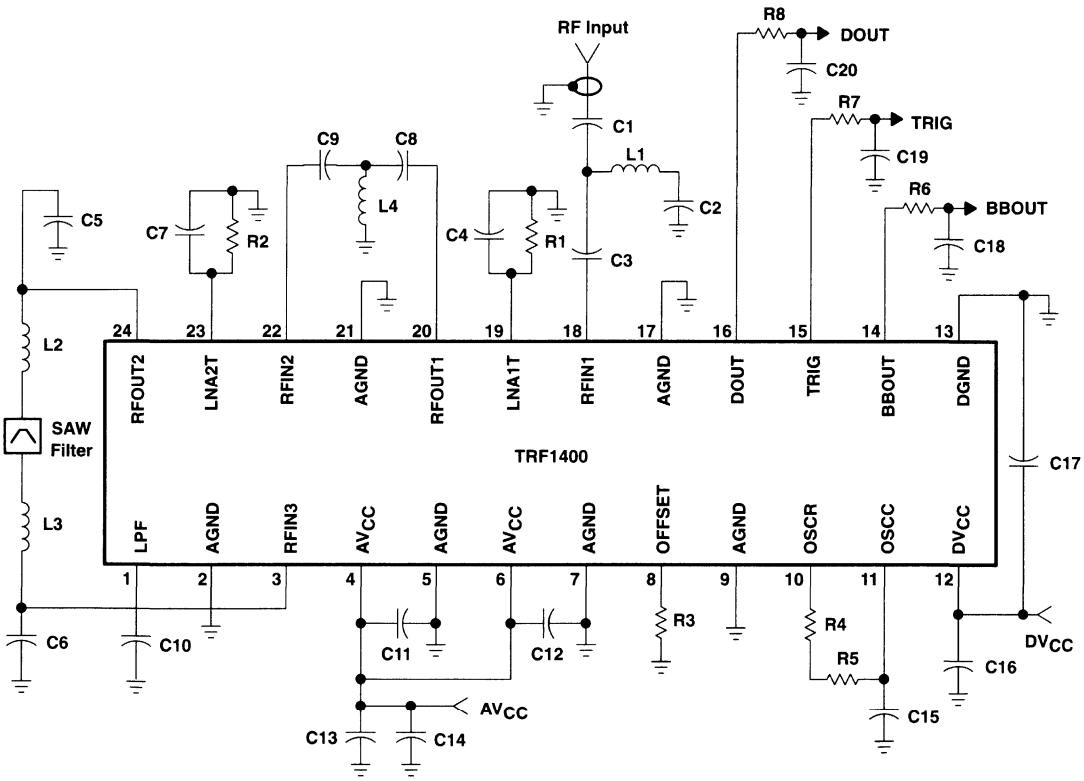

Figure 1. TRF1400 Test Circuit

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION

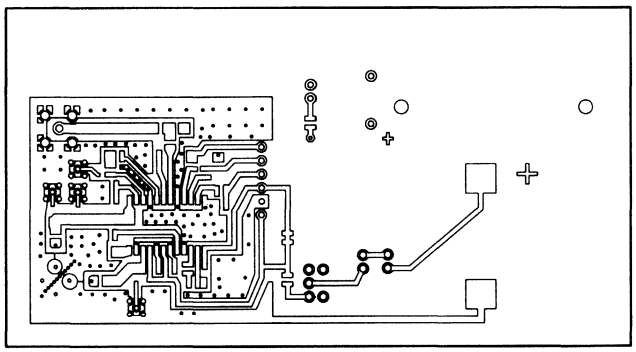

Figure 2. TRF1400 Test Circuit Board Layout — Top Side

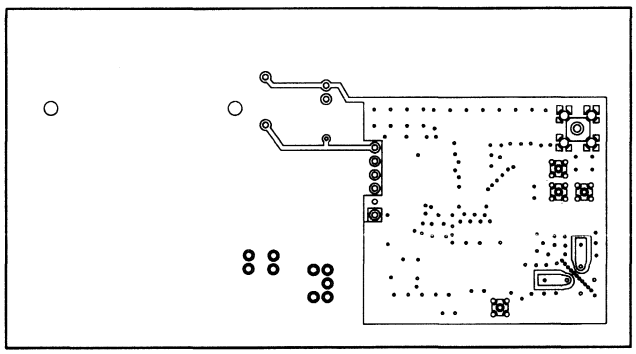

Figure 3. TRF1400 Test Circuit Board Layout — Bottom Side

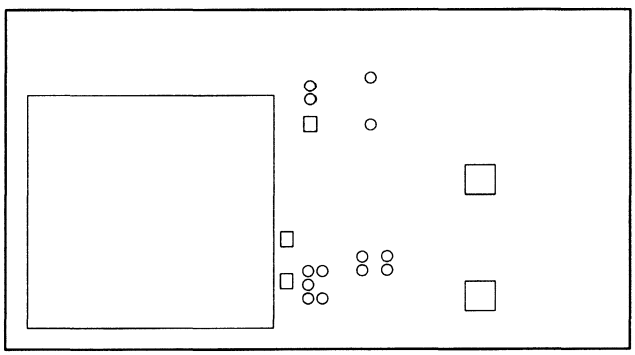

Figure 4. TRF1400 Test Circuit Board Solder Mask — Top Side

PARAMETER MEASUREMENT INFORMATION

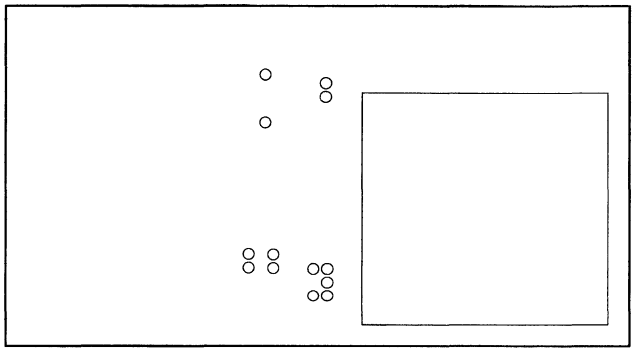

Figure 5. TRF1400 Test Circuit Board Solder Mask — Bottom Side

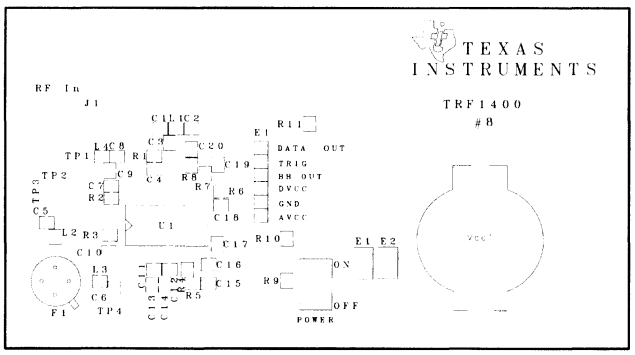

Figure 6. TRF1400 Test Circuit Board Silk Screen

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

Table 1. TRF1400 315-MHz Test Circuit Parts List

DESIGNATORS	DESCRIPTION	SIZE / VALUE / @ FREQ.	MANUFACTURER	MANUFACTURER P/N
C1	Capacitor	4 pF	Murata	GRM40C0G040C050V
C2	Capacitor	22 pF	Murata	GRM40C0G220J050BD
C3	Capacitor	22 pF	Murata	GRM40C0G220J050BD
C4	Capacitor	100 pF	Murata	GRM40C0G101J050BD
C5	Capacitor	5 pF	Murata	GRM40C0G050D050BD
C6	Capacitor	1.5 pF	Murata	GRM40C0G1R5C050BD
C7	Capacitor	100 pF	Murata	GRM40C0G101J050BD
C8	Capacitor	3 pF	Murata	GRM40C0G030C050BD
C9	Capacitor	18 pF	Murata	GRM40C0G180J050BD
C10	Capacitor	0.047 µF	Murata	GRM40X7R473K050
C11	Capacitor	2200 pF	Murata	GRM40X7R222K050BD
C12	Capacitor	2200 pF	Murata	GRM40X7R222K050BD
C13	Capacitor	0.022 µF	Murata	GRM40X7R223K050BL
C14	Capacitor Tantalum†	4.7 µF	Sprague	293D475X9050D2T
C15	Capacitor	220 pF, 5%	Murata	GRM40C0G221J050BD
C16	Capacitor Tantalum†	4.7 µF	Sprague	293D475X9050D2T
C17	Capacitor	2200 pF	Murata	GRM40X7R222K050BD
C18	Capacitor	0.022 µF	Murata	GRM40X7R223K050BL
C19	Capacitor	2200 pF	Murata	GRM40X7R222K050BD
C20	Capacitor	0.022 µF	Murata	GRM40X7R223K050BL
E1	2-Pin Connector		3M	2340–6111–TN
E2	2-Pin Connector		3M	2340–6111–TN
E3	6-Pin Connector		3M	2340–6111–TN
S1–S2	Header shunts		3M	929952–10
F1	SAW filter	RF1211	RFM	RF1211
L1	Inductor	47 nH	Coilcraft	0805HS470TMBC
L2	Inductor	82 nH	Coilcraft	0805HS820TKBC
L3	Inductor	120 nH	Coilcraft	0805HS121TKBC
L4	Inductor	39 nH	Coilcraft	0805HS390TMBC
P1	RF SMA Connector		Johnson	142–0701–201
R1	Resistor	1200 Ω		
R2	Resistor	1200 Ω		
R3	Resistor	1M Ω		
R4	Resistor	130 KΩ, 1%		
R5	Resistor	0 Ω		
R6	Resistor	1K Ω		
R7	Resistor	100 Ω		
R8	Resistor	1K Ω		

† Tantalum capacitors are rated at 6.3 Vdc minimum.

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PARAMETER MEASUREMENT INFORMATION

Table 1. TRF1400 315-MHz Test Circuit Parts List

DESIGNATOR	DESCRIPTION	SIZE / VALUE / @ FREQ.	MANUFACTURER	MANUFACTURER P/N
R9	Resistor	680 Ω		
R10	Resistor	short		
R11	Resistor	330 Ω		
S1	Switch		NKK	G-12AP
Vcc1	Batttery Clip		Keystone	1061
B1X	Battery, Lithium	3.3-V Coin Cell (2 ea.)	Panasonic	CR2016
U1	Receiver	TRF1400	TI	TRF1400

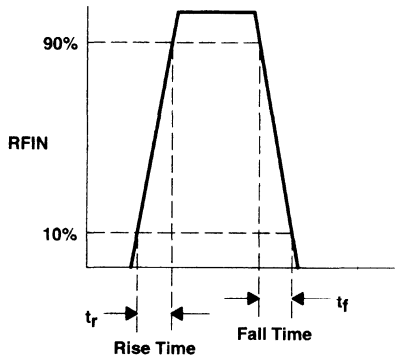


Figure 7. RFIN1 Rise and Fall Times

PARAMETER MEASUREMENT INFORMATION

Manchester data format and timing

The TRF1400 requires specific Manchester data formatting and timing to decode and output Manchester serial data. For the TRF1400 to output meaningful function data at the TRIG and DOUT terminals, the incoming RF signal must have the Manchester-encoded binary format and timing shown in Figure 8 (for 50 kHz SCLK). A wakeup time and frame-start time is required for the device to synchronize with the incoming data. The wakeup time is designated by a data-bit 0 and data-bit 1 data sequence repeated five times.

Figure 9 shows Manchester-encoded function data timing.

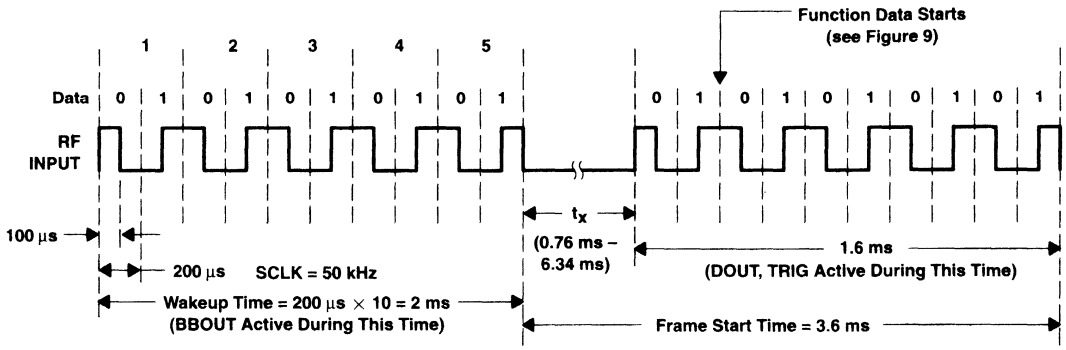


Figure 8. Manchester-Encoded RF Binary Data Format at RF Input

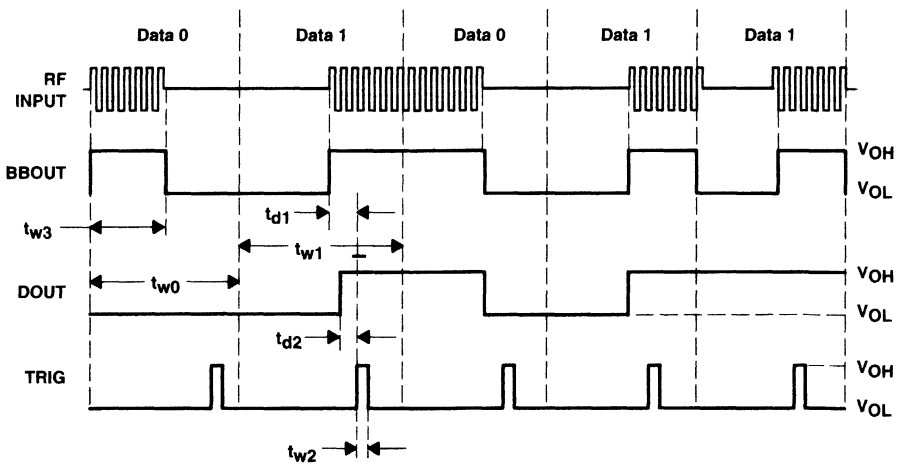


Figure 9. Manchester-Encoded Function Data Timing Diagram

ADVANCE INFORMATION

PRINCIPLES OF OPERATION

general

The TRF1400 VHF/UHF RZ ASK Remote Control Receiver demodulates AM RZ ASK modulated RF carriers between 200 MHz and 450 MHz with a 500-Hz to 10-kHz baseband data rate or a 250-Hz to 5-kHz Manchester data rate.

signal reception

The RF signal is collected by an antenna and then passed through an LC matching network to bandpass-filter the signal and compensate for various antenna loading impedances. The signal is then input to the RFIN1 terminal of the TRF1400.

signal path through device

The RF signal applied to the RFIN1 terminal is amplified by LNA1 and LNA2. The combined gain of the two LNAs is 40 dB, with a 1-dB compression point of –80 dBm, and a noise figure of 5 dB (nominal). The amplified signal is output at RFOUT2 and enters an external preselector bandpass filter before being applied to the third stage of amplification at terminal RFIN3.

The third stage of amplification consists of a single-ended-input to differential-output amplifier followed by six high-gain differential log-detecting amplifier stages with an equivalent gain of 60 dB (nominal). First, the signal is converted to a differential signal for increased noise immunity. Next, the differential signal is passed through the six high-gain differential log-detecting amplifiers, forming a detection circuit. Each log-detecting amplifier is biased such that when an RF signal is present, an imbalance is caused in its bias circuit. The imbalance in each of the six stages is converted to a voltage and then summed into a baseband envelope representation of the RF signal. This signal then passes through an autoleveling circuit before being applied to a comparator to produce the TTL-level baseband signal output that appears at BBOUT. An external low-pass filter connected to BBOUT attenuates high-frequency transients in the output signal.

The demodulated signal is also applied to the Manchester decoding and timing recovery logic section of the TRF1400. The Manchester decoding section has two outputs, TRIG and DOUT, which should be externally low-pass filtered to attenuate high frequency transients. The signals appearing at these outputs are meaningful only when the received Manchester-encoded data is formatted and timed as shown in Figure 9.

When Manchester-encoded data is received and demodulated, Manchester serial data is output at DOUT and a trigger pulse is output at TRIG. The TRIG pulse rises at the start of each decoded data bit appearing at DOUT. The DOUT and TRIG outputs are not required in an application incorporating a TI MARCSTAR TRC1300/1315 Remote Control Transmitter/Receiver due to the autosynchronization available on that decoder.

frequency adjustment

The TRF1400 requires no manual alignment. The receive frequency is dependent only on the choice of external matching networks and preselecting filters used. In that respect, the user has only to stock a different set of external components for each frequency, and no manual alignment or end-of-line frequency programming need be performed.

decoder interface

For baseband operation, the TRC1300/1315 4-function, 40-bit rolling-code decoder can be interfaced directly to the TRF1400 using the baseband-data output (BBOUT) of the device. The TRC1300/1315 decodes the received data into instructions that it then executes.

For Manchester operation, a standard microcontroller decoder must know when to poll its input for data. The TRF1400 provides an output terminal (TRIG) for this purpose that pulses on each valid received data cell . In this system configuration, Manchester-encoded binary data must be used in the format described below to allow the TRF1400 to synchronize properly and produce the TRIG and DOUT outputs.

PRINCIPLES OF OPERATION

external components and device performance

While the TRF1400 uses a minimum of external components in the typical application, the choice of those components greatly affects the performance of the device. When a SAW preselector is used, the selectivity (out-of-band rejection) and sensitivity of the TRF1400 are optimized as a result of the high Q of the SAW devices. If an LC preselector is used, these parameters change and the overall performance of the TRF1400 is reduced, but can still meet the requirements of many end-equipment applications.

An external resistor connected between OFFSET and ground adjusts the internal offset voltage of the receiver decoding section to maximize the noise rejection of the device. While a 1-MΩ resistor is suggested, this value can be changed to minimize toggling of outputs DOUT, TRIG, and BBOUT during periods of nonvalid received code.

internal clock/synchronization

An internal clock (SCLK) is used by the TRF1400 for processing the demodulated incoming data stream and for controlling the Manchester-decoding and timing-recovery logic sections of the device. The frequency of SCLK is set by an external resistor connected between the OSCR and OSCC terminals and an external capacitor connected between OSCC and GND, and is adjustable between 2.5 kHz and 50 kHz.

For baseband output, SCLK is set to 5× the received baseband data rate (500 Hz to 10 kHz). Incoming baseband data is then sampled at 5× its transmitted data rate. TTL-level baseband data is output at BBOUT whenever the TRF1400 receives ASK-modulated data in any format. This provides compatibility with systems that use other code formatting, and whose serial data decoders do not require the DOUT or TRIG outputs from the receiver.

For Manchester data output, SCLK must be set to 10× the received Manchester-encoded data rate (250 Hz to 5 kHz), for the output signals at TRIG and DOUT to be meaningful. The high sampling rate (10×) ensures accurate correlation of the received signal.

The received Manchester data rate (set by a clock on the transmitter/encoder end) can vary as much as ±8% and TRF1400 synchronization still results. This allows for frequency drift due to external component tolerances and temperature changes on the transmitter end. At the TRF1400 end, a ±8% frequency variation is also allowed. Thus, the total permissible frequency variation from transmitter clock to receiver clock can be as much as ±16%. For example, if a serial Manchester data rate of 1.5 kHz is used at the encoder/transmitter end, then the TRF1400 sample clock oscillator (SCLK) must be set to 10× the transmitted data rate, or 15 kHz. SCLK is allowed to vary ±8% in frequency, from 13.8 kHz to 16.2 kHz in this case, and the TRF1400 synchronizes successfully to the incoming data. The data rate of the incoming data itself can also vary the same amount. It is left to the user to design the system such that the transmitter/encoder data rate drifts ±8% or less. The TRF1400 can introduce as much as a ±5% frequency variation due to its internal tolerances and semiconductor process variations, so the external resistor and capacitor values used with the TRF1400 can have up to a ±3% value tolerance.

PRINCIPLES OF OPERATION

internal clock/synchronization (continued)

The internal clock speed is set by connecting a resistor between OSCR and OSCC and a capacitor between OSCC and GND. The following equation defines the sample clock (SCLK) speed as a function of the external resistor and capacitor:

$$F_{osc} = \frac{1}{1.386 \times (R_{ext} + R_s) \times (C_{ext} + C_p)}$$

Where: R_{ext} is the external resistor connected between OSCR and OSCC.
R_s is the internal series resistance, typically 100 Ω or less.
C_{ext} is the external capacitor connected between OSCC and GND.
C_p is parasitic capacitance and is dependant on board layout — typical value is 5 pF.

For minimum current draw, large values (in the thousands of ohms) for R_{ext} should be used. Typical R_{ext} values and the resulting SCLK frequency when C_{ext} = 100 pF are shown in Figure 10.

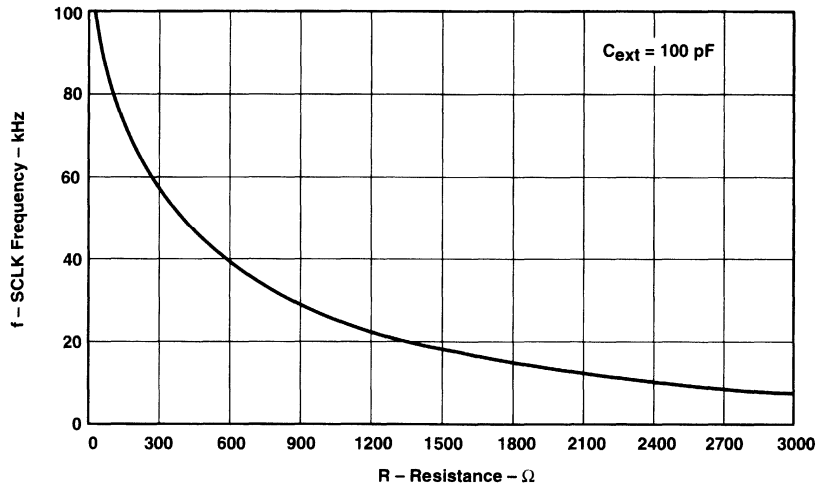


Figure 10. External Resistance Versus Sample Clock Frequency

ADVANCE INFORMATION

APPLICABLE REGULATIONS

Receiver design, as well as transmitter design, is regulated throughout the world. Since the TRF1400 is targeted for world-wide sales, the applicable standard for each region must be considered when the device is to be used in systems to be successfully marketed in that region. For this reason, the TRF1400 conforms to all requirements shown in Figure 11 and Table 2. The primary specifications of most of the standards address carrier frequency and spurious emissions.

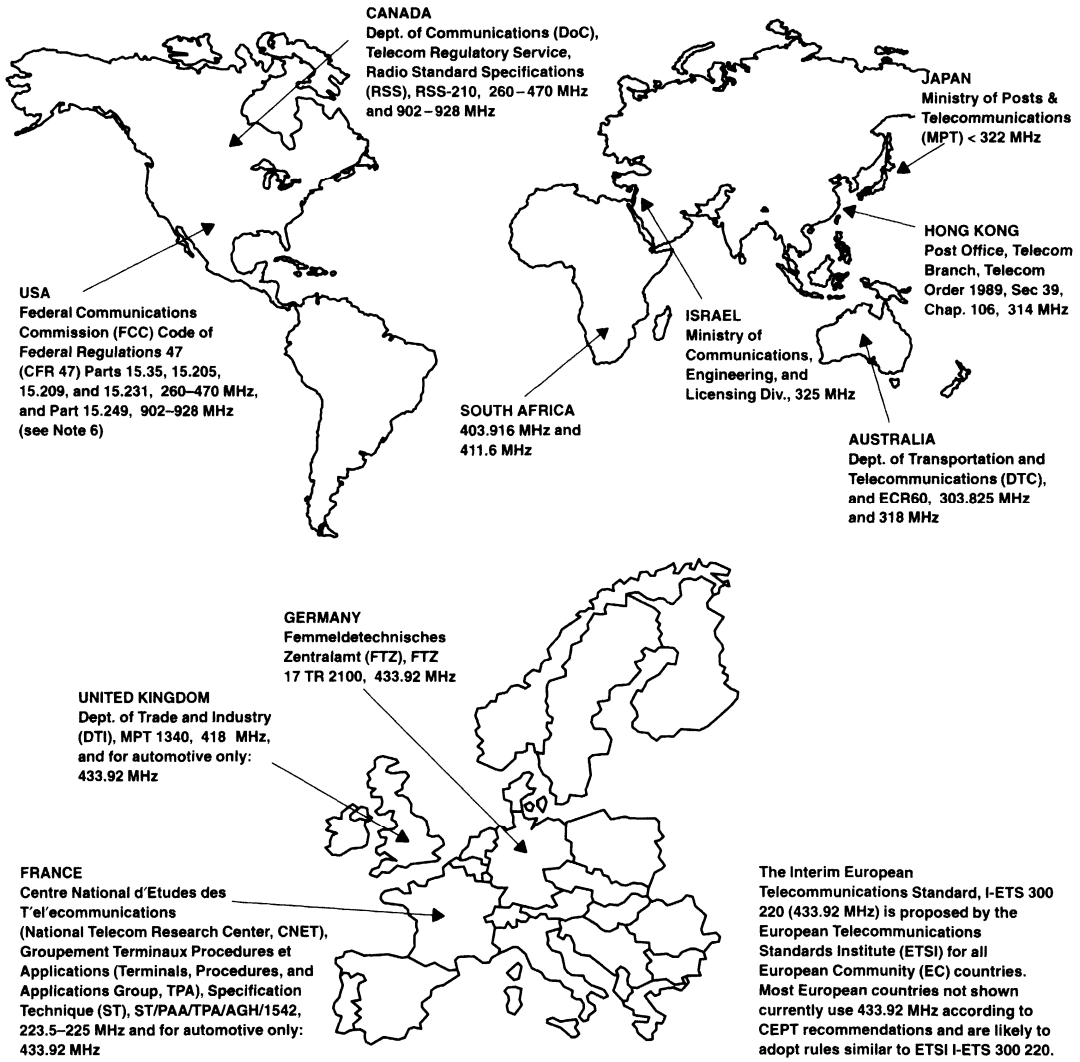


Figure 11. World-Wide Receiver Regulations

ADVANCE INFORMATION

APPLICABLE REGULATIONS

Table 2. World-Wide Regulations

REGION	REGULATION	FREQUENCY
USA	Federal Communications Commission (FCC) Code of Federal Regulations 47 (CFR 47) Parts 15.35, 15.205, 15.209, 15.231, and 15.249 (see Note 4)	260–470 MHz (Part 15.35, 15.205, 15.209) 902–928 MHz (Part 15.249, see Note 4)
Germany	Femmeldetechnisches Zentralamt (FTZ), FTZ 17 TR2100	433.92 MHz
France	Centre National d'Etudes des T'el'ecommunications (National Telecom Research Center, CNET), Groupement Terminaux Procedures et Applications (Terminals, Procedures and Applications Group, TPA), Specification Technique (ST), ST/PAA/TPA/AGH/1542	233.5–225 MHz (automotive only)
United Kingdom	Dept. of Trade and Industry (DTI), MPT 1340	418 MHz 433.92 MHz (automotive only)
Japan	Ministry of Posts and Telecommunications (MPT)	< 322 MHz
Canada	Dept. of Communications (DoC), Telecom Regulatory Service, Radio Standard Specifications (RSS), RSS-210	260–470 MHz (RSS-210) 902–928 MHz
Hong Kong	Post Office, Telecom Branch, Telecom Order 1989, Sec 39, Cap. 106	314 MHz
Australia	Dept. of Transportation and Telecommunications (DTC), and ECR60	303.825 MHz and 318 MHz
Israel	Ministry of Communications, Engineering & Licensing Div.	325 MHz
South Africa		403.916 MHz and 411.6 MHz

NOTE 4: Although the FCC Part 15.231 allows low-power unlicensed radios in the range of 260 MHz to 470 MHz, not all frequencies in this range are desirable. This is due to emission restrictions applying to fundamentals and harmonics in various forbidden bands as defined in Parts 15.205 and 15.209. USA frequencies shown above conform to these additional restrictions and are commonly used in the USA. Under Part 15.249, transmitters may continuously radiate 50 000 μV/m at 3 meters with simple modulation. Part 15.247 permits still higher power, but must use true spread-spectrum modulation. See FCC CFR 47, Part 47, Part 15 for details.

APPLICATION INFORMATION

typical receiver/decoder application

The application example shown in Figure 12 uses the TRF1400 VHF/UHF RZ ASK Remote Control Receiver interfaced with the TI MARCSTAR TRC1300/1315 Decoder, which illustrates the receive side of an RF-linked remote control system. This configuration is typically used in automotive and home security systems as well as in telemetry applications such as utility meter remote monitoring.

U1 is a TRF1400 and is supported by the external components shown. A parallel LC circuit can be substituted for the SAW preselector filter. Because the receiver is interfaced to the TI MARCSTAR decoder that self-synchronizes to baseband information, only the baseband output BBOUT is used.

U2 is a MARCSTAR 4-function, 40-bit rolling-code encoder/decoder device (TRC1315) configured as a serial data decoder (CONF low). The TRC1315 can be powered by a 12-V supply and provides a regulated 5 V for the TRF1400 receiver. PROG is held low to disable the program mode. Both the encoder (at the transmitting end, not shown) and decoder are set to a 1-kHz data clock frequency using an external RC network at OSCC and OSCR. When U2 receives valid function code, the corresponding output(s) on U2 go low and LED 1 – LED 4 light for the length of time valid code frames are received. The RX LED also lights during valid received code. In an actual system, the VCR/TX1 – VCR/TX4 outputs of the TRC1315 are connected to various functions, such as an auto alarm, door locks, or trunk lock activation.

Both devices require power supply bypassing. A 1-μF electrolytic capacitor in parallel with a 0.1-μF ceramic capacitor (low ESR, high-frequency capacitor, such as CK-05 type recommended) should be connected from the positive supply to ground. These capacitors should be placed as close as possible to the device V_{CC} and GND terminals.

APPLICATION INFORMATION

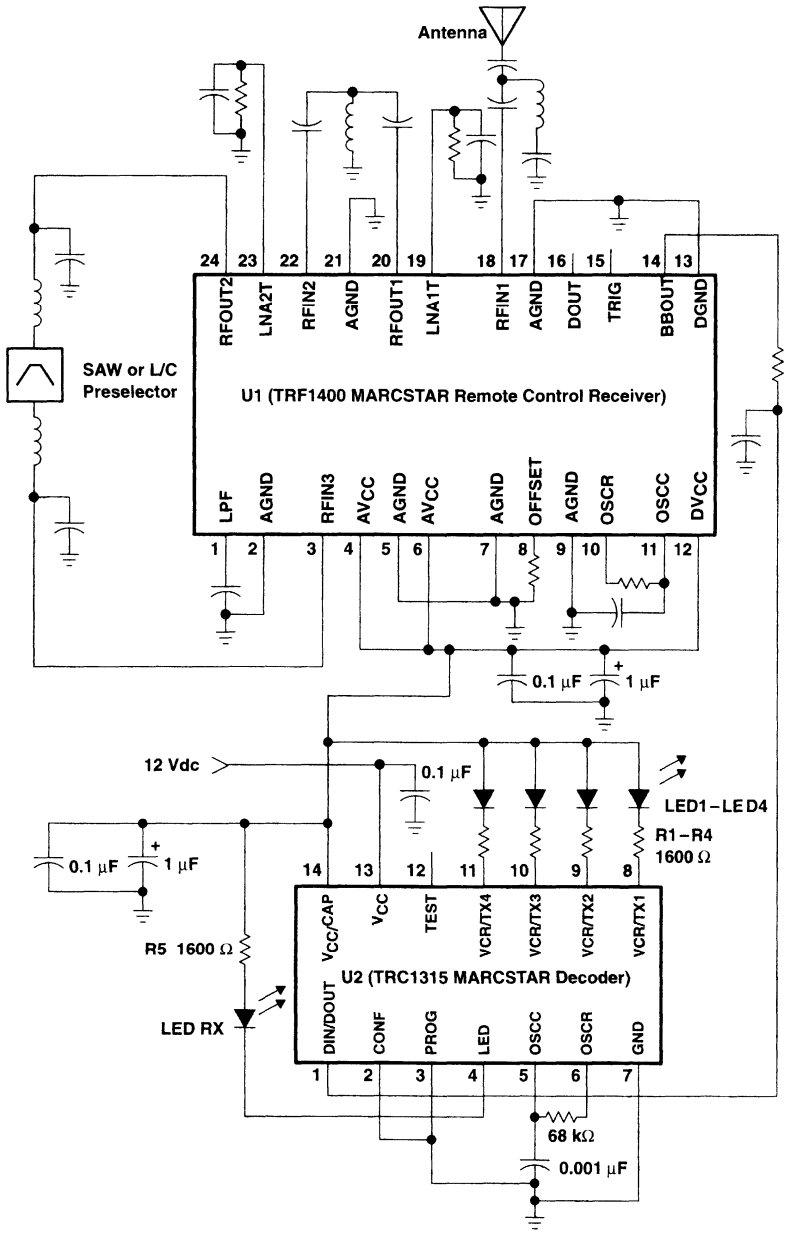


Figure 12. MARCSTAR Receiver/Decoder Using Baseband Data Output

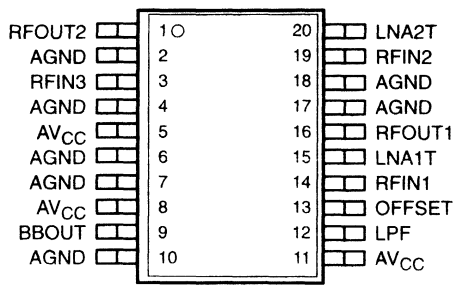
- **Wide VHF/UHF Frequency Range . . . 200 MHz to 450 MHz for World-Wide Remote Control Frequency Compatibility**
- **High Receiver Sensitivity . . . –102 dBm at 315 MHz**
- **Accepts Baseband Data Rates from 500 Hz to 10 kHz**
- **TRF (Tuned Radio Frequency) Design Eliminates Local Oscillator (No Emissions) and Reduces Many Government Type-Approvals (Including FCC)**
- **No Mixing Products Result in No Image to Reject**
- **Internal Amplifier and Comparator for Amplification and Shaping of Low-Level Input Signals with Average-Detecting Autobias Adaptive Threshold Circuitry for Improved Sensitivity**
- **Minimum External Component Count and Surface-Mount Packaging for Extremely Small Circuit Footprint – Typically Replaces more than 40 Components in an Equivalent Discrete Solution**
- **No Manual Alignment When Using SAW Filters**
- **Advanced Submicron BiCMOS Process Technology for Minimum Power Consumption**

description

The TRF1410 VHF/UHF RZ ASK Remote Control Receiver is a member of the MARCSTAR (Multichannel Advanced Remote Control Signalling Transmitter and Receiver) family of remote control serial data devices specifically designed for RZ ASK (Return-to-Zero Amplitude-Shift Keyed) communications systems operating in the 200 MHz – 450 MHz band. This device is targeted for use in automotive and home security systems, garage door openers, remote utility metering, and other low-power remote control and telemetry systems.

A complete RZ ASK receiver solution on a chip, the TRF1410 requires only a minimum of external components for operation. This significantly reduces the complexity and footprint of new designs compared with current discrete receiver designs. The TRF1410 requires no manual alignment when using external SAW (surface acoustic wave) filters. For a lower cost solution, the device is also compatible with external LC components.

DW PACKAGE
(TOP VIEW)



The TRF1410 also includes several on-chip features that would normally require additional circuitry in a receiver system design. These include two low-noise front-end amplifiers, an RF amplifier/comparator for detection and shaping of input signals, and a demodulated RZ ASK baseband TTL-level output that readily interfaces to self-synchronizing devices such as the TI rolling-code MARCSTAR decoder (TRC1300/TRC1315).

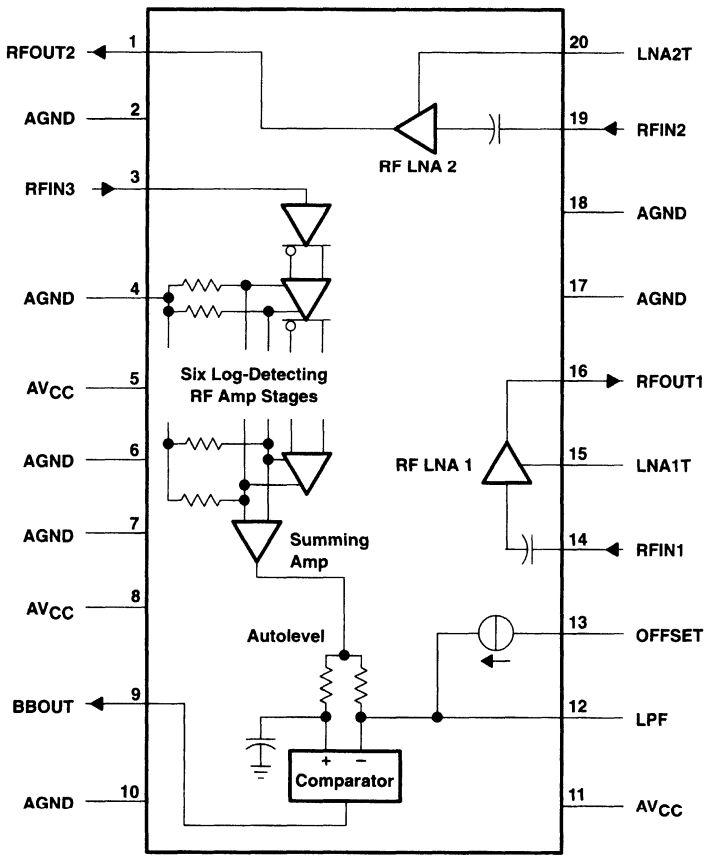
PRODUCT PREVIEW

MARCSTAR is a trademark of Texas Instruments Incorporated.

description (continued)

The TRF1410 VHF/UHF RZ ASK remote control receiver is available in a 20-pin SOIC (DW) package, and is characterized for operation over the temperature range of –40°C to 85°C. The DW package is available taped and reeled. Add R suffix to device type (e.g., TRF1410R).

functional block diagram



PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	2, 4, 6, 7, 10, 17, 18		Analog ground for all internal analog circuits. All analog signals are referenced to these terminals.
AV_{CC}	5, 8, 11		Positive power supply voltage for all analog circuits — 4.5 V to 5.5 V.
BBOUT	9	O	Baseband data output. This is the demodulated envelope of the recovered RF signal. BBOUT is active with any received ASK signal coding format.
LNA1T	15		Low-noise amplifier (LNA) #1 ground termination. LNA1T should be connected to AGND through a parallel resistor-capacitor bias network. If left unconnected, the LNA is disabled.
LNA2T	20		Low-noise amplifier (LNA) #2 ground termination. LNA2T should be connected to AGND through a parallel resistor-capacitor bias network. If left unconnected, the LNA is disabled.
LPF	12		External low-pass capacitor used in the average-detecting adaptive threshold circuitry.
OFFSET	13		Connection to external offset resistor. This resistor (1 MΩ suggested) sets the internal threshold detector offset voltage. Lowering the value of this resistor decreases device sensitivity.
RFIN1	14	I	RF input to first low-noise, high-gain amplifier stage.
RFIN2	19	I	RF input to second low-noise, high-gain amplifier stage.
RFIN3	3	I	RF input to the detecting RF amplifier stages. Filtered RF in the form of AM RZ ASK data at frequencies between 200 MHz and 450 MHz, at a baud rate between 500 Hz and 10 kHz can be applied to this terminal for detection and decoding.
RFOUT1	16	O	RF output of the first low-noise, high-gain amplifier.
RFOUT2	1	O	RF output of the second low-noise, high-gain amplifier. Typically, the input of an external SAW or LC filter is connected to this terminal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, AVCC, DVCC (see Note 1) . . . . . −0.6 to 6
Input voltage range, V_I . . . . . −0.6 to 6
Continuous total power dissipation . . . . . 180 mW
Operating free-air temperature range, T_A . . . . . −55°C to 85°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
ESD protection, all terminals: human body model . . . . . 2 kV
machine model . . . . . 200 V
JEDEC latchup . . . . . 150 mA or 11 V

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5		5.5	V
Input frequency, f_{in}	200		450	MHz
Operating free-air temperature, T_A	−40		85	°C
Minimum permissible AM modulation of RF envelope, measured at −102 dBm at RFINPUT		25%		

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature, typical values are at f_{in} = 315 MHz, V_{CC} = 5 V, and T_A = 25°C (unless otherwise noted)

current consumption

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
I_{CC}	Average supply current from V_{CC}	I/O pins terminated with typical loads		3	mA

digital interface

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	BBOUT	I_{OH} = 3.2 mA	V_{CC}−0.5		V
V_{OL}	Low-level output voltage		I_{OL} = −3.2 mA		0.5	V

VSWR (voltage standing-wave ratio), ripple rejection

PARAMETER	MIN	TYP	MAX	UNIT
VSWR into 50 Ω (requires external LC matching network), RFIN1, RFOUT1, RFIN2, RFOUT2, RFIN3		2:1		V/V
Ripple rejection, 1 MHz (injected at AV_{CC} and DV_{CC}), measured at BBOUT while maintaining BER = 3/100 with desired carrier at −50 dBm (see Note 2)		6% V_{CC}		

NOTE 2: BER (bit error rate — errors/number of bits) is qualified by integration of logic-level pulses (>50% high = 1, <50% low = 0).

PRODUCT PREVIEW

RF sensitivity/overload

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
RF input (average) at test board RF input required for BER 3/100 (see Note 2) at 5 kHz baseband data rate	V_{CC} = 5 V, T_A = 25°C, f_{in} = 315 MHz, external SAW preselector bandpass filter (see Note 3)			−102	dBm
Overload signal at fc with BER 3/100 at 5 kHz (see Note 2) baseband data rate	V_{CC} = 5 V, T_A = 25°C, f_{in} = 315 MHz		−20		dBm

NOTES: 2. BER (bit error rate = errors/number of bits) is qualified by integration of logic-level pulses (>50% high = 1, <50% low = 0).
3. The SAW bandpass filter must have a rejection level greater than or equal to 50 dB at ±0.5 fc, insertion loss of less than or equal to 3 dB, and a –3 dB passband width of 0.2% fc.

timing requirements

RF input data (see Figure 1)†

		MIN	MAX	UNIT
t_r	Rise time, RF input data		0.1 t_{c1}	µs
t_f	Fall time, RF input data		0.1 t_{c1}	µs

† t_{c1} is the duration of the modulated RF carrier.

received data

	MIN	MAX	UNIT
Baseband data frequency AM RZ ASK	0.5	10	kHz

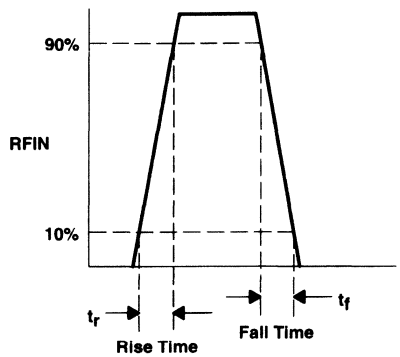


Figure 1. RFIN1 Rise and Fall Times

PRODUCT PREVIEW

PRINCIPLES OF OPERATION

general

The TRF1410 VHF/UHF RZ ASK Remote Control Receiver demodulates AM RZ ASK modulated RF carriers between 200 MHz and 450 MHz with a 500-Hz to 10-kHz baseband data rate.

signal reception

The RF signal is collected by an antenna and then passed through an LC matching network to band-pass filter the signal and compensate for various antenna loading impedances. The signal is then input to the RFIN1 terminal of the TRF1410.

signal path through device

The RF signal applied to the RFIN1 terminal is amplified by LNA1 and LNA2. The combined gain of the two LNAs is 40 dB, with a 1-dB compression point of –80 dBm, and a noise figure of 5 dB (nominal). The amplified signal is output at RFOUT2 and enters an external preselector band-pass filter before being applied to the third stage of amplification at terminal RFIN3.

The third stage of amplification consists of a single-ended-input to differential-output amplifier followed by six high-gain differential log-detecting amplifier stages with an equivalent gain of 60 dB (nominal). First, the signal is converted to a differential signal for increased noise immunity. Next, the differential signal is passed through the six high-gain differential log-detecting amplifiers, forming a detection circuit. Each log-detecting amplifier is biased such that when an RF signal is present, an imbalance is caused in its bias circuit. The imbalance in each of the six stages is converted to a voltage and then summed into a baseband envelope representation of the RF signal. This signal then passes through an autoleveling circuit before being applied to a comparator to produce the TTL-level baseband signal output that appears at BBOUT. An external low-pass filter connected to BBOUT attenuates high-frequency transients in the output signal.

frequency adjustment

The TRF1410 requires no manual alignment. The receive frequency is dependent only on the choice of external matching networks and preselecting filters used. In that respect, the user has only to stock a different set of external components for each frequency, and no manual alignment or end-of-line frequency programming need be performed.

decoder interface

The TRC1300/1315 four-function, 40-bit rolling-code decoder can be interfaced directly to the TRF1410 using the baseband-data output (BBOUT) of the device. The TRC1300/1315 decodes the received data into instructions that it then executes.

external components and device performance

While the TRF1410 uses a minimum of external components in the typical application, the choice of those components greatly affects the performance of the device. When a SAW preselector is used, the selectivity (out-of-band rejection) and sensitivity of the TRF1410 are optimized as a result of the high Q of the SAW devices. If an LC preselector is used, these parameters change and the overall performance of the TRF1410 is reduced, but can still meet the requirements of many end-equipment applications.

An external resistor connected between OFFSET and ground adjusts the internal offset voltage of the receiver decoding section to maximize the noise rejection of the device. While a 1-MΩ resistor is suggested, this value can be changed to minimize toggling of output BBOUT during periods of nonvalid received code.

APPLICABLE REGULATIONS

Receiver design, as well as transmitter design, is regulated throughout the world. Since the TRF1410 is targeted for world-wide sales, the applicable standard for each region must be considered when the device is to be used in systems to be successfully marketed in that region. For this reason, the TRF1410 conforms to all requirements shown in Figure 2 and Table 1. The primary specifications of most of the standards address carrier frequency and spurious emissions.

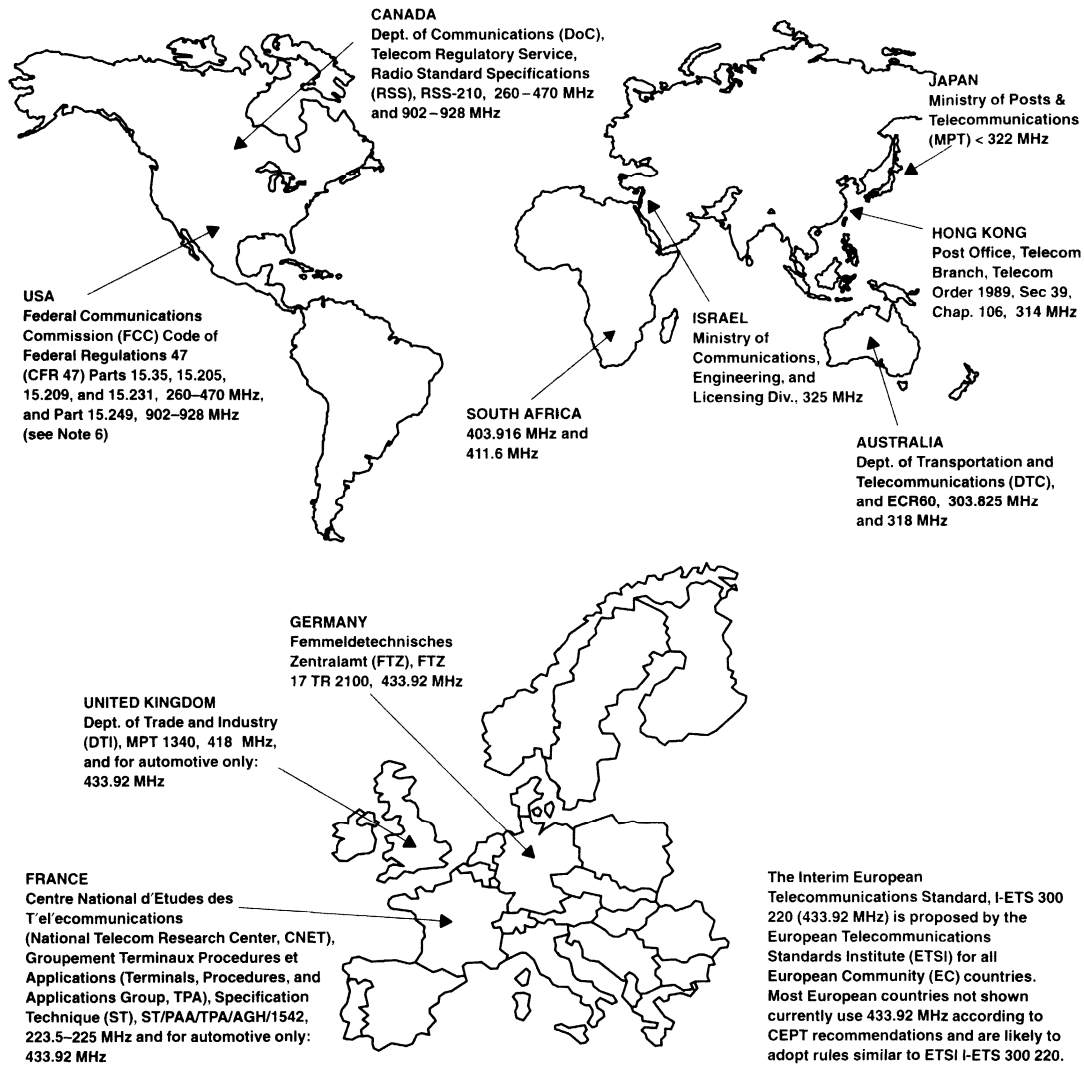


Figure 2. World-Wide Receiver Regulations

PRODUCT PREVIEW

APPLICABLE REGULATIONS

Table 1. World-Wide Regulations

REGION	REGULATION	FREQUENCY
USA	Federal Communications Commission (FCC) Code of Federal Regulations 47 (CFR 47) Parts 15.35, 15.205, 15.209, 15.231, and 15.249 (see Note 4)	260–470 MHz (Part 15.35, 15.205, 15.209) 902–928 MHz (Part 15.249, see Note 4)
Germany	Femmeldetechnisches Zentralamt (FTZ), FTZ 17 TR2100	433.92 MHz
France	Centre National d'Etudes des T'el'ecommunications (National Telecom Research Center, CNET), Groupement Terminaux Procedures et Applications (Terminals, Procedures and Applications Group, TPA), Specification Technique (ST), ST/PAA/TPA/AGH/1542	233.5–225 MHz (automotive only)
United Kingdom	Dept. of Trade and Industry (DTI), MPT 1340	418 MHz 433.92 MHz (automotive only)
Japan	Ministry of Posts and Telecommunications (MPT)	< 322 MHz
Canada	Dept. of Communications (DoC), Telecom Regulatory Service, Radio Standard Specifications (RSS), RSS-210	260–470 MHz (RSS-210) 902–928 MHz
Hong Kong	Post Office, Telecom Branch, Telecom Order 1989, Sec 39, Cap. 106	314 MHz
Australia	Dept. of Transportation and Telecommunications (DTC), and ECR60	303.825 MHz and 318 MHz
Israel	Ministry of Communications, Engineering & Licensing Div.	325 MHz
South Africa		403.916 MHz and 411.6 MHz

NOTE 4: Although the FCC Part 15.231 allows low-power unlicensed radios in the range of 260 MHz to 470 MHz, not all frequencies in this range are desirable. This is due to emission restrictions applying to fundamentals and harmonics in various forbidden bands as defined in Parts 15.205 and 15.209. USA frequencies shown above conform to these additional restrictions and are commonly used in the USA. Under Part 15.249, transmitters may continuously radiate 50 000 μV/m at 3 meters with simple modulation. Part 15.247 permits still higher power, but must use true spread-spectrum modulation. See FCC CFR 47, Part 47, Part 15 for details.

MARCSTAR™ RF Application Report

Gerald Coles
Mixed Signal and RF New Product Development

SLWA005

TEXAS INSTRUMENTS

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Introduction

The TRF1400 receiver was designed as an almost completely integrated VHF/UHF receiver. However, the interface to each working environment requires some attention to the external components and board layout to take full advantage of the device abilities. In addition, system design issues such as antenna design and proximity of local noise sources (microprocessors, motors, etc.) should be considered.

External components

As with any RF design, the successful integration of the device into a circuit board relies on the layout of the board and the quality of the external components. Component tolerances and, where applicable, Q should be noted and followed. Included in this report is a depiction of artwork for the production of an evaluation circuit board that can be employed to demonstrate TRF1400 performance at 315 MHz. A list of required external parts and tolerances is also provided. To obtain a complete set of Gerber photoplotter files, contact any TI Field Sales Office.

Antenna issues

The coupling of the signal into the device is of paramount importance in order to realize the maximum system sensitivity. The input network provided in the evaluation circuit is designed to match the receiver input to a nominal 50-Ω load. Also included in this network is a trap to reduce interference from 105-MHz broadcast signals.

Optimally, the antenna that is used with this receiver should not only be matched to the input impedance, but should be of an efficient design. A quarter wave monopole, for example, is a good choice. Loop antennas may also be used, but their performance may vary widely given the available area and proximity to the circuit board. Also, loop antennas, even those shorter than one wavelength, tend to exhibit distinct nulls in the antenna pattern. If possible, the antenna should be mounted away from the receiver circuit board. Unfortunately, in many instances system requirements prohibit this and impose conflicting requirements of space, ease of matching, and efficiency.

If requirements dictate that the antenna be included into a receiver module or other space-restricted areas, try to select an antenna that is close to an ideal form, and then look to see how it might be integrated into the mechanical confines. If this is not possible or not possible without folding the element over the circuit board, sweep the antenna with a network analyzer to determine the effects of the proximity to the ground plane and other devices. Where ever possible, trim the antenna to achieve matching or to approach a region on the Smith Chart® where a 1-one-element match to 50 Ω may be achieved. If possible, keep a folded antenna at least 0.5 inch from the ground plane to avoid extreme sensitivity to mechanical vibration. As is often the case in nonideal situations, design of an integrated antenna can be very empirical.

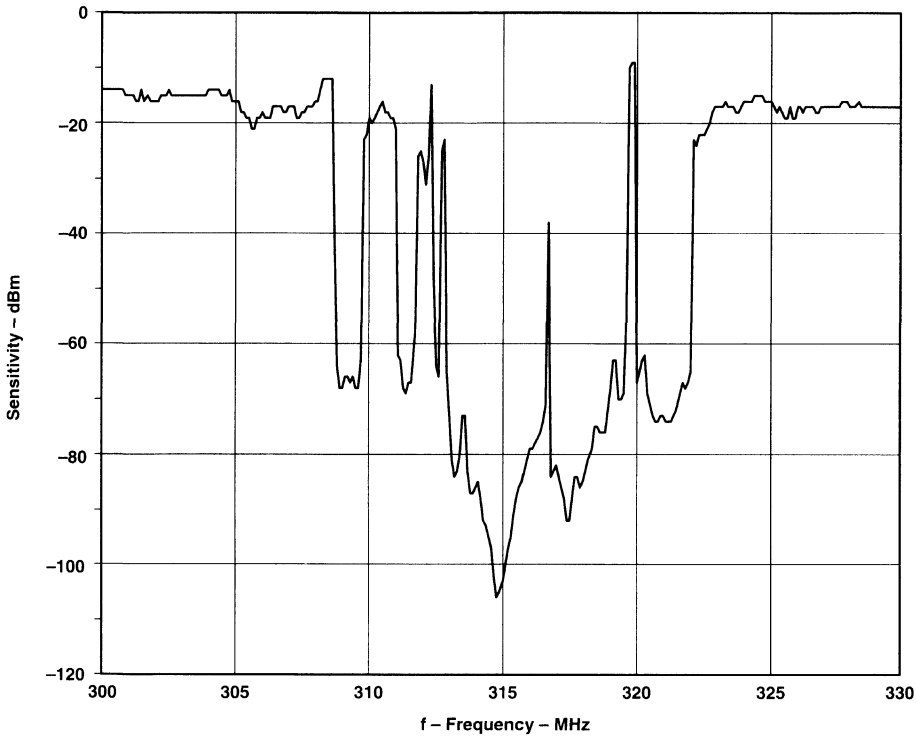
Proximity to local noise sources

Any receiver should be shielded from noise sources that may interfere with the reception of the intended signal, and the TRF1400 is no different. Care should be taken when integrating the device onto a board with microprocessors. Regulate and filter power supply lines, paying particular attention to filter the supply lines again at the receiver power supply terminals to ensure clean lines. Use both low-frequency and high-frequency filter sections. Due to their high harmonic content, digital signals produce broadband noise of sufficient power to interfere with receiver operation both through the front end and by coupling to board traces. Where possible, route digital lines around and away from the receiver and on mutilayer boards, consider running separate planes for these signals.

Care should also be taken to suppress transient noise from relays or broadband noise from motors and other sources.

Sensitivity/Out-of-band rejection

Out-of-band rejection (rejection of signals outside the intended passband of the receiver), depends to a large extent on the SAW (surface acoustic wave) filter. In the layout depicted, the pad for the SAW filter has been carefully designed to maximize the isolation between the input and output pins by including a ground "island" with low impedance paths (vias) between top and bottom ground planes. Figure 1 shows average sensitivity and out-of-band rejection.



NOTE A: RFM RF1211 SAW Filter

Figure 1. Average Sensitivity and Out-of-Band Rejection

Improvements

As a result of work accomplished with the use of the receiver test circuit (Figure 2) and board (Figure 3), several improvements can be suggested.

Do not use plate-through holes on the input and output pins of the SAW filter. Do use plate-through holes for all the ground vias, especially in the "island" area.

Figure 2 shows the schematic for the TRF1400 receiver test circuit. Components listed in Table 1 have been selected for 315 MHz.

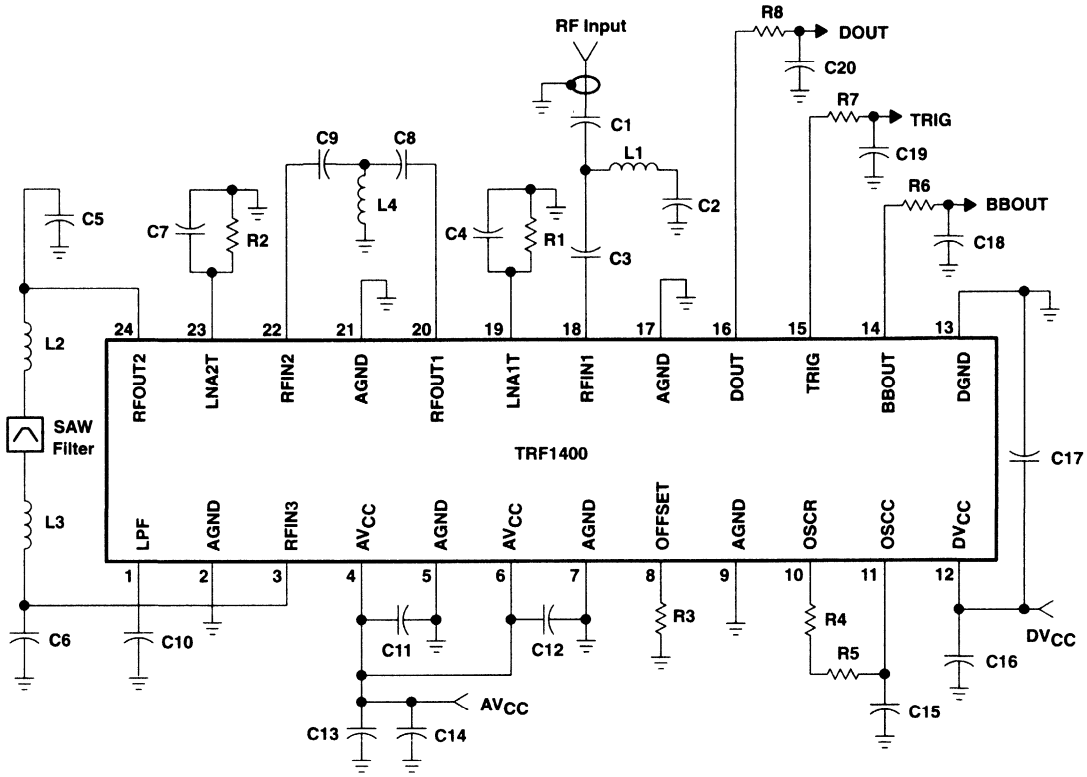


Figure 2. TRF1400 Receiver Test Circuit

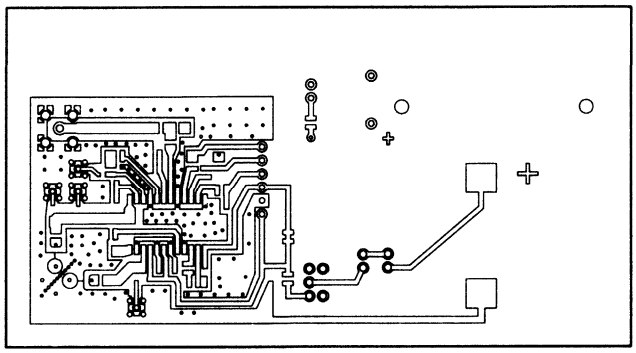


Figure 3. TRF1400 Receiver Test Circuit, Board Layout — Top Side

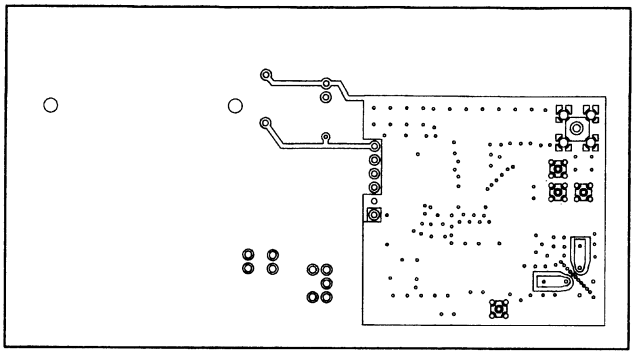


Figure 4. TRF1400 Receiver Test Circuit, Board Layout — Bottom Side

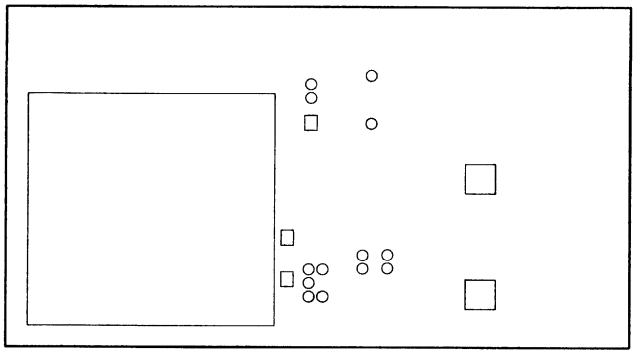


Figure 5. TRF1400 Receiver Test Circuit, Board Solder Mask — Top Side

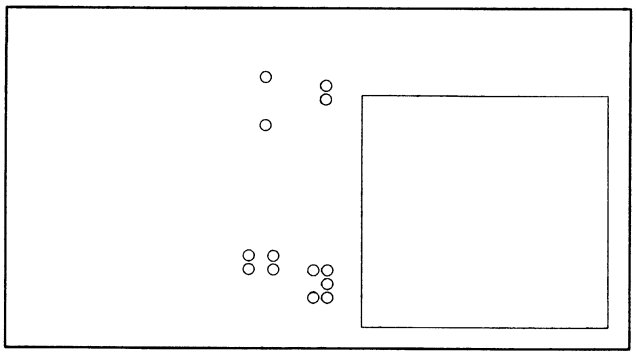


Figure 6. TRF1400 Receiver Test Circuit, Board Solder Mask — Bottom Side

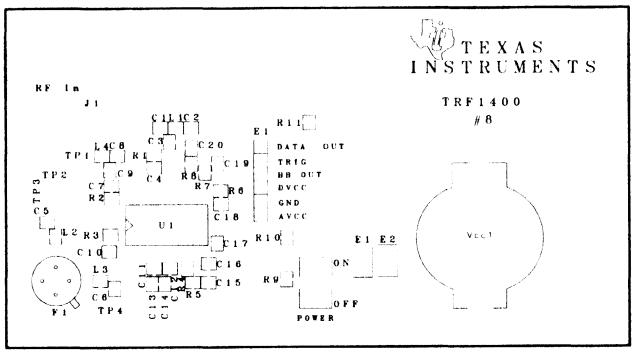


Figure 7. TRF1400 Receiver Test Circuit, Board Silk Screen

Table 1. TRF1400 315-MHz Receiver Test Circuit Parts List

DESIGNATORS	DESCRIPTION	SIZE / VALUE / @ FREQ.	MANUFACTURER	MANUFACTURER P/N
C1	Capacitor	4 pF	Murata	GRM40C0G040C050V
C2	Capacitor	22 pF	Murata	GRM40C0G220J050BD
C3	Capacitor	22 pF	Murata	GRM40C0G220J050BD
C4	Capacitor	100 pF	Murata	GRM40C0G101J050BD
C5	Capacitor	5 pF	Murata	GRM40C0G050D050BD
C6	Capacitor	1.5 pF	Murata	GRM40C0G1R5C050BD
C7	Capacitor	100 pF	Murata	GRM40C0G101J050BD
C8	Capacitor	3 pF	Murata	GRM40C0G030C050BD
C9	Capacitor	18 pF	Murata	GRM40C0G180J050BD
C10	Capacitor	0.047 µF	Murata	GRM40X7R473K050
C11	Capacitor	2200 pF	Murata	GRM40X7R222K050BD
C12	Capacitor	2200 pF	Murata	GRM40X7R222K050BD
C13	Capacitor	0.022 µF	Murata	GRM40X7R223K050BL
C14	Capacitor Tantalum†	4.7 µF	Sprague	293D475X9050D2T
C15	Capacitor	220 pF, 5%	Murata	GRM40C0G221J050BD
C16	Capacitor Tantalum†	4.7 µF	Sprague	293D475X9050D2T
C17	Capacitor	2200 pF	Murata	GRM40X7R222K050BD
C18	Capacitor	0.022 µF	Murata	GRM40X7R223K050BL
C19	Capacitor	2200 pF	Murata	GRM40X7R222K050BD
C20	Capacitor	0.022 µF	Murata	GRM40X7R223K050BL
E1	2-Pin Connector		3M	2340–6111–TN
E2	2-Pin Connector		3M	2340–6111–TN
E3	6-Pin Connector		3M	2340–6111–TN
S1–S2	Header shunts		3M	929952–10
F1	SAW filter	RF1211	RFM	RF1211
L1	Inductor	47 nH	Coilcraft	0805HS470TMBC
L2	Inductor	82 nH	Coilcraft	0805HS820TKBC
L3	Inductor	120 nH	Coilcraft	0805HS121TKBC
L4	Inductor	39 nH	Coilcraft	0805HS390TMBC
P1	RF SMA Connector		Johnson	142–0701–201
R1	Resistor	1200 Ω		
R2	Resistor	1200 Ω		
R3	Resistor	1M Ω		
R4	Resistor	130 KΩ, 1%		
R5	Resistor	0 Ω		
R6	Resistor	1K Ω		
R7	Resistor	100 Ω		
R8	Resistor	1K Ω		
R9	Resistor	680 Ω		
R10	Resistor	short		
R11	Resistor	330 Ω		
S1	Switch		NKK	G-12AP

Table 2: TRF1400 315-MHz Receiver Test Circuit Parts List

DESIGNATORS	DESCRIPTION	SIZE / VALUE / @ FREQ.	MANUFACTURER	MANUFACTURER P/N
Vcc1	Batttery Clip		Keystone	1061
B1X	Battery, Lithium	3.3-V Coin Cell (2 ea.)	Panasonic	CR2016
U1	Receiver	TRF1400	TI	TRF1400

† Tantalum capacitors are rated at 6.3 Vdc minimum.

5 Processors for Analog Cellular

SLWS008C – SEPTEMBER 1994 – REVISED JUNE 1996

- **Single Chip for AMPS/TACS Data and SAT Processing**
- **3.3-V or 5-V Operation**
- **Simple Serial Interface**
- **User-Configurable Interrupt Structure**
- **TX and RX Data Buffers**
- **Programmable Timer**
- **Independent Watchdog Timer**
- **RX/TX Automatic Mute Functions**
- **Arbitration Processing**
- **20 Programmable Expansion I/O Ports**
- **44-Pin Mini-QFP FR Package**

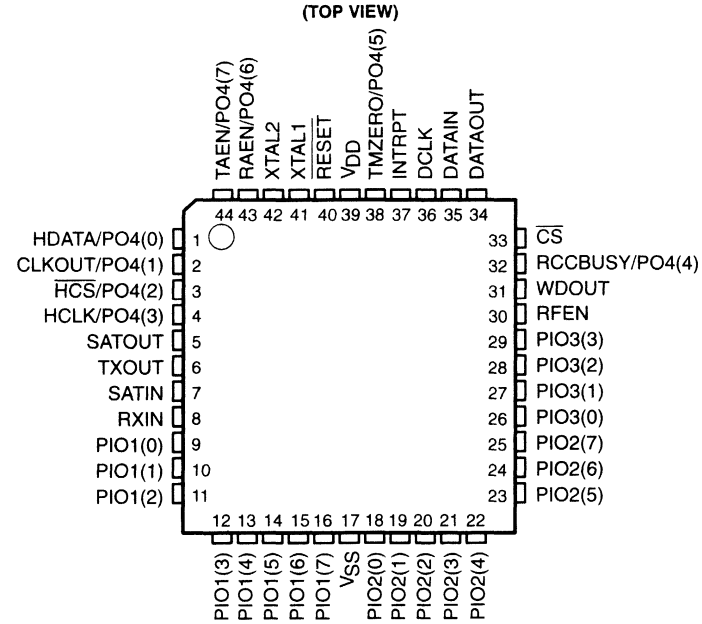
description

The TCM8002 provides the data transceiving, data processing, and SAT (supervisory audio tone) functions for the AMPS (advanced mobile phone service) and TACS (total access communications system) cellular telephone standards. A highly integrated device, the TCM8002 includes a number of additional functions that are helpful in the implementation of the typical cellular telephone. These extra functions include a watchdog timer, which is normally external to the telephone microcontroller, and two 8-bit- and one 4-bit-wide user-programmable general-purpose input/output ports. These can be used to provide port expansion for the microcontroller. An 8-bit counter/timer for user-defined purposes is also included.

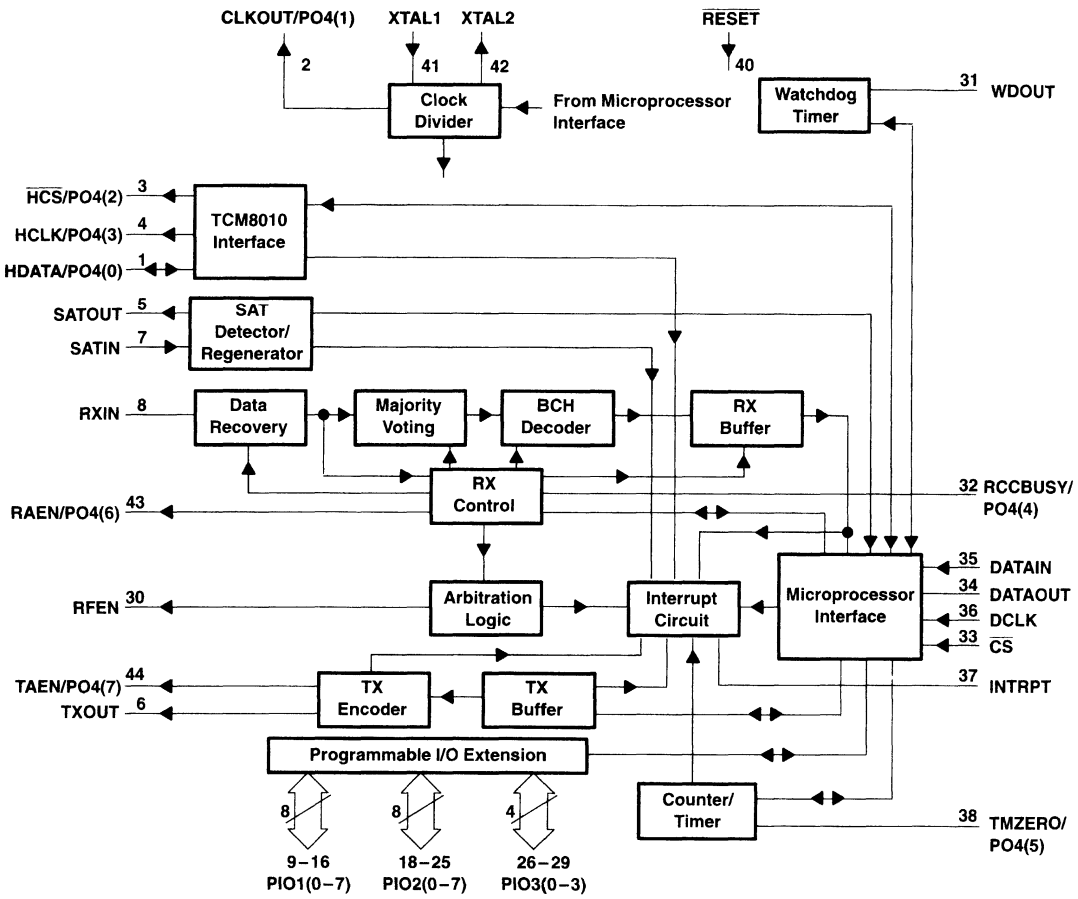
To facilitate the application of the TCM8002 and to minimize the number of connections, a single serial interface to the microcontroller is used for controlling, receiving, and transmitting data. There is also a dedicated interface, including a compatible clock signal, to the companion TCM8010 audio processor that performs most of the audio processing required in a cellular telephone. Additional outputs are also provided for interfacing to other audio processors.

The TCM8002 is built using a low-power CMOS process and operates with a 5-V or 3.3-V power supply. When used in conjunction with the TCM8010, a unique and very compact low-power solution for AMPS/TACS baseband processing in 5-V and 3-V systems is realized.

FR PACKAGE
(TOP VIEW)



functional block diagram



( ) = bit count

Terminal Functions†

TERMINAL‡ NAME	TERMINAL‡ NO.	I/O	DESCRIPTION
CLKOUT/PO4(1)	2	O	Clock output/programmable output #4, bit 1. A 2.56-MHz clock signal is output on this terminal or the device can be set so that it is bit 1 of PO4.
$\overline{CS}$	33	I	Chip select (active low). This is the chip select input from the microcontroller.
DATAIN	35	I	Data input. Serial data from the microcontroller is input on this terminal.
DATAOUT	34	O	Data output. This is the serial data output to the microcontroller (3-state).
DCLK	36	I	Data clock. This is the serial microcontroller interface clock input.
HCLK/PO4(3)	4	O	TCM8010 interface clock/programmable output #4, bit 3. A clock signal to the TCM8010 or bit 3 of programmable output 4 is output on this terminal.
HDATA/PO4(0)	1	I/O	TCM8010 interface data line/programmable output #4, bit 0. This terminal is used for data to and from the TCM8010, or is bit 3 of programmable output 4.
$\overline{HCS}$/PO4(2)	3	O	TCM8010 interface chip select output (active-low)/programmable output #4, bit 2. This terminal selects the TCM8010, or is bit 2 of programmable output 4.
INTRPT	37	O	Interrupt output. This is the interrupt line to the microprocessor.
PIO1(0–7)	9–16	I/O	Programmable I/O port #1, bits 0 – 7. This 8-bit port can be configured as either inputs or outputs (microcontroller port expansion).
PIO2(0–7)	18–25	I/O	Programmable I/O port #2, bits 0 – 7. This 8-bit port can be configured as either inputs or outputs (microcontroller port expansion).
PIO3(0–3)	26–29	I/O	Programmable I/O port #3, bits 0 – 3. This 4-bit port can be configured as either inputs or outputs (microcontroller port expansion).
RAEN/PO4(6)	43	O	Receive audio enable output/programmable output #4, bit 6. This terminal is used to enable the receive audio section of the phone, or is bit 6 of programmable output 4 (open drain).
RCCBUSY/PO4(4)	32	O	RECC busy status/programmable output #4, bit 4. This terminal outputs the status result of the majority vote of the three most recent busy/idle bits, or is bit 4 of programmable output 4.
$\overline{RESET}$	40	I	Reset input, active low. A low applied to this terminal resets the TCM8002 and loads the default values listed in the write map.
RFEN	30	O	RF enable. This terminal is used to enable the transmitter section of the phone (open drain).
RXIN	8	I	Baseband Manchester data input. Manchester-encoded data from control or voice channel is input on this terminal.
SATIN	7	I	SAT input. Square-wave SAT data from the TCM8010 audio processor is input on this terminal.
SATOUT	5	O	Regenerated SAT output. Regenerated SAT data is output to the TCM8010 audio processor on this terminal.
TAEN/PO4(7)	44	O	Transmit audio enable/programmable output #4, bit 7. The logic level on this terminal changes state during RVC message or ST transmission, or is bit 7 of programmable output 4 (open drain).
TMZERO/PO4(5)	38	O	Timer zero/programmable output #4, bit 5. The logic level on this terminal changes state when the counter/timer passes or reaches zero, or is bit 5 of programmable output 4.
TXOUT	6	O	Transmit data output. Encoded transmit data is output to the TMC8010 audio processor on this terminal.
V_{DD}	39		Positive supply voltage. Input is 3.3-V or 5-V.
V_{SS}	17		Ground supply voltage.
WDOUT	31	O	Watchdog timer output. A logic-low pulse is output on this terminal when the watchdog timer times out.
XTAL1	41	I	Crystal terminal 1/external clock source input. An external crystal is connected to this terminal for the internal clock oscillator. An external clock signal can also be input on this terminal.
XTAL2	42	O	Crystal terminal 2. An external crystal is connected to this terminal for the internal clock oscillator.

† All inputs feature Schmitt triggers. All of the PIO terminals also feature optional 10-μA pullups.
‡ ( ) = bit count when in the terminal column

detailed description

Data communication between the mobile station and the land station in AMPS and TACS systems is achieved over forward and reverse control channels when a call is not in progress, or in short bursts over the forward and reverse voice channels when a call is in progress. The TCM8002 device has a receive path that recovers data from the FOCC (forward control-channel) and FVC (forward voice-channel) formats. The transmit path encodes and formats data for the RECC (reverse control channel) and RVC (reverse voice channel).

For voice-channel communications, the received SAT is detected and regenerated for transmission. Communication with the microcontroller/microprocessor in the telephone is through a serial interface. The TCM8002 also provides interrupts to alert the processor to the occurrence of specific events. The receiver is made up of the Data Recovery, Majority Voting, BCH (Bose-Chaudhuri-Hocquenghem) Decoder, RX Buffer, Arbitration Logic, and RX Control blocks. The SAT Detector/Regenerator is used during FVC reception and RVC transmission.

The transmit path consists of the TX Buffer and TX Encoder blocks. A serial microprocessor interface and the interrupt logic are also provided. Four ancillary functions are included:

- TCM8010 interface
- Watchdog Timer
- Counter/Timer
- twenty programmable digital bidirectional I/O lines (eight of the output terminals can be reconfigured as processor output ports)

clock divider

The clock signal for the TCM8002 is supplied in two ways:

- A crystal can be connected to XTAL1 and XTAL2.
- A clock signal from another source can be connected to XTAL1.

When a crystal is used, a resistor (typical value 1 MΩ) should be connected between XTAL1 and XTAL2 to provide a bias for the oscillator. The crystal frequency must be 2.56 MHz, 5.12 MHz, 7.68 MHz, or 10.24 MHz. If an external clock signal is connected, it must be at one of these crystal frequencies or one of two additional frequencies: 15.36 MHz or 20.48 MHz.

The clock frequency defaults to 2.56 MHz when the TCM8002 is reset. The clock-divider circuit provides a 2.56-MHz clock for internal use and must be configured according to the selected crystal or external clock frequency. Control word 2, bits 5 and 6, and control word 4, bit 1, are used to configure the clock divider. The output from the clock-divider circuit is provided at CLKOUT and is always 2.56 MHz. This can be used to clock the TCM8010 advanced audio processor.

The bit rate of the transmitted Manchester-encoded data, the signaling-tone frequency, and the accuracy of the SAT measurement are all determined by the crystal or external clock. The AMPS and TACS system requirements both specify a maximum transmitted bit frequency error of ±100 ppm; therefore, over the operating temperature range of the phone, the crystal or clock frequency error must be no more than ±100 ppm.

absolute maximum ratings over operating temperature range†

Supply voltage range, V_{DD}, V_{SS} (see Note 1) . . . . . −0.5 V to 6 V
Input voltage range, V_I . . . . . −0.5 V to V_{DD} + 0.5 V
Output voltage range (includes open-drain outputs), V_O . . . . . −0.5 V to V_{DD} + 0.5 V
Operating ambient temperature range, T_A . . . . . −40°C to 85°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage Values are with respect to GND.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	V_{DD} = 3 V	2.7	3.3	3.6	V
	V_{DD} = 5 V	4.5	5	5.5	
Input voltage, V_I		0		V_{DD}	V
Output voltage, V_O		0		V_{DD}	V
High-level input voltage, V_{IH}		0.7 V_{DD}			
Low-level input voltage, V_{IL}	V_{DD} = 3 V			0.3 V_{DD}	V
	V_{DD} = 5 V			0.2 V_{DD}	
Operating ambient temperature range, T_A		−40	25	85	°C

electrical characteristics over recommended operating conditions, V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −0.9 mA	V_{DD}−0.55			V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.5	V
V_{IT+}	Positive-going input threshold voltage				0.7 V_{DD}	V
V_{IT-}	Negative-going input threshold voltage		0.3 V_{DD}			V
V_{hys}	Hysteresis ($V_{IT+} - V_{IT-}$)		0.1 V_{DD}		0.3 V_{DD}	V
I_{OZ}	High-impedance output current	V_I = V_{DD} or V_{SS}			±10	µA
I_{IL}	Low-level input current	V_I = V_{SS}			−1	µA
I_{IH}	High-level input current	V_I = V_{DD}			1	µA
I_O	Pullup output current	V_I = V_{SS}	−2.12	−5.32	−10.18	µA
I_{DD}	Supply current with 2.56-MHz crystal	Default mode		1.4		mA
		Low-power mode		1.1		
		Low-power mode, SAT off		0.9		

electrical characteristics over recommended operating conditions, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −2 mA	V_{DD}−0.8			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.5	V
V_{IT+}	Positive-going input threshold voltage				0.7 V_{DD}	V
V_{IT-}	Negative-going input threshold voltage		0.2 V_{DD}			V
V_{hys}	Hysteresis ($V_{IT+} - V_{IT-}$)		0.1 V_{DD}		0.3 V_{DD}	V
I_{OZ}	High-impedance output current	V_I = V_{DD} or V_{SS}			±10	µA
I_{IL}	Low-level input current	V_I = V_{SS}			−1	µA
I_{IH}	High-level input current	V_I = V_{DD}			1	µA
I_O	Pullup output current	V_I = V_{SS}	−7.2	−14.84	−24.47	µA
I_{DD}	Supply current with 2.56-MHz crystal	Default mode		3.6		mA
		Low-power mode		2.8		
		Low-power mode, SAT off		2.5		

timing requirements over recommended ranges of operating conditions (see Figure 1)

		MIN	MAX	UNIT
t_{su1}	Setup time, $\overline{CS}$ low before DCLK↑	300		ns
t_{h1}	Hold time, $\overline{CS}$ low after DCLK↓	300		ns
t_{su2}	Setup time, DATAIN before DCLK↑	300		ns
t_{h2}	Hold time, DATAIN after DCLK↑	300		ns
t_c	DCLK clock period (nominal)	1		µs
$t_{c(er)}$	DCLK clock period, Read start bit – Event Register	2		µs
$t_{c(or)}$	DCLK clock period, Read start bit – Other Register	1		µs
	Period that $\overline{CS}$ must be high between read or write operations	100		ns

PARAMETER MEASUREMENT INFORMATION

Figure 1 shows the timing for processor read and write operations. DATAOUT has a 3-state driver and normally presents the high-impedance state as shown in Figure 1. This allows DATAIN and DATAOUT be be tied together to a bidirectional microprocessor pin.

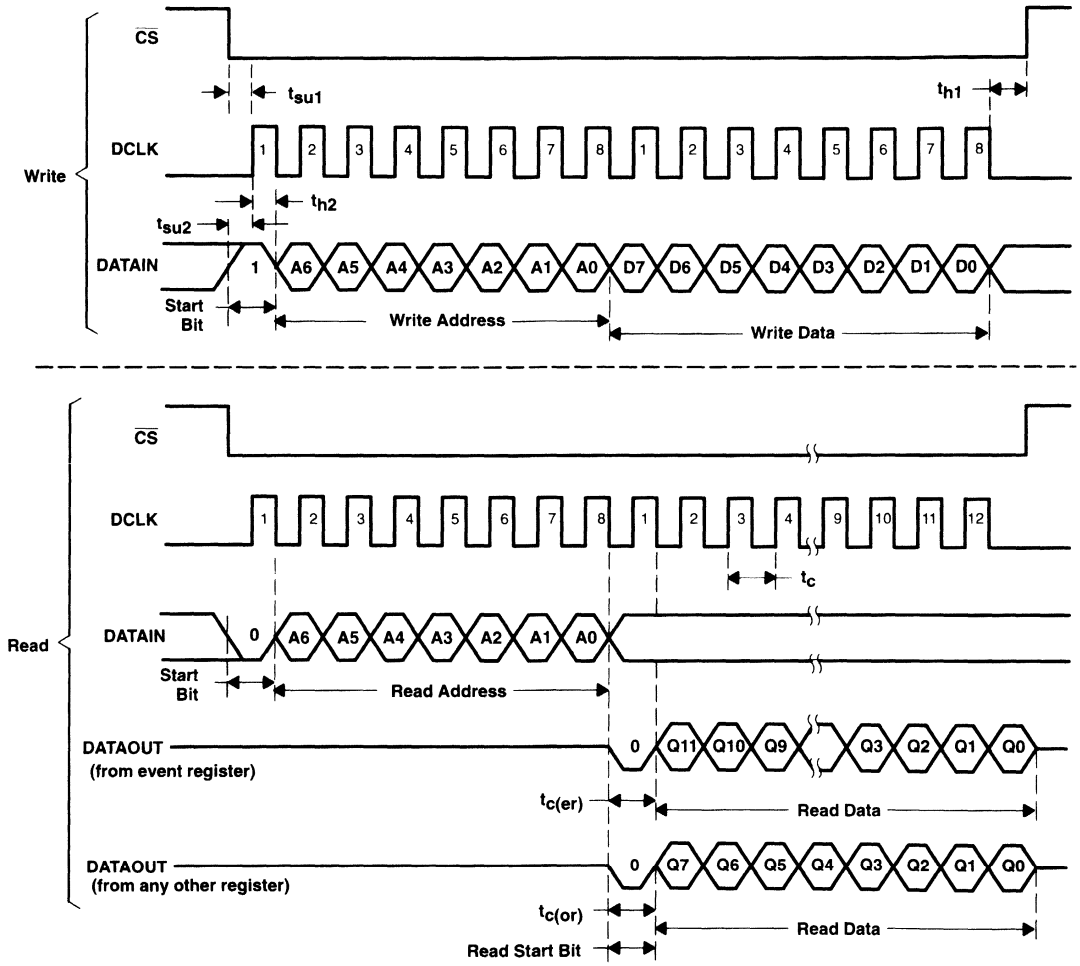


Figure 1. Microprocessor-Interface Timing

PRINCIPLES OF OPERATION

receive path

The following paragraphs detail the TCM8002 receive path, which includes the function blocks as given in the functional block diagram.

Data Recovery

The input to the Data Recovery block is RXIN and the signal applied to this terminal should be a digital version of the output from the FM demodulator/discriminator in the phone. Data recovery is performed by a digital phase-lock circuit with its center frequency at the designated bit rate (i.e., 10 kbps for AMPS and 8 kbps for TACS).

The dotting preamble produces a square wave with a frequency one-half of the bit rate and transitions at the center of each bit period. This is used by the data recovery circuit to acquire bit synchronization with the acquisition coefficient (DATAREC coef 1). After synchronization is achieved, the lock coefficient is used (DATAREC coef 2) to allow phase adjustment during subsequent occurrences of dotting.

RX Control

The receiver control circuit detects the dotting sequence and the frame synchronization code (11100010010). Once frame synchonization has been achieved, the received data stream is separated. The FOCC stream is separated into busy/idle bits, bits of word A, and bits of word B. Recovered FVC bits are separated into bits of the received word, dotting bits, and word sync bits. For both FOCC and FVC, a word repeat count is also maintained. For the FOCC, a count is maintained of the number of consecutive sync words matched and the number not matched. Two matches are required to acquire and confirm frame synchronization. Five consecutive mismatches indicate loss-of-frame synchronization.

During FOCC reception, the busy/idle bits are fed directly to the Arbitration Logic block. A majority vote of the most recent three busy/idle bits is made available at RCCBUSY and at status word 1, bit 4.

During FVC message reception, the receive audio enable output (RAEN) changes state. The output changes on frame synchronization and returns to the initial state 928 bit periods later. Status word 2, bit 1 is set for this period.

The receive audio circuit in a connected TCM8010 can be automatically controlled through the TCM8010 interface (see control word 2). During FVC wideband data reception, a copy of the previous TCM8010 control word 1 is resent with bits 0 and 1 set to 0, muting the received audio path. After the end of data reception, the original TCM8010 control word 1 is resent.

Majority Voting

The Majority Voting function performs a bit-wise majority vote on the repeated FOCC or FVC words. All five repeats of the (A or B) FOCC word are used and up to 11 repeats of the FVC word are used. The result is to recognize each of the 40 bits as a logic 0 or logic 1.

BCH Decoder

The error-correction circuit corrects the received BCH code. This is a 40-bit code word consisting of 28 data bits and 12 parity bits. The circuit is able to correct errors in the received majority-voted 40-bit word from the 12 parity bits. Up to two errors in either the data or parity can be detected. The corrected 28 data bits together with 4 correction status bits may be read from the RX data word 0 to RX data word 3 locations. In low-power mode, this block is turned on only when there is data to be corrected and is selected by control word 4, bit 0.

PRINCIPLES OF OPERATION

RX Buffer

The 28-bit output from the BCH Decoder is fed into the RX Buffer, which can then be read by the microprocessor. Every time new data is available, an interrupt is generated and a status bit is set. The interrupt may be masked. The data is read in four 8-bit bytes, and when the last byte (least significant bit) is read, the status bit is reset.

Arbitration Logic

During FOCC reception, the arbitration logic uses the busy/idle bits to determine the status of the RECC. The arbitration logic monitors the busy/idle status of the FOCC at the start of each RECC transmission. A collision is detected when the status becomes busy within the first 56 bit periods or when it remains idle after 104 bit periods. When a collision is detected, the arbitration-failure flag in the event register is set and an interrupt can be generated (depending on interrupt control word 1). RFEN changes state and the transmission of data to TXOUT is also aborted if bit 5 of control word 1 is set. To reset the state of RFEN and allow the transmission of data to TXOUT after an arbitration failure, it is necessary to reset the arbitration-fail latch by writing to address 26 (reset arbitration).

SAT Detector/Regenerator

The SAT detection and regeneration circuit takes the square wave at SATIN as its input. The detection and regeneration functions are performed by a digital phase-locked loop. The regenerated SAT is output at SATOUT. SAT determination is performed using this circuit and the result is updated every 0.2 seconds and then output to the microcontroller interface. The SAT color code (SCC) is determined from the frequency measurement and the result is available from status word 1, bit 6 and bit 7. If the SAT output frequency is outside of the SAT frequency range, the SAT is considered invalid and zeros are loaded into word 1, bit 6 and bit 7. In low-power mode (selected by control word 4, bit 0), this functional block can be turned off by control word 1, bit 7.

transmit path

The TCM8002 transmit path includes the following function blocks as given in the functional block diagram:

TX Buffer

The TX Buffer is a 36-bit buffer that is written to by the processor in five write operations. After the fifth write (the least significant bit), the TX buffer-available status bit is reset. The status bit is set when the transmit data is read by the TX Encoder.

TX Encoder

The TX Encoder reads the contents of the TX Buffer and then performs BCH encoding, Manchester encoding, and RECC or RVC frame formatting. The result is output at TXOUT. The encoding and transmit cycle is initiated by one of the following conditions:

- With the TX Encoder function not active, transmission is initiated by a processor write to the Commence-TX address.
- With data to be read from the TX Buffer and the TX Encoder active, transmission of the next frame follows directly after completion of an active frame and the seizure precursor is omitted.

Under processor control, the TX Encoder generates a signaling tone (ST), which is 10 kHz for AMPS and 8 kHz for TACS.

During RVC message transmission or ST transmission, the transmit audio enable output (TAEN) changes state.

The transmit audio circuit in a connected TCM8010 can be automatically controlled via the TCM8010 interface (see control word 2). During RVC wide-band data transmission, a copy of the previous TCM8010 control word 1 is resent with bit 5 cleared to 0 and bit 6 set to 1. This mutes the transmit audio path and enables the transmit data path. At the end of data reception, the original TCM8010 control word 1 is resent.

PRINCIPLES OF OPERATION

miscellaneous functions

The following paragraphs detail TCM8010 miscellaneous functions shown in the functional block diagram.

TCM8010 Interface

The TCM8010 Interface provides a serial communication channel to the TCM8010 advanced audio processor using terminals $\overline{HCS}$, HCLK, and HDATA.

Write operation: The TCM8010 address bits and data bits are written in two write operations to the TCM8010 interface with word 1 first and then word 0. On completion of the write to the TCM8010 interface word 0, the data is clocked out to the TCM8010 chip over the 3-wire serial interface. The TCM8010 interface status bit (status word 2, bit 0) indicates when the interface is active.

Read operation: The TCM8010 address bits and HCLK speed are written to the TCM8010 interface word 0. This initiates an A/D conversion and results in retrieval using the 3-bit serial interface. The status bit (status word 2, bit 0) is set for the duration of the interaction. On completion, the 8-bit result can be read from the TCM8010 result location. The HCLK speed is detailed in Table 1.

Table 1. TCM8010 HCLK Speed Control Bits (Interface Word 0)

7	6	5	4	HCLK SPEED CONTROL BITS		1	0	HCLK SPEED IN kHz
				3	2			
0	TCM8010 Read Address			0	0	X	X	20
				0	1			40
				1	0			80
				1	1			160

Counter/Timer

The Counter/Timer is an 8-bit down counter that counts at the bit rate (i.e., 10 kHz for AMPS, 8 kHz for TACS). This circuit can be configured to repeatedly count down from the programmed coefficient or to count down once only and stop at zero. A countdown is initiated by a write to the coefficient location. TMZERO can be used to detect when the counter passes/reaches zero. When the counter/timer is configured to cycle continuously, TMZERO changes state for one bit period. An interrupt can also be generated.

Watchdog Timer

The watchdog timer provides a timeout of a minimum of 1 second to a maximum of 1.2 seconds. The timer is initially started by the first write to address 21 (start/restart watchdog). After this first write, timeout is prevented by writing to the watchdog timer address at intervals not exceeding 1 second.

When timeout occurs, WDOUT pulses low for 100 µs (AMPS operation) or 125 µs (TACS operation) and RFEN changes state, but the data in the control registers remain unchanged. It is then necessary to reset the TCM8002 to return the RFEN output to its original state.

WDOUT is also held low for the duration of a low input at $\overline{RESET}$. WDOUT remains high in its normal (high) state during a software reset (write to location reset).

PRINCIPLES OF OPERATION

Programmable I/O Extension

The Programmable I/O Extension provides processor port expansion. PIO1(0–7), PIO2(0–7), and PIO3(0–3) can be configured as either inputs or outputs. For those pins configured as outputs, the output values are set through the microprocessor interface. The values at all of the ports can be read through the microprocessor interface.

Eight output terminals can also be configured as programmable outputs instead of the named functions. The programmable outputs are the terminals with the /PO4(. . .) in their names. All inputs feature Schmitt triggers and all the PIO terminals feature optional 10-μA pullups.

$\overline{\text{RESET}}$

A low logic level at $\overline{\text{RESET}}$ performs a chip reset. The default values listed in the write address map are loaded.

microcontroller interface

The TCM8002 microcontroller interface is described in subsequent paragraphs.

write

For a write operation, $\overline{\text{CS}}$ is taken low and data on DATAIN is clocked into the TCM8002 on each rising edge of DCLK. It is important that $\overline{\text{CS}}$ is taken low when DCLK is low for the correct operation of the read/write selection logic in the microprocessor interface. The input sequence is start bit (logic 1), 7-bit address, then 8 bits of data. The operation is completed by $\overline{\text{CS}}$ returning to a high logic level with DCLK low. If DCLK is not low, an extra clock pulse is required. The address and data to be written to control the TCM8002 and to transmit Manchester-encoded signals are detailed in the write address map (Table 2). Eight bits of data are always written to the interface and data is right-justified. When writing to addresses 20 – 26, it is necessary to supply clock cycles to write dummy data to the microprocessor interface to start the actions. The state of DATAIN during these write-data clock cycles is not important.

read

For a read operation, the start bit is cleared to 0. Following the seven address bits, DATAOUT is enabled and the output data is updated on each falling edge of DCLK. DCLK must be low when $\overline{\text{CS}}$ is taken low for correct operation of the read/write selection logic in the microprocessor interface. The operation is completed by $\overline{\text{CS}}$ returning to a high logic level with DCLK low. When DCLK is not low, an extra clock pulse is required.

When reading from the event register only, DCLK must be changed from its nominal period of 1 μs to a period of 2 μs so that the start bit is 2 μs long. This can be accomplished by skipping a clock pulse while the start bit is low. Reading from all other registers requires no adjustment to the DCLK nominal period of 1 μs.

DATAOUT returns to the high-impedance state when $\overline{\text{CS}}$ returns high. During the read operation, eight bits of data are output on DATAOUT in the order of bit 7 to bit 0. During a read from the event register, however, 12 bits of data appear in the order of bit 11 to bit 0; i.e., 12 DCLK cycles should be made before $\overline{\text{CS}}$ returns high. The data is right-justified.

Interrupt Circuit

Interrupt-control words 1 and 2 are used to program which events cause an interrupt. When any of the events occur, the associated bit of the event register is set. INTRPT is set whenever an enabled interrupt occurs.

When the event register is read, its contents are first transferred to a buffer and the register is cleared. The bits are then read out in series. At the end of the read sequence, INTRPT is reset. When an interrupt event occurs during the read operation, INTRPT remains low for approximately 1 μs and then returns high.

PRINCIPLES OF OPERATION

write address map

Table 2 shows the write address map. Table 3 through Table 12 explain control words listed in Table 2; the other addresses are described in subsequent paragraphs.

Table 2. Write Address Map

ADDRESS (7 BITS) HEX	NAME	FUNCTION	NO. OF SIGNIFICANT BITS	DEFAULT VALUE
00	Control Word 1	Operational control word	8	00
01	Control Word 2	Operational control word	8	00
02	Control Word 3	Signal polarity selection	8	00
03	Interrupt Control Word 1	Interrupt enables	7	00
04	Interrupt Control Word 2	Interrupt enables	5	00
05	PIO1 Control Word	PIO1 direction selection	8	00
06	PIO1 Output Word	PIO1 values for outputs	8	00
07	PIO2 Control Word	PIO2 direction selection	8	00
08	PIO2 Output Word	PIO2 values for outputs	8	00
09	PIO3 Control Word	PIO3 direction selection	4	00
0A	PIO3 Output Word	PIO3 values for outputs	4	00
0B	PO4 Control Word	PO4 configuration selection	8	00
0C	PO4 Output Word	PO4 values for selected terminals	8	00
20	Commence TX	Commence TX command	0	—
21	Start Watchdog	Start/restart watchdog	0	—
22	Abort TX	Abort TX command	0	—
23	Clear TX Buffer	Clear TX buffer command	0	—
24	Restart Frame Sync	Restarted frame-sync command	0	—
25	Reset	Reset chip command	0	—
26	Reset Arbitration	Reset arbitration circuit	0	—
40	TX Data Word 0	TX data bits 35–32	4	00
41	TX Data Word 1	TX data bits 31–24	8	00
42	TX Data Word 2	TX data bits 23–16	8	00
43	TX Data Word 3	TX data bits 15–8	8	00
44	TX Data Word 4	TX data bits 7–0 (LSBs)	8	00
48	TCM8010 Interface Word 0	Read/write bit, address and D9 – D6	8	00
49	TCM8010 Interface Word 1	TCM8010 data bits D5 – D0	6	00
4D	Counter/Timer Coef	Coef and start command	8	00
50	SAT Coef	SAT circuit-time constant coefficient	5	20
51	DATAREC Coef 1	Acquisition coefficient	6	16
52	DATAREC Coef 2	Lock coefficient	6	63
53	Control Word 4	Operational control word	2	00
57	Mismatch	Frame mismatch coefficient	4	04
59	FOCC Dotting	Detect coefficient	4	07
5A	FVC Dotting	Detect coefficient	7	29

PRINCIPLES OF OPERATION

Table 3. Address 00 – Control Word 1

BIT	FUNCTION (WHEN BIT IS SET)
0	Enable SATOUT output
1	Signalling tone (ST) select (to TXOUT)
2	Voice-channel operation (RVC) (not control channel RECC)
3	Digital color code first bit (DCC) (see Table 4)
4	Digital color code second bit (DCC) (see Table 4)
5	Enable RFEN and TOUT; disable on detection of an arbitration fail
6	Timer/counter continuously cycles
7	Disable SAT detector and regenerator (only in low-power mode)

The translation between the 2-bit DCC code and the transmitted data is shown in Table 4.

Table 4. Two-Bit DCC Code Translation

CONTROL WORD 1		TRANSMITTED CODE
BIT4	BIT3	
0	0	0000000
0	1	0011111
1	0	1100011
1	1	1111100

Table 5. Address 01 – Control Word 2

BIT	FUNCTION (WHEN BIT IS SET)
0	AMPS (not TACS)
1	FOCC B word (not A word)
2	Enable automatic control of TCM8010 receive audio circuit through the TCM8010 interface
3	Enable automatic control of TCM8010 transmit audio circuit through the TCM8010 interface
4	Disable all 10-μA pullups of PIO1, PIO2, and PIO3
5	Clock selection (along with bit 1 of control word 4)
6	Clock selection (along with bit 1 of control word 4)
7	TCM8010 interface write-speed selection

PRINCIPLES OF OPERATION

Table 6. Clock-Selection Bits

CONTROL WORD 4	CONTROL WORD 2			SELECTED CLOCK FREQUENCY	TCM8010 INTERFACE CLOCK
BIT 1	BIT 7	BIT 6	BIT 5		
0	0	0	0	2.56 MHz	320 kHz
0	0	0	1	5.12 MHz	320 kHz
0	0	1	0	7.68 MHz	320 kHz
0	0	1	1	10.24 MHz	320 kHz
0	1	0	0	2.56 MHz	1.28 MHz
0	1	0	1	5.12 MHz	1.28 MHz
0	1	1	0	7.68 MHz	1.28 MHz
0	1	1	1	10.24 MHz	1.28 MHz
1	0	0	0	Not used	Not used
1	0	0	1	Not used	Not used
1	0	1	0	15.36 MHz	320 kHz
1	0	1	1	20.48 MHz	320 kHz
1	1	0	0	Not used	Not used
1	1	0	1	Not used	Not used
1	1	1	0	15.36 MHz	1.28 MHz
1	1	1	1	20.48 MHz	1.28 MHz

Table 7. Address 02 – Control Word 3 Functions

BIT	FUNCTION (WHEN BIT IS SET)
0	Invert polarity of RXIN
1	Invert polarity of TXOUT
2	Invert polarity of RFEN†
3	Invert polarity of INTRPT, active low
4	RAEN active low†
5	TAEN active low†
6	TMZERO active low
7	RCCBUSY active low

† RFEN, RAEN, and TAEN have open-drain output drivers. These drivers have active pulldowns and require provision of external pullups.

PRINCIPLES OF OPERATION

Table 8. Address 03 – Interrupt-Control Word 1

BIT	INTERRUPT ENABLED (WHEN BIT IS SET)
0	RX data available
1	TX buffer available
2	Arbitration failure
3	TX sequence completed
4	Change of RECC bus/idle status
5	Counter/timer reaches zero state
6	SAT measurement decision changes

Table 9. Address 04 – Interrupt-Control Word 2

BIT	INTERRUPT ENABLED (WHEN BIT IS SET)
0	TCM8010 interface activity completed
1	FVC dotting detected
2	FVC frame sync achieved
3	Change of FOCC frame-sync status
4	SAT measurement update (every 0.2 seconds)

Table 10. Address 05 – PIO1 Control Word

BIT (0–7)	CORRESPONDING TERMINAL FUNCTION (0–7)
0	Input
1	Output

The eight terminals of the port are configured as inputs by default. The terminals have programmable 10-μA pullups that can be disabled using bit 4 of control word 2.

address 06 – PIO1 output word

This sets the state of the PIO1 terminals when configured as outputs.

address 07 – PIO2 control word

This selects whether the individual port 2 terminals are configured as inputs or outputs.

address 08 – PIO2 output word

This sets the state of the PIO2 terminals when configured as outputs.

address 09 – PIO3 control word

This selects whether the individual port 3 terminals are configured as inputs or outputs.

PRINCIPLES OF OPERATION

address 0A – PIO3 output word

This sets the state of the PIO3 terminals when configured as outputs.

address 0B – PO4 control word

The eight output terminals HDATA, CLKOUT, $\overline{\text{HCS}}$, HCLK, RCCBUSY, TMZERO, RAEN, and TAEN can be independently reconfigured as outputs. Control bits set the terminals as programmable outputs.

address 0C – PO4 output word

This sets the value of the PO4 terminals configured as outputs. RAEN and TAEN remain open-drain outputs when configured as programmable outputs.

address 20 – commence TX

Writing to address 20 transfers data from the TX Buffer to the TX Encoder and starts the encoding and transmission of the data.

address 21 – start watchdog

Writing to address 21 starts one cycle of the Watchdog Timer.

address 22 – abort TX

Writing to address 22 immediately stops a transmission sequence that is in progress.

address 23 – clear TX buffer

Writing to address 23 clears the contents of the TX Buffer. This command can be used to stop the automatic transmission of a second word written to the TX Buffer when the TX Encoder is active. This command does not stop the complete transmission of the first word.

address 24 – restart frame sync

Writing to address 24 resets the data-recovery circuit, which then uses the acquisition coefficient initially to achieve bit synchronization to the received data. It can be used when the phone switches to a new FOCC (forward control channel) to reduce the time taken to acquire bit synchronization. The data-recovery circuit does not have to wait until it has detected loss of bit synchronization to change from using the lock coefficient to using the acquisition coefficient.

address 25 – reset

Writing to address 25 performs a device reset. Its function is identical to that of $\overline{\text{RESET}}$ except that it does not affect WDOUT. The default values listed in the write address map are then loaded.

address 26 – reset arbitration

Writing to address 26 resets the arbitration-failure circuit.

addresses 40 to 44 – TX data words 0 to 4

The data to be transmitted is written to these five addresses, thereby loading the TX Buffer.

PRINCIPLES OF OPERATION

address 48 – TCM8010 interface word 0

Table 11. Interface Word 0

BIT	FUNCTION
7	Value = 0 for TCM8010 read operation, 1 for write operation
6–4	TCM8010 address
3–0	TCM8010 write data bits D9–D6

Writing to the TCM8010 interface word 0 initiates a TCM8010 interaction. The result of any read operation (i.e., an ADC conversion result) can be accessed by a subsequent read from the TCM8010 result location.

address 49 – TCM8010 interface word 1

These are the TCM8010 data bits D5 to D0.

address 4D – counter/timer coefficient

Writing to address 4D sets the count length and starts a down count from the value written.

address 50 – SAT coef

This coefficient controls the SAT detector digital phase-locked loop time constant.

address 51 – DATAREC coef 1

This controls the data-recovery circuit acquisition performance before bit synchronization is achieved.

address 52 – DATAREC coef 2

This controls the data-recovery circuit lock performance after bit synchronization is achieved.

address 53 – control word 4

Table 12. Control Word 4

BIT	FUNCTION (WHEN BIT IS SET)
0	Low-power mode select
1	Clock selection (with control word 2)

With low-power mode selected, the BCH decoder circuit is turned on only when there is data to be error-corrected. The SAT detector and regenerator can be turned off when not required (control word 1).

address 57 – mismatch

This relates to the number of successive frames that are not recognized during data recovery before bit synchronization is searched again.

address 59 – FOCC dotting

This is a coefficient for the data-recovery circuit and is related to how much of the dotting preamble of the forward control channel data is required before it is accepted that bit synchronization has been achieved.

address 5A – FVC dotting

This is a coefficient for the data-recovery circuit and is related to how much of the dotting preamble of the forward voice channel data is required before it is accepted that bit synchronization has been achieved.

PRINCIPLES OF OPERATION

read address map

Table 13 shows the read address map. This is followed by an explanation of all the bits contained in this address map including detailed information in Table 14 through Table 19.

Table 13. Read Address Map

ADDRESS (7 BITS) HEX	NAME	FUNCTION	NO. OF SIGNIFICANT BITS
00	Status Word 1	Status word 1	8
01	Status Word 2	Status word 2	3
02	Event Register	Event register	12
04	PIO1 Status Word	State of PIO1 terminals	8
05	PIO2 Status Word	State of PIO2 terminals	8
06	PIO3 Status Word	State of PIO3 terminals	4
10	RX Data Word 0	RX bits 27–20	8
11	RX Data Word 1	RX bits 19–12	8
12	RX Data Word 2	RX bits 11–4	8
13	RX Data Word 3 (bits 7–4)	RX bits 3–0 and error-correction status	8
18	Uncorrected RX Data Word 0	Uncorrected received data bits 39–32	8
19	Uncorrected RX Data Word 1	Uncorrected received data bits 31–24	8
1A	Uncorrected RX Data Word 2	Uncorrected received data bits 23–16	8
1B	Uncorrected RX Data Word 3	Uncorrected received data bits 15–8	8
1C	Uncorrected RX Data Word 4	Uncorrected received data bits 7–0	8
1D	RX Repeat Count	Number of word repeats used for the majority voting	4
20	TCM8010 Result	8-bit result of TCM8010 A/D conversion	8
30	SAT (supervisory audio tone)	SAT frequency measurement	8

Table 14. Address 00 – Status Word 1

BIT	STATUS (WHEN BIT IS SET)
0	RX data available
1	TX buffer available
2	Most recent TX aborted or arbitration failure
3	TX encoder active
4	RECC busy (not idle)
5	Counter/timer at zero state
6	SAT frequency band as detailed in Table 13
7	SAT frequency band as detailed in Table 13

PRINCIPLES OF OPERATION

Table 15. SAT Frequency Band

STATUS WORD 1		MEASURED FREQUENCY
BIT 7	BIT 6	
0	0	6047 Hz < f < 5957 Hz†
0	1	5957 Hz < f < 5987 Hz
1	0	5987 Hz < f < 6017 Hz
1	1	6017 Hz < f < 6047 Hz

† This indicates an invalid SAT.

Table 16. Address 01 – Status Word 2

BIT	STATUS (WHEN BIT IS SET)
0	TCM8010 interface active
1	FVC message being received
2	In FOCC frame sync

Table 17. Address 02 – Event Register

BIT	OCCURRENCES SINCE PREVIOUS READ OF THIS WORD (WHEN BIT IS SET)
0	RX data available
1	TX buffer available
2	Arbitration failure
3	TX sequence completed
4	Change of FOCC busy/idle status
5	Counter/timer reaches zero state
6	SAT result changed value
7	TCM8010 interface activity completed
8	FVC dotting detected
9	FVC frame sync achieved
10	Change of FOCC frame-sync status
11	SAT measurement update (every 0.2 seconds)

These flags indicate which event(s) have occurred since the previous read, regardless of their associated interrupt control bits.

addresses 04, 05, and 06 – PIO1, PIO2, and PIO3 status words

These registers contain the states of the PIO1, PIO2, and PIO3 terminals.

address 10 – RX data word 0

This register contains the corrected received data bits 27–20.

address 11 – RX data word 1

This register contains the corrected received data bits 19–12.

address 12 – RX data word 2

This register contains the corrected received data bits 11–4.

PRINCIPLES OF OPERATION

address 13 – RX data word 3

This register contains the corrected received data bits 3–0 and the error-correction status detailed in Table 17.

Table 18. Received Data Word 3

BIT	FUNCTION
7	RX data bit 3
6	RX data bit 2
5	RX data bit 1
4	RX data bit 0
3–0	Received-data decode status

Table 19. Error-Correction Status

RECEIVED DATA WORD 3				DECODE STATUS
BIT 3	BIT 2	BIT 1	BIT 0	
0	0	0	0	No errors detected
0	0	0	1	One error detected in parity bits
0	0	1	0	Two errors detected in parity bits
0	0	1	1	Not used
0	1	0	0	One error corrected in data
0	1	0	1	One error corrected in data, one error detected in parity bits
0	1	1	0	Not used
0	1	1	1	Not used
1	0	0	0	Two errors corrected in data
1	0	0	1	Not used
1	0	1	0	Not used
1	0	1	1	Not used
1	1	0	0	More than two erasures occurred (see Note 2). Up to two data bits are corrected.
1	1	0	1	More than two erasures occurred (see Note 2). One error detected in parity bits. Up to one data bit are corrected.
1	1	1	0	More than two erasures occurred (see Note 2). Two errors in parity bits are detected.
1	1	1	1	More than two errors detected. Data is not corrected.

NOTE 2: A bit erasure occurs when the bit is detected an equal number of times as a 1 and as a 0 over the valid repeats.

PRINCIPLES OF OPERATION

addresses 18 to 1C – uncorrected received data

The uncorrected received data can be read from the five uncorrected received data words. The 12 LSBs are the received parity bits, and the remaining 28 bits are the received data.

address 1D – received repeat count

The received repeat count gives the number of repeats of the received word that were used by the bit-wise majority voting circuit to generate the uncorrected received data.

address 20 – TCM8010 read result

Address 20 contains the ADC result retrieved from the TCM8010 audio processor. This data is valid once the TCM8010 interface has completed the read operation.

address 30 – SAT (supervisory audio tone)

The SAT tone provides the SAT frequency measurement in 2's-complement format with a resolution of 1 Hz and with respect to the frequency of 6 kHz, as shown in Table 20.

Table 20. SAT Frequency Measurements

FREQUENCY IN kHz	MEASUREMENT CODE
6.004	00000011
6.000	11111111
5.996	11111011

APPLICATION INFORMATION

Figure 2 shows a typical complete baseband solution using a TCM8002 data processor and a TCM8010 audio processor.

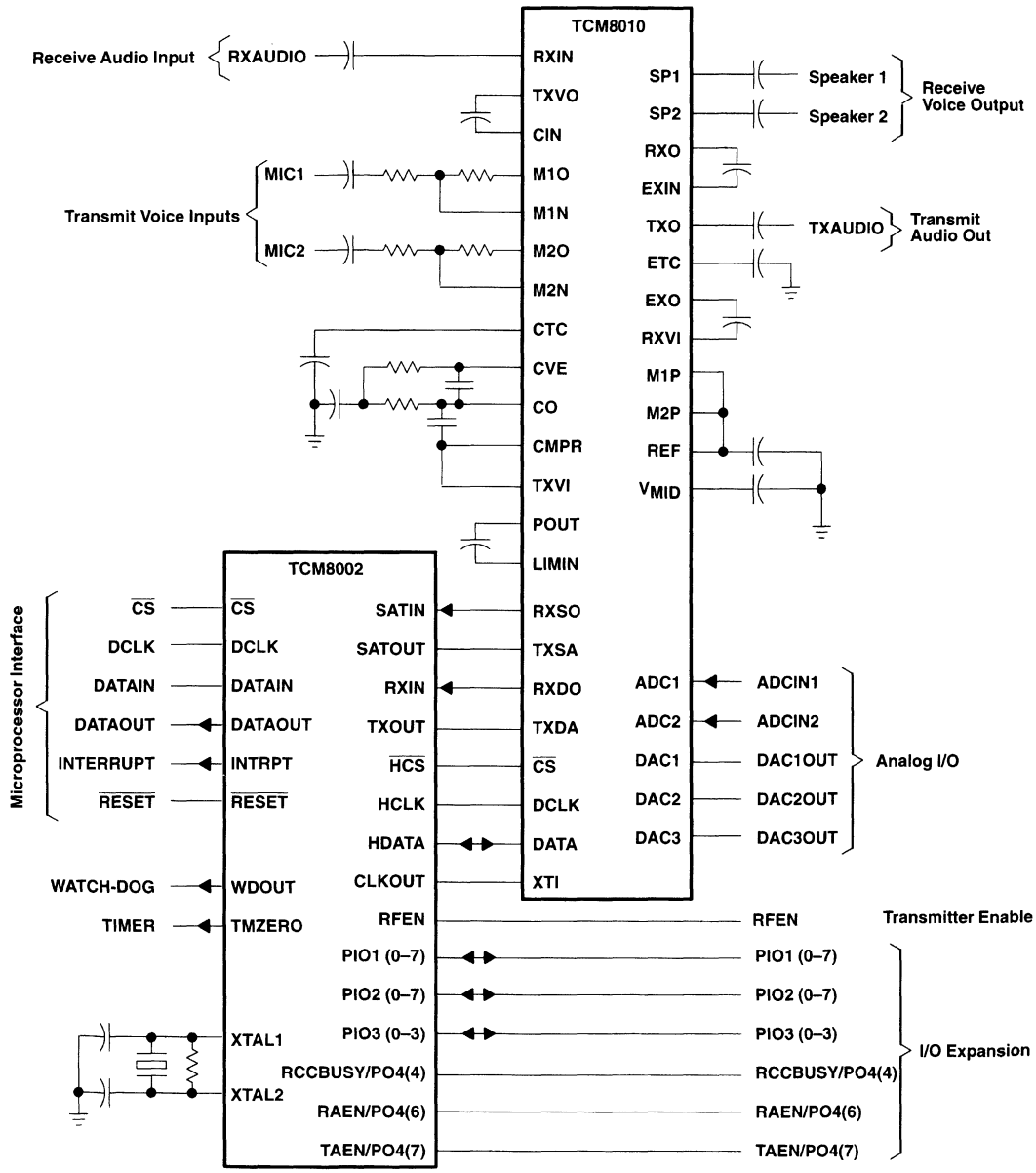
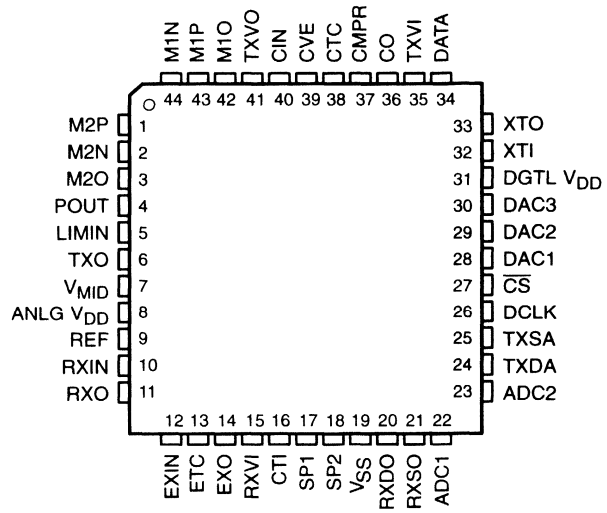


Figure 2. Complete Baseband Solution

SLWS034 – JUNE 1996

- **TACS and AMPS Operation**
- **Integrated RX and TX Voice Filters**
- **Integrated RX and TX Data Filters**
- **RX and TX Narrow-Band SAT Filters**
- **RX Data Recovery Comparator**
- **Pre-emphasis and De-emphasis Filtering**
- **Adjustable TX Limiter**
- **Microphone Preamplifiers**
- **Digitally Controlled Gains and Signal Selection or Muting**
- **Three 8-Bit DACs With Output Buffers**
- **8-Bit ADC With Input Multiplexer**
- **DTMF Generator**
- **On-Chip Compandor**
- **Flexible Clock or Oscillator Operation**
- **Simple 3-Wire Digital Interface**
- **Low-Power . . . 2-mA Standby Current**
- **44-Pin Mini QFP (FR) Package**
- **Advanced LinBiCMOS Technology**

FR PACKAGE
(TOP VIEW)



description

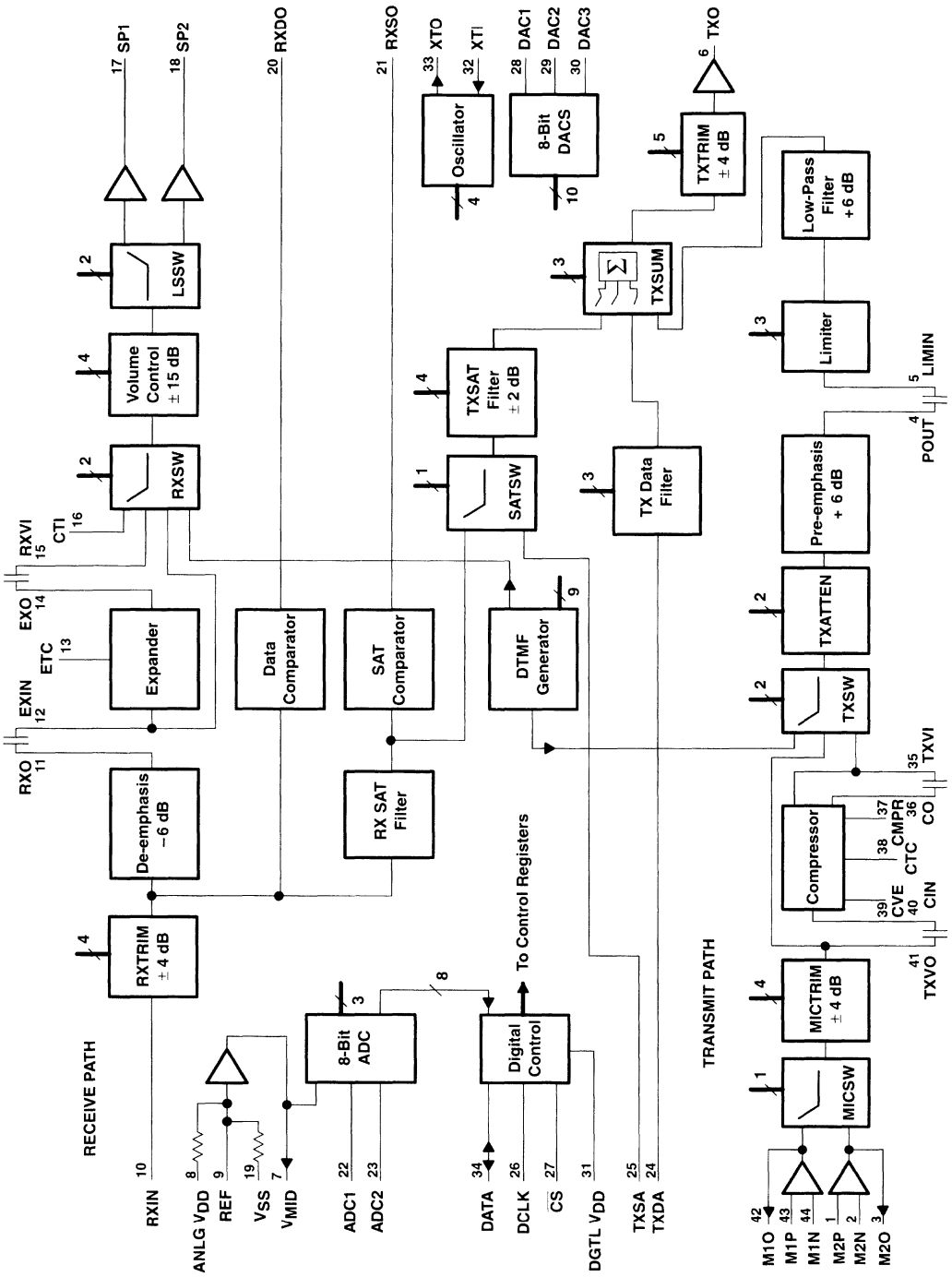
The TCM8010-37 is a complete AMPS/TACS (advanced mobile telephone service/total access communications system) audio processor built using the Texas Instruments Advanced LinBiCMOS™ technology and packaged in a 44-pin mini QFP (FR) package. This device provides a highly integrated solution for analog-signal processing in mobile and hand-held FM cellular telephones while conserving circuit board area and vertical height within the finished product. All necessary voice and data filters, and all appropriate antialiasing and smoothing filters are incorporated in the device. Continuous-time filters are used for the antialiasing and smoothing functions while switched-capacitor techniques are used only where appropriate. Ancillary functions such as microphone preamplifiers, differential loudspeaker outputs, CCITT-compatible compander, DTMF (dual-tone multi-frequency) generator, three 8-bit DACs (digital-to-analog converters), and an 8-bit ADC (analog-to-digital converter) with input multiplexer are also included in the device. A simple 3-wire serial interface provides digital control of signal-path switching, muting and gain adjustment, the 8-bit DACs, transmit limit level, DTMF code and amplitude, and ADC multiplexer input select, and also allows the ADC output to be read.

In active mode, the TCM8010-37 consumes less than 12 mA of supply current. When the DTMF generator or the ADC are not in operation, the power consumption is even less. The device can be put into a standby mode in which only the receive (RX) data path is active, reducing the supply current to a typical value of 2 mA or less.

Either the integrated-clock oscillator or an external clock signal (with several frequency options) can be used.

Advanced LinBiCMOS is a trademark of Texas Instruments Incorporated.

functional block diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ADC1 – ADC2	22, 23	I	ADC input 1 and 2. Various voltages can be applied to these terminals for selective conversion and measurement by the internal A/D converter (analog).
ANLG V_{DD}	8		Analog positive power supply. V_{DD} = 3.7 V – 4 V
CIN	40	I	Compressor input. The signal from TXVO is ac coupled to CIN through an external capacitor (analog).
CMPR	37	I	Compressor rectifier input . The Compressor output signal at CO is ac coupled to CMPR and TXVI through an external capacitor (analog).
CO	36	O	Compressor output. The Compressor output signal at CO is ac coupled to CMPR and TXVI through an external capacitor (analog).
$\overline{CS}$	27	I	Chip select of serial interface, active low. When pulled low, the TCM8010-37 is selected (digital).
CTC	38	O	Compressor time constant. An external capacitor connected from CTC to GND (V_{SS}) sets the compressor attack and recovery times (analog).
CTI	16	I	Call tone input to RXSW. An external call tone signal can be applied to the receive channel at RXSW through CTI (analog and digital).
CVE	39	I	Compressor virtual ground. An external capacitor should be connected between CVE and CO to improve the compressor high–frequency stability (analog).
DAC1 – DAC3	28, 29, 30	O	DAC outputs. The result of D/A conversions appear at these terminals (analog).
DATA	34	I/O	Data line of serial interface. Serial data passes into and out of the TCM8010–37 through this terminal (digital).
DCLK	26	I	Clock input of serial interface. An external clock signal applied to this terminal clocks the serial interface and is also used to drive the A/D converter (digital).
DGTL V_{DD}	31		Digital positive power supply. V_{DD} = 3.7 V – 4 V
ETC	13	O	Expander time constant. An external capacitor connected from ETC to GND (V_{SS}) sets the compressor attack and recovery times (analog).
EXIN	12	I	Expander input. The signal from RXO is ac coupled to EXIN through an external capacitor (analog).
EXO	14	O	Expander output. The Expander output signal at EXO is ac coupled to RXVI through an external capacitor (analog).
LIMIN	5	I	Limiter input. The signal from POUT is ac coupled to LIMIN through an external capacitor (analog).
M1O	42	O	Microphone amplifer 1 output. The output signal at this terminal can be applied to the transmit path or used for an external accessory. It is also used for setting the gain of Microphone amplifer 1 (analog).
M1P, M1N	43, 44	I	Microphone amplifier 1 differential inputs. Voice signals are input on these terminals (analog).
M2O	3	O	Microphone amplifer 2 output. The output signal at this terminal can be applied to the transmit path or used for an external accessory. It is also used for setting the gain of Microphone amplifer 2 (analog).
M2P, M2N	1, 2	I	Microphone amplifier 2 differential inputs. Voice signals are input on these terminals (analog).
POUT	4	O	Pre-emphasis output. The output signal at POUT is ac coupled to LIMIN through an external capacitor (analog).
REF	9		Midrail reference. REF should be decoupled to V_{SS} with an external capacitor.
RXDO	20	O	Receive section data output. The Data Comparator output signal is available at RXDO (digital).
RXIN	10	I	Receive section input. The demodulated signal from the RF receiver is input through RXIN (analog).
RXO	11	O	Receive section deemphasis voice filter output. The signal at RXO is ac coupled to EXIN through an external capacitor (analog).
RXSO	21	O	Receive section supervisory audio tone output. Recovered SAT signals or the output of the RX SAT Filter block is available at this terminal (digital or analog).
RXVI	15	I	Voice input to Volume Control stage. The Expander output signal at EXO is ac coupled to RXVI through an external capacitor (analog).
SP1, SP2	17, 18	O	Speaker outputs 1 and 2. These outputs can be configured as differential drive (both terminals), one or the other as a single–ended (one terminal active), or both terminals muted (analog).
TXDA	24	I	Transmit data filter input. An external Manchester–encoded digital signal is applied to this terminal (digital).

Terminal Functions

TXO	6	O	Transmit section output. Voice, SAT, and data signals, summed together in any combination, are output at TXO to be routed to the RF transmitter.
TXSA	25	I	Transmit SAT input. External SAT data is input at TXSA.
TXVI	35	I	Voice input to transmit output stages. The Compressor output signal at CO is ac coupled to TXVI through an external capacitor (analog).
TXVO	41	O	Transmit voice input stage output. The voice output signal at TXVO is ac coupled to CIN through an external capacitor (analog).
V_{MID}	7		Buffered midrail voltage. V_{MID} should be decoupled to V_{SS} with an external capacitor.
V_{SS}	19		Negative power supply. V_{SS} = 0 V.
XTI	32		Crystal/external clock input. A crystal is connected between XTI and XTO for internal oscillator operation or an external clock signal (≥ 0.5 V peak sinusoidal) is applied to XTI.
XTO	32, 33		Crystal inputs. A crystal is connected between XTO and XTI for internal oscillator operation.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{DD} (see Note 1) . . . . . −0.3 V to 7 V
Input voltage, V_I (any pin) . . . . . V_{SS} − 0.3 V to V_{DD} + 0.3 V
Operating free-air temperature range, T_A . . . . . −30°C to 70°C
Continuous total power dissipation at (or below) T_A = 25°C . . . . . 893 mW
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to V_{SS}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, DGTL V_{DD} and ANLG V_{DD}	3.7		4	V
High-level input voltage, V_{IH}	0.8V_{DD}			V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature range, TA	−30		70	°C

electrical characteristics over recommended operating virtual junction temperature range, V_{DD} = 4 V, f_{xtal} = 2.56 MHz

PARAMETER			MIN	TYP	MAX	UNIT
$I_{DD(A)}$	Analog supply current	Standby mode, DACs off	0.9		1.52	mA
		Standby mode, DACs on	1.3		1.88	
		Operating mode	9.5		14.82	
		Including DTMF generator	10.1		15.82	
$I_{DD(D)}$	Digital supply current	Standby mode		85	882	µA
		Operating mode		0.41	1.29	mA
		ADC operating		1		
REF	Mid-supply voltage at REF terminal	Operating mode	1.92	2	2.08	V
V_{MID}	Buffered mid-supply reference voltage	Operating mode	1.92	2	2.08	

analog inputs

PARAMETER		MIN	TYP	MAX	UNIT
I_I	Input current at M1P, M1N, M2P, M2N, ADC1, ADC2, CTI		1		µA
Z_i	Input impedance at RXIN, RXVI, LIMIN, TXSA, TXDA	100			kΩ
	Input impedance at EXIN, CIN, CMPR, TXVI	25			

digital interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level input current	V_I = 5 V			1	µA
I_{IL}	Low-level input current	V_I = 0 V			1	
f_{CLK}	Serial clock frequency, DCLK input				1	MHz
V_{OH}	High-level output voltage	I_{OH} = 500 µA	0.9V_{DD}			V
V_{OL}	Low-level output voltage	I_{OL} = 500 µA			0.1V_{DD}	

transmit path electrical characteristics (see the functional block diagram)

input stage gain M1O/M2O to TXVO, V_{DD} = 4 V

PARAMETER	TEST CONDITIONS†		MIN	MAX	UNIT
Gain	MICTRIM = <1000>		−0.5	0.5	dB
MICTRIM positive range	MICTRIM = <1111>		3.3	4.3	dB
MICTRIM negative range	MICTRIM = <0000>		−4.8	−3.8	dB
MICTRIM step size			0.38	0.68	dB
Preamp CMRR			48		dB
Distortion	V_I = 0.8 V,	f = 1 kHz		0.5%	
MICSW isolation	V_I = 80 mV,	f = 1 kHz	50		dB

† The control bits associated with a block or function are shown in < > (see Table 1).

compressor CIN to CO, V_{DD} = 4 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Unity gain level†		60.7	82	102.3	mV
E_L	Relative linearity error	$V_I = V_{ref}$ + 2 dB to V_{ref} − 18 dB		−0.01	±0.5	dB
		$V_I = V_{ref}$ − 18 dB to V_{ref} − 48 dB		−0.16	±1	dB
R_{COMP}	Compressor resistance		37	47	67	kΩ

‡ This parameter becomes V_{ref} for the relative-linearity-error test conditions.

output stage TXVI to TXO, V_{DD} = 4 V

PARAMETER	TEST CONDITIONS†	MIN	MAX	UNIT
TXTRIM step size		0.16	0.36	dB
TXTRIM positive range	TXTRIM = <11111>	3.5	4.5	dB
TXTRIM negative range	TXTRIM = <00000>	−4.8	−3.8	dB
TXATTEN step size		7	9	dB
TXATTEN range		21	27	dB

† The control bits associated with a block or function are shown in < > (see Table 1).

output stage limiter TXVI to TXO, V_{DD} = 4 V

PARAMETER	TEST CONDITIONS†	MIN	MAX	UNIT
Maximum output signal	TXVI = 253 mV, f = 300 Hz to 25000 Hz, LIM = <110>		1520	mVpp
Distortion	f = 1 kHz, Level at TXO = 2/3 × level measured in previous test, LIM = <110>		3%	
Trim step size, analog test mode A, output at RXDO	TXVI = 253 mV	0.8	1.2	dB
Trim positive range, analog test mode A, output at RXDO	LIM = <111>	2.5	3.5	dB
Trim negative range, analog test mode A, output at RXDO	LIM = <000>	−4.5	−3.5	dB

† The control bits associated with a block or function are shown in < > (see Table 1).

output stage frequency response TXVI to TXO, V_{DD} = 4 V

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Frequency response	0-dB reference at f = 1 kHz, TXVI = 20.8 mV	f < 200 Hz		–20	dB
		f = 300 Hz	–13.46	–9.46	dB
		f = 500 Hz	–9.02	–5.02	dB
		f = 2000 Hz	3.02	7.02	dB
		f = 2500 Hz	4.96	8.96	dB
		f = 3000 Hz	4.96	10.54	dB
		f = 5900 Hz		–35	dB
		f = 6000 Hz		–35	dB

overall transmit path electrical characteristics M1O/M2O to TXO, TXATT = <00>, V_{DD} = 4 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Compressor bypass gain	MICT = <1000>, TXT = <10000>		10.8	12	13.0	dB
Output noise, compressor enabled, M1O/M2O = V_{MID} psophometric weighting	RXIN = 320 mV,	f = 1 kHz		2.3	6.47	mVrms
Voice mute attenuation	M1O/M2O = 80 mV,	f = 1 kHz	50	–80		dB

† The control bits associated with a block or function are shown in < > (see Table 1).

DATA output levels TXDA to TXO, V_{DD} = 4 V

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
Output level	AMPS	f_I = 10-kHz square wave, amplitude 0 V to 4 V	856	950	mVpp
	TACS	f_I = 8-kHz square wave, amplitude 0 V to 4 V	856	950	mVpp
Frequency response	AMPS	–3 dB relative to 1 kHz, Analog test mode B	17	22	kHz
	TACS		14.4	17.6	kHz
Transmit data mute attenuation			50		dB

SAT output levels TXSA to TXO, V_{DD} = 4 V

PARAMETER	TEST CONDITIONS†		MIN	MAX	UNIT
Output level	ISAT = <0>, f_I = 6-kHz square wave, amplitude 0 V to 4 V		76.2	93.1	mV
SAT trim positive range			1.9	2.4	dB
SAT trim negative range			–2.8	–2.2	dB
SAT trim step size			0.2	0.4	dB
Frequency response	0-dB reference at f = 6 kHz, ISAT = <0>	f < 3 kHz		–35	dB
		f = 4.8 kHz		–25	dB
		f = 5.1 kHz		–20	dB
		f = 5.8 kHz	–5	0.5	dB
		f = 5.94 kHz	–0.5	0.5	dB
		f = 6.06 kHz	–0.5	0.5	dB
		f = 6.2 kHz	–5	0.5	dB
		f = 7.2 kHz		–20	dB
		f > 9 kHz		–35	dB
Transmit SAT mute attenuation			50		dB

† The control bits associated with a block or function are shown in < > (see Table 1).

SAT output level RXIN to TXO, RXT = <1000>, SAT = <1000>, TXT = <10000>, V_{DD} = 4 V

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
SAT output level	ISAT = <1>, Input to RXIN = 6-kHz sine wave, amplitude 480 mV		320		mV

† The control bits associated with a block or function are shown in < > (see Table 1).

receive path electrical characteristics (see the functional block diagram)

input stage RXIN to RXO, V_{DD} = 4 V

PARAMETER	TEST CONDITIONS†		MIN	MAX	UNIT
Gain	RXTRIM = <1000>		−6.4	−5.2	dB
RXTRIM positive range	RXTRIM = <1111>		3.2	4.2	dB
RXTRIM negative range	RXTRIM = <0000>		−4.5	−3.8	dB
RXTRIM step size			0.39	0.69	dB
Frequency response	0-dB reference at f = 1 kHz, RXIN = 320 mV	f <100 Hz		−28	dB
		f = 240 Hz		12.9	dB
		f = 300 Hz	8	11	dB
		f = 400 Hz	7.5	8.6	dB
		f = 2400 Hz	−8.2	−7.1	dB
		f = 3000 Hz	−12	−9	dB
		f > 5900 Hz		−40	dB

† The control bits associated with a block or function are shown in < > (see Table 1).

Expander EXIN to EXO, V_{DD} = 4 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Unity gain level = V_{ref}‡		64.1	100	104.1	mV
Relative linearity error	EXIN = V_{ref} +9.5 dB to V_{ref} −2.8 dB		−0.3	±1	dB
	EXIN = V_{ref} −2.8 dB to V_{ref} −23.8 dB		−0.8	±2	dB
Internal Expander resistance (R_{EXP})		37.5	47	71.6	kΩ

‡ This parameter becomes V_{ref} for the relative-linearity-error test conditions.

output stage

PARAMETER		TEST CONDITIONS†	MIN	MAX	UNIT
Volume control	Gain RXVI to SP1/SP2	VOL = <1000>	0.5	1.5	dB
	Positive range	VOL = <1111>	13	15	dB
	Negative range	VOL = <0000>	−16.5	−15.5	dB
	Step size		1.75	2.25	dB
CTI input	Gain to SP1/SP2	VOL = <1000>	0	2	dB
Expander bypass gain from RXIN to SP1/SP2		VOL = <1000>	−5.5	−4	dB
Output load at SP1/SP2			500		Ω
Output voltage at SP1/SP2		R_L = 500 Ω	1.96		Vpp
Distortion at SP1/SP2, expander enabled		RXIN = 400 mV, f = 1 kHz, No load		2%	
Noise at SP1/SP2, expander bypassed		RXIN = V_{MID}, psophometric weighting		3	mV
Voice mute attenuation		RXIN = 400 mV, f = 1 kHz	50		dB

† The control bits associated with a block or function are shown in < > (see Table 1).

RX DATA comparator RXIN to RXDO, V_{DD} = 4 V

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Must-detect level	f = 4 kHz, 5 kHz, 8 kHz, and 10 kHz		168.2		mVpp
Must-not-detect level				35.4	
Output duty cycle		RXIN = 900 mV peak to peak	47.5%	52.5%	

RX SAT frequency response RXIN to RXSO, SATDIG = <1>, V_{DD} = 4 V

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Frequency response	0-dB reference at f = 6 kHz	f < 3 kHz		−35	dB
		f = 4.8 kHz		−25	dB
		f = 5.1 kHz		−19	dB
		f = 5.8 kHz	−5	0.5	dB
		f = 5.94 kHz	−0.5	0.5	dB
		f = 6.06 kHz	−0.5	0.5	dB
		f = 6.2 kHz	−5	0.5	dB
		f = 7.2 kHz		−20	dB
		f > 9 kHz		−35	dB

RX SAT comparator RXIN to RXSO, SATDIG = <0>, V_{DD} = 4 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Must-detect level	f = 6 kHz	51	30		mVrms

miscellaneous block electrical characteristics

digital-to-analog converters DAC1, DAC2, and DAC3

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
Output voltage at code 255	DACX2 = <1>	V_{DD}−130			mV
Output voltage at code 255	DACX2 = <0>	V_{DD}/2 −100		V_{DD}/2 + 100	mV
Zero code offset			13	40.3	mV
Differential nonlinearity (codes 5 – 250)			0.3	1	LSB
Integral nonlinearity (codes 5 – 250)			0.3	1	LSB

† The control bits associated with a block or function are shown in < > (see Table 1).

analog-to-digital converters, DCLK = 160 kHz, V_{DD} = 4 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Full scale for inputs ADC1, ADC2, and V_{MID}		2.3		2.6	V
Differential nonlinearity			0.5	1	LSB
Integral nonlinearity			0.5	1	LSB
Clock rate (DCLK)				200	kHz

DTMF generator transmit levels at TXO, TXTRIM = <10000>, V_{DD} = 4 V

PARAMETER	DTTR†	TEST CONDITIONS	MIN	TYP	MAX	UNIT
697-Hz tone, low tone	<0100>	AMPS mode	86.8	117	129.6	mV
1477-Hz tone, high tone			238.8	264	296.5	mV
697-Hz tone, low tone		TACS mode	48.6	60	71.5	mV
1477-Hz tone, high tone			110.6	137	153.5	mV
DTMF trim steps	<0000> – <0001>			0.4		dB
	<0001> – <0010>			0.4		dB
	<0010> – <0011>			0.4		dB
	<0011> – <0100>			0.5		dB
	<0100> – <0101>			0.5		dB
	<0101> – <0110>			0.6		dB
	<0110> – <0111>			0.6		dB
	<0111> – <1000>			0.7		dB
	<1000> – <1001>			0.7		dB
	<1001> – <1010>			0.8		dB
	<1010> – <1011>			0.9		dB
	<1011> – <1100>			1.0		dB
	<1100> – <1101>			1.1		dB
	<1101> – <1110>			1.3		dB
	<1110> – <1111>			1.5		dB
Positive range	<0100> – <1111>		7.63	9.8	11.75	dB
Negative range	<0100> – <0000>		−2.58	−1.39	−1.29	dB
Skew, change in level of high tone	<0100>		1.3	1.85	2.2	dB
Distortion products	<0100>	Relative to low tone		−30		dB

† The control bits associated with a block or function are shown in < > (see Table 1).

DTMF generator receive levels at SP1 and SP2, DTTR = <0100>, VOL = <1000>, V_{DD} = 4 V

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
All tones	AMPS mode	45.6	54.6	mV
	TACS mode	22.5	29.1	mV
Distortion products	Relative to low tone		−40	dB

TYPICAL CHARACTERISTICS

TRANSMIT VOICE FREQUENCY RESPONSE

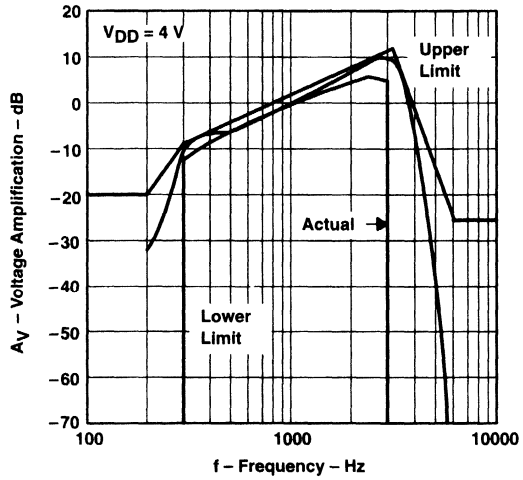


Figure 1

TRANSMIT PASS-BAND DETAIL

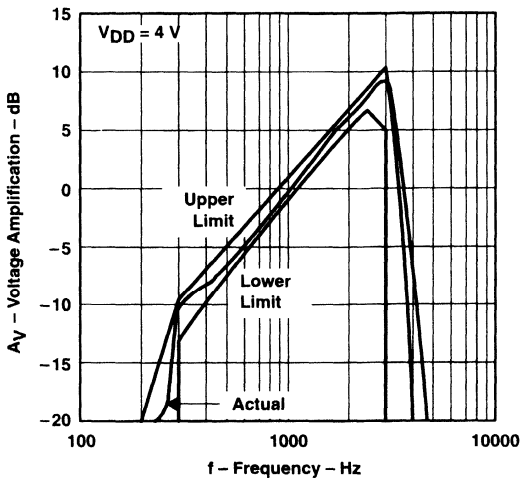


Figure 2

RECEIVE VOICE FREQUENCY RESPONSE

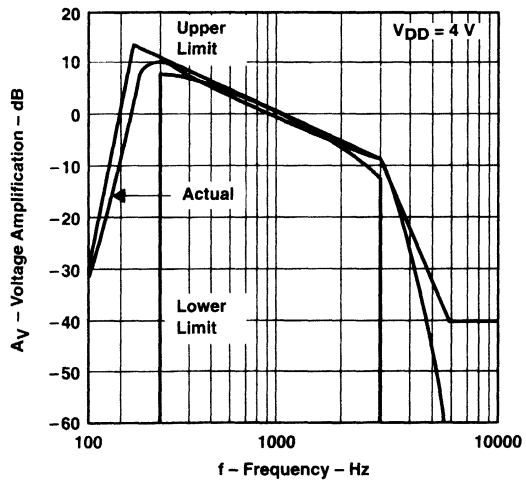


Figure 3

RECEIVE PASS-BAND DETAIL

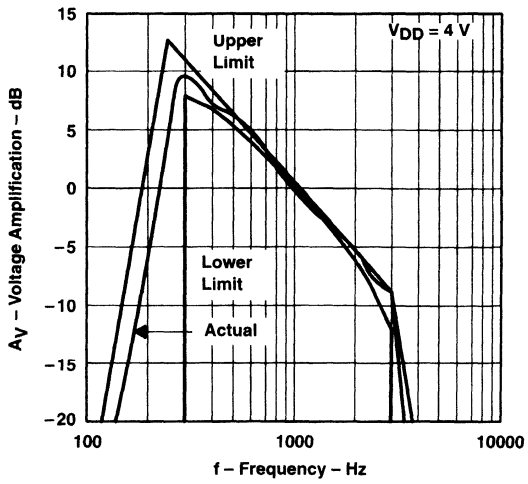


Figure 4

TYPICAL CHARACTERISTICS

TRANSMIT SAT FREQUENCY RESPONSE

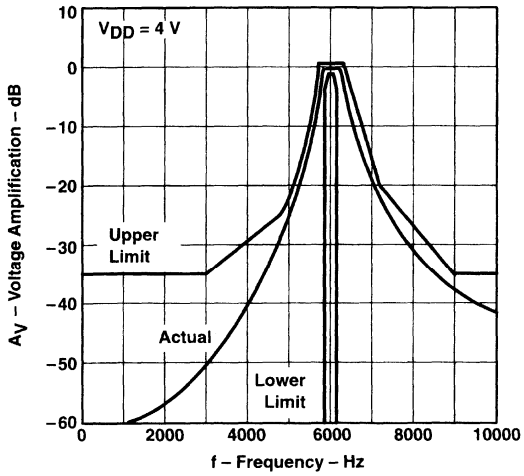


Figure 5

TRANSMIT PASS-BAND DETAIL

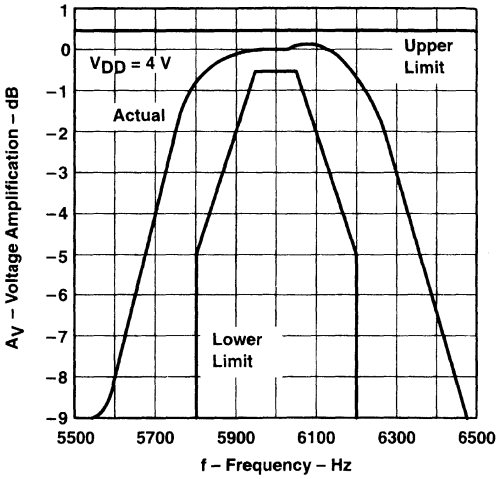


Figure 6

RECEIVE SAT FREQUENCY RESPONSE

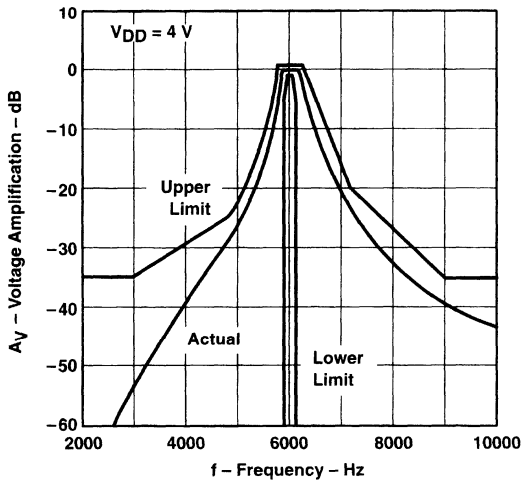


Figure 7

RECEIVE PASS-BAND DETAIL

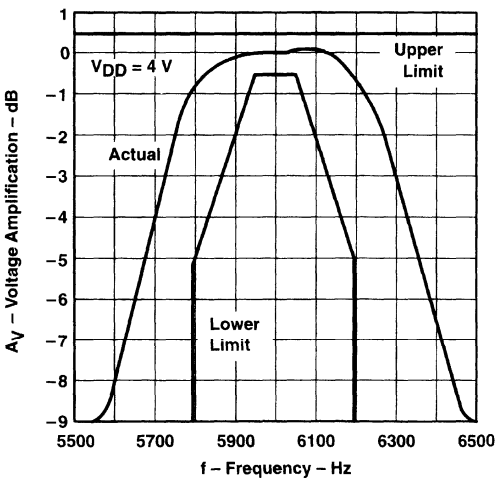


Figure 8

TYPICAL CHARACTERISTICS

TRANSMIT DATA FREQUENCY RESPONSE – AMPS

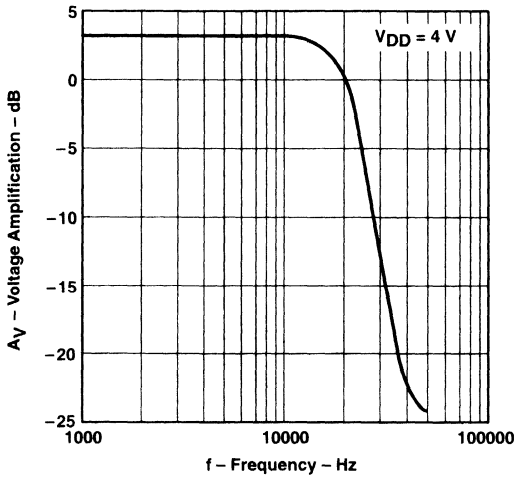


Figure 9

TRANSMIT DATA FREQUENCY RESPONSE – TACS

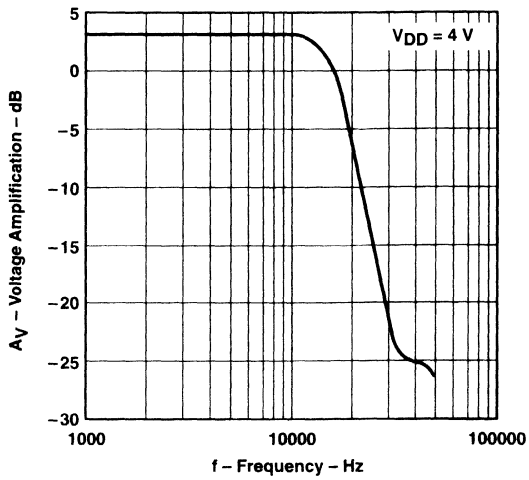


Figure 10

COMPRESSOR LINEARITY

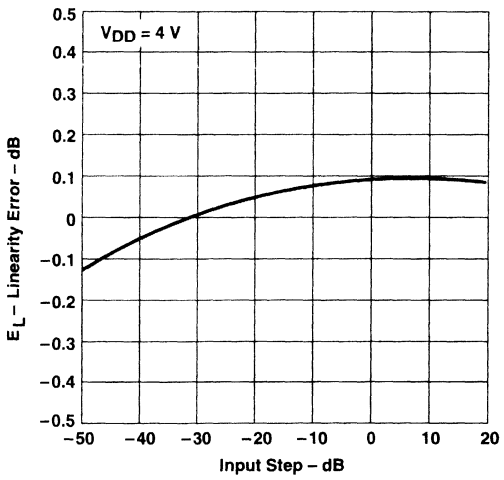


Figure 11

EXPANDER LINEARITY

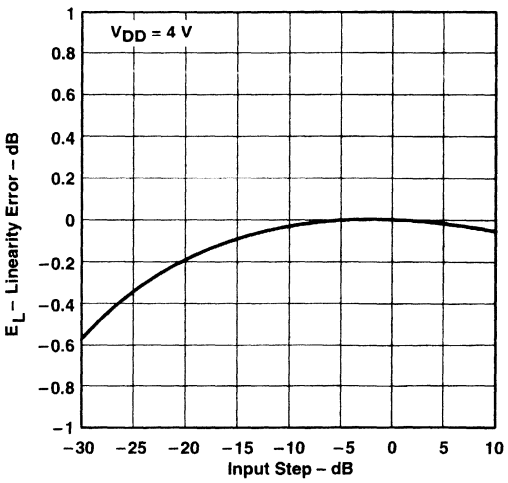


Figure 12

PRINCIPLES OF OPERATION

general

The TCM8010-37 consists of a number of functional blocks and is controlled by the digital control interface. The control bits associated with each block are shown in the angled brackets symbol < >. In standby mode <STBY>, the receive data path from RXIN to RXDO is on and the DACs can be on or off as required. All other parts of the device, including the crystal oscillator, are off. When in the active mode, the receive and transmit paths and the DAC blocks are continuously on, and the DTMF generators and ADCs are turned on as required.

Control bits <MD_1 – MD_0> set the TCM8010-37 for the desired system (AMPS or TACS).

transmit path

The transmit path on the TCM8010-37 consists of a number of functional blocks, which are described in the following paragraphs.

MIC INPUTS

Voice signals are input on M1P, M1N, M2P, and M2N to a pair of microphone preamplifiers, which are stable for gains between 0 dB and 20 dB. All voice-path specifications are given with the preamplifiers configured as unity-gain inverting amplifiers. In standby mode, the bias to the microphone preamplifiers is turned off and the outputs M1O and M2O are in the high-impedance state.

MICSW

The MICSW block is a 2-input switch that selects either of the preamplifier outputs, and is under control of the digital control interface through the control word <MICSEL>.

MICTRIM

The MICTRIM block provides gain adjustment to compensate for differing microphone sensitivities <$MICT_3$ – $MICT_0$>. A second-order Sallen-Key low-pass filter is incorporated in this block to provide antialiasing for the transmit voice signal.

COMPRESSOR

The compressor provides a 1-dB change in output signal level for a 2-dB change in input level over an operating input range of 50 dB. The unity-gain point, V_{ref}, is proportional to the value of V_{DD} (see the compressor table in the transmit path electrical charactistics). Attack time is measured by increasing the input-signal amplitude by a 12-dB step relative to 13 mV rms and is defined as the time required for the output envelope to reach 1.5 times the final steady-state level. Recovery time is measured by reducing the input signal amplitude by a 12-dB step to 13 mV rms and is defined as the time required for the output envelope to settle to 0.75 times the final steady-state level.

The attack and recovery times are determined by an internal resistor (R_{COMP}) and the external capacitor, C_{CTC}, connected between CTC and V_{SS} (0 V).

Attack time = $0.151 \times C_{CTC} \times R_{COMP}$

Recovery time = $0.693 \times C_{CTC} \times R_{COMP}$

TXSW

This functional block is a 3-input switch that selects either the compressor output, compressor bypass (for testing), or the output of the DTMF generator. TXSW is controlled by <$TXSW_1$ – $TXSW_0$>.

PRINCIPLES OF OPERATION

TXATTEN

The output of TXSW passes through the TXATTEN block, which provides four levels of attenuation.

PRE-EMPHASIS

The output from TXATTEN is connected to the Pre-emphasis block, which provides the necessary 6 dB per octave increase in gain with frequency by using a second-order filter. Also included in this block is an eighth-order band-pass filter function with a 300-Hz to 3-kHz passband. The nominal gain of this stage is 6 dB at 1 kHz and its output is routed to the POUT terminal.

LIMITER

The Limiter block limits the maximum output under overload signal conditions, and the limit level is adjustable under control serial interface bits <LIM_2 – LIM_0>. The limiter range is designed to allow the transmit path distortion and maximum signal output specifications to be achieved at a single limiter-adjustment code. The output of the Pre-emphasis block is ac coupled (through an external capacitor) into the LIMIN terminal to ensure symmetrical limiting.

LOW-PASS FILTER

The limiter output is processed by the Low-Pass Filter block, which is a fourth-order low-pass filter plus second-order equalizer, to remove excessive harmonics produced by the limiting process.

TXSUM

This block can sum together or mute any of its three inputs (SAT, data, and voice) under the control of the <TXSAT, TXDAT, TXVOX> bits respectively.

TXTRIM

The TXTRIM gain-adjust block can compensate for different modulator sensitivities using bits <TXT_4 – TXT_0>. A continuous-time output low-pass smoothing filter is included with a typical cutoff frequency of 30 kHz.

TX DATA FILTER

Transmit data is input to terminal TXDA and is routed to the TX Data Filter block where the data is first conditioned by a second-order antialiasing filter before going on to the transmit data filter.

The transmit data is a Manchester-encoded digital signal at 10k bit/s for AMPS or 8k bits/s for TACS. The transmit data filter for these two modes is a fourth-order Butterworth low-pass filter, with its –3-dB point switchable between AMPS and TACS modes.

The filtered AMPS or TACS wide-band data signal is summed into the transmit signal path in the TXSUM block.

TXSAT FILTER PATH – TXSA to TXO

The input to the transmit SAT signal path is determined by the SATSW block, which selects between the TXSA terminal and the output of the receive SAT filter (RXSAT). The signal is processed by the TXSAT filter block, which includes an antialiasing filter, a fourth-order narrow-band band-pass filter centered at 6 kHz, and a gain-adjust stage <SAT_3 – SAT_0>. The output of this block is then applied to an input of TXSUM to be summed into the voice path when selected.

PRINCIPLES OF OPERATION

receive path – voice

The demodulated signal from the receiver is input to the TCM8010-37 at the RXIN terminal. A pair of loudspeaker drivers are provided, producing output signals on terminals SP1 and SP2, and are capable of driving 500-Ω loads.

RXTRIM

A gain-adjust block, RXTRIM, is provided to allow variations in the receiver FM demodulator/discriminator characteristics to be accommodated <RXT_3 – RXT_0>. This block is enabled in both active and standby modes. A second-order continuous-time filter with a typical cutoff frequency of 30 kHz provides an antialiasing function for the receive signal path.

DE-EMPHASIS

The De-emphasis filter block exhibits a 6-dB/octave decrease in gain versus frequency characteristic. It also includes an eighth-order band-pass filter (passband = 300 Hz to 3 kHz) to separate the received voice signal from the data and SAT signals. A continuous-time smoothing filter is incorporated at the output, and the output signal appears at terminal RXO.

EXPANDER

The Expander block provides a 2-dB change in output signal level for a 1-dB change in input level over an operating input range of 33 dB. The unity-gain level, V_{ref}, is proportional to V_{DD} (see the expander table in the receiver path electrical charactistics). Attack time is measured by increasing the input signal amplitude by a 6-dB step relative to 72.5 mV and is defined as the time required for the output envelope to reach 0.57 times the final steady-state level. Recovery time is measured by reducing the input signal amplitude by a 6-dB step to 72.5 mV and is defined as the time required for the output envelope to settle to 1.5 times the final steady-state level.

The attack and recovery times are determined by an internal resistor, R_{EXP}, and the external capacitor, C_{EXP}, connected to ETC and 0 V, V_{SS}.

Attack time = $0.173 \times C_{ETC} \times R_{EXP}$

Recovery time = $0.693 \times C_{ETC} \times R_{EXP}$

RXSW

RXSW is a 4-input switch block that provides a selection between the call-tone input terminal (CTI), the expander output (externally capacitively coupled to terminal RXVI), the expander-bypass path (for testing), and the output from the DTMF generator as the input to the volume-control block. The control bits are <$RXSW_1$ and $RXSW_0$>.

To simplify the connection of a digital signal for a *user alert* tone (typically between 200 Hz and 400 Hz), no internal bias is provided for the CTI input. If an ac-coupled signal is applied to CTI, an external bias resistor with a typical value of 100 kΩ is required and should be connected between CTI and V_{MID}.

VOLUME CONTROL

The Volume Control block provides output level adjustment to implement a user-adjustable level control using control bits <VOL_3 – VOL_0>.

LSSW

The loudspeaker control switch block (LSSW) allows selection between either SP1 or SP2 outputs, muting, or differential drive of both terminals through the control bits <LS_1 – LS_0>.

PRINCIPLES OF OPERATION

receive path – data/SAT

The demodulated signal from the receiver is input to the TCM8010-37 at the RXIN terminal. This signal, containing voice, data, and SAT components, is processed and antialias-filtered by the RXTRIM block.

receive data path – DATA COMPARATOR

The signal from RXTRIM is applied to the data comparator block, which has defined threshold levels. The data signal is Manchester-encoded at 10 kbit/s for AMPS mode and at 8 kbit/s for TACS mode. Detected data appears at RXDO. This signal path is enabled in the standby mode.

receive SAT path – RX SAT FILTER

The RX SAT Filter block uses a fourth-order Butterworth band-pass filter centered at 6 kHz to separate received SAT signals from the voice signal. The output of the band-pass filter is routed to an input of the SATSW block and to the SAT Comparator block.

receive SAT path – SATSW

SATSW is a 2-input switch block that selects between the output of the RX SAT filter and an external SAT source (applied to terminal TXSA) using control bit <ISAT>.

receive SAT path – SAT COMPARATOR

The SAT Comparator block recovers the SAT signal and has defined hysteresis levels for improved noise immunity. The output is routed to terminal RXSO. An internal switch, controlled by bit <SATDIG>, bypasses the SAT comparator and applies the output from the RX SAT Filter block directly to terminal RXSO.

digital interface

The TCM8010-37 is controlled by a 3-wire digital interface, consisting of a clock signal (DCLK), a chip select ($\overline{CS}$), and a bidirectional data line (DATA). The logic signal present on DATA is written into the device on the rising edge of DCLK when $\overline{CS}$ is low. Serial messages to and from the device contain a read/write bit, an address field, and a data word. Results from the ADC are read back using the serial interface, and the DCLK signal is used to drive the converter. Test access to analog and digital sections of the device are provided using the serial interface.

write operations

A timing diagram for a write operation to the device is shown in Figure 13. In this case, the read/write bit is set to 1, followed by a 3-bit address word (A2–A0), and a 10-bit data word (D9–D0). Data shifts into the device on the rising edge of DCLK and is transferred to internal registers on the falling edge of the fourteenth clock pulse after $\overline{CS}$ goes low. If $\overline{CS}$ returns high before this time, no transfer takes place and the input interface is reset.

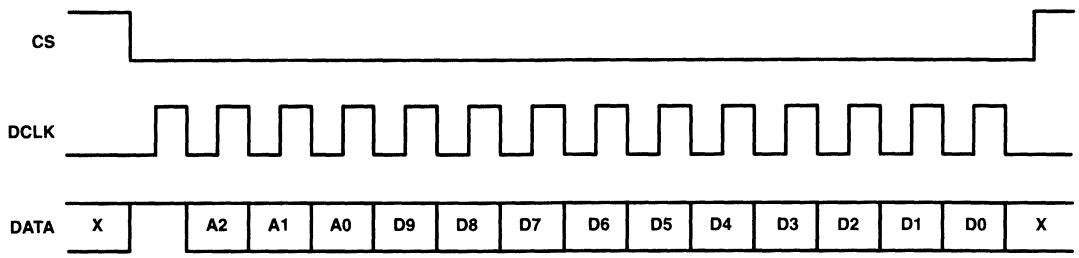


Figure 13. Write-Operation Timing

PRINCIPLES OF OPERATION

control words

Table 1 shows control-word and configuration assignments for the device. Table 2 shows control-word descriptions, Table 3 shows test modes, and Table 4 details DTMF control words.

Table 1. Control-Word and Configuration Assignments

	Address Bits			CONTROL DATA BITS									
	A_2	A_1	A_0	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Word 0	0	0	0	STBY	MD_1	MD_0	ISAT	SATDIG	DACX2	CKSEL	$CKRT_2$	$CKRT_1$	$CKRT_0$
Word 1	0	0	1	$TXSW_1$	$TXSW_0$	TXSAT	TXDAT	TXVOX	$TXATT_1$	$TXATT_0$	DACON	LS_1	LS_0
Word 2	0	1	0	MICSEL	$MICT_3$	$MICT_2$	$MICT_1$	$MICT_0$	TXT_4	TXT_3	TXT_2	TXT_1	TXT_0
Word 3	0	1	1	LIM_2	LIM_1	LIM_0	SAT_3	SAT_2	SAT_1	SAT_0	1	0	0
Word 4	1	0	0	RXT_3	RXT_2	RXT_1	RXT_0	$RXSW_1$	$RXSW_0$	VOL_3	VOL_2	VOL_1	VOL_0
Word 5	1	0	1	DTSK	$DTTR_3$	$DTTR_2$	$DTTR_1$	$DTTR_0$	0	0	0	$TEST_1$	$TEST_0$
Word 6	1	1	0	$DACAD_1$	$DACAD_0$	DAC_7	DAC_6	DAC_5	DAC_4	DAC_3	DAC_2	DAC_1	DAC_0
Word 7	1	1	1	—	—	—	—	—	—	$DTMF_3$	$DTMF_2$	$DTMF_1$	$DTMF_0$

Table 2. Control-Word Descriptions

	DESCRIPTION
Word 0	STBY = Standby select: 0 = Standby, 1 = Active MD_1 – MD_0 = Mode select: 00 = AMPS, 01 = Undefined, 10 = TACS, 11 = Undefined ISAT = SAT select: 0 = External, 1 = Internal SATDIG = Digital/Analog RX SAT: 0 = Digital, 1 = Analog DACX2 = DAC range select: 0 = 0 – $V_{DD}/2$, 1 = 0 – V_{DD} CKSEL = Clock source select: 0 = Oscillator, 1 = Sinusoidal input $CKRT_2$ – $CKRT_0$ = Clock rate select: 000 = 3.58 MHz, 001 = 7.16 MHz, 010 = 10.74 MHz, 011 = 14.32 MHz, 100 = 2.56 MHz, 101 = 10.24 MHz, 110 = 12.80 MHz, 111 = 15.36 MHz
Word 1	$TXSW_1$ – $TXSW_0$ = TX Voice select: 00 = Mute, 01 = Compressor O/P, 10 = Compressor bypass, 11 = DTMF TXSAT = Transmit SAT enable: 0 = Mute, 1 = Enable TXDAT = Transmit Wide-band data enable: 0 = Mute, 1 = Enable TXVOX = Transmit Voice enable: 0 = Mute, 1 = Enable $TXATT_1$ – $TXATT_0$ = TX attenuation: 00 = 0 dB, 01 = 8 dB, 10 = dB, 11 = 24 dB DACON = DACS on select in standby: 0 = Off, 1 = On LS_1 – LS_0 = Loudspeaker configuration: 00 = Mute, 01 = SP2 enable, 10 = SP1 enable, 11 = Differential
Word 2	MICSEL = Microphone select: 0 = M1, 1 = M2 $MICT_3$ – $MICT_0$ = Microphone trim: 0000 – minimum gain, 1111 = maximum gain TXT_4 – TXT_0 = TX Deviation trim: 00000 = minimum gain, 11111 = maximum gain
Word 3	LIM_2 – LIM_0 = Deviation limiter adjust: 000 = minimum deviation, 111 = maximum deviation SAT_3 – SAT_0 = TXSAT adjust: 0000 = minimum, 1111 = maximum D_0 – D_1 = 0, D_2 = 1
Word 4	RXT_3 – RXT_0 = RX input adjust: 0000 = minimum, 1111 = maximum $RXSW_1$ – $RXSW_0$ = RX switch control: 00 = CT input, 01 = Expander O/P, 10 = Expander bypass, 11 = DTMF VOL_3 – VOL_0 = RX path audio volume control: 0000 = minimum, 1111 = maximum
Word 5	DTSK = DTMF Skew enable: 0 = disabled, 1 = enabled $DTTR_3$ – $DTTR_0$ = DTMF adjust: 0000 = minimum, 1111 = maximum $TEST_1$ – $TEST_0$ = Test mode: (see Table 3) D_2 – D_4 = 0
Word 6	$DACAD_1$ – $DACAD_0$ = DAC address: 00 = DAC 1, 01 = DAC 2, 10 = DAC 3, 11 = all DACs
Word 7	$DTMF_3$ – $DTMF_0$ = DTMF control: (see Table 4)

PRINCIPLES OF OPERATION

Table 3. Test Modes (Word 5)

CONTROL BITS			MODE	TEST OUTPUTS	
SATDIG	$TEST_1$	$TEST_0$		AT RXDO	AT RXSO
X	0	0	Normal		
0	0	1	Digital Test	Digital DTMF High Tone	Digital DTMF Low Tone
1	1	0	Analog Test A	Receive Data (analog)	Limiter Output (dc)
1	1	1	Analog Test B	Bandgap Output	Transmit Data (analog)
0	1	0	Other States	Recieve Data (digital)	Receive SAT (digital)
0	1	1	Other States	Digital DTMF High Tone	Digital DTMF Low Tone
1	0	1	Other States	Digital DTMF High Tone	RXSAT (analog)

Table 4. DTMF Control (Word 7)

CONTROL BITS					DTMF GENERATOR OUTPUT	
$DTMF_3$	$DTMF_2$	$DTMF_1$	$DTMF_0$	KEY	LOW TONE (Hz)	HIGH TONE (Hz)
0	0	0	0	1	697	1209
0	0	0	1	4	770	1209
0	0	1	0	7	852	1209
0	0	1	1	*	941	1209
0	1	0	0	2	697	1336
0	1	0	1	5	770	1336
0	1	1	0	8	852	1336
0	1	1	1	0	941	1336
1	0	0	0	3	697	1477
1	0	0	1	6	770	1477
1	0	1	0	9	852	1477
1	0	1	1	#	941	1477
1	1	0	0	—	697	Off
1	1	0	1	—	Off	1209
1	1	1	0	—	Off	1477
1	1	1	1	—	Off	Off

PRINCIPLES OF OPERATION

read operations

A timing diagram of a read operation, which outputs ADC results from the device, is shown in Figure 14. The first bit driven into the device is a logic 0, followed by a 3-bit address word. The device then assumes control of the DATA line on the falling edge of the fifth clock pulse after $\overline{CS}$ goes low. The conversion result is output MSB first, with the MSB being output on the falling edge of the seventh clock pulse after $\overline{CS}$ goes low. Control of the DATA line is released (returned to input mode) when $\overline{CS}$ goes high.

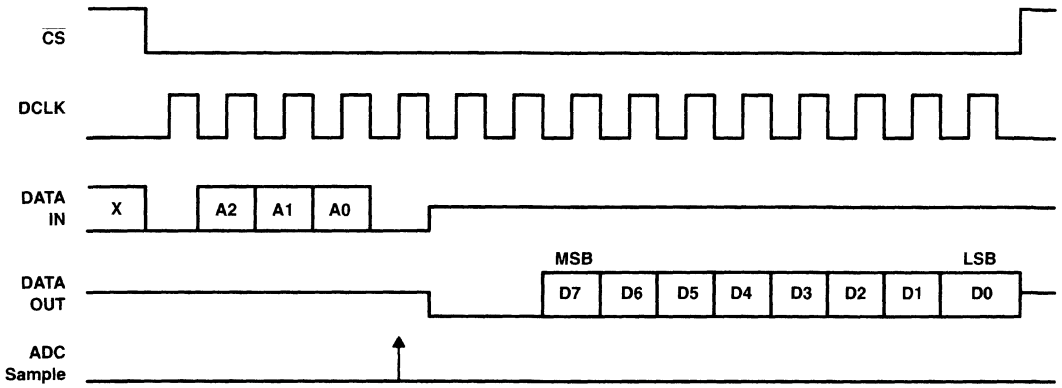


Figure 14. Read-Operation Timing

Table 5 details the decoding of the three address bits.

Table 5. Address Bit Decoding

A2	A1	A0	REFERENCE	MEASUREMENT
0	0	0	Band gap	V_{MID}
0	0	1	Band gap	ADC1
0	1	0	Band gap	ADC2

additional functions

The following paragraphs detail some additional functions of the TCM8010-37.

digital-to-analog converters

Three 8-bit, voltage-output DACs are provided, with outputs on terminals DAC1, DAC2, and DAC3. The output range of each converter is from 0 V to $V_{DD}/2$ or 0 V to V_{DD} with an LSB step size of $V_{DD}/256$ or $V_{DD}/2 \times 1/256$ as selected by <DACX2>. All DAC outputs can either go to 0 V in standby mode or be active depending on the state of control bit <DACON>. For correct operation of the TCM8010-37, < DACON > must be cleared to 0 in active mode. Previously written values are restored to the DAC outputs on entry to active mode. $<DACAD_1-DACAD_0>$ selects which DAC is being addressed, and $<DAC_7-DAC_0>$ sets the output voltage.

PRINCIPLES OF OPERATION

analog-to-digital converter

The TCM8010-37 contains an 8-bit ADC with a 3-channel analog-input multiplexer. This allows conversion of signals on ADC1, ADC2, and V_{MID}. An internal band-gap voltage reference multiplied by two is used when measuring ADC1, ADC2, and V_{MID}.

Fifteen periods of DCLK are required to complete a conversion.

DTMF Generator

The DTMF generator produces the seven standard tones with a frequency accuracy of ±1%. The desired DTMF signal is selected by <$DTMF_3$–$DTMF_0$>. A switchable pre-emphasis or skew between the low and high tone groups is provided for TACS operation and is selected by bit <DTSK>.

DTMF signal levels scale directly with supply voltage. A 4-bit trim is provided to allow adjustment of DTMF amplitude to meet system specifications and allow flexibility for user-generated call-tone-type signals (<$DTTR_3$–$DTTR_0$>). When DTMF is selected in the transmit or receive paths, typical voice signals are attenuated by 50 dB.

clock and supply

Power supply and clock considerations are covered in the following paragraphs.

supply voltage

Specifications are given for a supply voltage of 5 V. Signal levels such as SAT, DATA, and DTMF are derived from this. Other parameters such as the compressor and expander unity-gain levels are also dependent on the supply voltage.

supply current

The TCM8010-37 has two basic operating modes: standby and active. In the standby mode, only the receive data path is enabled and current consumption is less than 2 mA. There is also the option of keeping the DACs powered up in the standby mode, depending on the setting of <DACON>. In the active mode, all functional blocks are powered up and the current consumption is less than 12 mA.

crystal oscillator and clock interface

The clock signal for the device can be generated by the internal Oscillator block using an external crystal connected to the XTO and XTI terminals. Or, an external 0.5-V (minimum) peak sinusoidal clock signal can be applied to XTI. The external clock signal or the crystal can be one of eight frequencies, selected by control bits <$CKRT_2$–$CKRT_0$>. Crystal or external clock operation is selected by <CKSEL>.

APPLICATION INFORMATION

analog cellular telephone baseband solution

The TCM8002 and TCM8010-37 chip set provides a complete solution to the audio and data filtering, decoding, and encoding required in a cellular telephone for the AMPS or TACS systems. The applications circuit schematic is shown in Figure 15 and demonstrates that a minimum of external components is required.

The following extra functions are included in the TCM8010-37 and TCM8002:

- Three digital-to-analog converters
- An analog-to-digital converter
- Two timers
- I/O expansion

overall description

The following paragraphs detail the various function of the TCM8010-37 and TCM8002 chip set when used in this application.

TCM8010-37 transmit path

The inputs to the microphone amplifiers are MIC1 and MIC2. MIC1 could be used for the internal microphone and MIC2 for accessories (a hands-free unit, for example). the TCM8010-37 is designed for single-supply operation. REF is provided to bias the noninverting inputs of the microphone amplifiers, M1P and M2P. The wide-band data to be transmitted is input as a digital signal to TXDA. The TCM8010-37 then filters the signal and provides a level trim for it.

The TCM8002 produces a digitally-filtered signal, phase locked to the received SAT. This is then connected to the input TXSA of the TCM8010-37, which filters and provides level adjustment for the digital signal. The output from the TCM8010-37 is at TXO and should be connected to the modulator in the RF section. The voice, wide-band data, and SAT signal levels are programmable, eliminating the need for external adjustments.

TCM8010-37 receive path

The output from the FM demodulator/discriminator should be connected to the receive audio input (RXIN) of the TCM8010-37. Two audio outputs are provided at SP1 and SP2. These outputs can be configured to be two separate outputs, with one driving the telephone earpiece and the other for test or accessories, a hands-free unit for example, or optionally the outputs can be configured to provide a differential output to increase the maximum level.

The TCM8010-37 filters and converts the received wide-band data to a digital signal and outputs this at RXDO for connection to the TCM8002. The received SAT signal is filtered and converted to a digital signal. It is then made available at RXSO for transmission to the TCM8002.

TCM8010-37 digital-to-analog converters

Three uncommitted 8-bit DACs are included in the TCM8010-37 (DAC1OUT, DAC2OUT, and DAC3OUT). One can be used for power control of the RF transmit amplifier. The other two could be used to provide adjustment voltages for the RF stage such as calibrating the temperature-compensated crystal oscillator (TCXO) and trimming the first intermediate frequency (IF) stage.

TCM8010-37 analog-to-digital converter

Two multiplexed inputs to an ADC included in the TCM8010-37 are provided (ADCIN 1 and ADCIN 2). Possible uses are to measure battery voltage (using a potential divider) or received-signal-strength indicator (RSSI) voltage.

APPLICATION INFORMATION

TCM8002 transmit path

The data encoder includes all the necessary formatting for transmission on the control and voice channels. This digital signal is output at TXOUT. The received SAT digital signal is connected to TCM8002 SATIN and then the signal is recovered from the noise before being measured and regenerated. The digital output signal appears at TCM8002 SATOUT.

TCM8002 receive path

The received digital data signal is connected to RXIN for the control-and-voice channel data-recovery circuit. The data is then majority-voted and error-corrected. Finally, an interrupt is generated to signal the microcontroller that there is received data available.

TCM8002 timers

A watchdog timer is provided that can reset the microcontroller in the telephone if a fault occurs. This is a requirement of both the AMPS and TACS systems.

An uncommitted programmable 8-bit timer is also available with an output labeled TMZERO that pulses low when the count reaches zero.

TCM8002 I/O expansion

Twenty programmable I/O lines are provided for the telephone microcontroller. These are individually bit-programmable as outputs or inputs with optional current source pullups.

An intelligent interface to the TCM8010-37 audio processor provides an automatic audio-mute function when wide-band data is being transmitted or received.

TCM8002 and TCM8010-37 clock and control

Both the TCM8002 and TCM8010-37 are connected to the microcontroller through the serial interface ($\overline{CS}$, DCLK, DATAIN, DATAOUT, INTERRUPT). The TCM8002 can be programmed to generate interrupts when events such as received data available or the counter/timer reaching zero state occurs.

A low-power crystal oscillator is integrated into the TCM8002, and the CLKOUT output is provided for connection to the TCM8010-37.

APPLICATION INFORMATION

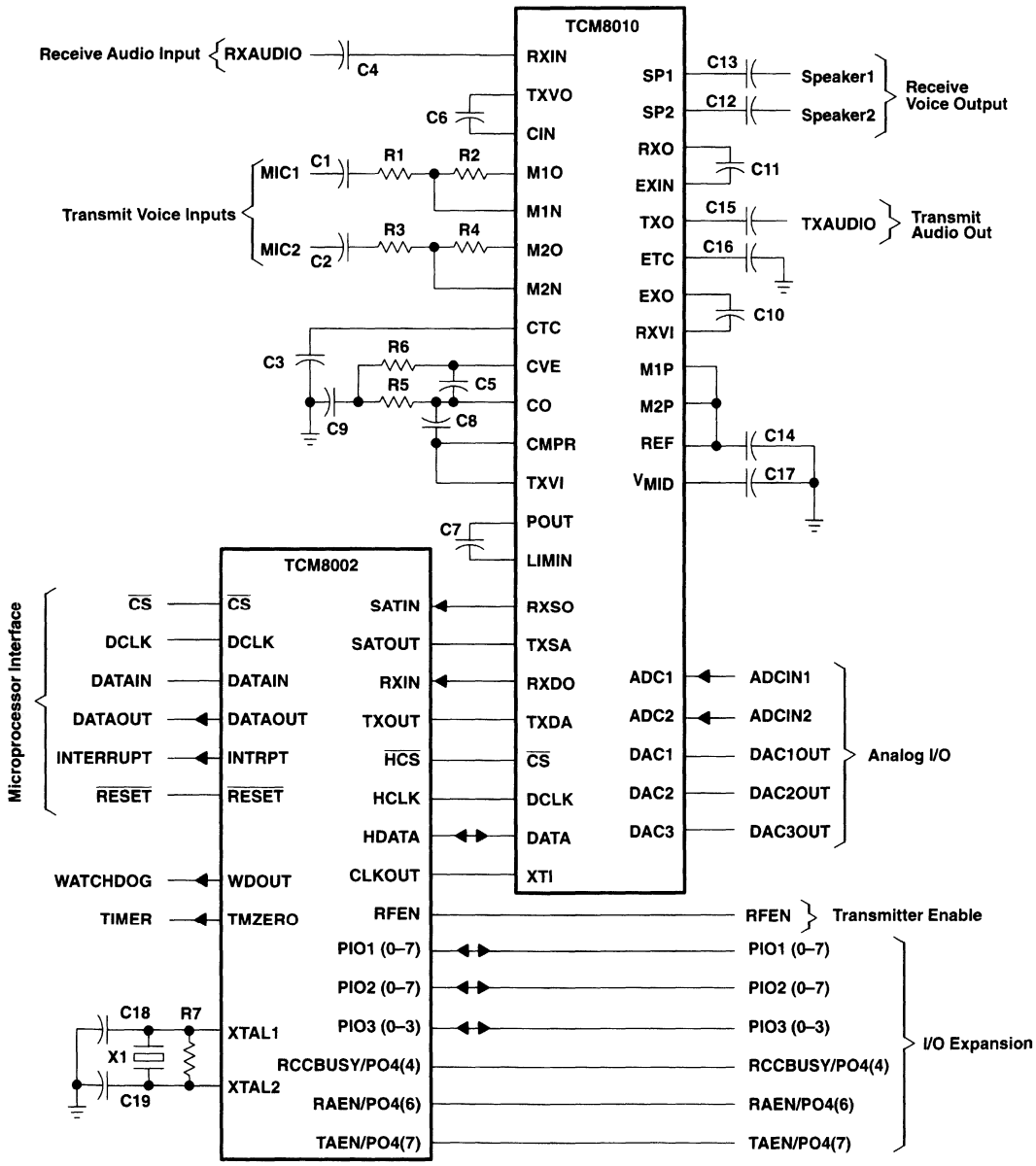


Figure 15. Complete Baseband Solution

APPLICATION INFORMATION

external component selection

COMPONENT DESIGNATION	TYPICAL VALUE	FUNCTION
R1	47 kΩ	Sets microphone preamplifier number 1 gain . . . R2/R1
R2	47 kΩ	Recommended minimum value
R3	47 kΩ	Sets microphone preamplifier number 2 gain . . . R4/R3
R4	47 kΩ	Recommended minimum value
R5	100 kΩ	Provides dc bias for the compressor
R6	100 kΩ	
R7	1 MΩ	Biasing resistor for crystal oscillator
C1	100 nF	AC couples the input to microphone preamplifier number 1 (MIC 1)
C2	100 nF	AC couples the input to microphone preamplifier number 2 (MIC 2)
C3	390 nF	Sets the attack and recovery times of the compressor
C4	10 nF	AC couples the receive audio and data input from the FM demodulator/discriminator
C5	47 pF	Required for HF stability of the compressor
C6	100 nF	AC couples the output of the selected microphone preamplifier to the compressor input. This is required because any dc offset would cause linearity errors.
C7	100 nF	AC couples the output of the preemphasis and band-pass filter to the limiter stage to ensure symmetrical clipping
C8	100 nF	AC couples the output of the compressor to the transmit switch (TXSW). Since this is also the compressor rectifier input, any dc offset would cause linearity errors.
C9	100 nF	AC decouples the compressor dc feedback
C10	100 nF	AC couples the output from the expander to the receive switch (RXSW)
C11	100 nF	AC couples the input to the expander to remove offsets that would otherwise cause linearity errors at low signal levels
C12	—	Required when the earpiece drive is single ended (not differential)
C13	—	
C14	470 nF	Decouples the resistor divider that produces REF, the input for the V_{MID} generator
C15	100 nF	AC couples the output from the transmit voice, data, and SAT signals to the FM modulator in the RF section
C16	330 nF	Sets the attack and recovery times of the expander
C17	470 nF	Provides a low ac impedance reference for the transmit and receive paths
C18	33 pF	Provides X1 with the required capacitive loading
C19	33 pF	Provides X1 with the required capacitive loading
X1	2.56 MHz	Crystal

printed circuit board layout precautions

Resistors R5 and R6 should be placed close to the TCM8010-37 to minimize stray capacitance between CO and CVE. Otherwise, compressor gain errors are caused at low signal levels and high frequencies.

suggested trim sequence

The TCM8010-37 and TCM8002 are designed so that no manual trims are required. All levels can be adjusted to meet the system requirements and compensate for production tolerances by writing to the digital interface. The data required can then be stored in a nonvolatile memory by the microcontroller in the telephone. When the telephone is turned on, an initialization routine can write this calibration data to the TCM8010-37.

APPLICATION INFORMATION

suggested trim sequence (continued)

The suggested sequence of adjustments for trimming is detailed below.

To begin the transmission portion of the trim sequence:

Step 1. TXTRIM

a. Set the transmit data trim <DAT_2 – DAT_0> to nominal = <100>.
b. Set the TCM8002 and TCM8010-37 to transmit signaling tone.
c. Adjust <TXT_4 – TXT_0> to set the frequency deviation to that required by either the AMPS or TACS system.

Step 2. TXSAT

a. Turn the signaling tone off and turn on the SAT path. Input a 6-kHz signal to RXIN.
b. Adjust <SAT_3 – SAT_0> to give the required frequency deviation.

Step 3. MICTRIM

a. Mute the signaling tone and SAT.
b. Inject an audio signal at the desired level into the microphone preamplifier.
c. Adjust <$MICT_3$ – $MICT_0$> to set the frequency deviation.

Step 4. LIMITER TRIM

a. Increase the audio signal level by 20 dB typically.
b. Adjust <LIM_2 – LIM_0> to produce the required maximum deviation.

Step 5. DTMF TRIM

a. Mute the signaling tone, audio, and SAT.
b. For TACS, set bit <DTSK> to enable the skew of the levels between the low and high tones.
c. Turn on the DTMF generator and adjust <$DTTR_3$ – $DTTR_0$> to give the desired frequency deviation.

Continue with the receive portion of the trim sequence;

Step 6. RXTRIM

Input a modulated signal to the telephone and adjust <RXT_3 – RXT_0> to produce the required level at SP1 and SP2.

Ending with the RF stage:

Step 7. DACs to trim RF section

Three 8-bit DACs can be used to trim sections of the RF stage using <$DACCAD_1$ – $DACAD_0$> to select the DAC and <DAC_7 – DAC_0> to set the level. <DACX2> sets the range of all three DACs and <DACON> enables all three outputs when the TCM8010-37 is in standby.

Typical uses would be RF transmit power control, TCXO trim, and first IF section trim.

APPLICATION INFORMATION

transmit signal levels

The TCM8010-37 is designed for signal levels detailed in the following tables for the AMPS and TACS systems. These tables suggest levels for both the transmitted and received audio, SAT, and DATA signals.

AMPS mode

SIGNAL	PEAK FREQUENCY DEVIATION (kHz)	LEVEL AT TXO	UNIT
Design level	8	400	mVrms
Peak voice level	12	1697.1	mVpp
SAT	2	100	mVrms
DATA	8	1131.4	mVpp
DTMF low tone, 697 Hz	3.1365	156.8	mVrms
DTMF high tone, 1477 Hz	6.6465	332.3	mVrms

TACS mode

SIGNAL	PEAK FREQUENCY DEVIATION (kHz)	LEVEL AT TXO	UNIT
Design level	5.7	356.3	mVrms
Peak voice level	9.5	1697.6	mVpp
SAT	1.7	106.3	mVrms
DATA	6.4	1131.5	mVpp
DTMF low tone, 697 Hz	1.2 max	75	mVrms
DTMF high tone, 1477 Hz	3.19 max	199.4	mVrms

receive signal levels

AMPS mode

SIGNAL	PEAK FREQUENCY DEVIATION (kHz)	LEVEL AT RXIN	UNIT
Design level	8	400	mVrms
Peak voice level	12	1697.1	mVpp
SAT	2	100	mVrms
DATA	8	1131.4	mVpp

TACS mode

SIGNAL	PEAK FREQUENCY DEVIATION (kHz)	LEVEL AT RXIN	UNIT
Design level	5.7	356.3	mVrms
Peak voice level	9.5	1697.6	mVpp
SAT	1.7	106.3	mVrms
DATA	6.4	1131.5	mVpp

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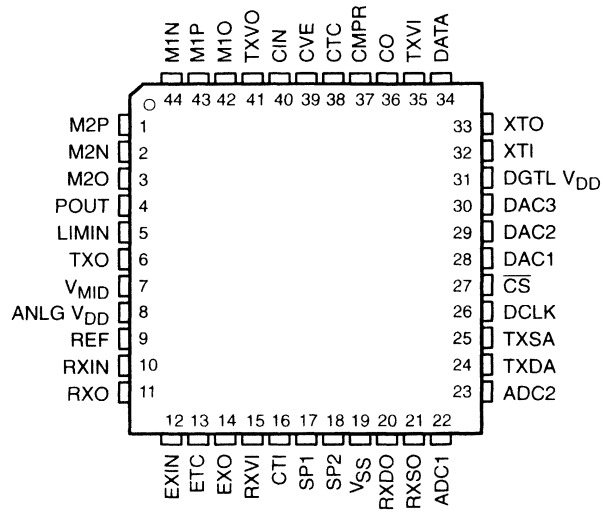
- **TACS and AMPS Operation**
- **Integrated RX and TX Voice Filters**
- **Integrated RX and TX Data Filters**
- **RX and TX Narrow-Band SAT Filters**
- **RX Data Recovery Comparator**
- **Preemphasis and Deemphasis Filtering**
- **Adjustable TX Limiter**
- **Microphone Preamplifiers**
- **Digitally Controlled Gains and Signal Selection or Muting**
- **Three 8-Bit DACs With Output Buffers**
- **8-Bit ADC With Input Multiplexer**
- **DTMF Generator**
- **On-Chip Compandor**
- **Flexible Clock or Oscillator Operation**
- **Simple 3-Wire Digital Interface**
- **Low-Power, 2-mA Standby Current**
- **44-Pin Mini QFP (FR) Package**

FR PACKAGE
(TOP VIEW)



description

The TCM8010-50 is a complete advanced mobile phone service (AMPS)/total access communications system (TACS) audio processor built using the Texas Instruments Advanced LinBiCMOS™ technology and packaged in a 44-pin mini QFP (FR) package. This device provides a highly integrated solution for analog-signal processing in mobile and hand-held FM cellular telephones while conserving circuit board area and vertical height within the finished product. All necessary voice and data filters, and all appropriate antialiasing and smoothing filters are incorporated in the device. Continuous-time filters are used for the anti-aliasing and smoothing functions and switched-capacitor techniques are used only where appropriate. Ancillary functions such as microphone preamplifiers, differential loudspeaker outputs, CCITT-compatible compander, dual tone multi-frequency (DTMF) generator, three 8-bit digital-to-analog converters (DACs), and an 8-bit analog-to-digital converter (ADC) with input multiplexer are also included in the device. A simple 3-wire serial interface provides digital control of signal-path switching, muting and gain adjustment, the 8-bit DACs, transmit (TX) limit level, DTMF code and amplitude, ADC multiplexer input select, and allows the ADC output to be read.

In active mode, the TCM8010-50 consumes less than 12 mA of supply current. When the DTMF generator or the ADC are not in operation, the power consumption is even less. The device can be put into a standby mode in which only the receive (RX) data path is active, reducing the supply current to a typical value of 2 mA or less.

Either the integrated-clock oscillator or an external clock signal (with several frequency options) can be used.

Advanced LinBiCMOS is a trademark of Texas Instruments Incorporated.

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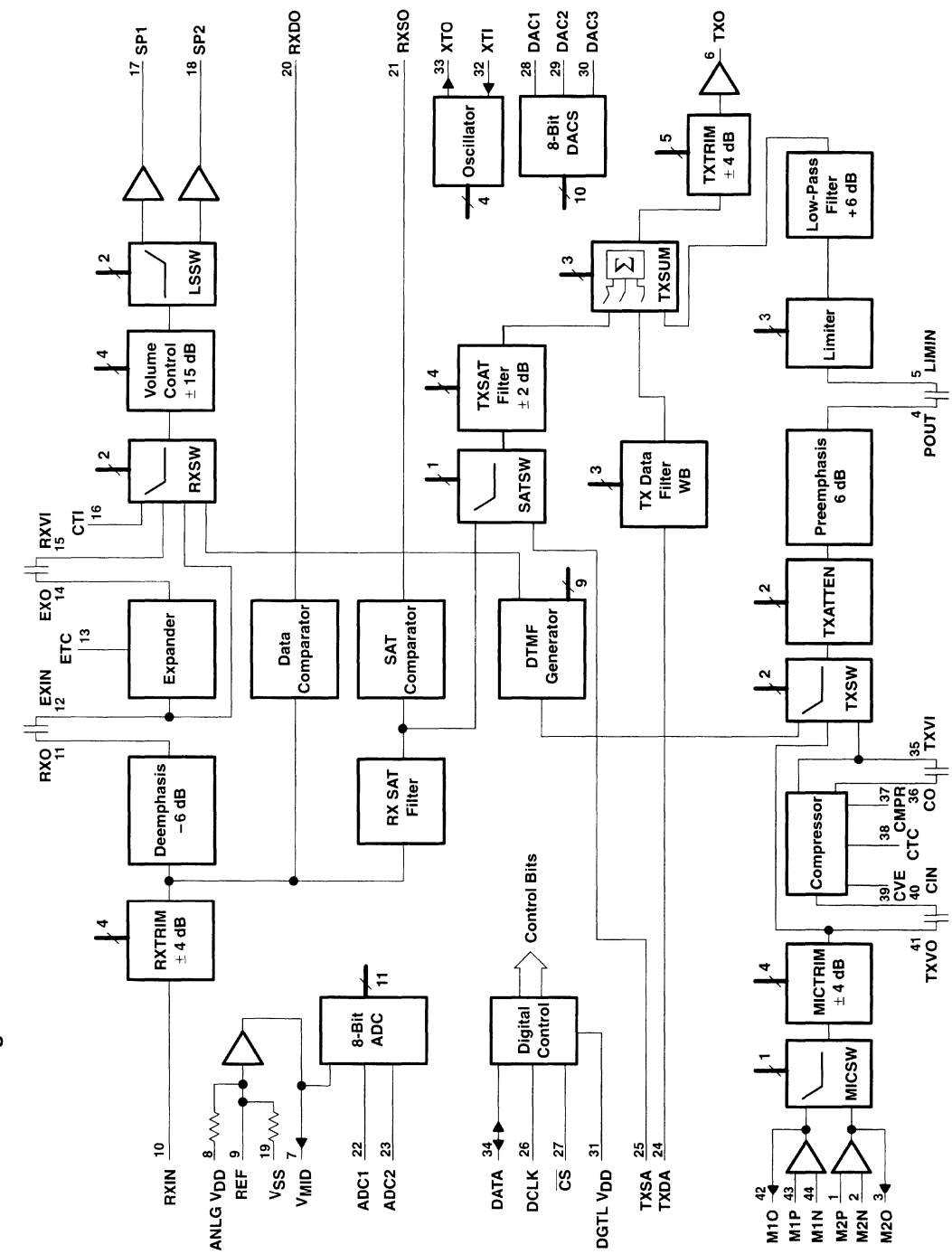
functional block diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655303• DALLAS, TEXAS 75265

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ADC1–ADC2	22, 23	I	ADC input 1 and 2 (analog)
ANLG V_{DD}	8		Analog positive supply
CIN	40	I	Compressor input (analog)
CMPR	37	I	Compressor rectifier input (analog)
CO	36	O	Compressor output, ac coupled to CMPR and to TXVI (analog)
$\overline{CS}$	27	I	Serial interface chip select, active low (digital)
CTC	38	O	Compressor time constant (analog)
CTI	16	I	Call tone input (analog and digital)
CVE	39	I	Compressor virtual ground (analog)
DAC1–DAC3	28, 29, 30	O	DAC outputs (analog)
DATA	34	I/O	Serial interface data signal (digital)
DCLK	26	I	Serial interface clock signal (digital)
DGTL V_{DD}	31		Digital positive supply
ETC	13	O	Expander time constant (analog)
EXIN	12	I	Expander input (analog)
EXO	14	O	Expander output, ac coupled to RXVI (analog)
LIMIN	5	I	Limiter input (analog)
M1O	42	O	Microphone preamplifer 1 output (analog)
M1P/N	43, 44	I	Microphone preamplifier 1 differential inputs (analog)
M2O	3	O	Microphone preamplifer 2 output (analog)
M2P/N	1, 2	I	Microphone preamplifier 2 differential inputs (analog)
POUT	4	O	Preemphasis output, ac coupled to LIMIN (analog)
REF	9		Midrail reference – decouple to V_{SS} with external capacitor
RXDO	20	O	Receive section data output (digital)
RXIN	10	I	Receive section input (analog)
RXO	11	O	Receive section deemphasis voice filter output (analog)
RXSO	21	O	Receive section supervisory audio tone (SAT) output (digital or analog)
RXVI	15	I	Voice input to volume control stage (analog)
SP1/2	17, 18	O	Speaker outputs 1 and 2 (analog)
TXDA	24	I	Transmit data filter input (digital or analog)
TXO	6	O	Transmit section output (analog)
TXSA	25	I	Transmit SAT input (digital or analog)
TXVI	35	I	Input to TX voice-path output stages (analog)
TXVO	41	O	Transmit voice input stage output, ac coupled to CIN (analog)
V_{MID}	7		Buffered midrail voltage – decouple to V_{SS} with external capacitor
V_{SS}	19		Negative supply (0 V)
XTI/XTO	32, 33		Crystal oscillator and clock recovery inputs

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{DD} (see Note 1) ..... −0.3 V to 7 V
Input voltage, V_I (any pin) ..... V_{SS} − 0.3 V to V_{DD} + 0.3 V
Operating free-air temperature range, T_A ..... 0°C to 70°C
Continuous total power dissipation at (or below) T_A = 25°C ..... 893 mW
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to V_{SS}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, DGTL V_{DD} and ANLG V_{DD}	4.5	5	5.5	V
High-level input voltage, V_{IH}	0.8V_{DD}			V
Low-level input voltage, V_{IL}			0.8	V
Operating virtual junction temperature, T_J	−30		70	°C

electrical characteristics over recommended operating virtual junction temperature range, V_{DD} = 5 V, f_{xtal} = 2.56 MHz

PARAMETER			MIN	TYP	MAX	UNIT
$I_{DD(A)}$	Analog supply current	Standby mode, DACs off		1	1.7	mA
		Standby mode, DACs on		1.4	2	
		Operating mode		11	16	
		Including DTMF generator		12	17	
$I_{DD(D)}$	Digital supply current	Standby mode		160	1000	µA
		Operating mode		0.5	1.7	mA
		ADC operating		1		
REF	Midsupply reference voltage	Operating mode	2.4	2.5	2.6	V
V_{MID}	Buffered midsupply reference voltage	Operating mode	2.4	2.5	2.6	

analog inputs

PARAMETER		MIN	TYP	MAX	UNIT
I_I	Input current at M1P, M1N, M2P, M2N, ADC1, ADC2, CTI		1		µA
Z_i	Input impedance at RXIN, RXVI, LIMIN, TXSA, TXDA	100			kΩ
	Input impedance at EXIN, CIN, CMPR, TXVI	25			

digital interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level input current	V_I = 5 V			1	µA
I_{IL}	Low-level input current	V_I = 0 V			1	
f_{CLK}	Serial clock frequency, DCLK input				1	MHz
V_{OH}	High-level output voltage	I_{OH} = 500 µA	0.9V_{DD}			V
V_{OL}	Low-level output voltage	I_{OL} = 500 µA			0.1V_{DD}	

transmit path electrical characteristics

input stage gain M1O/M2O to TXVO, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Gain	MICTRIM = <1000> (see Note 2)	−0.5	0.5	dB
MICTRIM positive range	MICTRIM = <1111>	3.3	4.3	dB
MICTRIM negative range	MICTRIM = <0000>	−4.8	−3.8	dB
MICTRIM step size		0.38	0.68	dB
Preamp CMRR		48		dB
Distortion	V_I = 1 V, f = 1 kHz		0.5%	
MICSW isolation	V_I = 100 mV, f = 1 kHz	50		dB

NOTE 2: The control bits associated with a block or function are shown in < >.

compressor CIN to CO, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Unity gain level†		76	103	127	mV
Relative linearity error	$V_I = V_{ref}$ + 2 dB to V_{ref} − 18 dB		−0.01	±0.5	dB
	$V_I = V_{ref}$ − 18 dB to V_{ref} −48 dB		−0.16	±1	dB
R_{COMP} compressor resistance		37	47	67	kΩ

† This parameter becomes V_{ref} for the relative-linearity-error test conditions.

output stage TXVI to TXO, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
TXTRIM step size		0.16	0.36	dB
TXTRIM positive range	TXTRIM = <11111>	3.5	4.5	dB
TXTRIM negative range	TXTRIM = <00000>	−4.8	−3.8	dB
TXATTEN step size		7	9	dB
TXATTEN range		21	27	dB

output stage limiter TXVI to TXO, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Maximum output signal	TXVI = 316 mV, f = 300 Hz to 25 000 Hz, LIM = <110>		1900	mVp-p
Distortion	f = 1 kHz, level at TXO = 2/3 × level measured in previous test, LIM = <110>		3%	
Trim step size, analog test mode A, output at RXDO	TXVI = 316 mV	0.8	1.2	dB
Trim positive range, analog test mode A, output at RXDO	LIM = <111>	2.5	3.5	dB
Trim negative range, analog test mode A, output at RXDO	LIM = <000>	−4.5	−3.5	dB

output stage frequency response TXVI to TXO, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Frequency response	0-dB reference at f = 1 kHz, TXVI = 26 mV	f < 200 Hz		−20	dB
		f = 300 Hz	−13.46	−9.46	dB
		f = 500 Hz	−9.02	−5.02	dB
		f = 2000 Hz	3.02	7.02	dB
		f = 2500 Hz	4.96	8.96	dB
		f = 3000 Hz	4.96	10.54	dB
		f = 5900 Hz		−35	dB
		f = 6000 Hz		−35	dB

overall transmit path electrical characteristics M1O/M2O to TXO, TXATT = <00>, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Compressor bypass gain	MICT = <1000>, TXT = <10000>	10.8	12	13.0	dB
Output noise, compressor enabled, M1O/M2O = V_{MID} psophometric weighting	RXIN = 400 mV, f = 1 kHz		2.3		mVrms
Voice mute attenuation	M1O/M2O = 100 mV, f = 1 kHz	50	−80		dB

DATA output levels TXDA to TXO, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
Output level	AMPS	f_I = 10-kHz square wave, amplitude 0 V to 5 V	1070	1188	mVp-p
	TACS	f_I = 8-kHz square wave, amplitude 0 V to 5 V	1070	1188	mVp-p
Frequency response	AMPS	−3 dB relative to 1 kHz, Analog test mode B	17	22	kHz
	TACS		14.4	17.6	kHz
TX data mute attenuation			50		dB

SAT output levels TXSA to TXO, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Output level	ISAT = <0>, f_I = 6-kHz square wave, amplitude 0 V to 5 V		95	116	mV
SAT trim positive range			2	2.3	dB
SAT trim negative range			−2.7	−2.3	dB
SAT trim step size			0.2	0.4	dB
Frequency response	0-dB reference at f = 6 kHz, ISAT = <0>	f < 3 kHz		−35	dB
		f = 4.8 kHz		−25	dB
		f = 5.1 kHz		−20	dB
		f = 5.8 kHz	−5	0.5	dB
		f = 5.94 kHz	−0.5	0.5	dB
		f = 6.06 kHz	−0.5	0.5	dB
		f = 6.2 kHz	−5	0.5	dB
		f = 7.2 kHz		−20	dB
		f > 9 kHz		−35	dB
TX SAT mute attenuation			50		dB

SAT output level RXIN to TXO, RXT = <1000>, SAT = <1000>, TXT = <10000>, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output level	ISAT = <1>, Input to RXIN = 6-kHz sine wave, amplitude 600 mV		400		mV

receive path electrical characteristics

input stage RXIN to RXO, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain	RXTRIM = <1000>		−6.3	−5.2	dB
RXTRIM positive range	RXTRIM = <1111>		3.2	4.2	dB
RXTRIM negative range	RXTRIM = <0000>		−4.5	−3.8	dB
RXTRIM step size			0.39	0.69	dB
Frequency response	0-dB reference at f = 1 kHz, RXIN = 400 mV	f <100 Hz		−28	dB
		f = 240 Hz		12.9	dB
		f = 300 Hz	8	11	dB
		f = 400 Hz	7.5	8.5	dB
		f = 2400 Hz	−8.2	−7.1	dB
		f = 3000 Hz	−12	−9	dB
		f > 5900 Hz		−40	dB

expander EXIN to EXO, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Unity gain level = V_{ref}†		80	100	130	mV
Relative linearity error	EXIN = V_{ref} +9.5 dB to V_{ref} −2.8 dB		−0.3	±1	dB
	EXIN = V_{ref} −2.8 dB to V_{ref} −23.8 dB		−0.8	±2	dB
R_{EXP} expander resistance		37.5	47	71.6	kΩ

† This parameter becomes V_{ref} for the relative-linearity-error test conditions.

output stage

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
Volume control	Gain RXVI to SP1/SP2	VOL = <1000>	0.5	1.5	dB
	Positive range	VOL = <1111>	13	15	dB
	Negative range	VOL = <0000>	−16.5	−15.5	dB
	Step size		1.75	2.25	dB
CTI input	Gain to SP1/SP2	VOL = <1000>	0	2	dB
Expander bypass gain from RXIN to SP1/SP2		VOL = <1000>	−5.5	−4	dB
Output load at SP1/SP2			500		Ω
Output voltage at SP1/SP2		R_L = 500 Ω	2.5		Vp-p
Distortion at SP1/SP2, expander enabled		RXIN = 400 mV, f = 1 kHz, No load		2%	
Noise at SP1/SP2, expander bypassed		RXIN = V_{MID}, psophometric weighting		3	mV
Voice mute attenuation		RXIN = 400 mV, f = 1 kHz	50		dB

RX DATA comparator RXIN to RXDO, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Must-detect level	f = 4 kHz, 5 kHz, 8 kHz, and 10 kHz		210		mVp-p
Must-not-detect level				40	
Output duty cycle		RXIN = 900 mV peak to peak	47.5%	52.5%	

RX SAT frequency response RXIN to RXSO, SATDIG = <1>, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Frequency response	0-dB reference at f = 6 kHz	f < 3 kHz		−35	dB
		f = 4.8 kHz		−25	dB
		f = 5.1 kHz		−19	dB
		f = 5.8 kHz	−5	0.5	dB
		f = 5.94 kHz	−0.5	0.5	dB
		f = 6.06 kHz	−0.5	0.5	dB
		f = 6.2 kHz	−5	0.5	dB
		f = 7.2 kHz		−20	dB
		f > 9 kHz		−35	dB

RX SAT comparator RXIN to RXSO, SATDIG = <0>, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Must-detect level	f = 6 kHz	64	30		mVrms

miscellaneous block electrical characteristics

digital-to-analog converters DAC1, DAC2, and DAC3

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage at code 255	DACX2 = <1>	V_{DD}−130			mV
Output voltage at code 255	DACX2 = <0>	V_{DD}/2 −100		V_{DD}/2 + 100	mV
Zero code offset			13	55	mV
Differential nonlinearity (codes 5 – 250)			0.3	1	LSB
Integral nonlinearity (codes 5 – 250)			0.3	1	LSB

analog-to-digital converter, DCLK = 160 kHz, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Full scale for inputs ADC1, ADC2, and V_{MID}		2.3		2.6	V
Differential nonlinearity			0.5	1	LSB
Integral nonlinearity			0.5	1	LSB
Clock rate (DCLK)				200	kHz

DTMF generator transmit levels at TXO, TXTRIM = <10000>, V_{DD} = 5 V

PARAMETER	DTTR	TEST CONDITIONS	MIN	TYP	MAX	UNIT
697-Hz tone, low tone	<0100>	AMPS mode	108	153	164.9	mV
1477-Hz tone, high tone			300	340	348.6	mV
697-Hz tone, low tone		TACS mode	61	78	88	mV
1477-Hz tone, high tone			140	175	190	mV
DTMF trim steps	<0000> – <0001>			0.4		dB
	<0001> – <0010>			0.4		dB
	<0010> – <0011>			0.4		dB
	<0011> – <0100>			0.5		dB
	<0100> – <0101>			0.5		dB
	<0101> – <0110>			0.6		dB
	<0110> – <0111>			0.6		dB
	<0111> – <1000>			0.7		dB
	<1000> – <1001>			0.7		dB
	<1001> – <1010>			0.8		dB
	<1010> – <1011>			0.9		dB
	<1011> – <1100>			1.0		dB
	<1100> – <1101>			1.1		dB
	<1101> – <1110>			1.3		dB
	<1110> – <1111>			1.5		dB
Positive range	<0100> – <1111>		7.1	9.8	12.1	dB
Negative range	<0100> – <0000>		−2.7	−1.9	−1	dB
Skew, change in level of high tone	<0100>		1.3	1.85	2.2	dB
Distortion products	<0100>	Relative to low tone		−30		dB

DTMF generator receive levels at SP1 and SP2, DTTR = <0100>, VOL = <1000>, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
All tones	AMPS mode	58	67	mV
	TACS mode	29	35	mV
Distortion products	Relative to low tone		−40	dB

TYPICAL CHARACTERISTICS

TX VOICE FREQUENCY RESPONSE

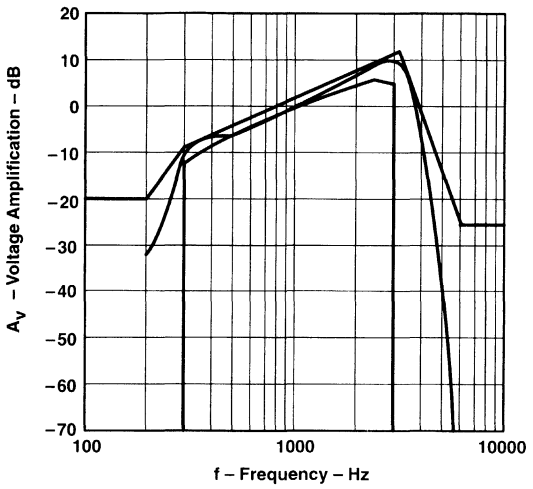


Figure 1

TX PASS-BAND DETAIL

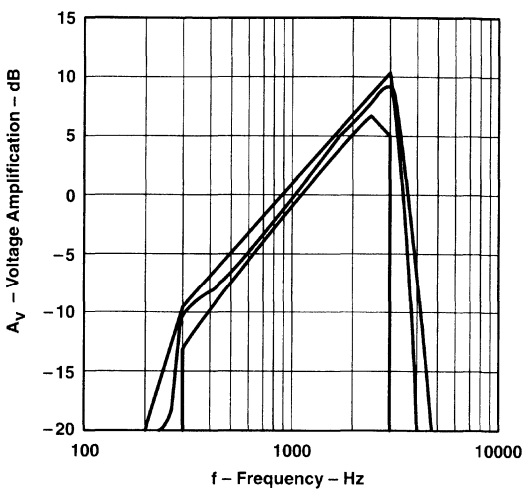


Figure 2

RX VOICE FREQUENCY RESPONSE

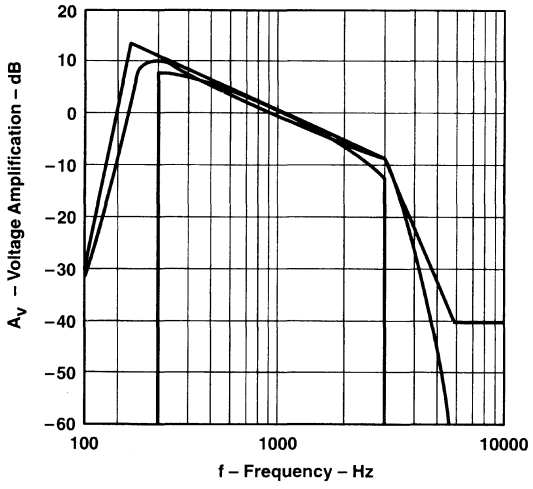


Figure 3

RX PASS-BAND DETAIL

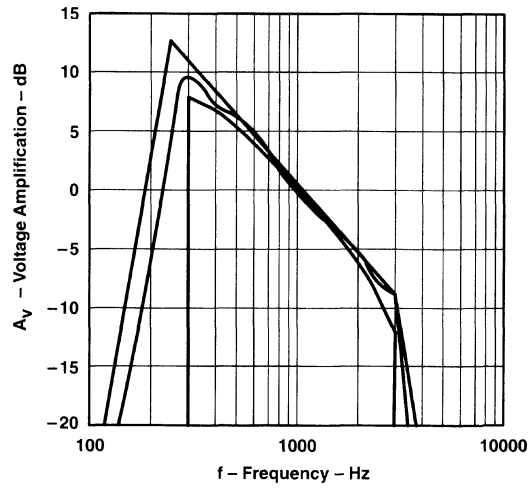


Figure 4

TYPICAL CHARACTERISTICS

TX SAT FREQUENCY RESPONSE

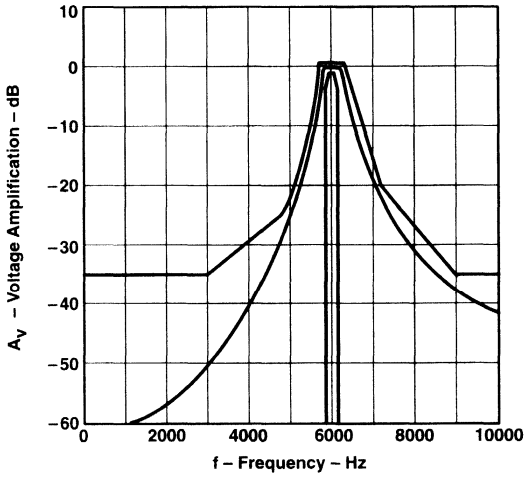


Figure 5

TX PASS-BAND DETAIL

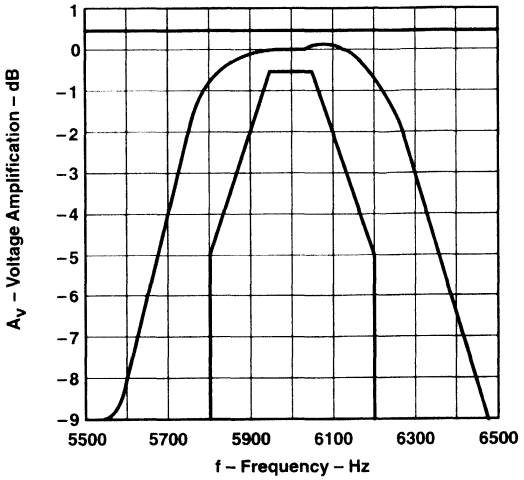


Figure 6

RX SAT FREQUENCY RESPONSE

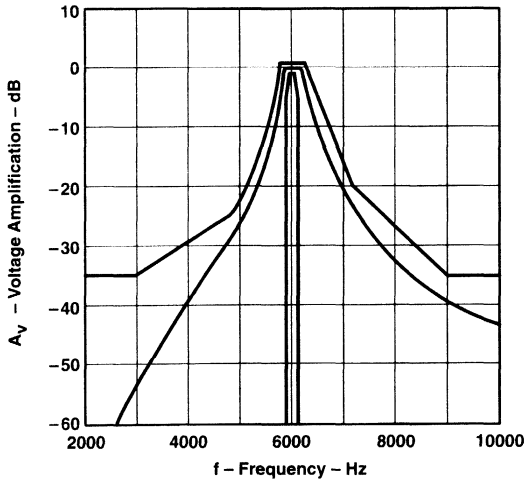


Figure 7

RX PASS-BAND DETAIL

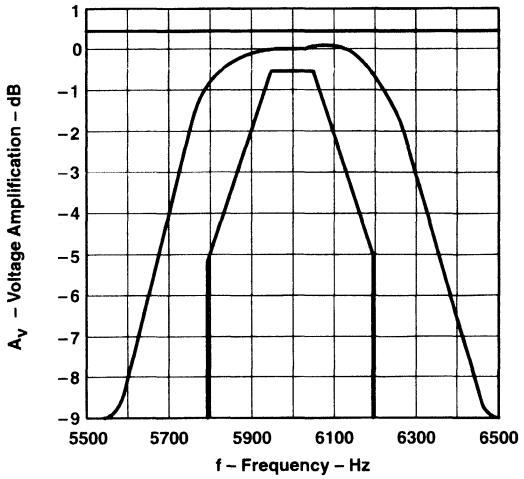


Figure 8

TYPICAL CHARACTERISTICS

TX DATA FREQUENCY RESPONSE – AMPS

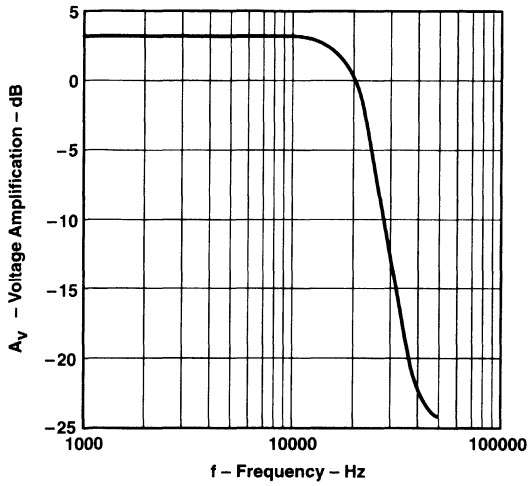


Figure 9

TX DATA FREQUENCY RESPONSE – TACS

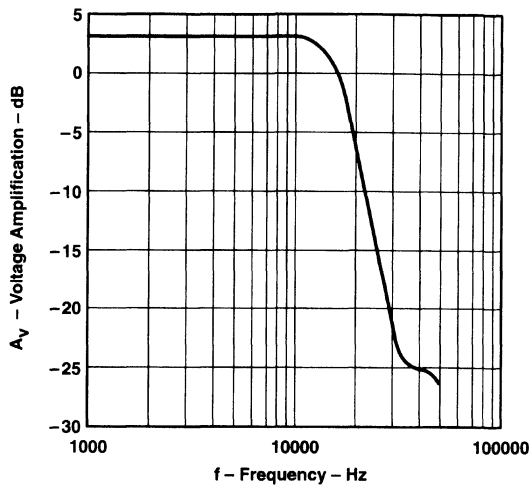


Figure 10

COMPRESSOR LINEARITY

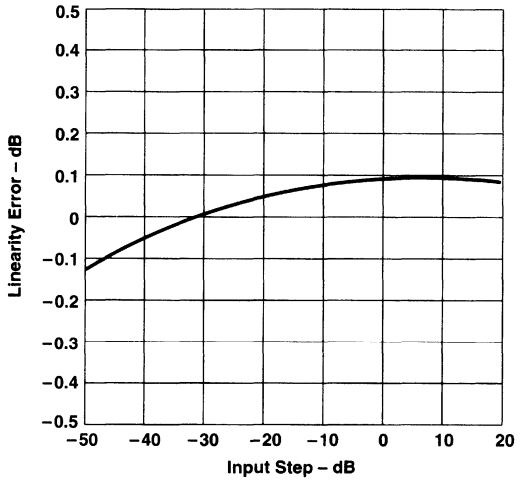


Figure 11

EXPANDER LINEARITY

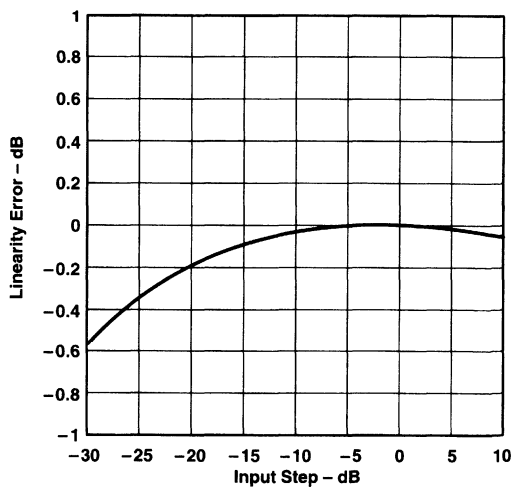


Figure 12

APPLICATION INFORMATION

analog cellular telephone baseband solution

The TCM8002 and TCM8010-50 chip set provides a complete solution to the audio and data filtering, decoding, and encoding required in a cellular telephone for the AMPS or TACS systems. The applications-circuit schematic is shown in Figure 13 and demonstrates that a minimum of external components is required.

The following extra functions are included in the TCM8010-50 and TCM8002:

- Three digital-to-analog converters
- Analog-to-digital converter
- Two timers
- I/O expansion

overall description

The following paragraphs detail the various function of the TCM8010-50 and TCM8002 chip set when used in this application.

TCM8010-50 transmit path

The inputs to the microphone amplifiers are MIC1 and MIC2. MIC1 could be used for the internal microphone and MIC2 for accessories (a hands-free unit). The TCM8010-50 is designed for single-supply operation. REF is provided to bias the noninverting inputs of the microphone amplifiers, M1P and M2P. The wideband data to be transmitted is input as a digital signal to TXDA. The TCM8010-50 then filters and provides a level trim for the signal.

The TCM8002 produces a digitally-filtered signal, phase locked to the received SAT. This is then connected to the input TXSA of the TCM8010-50, which filters and provides level adjustment for the digital signal. The output from the TCM8010-50 is at TXO and should be connected to the modulator in the RF section. The voice, wideband data, and SAT signal levels are programmable, eliminating the need for external adjustments.

TCM8010-50 receive path

The output from the FM demodulator/discriminator should be connected to the receive audio input (RXIN) of the TCM8010-50. Two audio outputs are provided at SP1 and SP2. These can be configured to be two separate outputs, with one driving the phone earpiece and the other for test or accessories (a hands-free unit) for example, or optionally can be configured to provide a differential output to increase the maximum level.

The TCM8010-50 filters and converts the received wideband data to a digital signal and outputs this at RXDO for connection to the TCM8002. The received SAT signal is filtered and converted to a digital signal. It is then made available at RXSO for transmission to the TCM8002.

TCM8010-50 digital-to-analog converters

Three uncommitted 8-bit DACs are included in the TCM8010-50 (DAC1OUT, DAC2OUT, and DAC3OUT). One can be used for power control of the RF transmit amplifier. The other two could be used to provide adjustment voltages for the RF stage such as calibrating the temperature-compensated crystal oscillator (TCXO) and trimming the first intermediate frequency (IF) stage.

TCM8010-50 analog-to-digital converter

Two multiplexed inputs to an ADC included in the TCM8010-50 are provided (ADCIN 1 and ADCIN 2). Possible uses are to measure battery voltage (using a potential divider) or received-signal-strength indicator (RSSI) voltage.

APPLICATION INFORMATION

TCM8002 transmit path

The data encoder includes all the necessary formatting for transmission on the control and voice channels. This digital signal is output at TXOUT. The received SAT digital signal is connected to TCM8002 SATIN and then the signal is recovered from the noise before being measured and regenerated. The digital output signal appears at TCM8002 SATOUT.

TCM8002 receive path

The received digital data signal is connected to RXIN for the control-and-voice channel data-recovery circuit. The data is then majority voted and error corrected. Finally, an interrupt is generated to signal to the microcontroller that there is received data available.

TCM8002 timers

A watchdog timer is provided that can reset the microcontroller in the telephone if a fault occurs. This is a requirement of both the AMPS and TACS systems.

An uncommitted programmable 8-bit timer is also available with an output labelled TMZERO that pulses low when the count reaches zero.

TCM8002 I/O expansion

Twenty programmable I/O lines are provided for the telephone microcontroller. These are individually bit-programmable as outputs or inputs with optional current source pullups.

An intelligent interface to the audio processor (TCM8010-50) provides an automatic audio-mute function when wideband data is being transmitted or received.

TCM8002 and TCM8010-50 clock and control

Both the TCM8002 and TCM8010-50 are connected to the microcontroller through the serial interface ($\overline{CS}$, DCLK, DATAIN, DATAOUT, INTERRUPT). The TCM8002 can be programmed to generate interrupts when events such as RX data available (data received) or the counter/timer reaching zero state occurs.

A low-power crystal oscillator is integrated into the TCM8002, and the CLKOUT output is provided for connection to the TCM8010-50.

APPLICATION INFORMATION

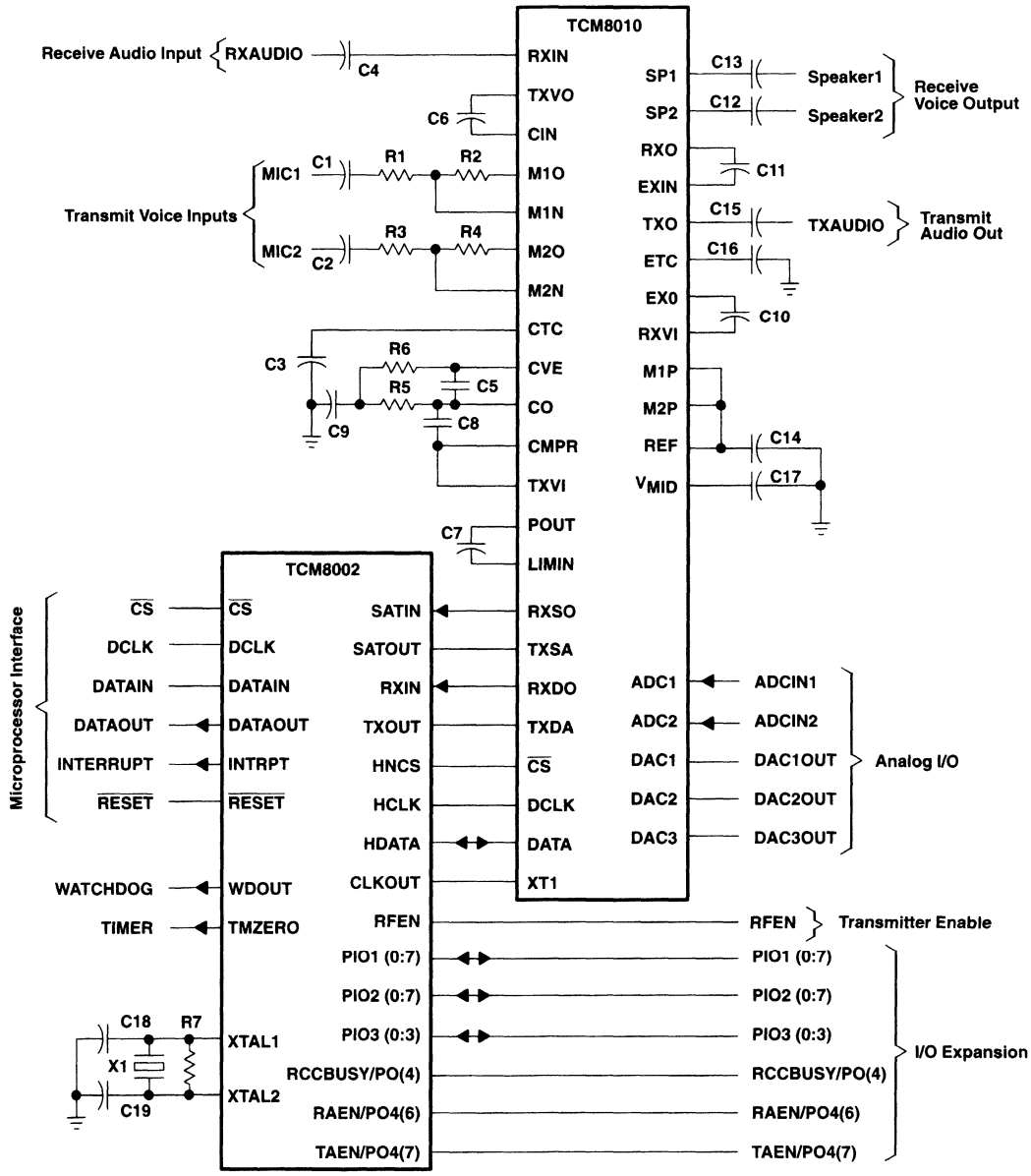


Figure 13. Complete Baseband Solution

APPLICATION INFORMATION

external component selection

COMPONENT DESIGNATION	TYPICAL VALUE	FUNCTION
R1	47 kΩ	Microphone preamplifier number 1 gain = R2/R1
R2	47 kΩ	Recommended minimum value
R3	47 kΩ	Microphone preamplifier number 2 gain = R4/R3
R4	47 kΩ	Recommended minimum value
R5	100 kΩ	Provides dc bias for the compressor
R6	100 kΩ	
R7	1 MΩ	Biasing resistor for crystal oscillator
C1	100 nF	AC couples the input to microphone preamplifier number 1 (MIC 1)
C2	100 nF	AC couples the input to microphone preamplifier number 2 (MIC 2)
C3	390 nF	Determines the attack and recovery times of the compressor
C4	10 nF	AC couples the receive audio and data input from the FM demodulator/discriminator
C5	47 pF	Required for HF stability of the compressor
C6	100 nF	AC couples the output of the selected microphone preamplifier to the compressor input. This is required because any dc offset would cause linearity errors.
C7	100 nF	AC couples the output of the preemphasis and bandpass filter to the limiter stage to ensure symmetrical clipping
C8	100 nF	AC couples the output of the compressor to the transmit switch (TXSW). Since this is also the compressor rectifier input, any dc offset would cause linearity errors.
C9	100 nF	AC decouples the compressor dc feedback
C10	100 nF	AC couples the output from the expander to the receive switch (RXSW)
C11	100 nF	AC couples the input to the expander to remove offsets that would otherwise cause linearity errors at low signal levels
C12	—	Required when the earpiece drive is single ended (not differential)
C13	—	
C14	470 nF	Decouples the resistor divider that produces REF, the input for the V_{MID} generator
C15	100 nF	AC couples the output from the transmit voice, data, and SAT signals to the FM modulator in the RF section
C16	330 nF	Determines the attack and recovery times of the expander
C17	470 nF	Provides a low ac impedance reference for the transmit and receive paths
C18	33 pF	Provides X1 with the required capacitive loading
C19	33 pF	Provides X1 with the required capacitive loading
X1	2.56 MHz	Crystal

printed circuit board layout precautions

Resistors R5 and R6 should be placed close to the TCM8010-50 to minimize stray capacitance between CO and CVE. Otherwise, compressor gain errors are caused at low signal levels and high frequencies.

suggested trim sequence

The TCM8010-50 and TCM8002 are designed so that no manual trims are required. All levels can be adjusted to meet the system requirements and compensate for production tolerances by writing to the digital interface. The data required can then be stored in a nonvolatile memory by the microcontroller in the telephone. When the telephone is turned on, an initialization routine can write this calibration data to the TCM8010-50.

APPLICATION INFORMATION

suggested trim sequence (continued)

The suggested sequence of adjustments for trimming is detailed below.

transmit

Step 1. TXTRIM

d. Set the TX data trim <DAT_2 – DAT_0> to nominal = <100>.

e. Set the TCM8002 and TCM8010-50 to transmit signaling tone.

f. Adjust <TXT_4 – TXT_0> to set the frequency deviation to that required by the system, AMPS or TACS.

Step 2. TXSAT

a. Turn the signaling tone off and turn on the SAT path. Input a 6-kHz signal to RXIN.

b. Adjust <SAT_3 – SAT_0> to give the required frequency deviation.

Step 3. MICTRIM

a. Mute the signaling tone and SAT.

b. Inject an audio signal at the desired level into the microphone preamplifier.

c. Adjust <$MICT_3$ – $MICT_0$> to set the frequency deviation.

Step 4. LIMITER TRIM

a. Increase the audio signal level by 20 dB typically.

b. Adjust <LIM_2 – LIM_0> to produce the required maximum deviation.

Step 5. DTMF TRIM

a. Mute the signaling tone, audio, and SAT.

b. For TACS, set bit <DTSK> to enable the skew of the levels between the low and high tones.

c. Turn on the DTMF generator and adjust <$DTTR_3$ – $DTTR_0$> to give the desired frequency deviation.

receive

Step 6. RXTRIM

Input a modulated signal to the telephone and adjust <RXT_3 – RXT_0> to produce the required level at SP1 and SP2.

RF stage

Step 7. DACs to trim RF section

Three 8-bit DACs can be used to trim sections of the RF stage using <$DACCAD_1$ – $DACAD_0$> to select the DAC and <DAC_7 – DAC_0> to set the level. <DACX2> sets the range of all three DACs and <DACON> enables all three outputs when the TCM8010-50 is in standby.

Typical uses would be RF transmit power control, TCXO trim, and first IF section trim.

The TCM8010-50 is designed for signal levels detailed in the following tables for AMPS and TACS systems. These tables suggest levels for both the transmitted and received audio, SAT, and DATA signals.

APPLICATION INFORMATION

transmit signal levels

AMPS mode

SIGNAL	PEAK FREQUENCY DEVIATION (kHz)	LEVEL AT TXO	UNIT
Design level	8	400	mVrms
Peak voice level	12	1697.1	mV peak to peak
SAT	2	100	mVrms
DATA	8	1131.4	mV peak to peak
DTMF low tone, 697 Hz	3.1365	156.8	mVrms
DTMF high tone, 1477 Hz	6.6465	332.3	mVrms

TACS mode

SIGNAL	PEAK FREQUENCY DEVIATION (kHz)	LEVEL AT TXO	UNIT
Design level	5.7	356.3	mVrms
Peak voice level	9.5	1697.6	mV peak to peak
SAT	1.7	106.3	mVrms
DATA	6.4	1131.5	mV peak to peak
DTMF low tone, 697 Hz	1.2 max	75	mVrms
DTMF high tone, 1477 Hz	3.19 max	199.4	mVrms

receive signal levels

AMPS mode

SIGNAL	PEAK FREQUENCY DEVIATION (kHz)	LEVEL AT RXIN	UNIT
Design level	8	400	mVrms
Peak voice level	12	1697.1	mV peak to peak
SAT	2	100	mVrms
DATA	8	1131.4	mV peak to peak

TACS mode

SIGNAL	PEAK FREQUENCY DEVIATION (kHz)	LEVEL AT RXIN	UNIT
Design level	5.7	356.3	mVrms
Peak voice level	9.5	1697.6	mV peak to peak
SAT	1.7	106.3	mVrms
DATA	6.4	1131.5	mV peak to peak

PRINCIPLES OF OPERATION

general

The TCM8010-50 consists of a number of functional blocks and is controlled by the digital interface. The control bits associated with each block are shown in the angled brackets symbol < >. In standby mode <STBY>, the receive data path from RXIN to RXDO is on and the DACs can be on or off as required. All other parts of the device, including the crystal oscillator, are off. When in the active mode, the receive and transmit paths and the DAC blocks are continuously on, and the DTMF and ADC blocks are turned on as required.

Control bits <MD_1 – MD_0> set the TCM8010-50 for the desired system (AMPS or TACS).

transmit path

The transmit path on the TCM8010-50 consists of a number of functional blocks, which are described in the following paragraphs.

mic inputs

Voice signals are input via a pair of microphone preamplifiers, which are stable for gains between 0 dB and 20 dB. All voice-path specifications are given with the preamplifiers configured as unity-gain inverting amplifiers. In standby mode, the bias to the microphone preamplifiers is turned off and the outputs M1O and M2O are in the high-impedance state.

MICSW

The MICSW block is a 2-input switch that selects either of the preamplifier outputs, and is under control of the digital interface (<MICSEL>).

MICTRIM

The MICTRIM block provides gain adjustment to compensate for differing microphone sensitivities (<$MICT_3$ – $MICT_0$>). A second-order Sallen-Key low-pass filter is incorporated in this block to provide antialiasing for the TX voice signal.

compressor

The compressor provides a 1-dB change in output signal level for a 2-dB change in input level over an operating input range of 50 dB. The unity-gain point, $V_{ref,}$ is proportional to the value of V_{DD} (see the compressor table in the transmit path electrical charactistics). Attack time is measured by increasing the input-signal amplitude by a 12-dB step relative to 13 mV rms and is defined as the time required for the output envelope to reach 1.5 times the final steady-state level. Recovery time is measured by reducing the input signal amplitude by a 12-dB step to 13 mV rms and is defined as the time required for the output envelope to settle to 0.75 times the final steady-state level.

The attack and recovery times are determined by an internal resistor (R_{COMP}) and the external capacitor, C_{CTC}, connected between CTC and 0 V, V_{SS}.

Attack time = $0.151 \times C_{CTC} \times R_{COMP}$

Recovery time = $0.693 \times C_{CTC} \times R_{COMP}$

TXSW

This block is a 3-input switch that selects either the compressor output, compressor bypass (for testing), or the output of the DTMF generator. TXSW is controlled by <$TXSW_1$ – $TXSW_0$>.

PRINCIPLES OF OPERATION

TXATTEN

The output of TXSW passes through the TXATTEN block, which provides four levels of attenuation.

preemphasis

The output from TXATTEN is connected to the preemphasis block, which provides the necessary 6 dB per octave increase in gain with frequency by using a second-order filter. Also included in this block is an eighth-order band-pass filter function with a 300-Hz to 3-kHz passband. The nominal gain of this stage is 6 dB at 1 kHz and its output is routed to the POUT terminal.

limiter

The limiter block limits the maximum output under overload signal conditions, and the limit level is adjustable under control of the serial interface <LIM_2 – LIM_0>. The limiter range is designed to allow the TX path distortion and maximum signal output specifications to be achieved at a single limiter-adjustment code. The output of the preemphasis block is ac coupled (via an external capacitor) into the LIMIN terminal to ensure symmetrical limiting.

low-pass filter

The limiter output is processed by the low-pass filter block, which is a fourth-order low-pass filter plus second-order equalizer, to remove excessive harmonics produced by the limiting process.

TXSUM

This block can sum together or mute any of its three inputs (SAT, data, and voice) under the control of the <TXSAT, TXDAT, TXVOX> bits, respectively.

TXTRIM

The TXTRIM gain-adjust block can be used to compensate for different modulator sensitivities using bits <TXT_4 – TXT_0>. A continuous-time output low-pass smoothing filter is included with a typical cutoff frequency of 30 kHz.

TX data filter

Transmit data is input to terminal TXDA and is routed to the TX data filter block where the data is first conditioned by a second-order antialiasing filter before going on to the transmit data filter.

In the AMPS and TACS modes, the transmit data is a Manchester-encoded digital signal at 10k bit/s for AMPS or 8k bits/s for TACS. The transmit data filter for these two modes is a fourth-order Butterworth low-pass filter, with its – 3-dB point switchable between AMPS and TACS modes.

The filtered AMPS or TACS wideband-data signal is summed into the transmit signal path in the TXSUM block.

TXSAT filter path – TXSA to TXO

The input to the transmit SAT signal path is determined by the SATSW block, which selects between the TXSA terminal and the output of the receive SAT filter (RXSAT). The signal is processed by the TXSAT filter block, which includes an antialiasing filter, a fourth-order narrow-band band-pass filter centered at 6 kHz, and a gain adjust stage <SAT_3 – SAT_0>. The output of this block is then applied to an input of TXSUM to be summed into the voice path when selected.

PRINCIPLES OF OPERATION

receive path – voice

The demodulated signal from the receiver is input to the TCM8010-50 at the RXIN terminal. A pair of loudspeaker drivers are provided, producing output signals on terminals SP1 and SP2, and are capable of driving 500-Ω loads.

RXTRIM

A gain-adjust block, RXTRIM, is provided to allow variations in the receiver FM demodulator/discriminator characteristics to be accommodated <RXT_3 – RXT_0>. This block is enabled in both active and standby modes. A second-order continuous-time filter with a typical cutoff frequency of 30 kHz provides an antialiasing function for the receive signal path.

deemphasis

The deemphasis filter block exhibits a 6-dB/octave decrease in gain versus frequency characteristic. It also includes an eighth-order band-pass filter (pass band = 300 Hz to 3 kHz) to separate the received voice signal from the data and SAT signals. A continuous-time smoothing filter is incorporated at the output, and the output signal appears at terminal RXO.

expander

The expander block provides a 2-dB change in output signal level for a 1-dB change in input level over an operating input range of 33 dB. The unity-gain level, V_{ref}, is proportional to V_{DD} (see the expander table in the receiver path electrical charactistics). Attack time is measured by increasing the input signal amplitude by a 6-dB step relative to 72.5 mV and is defined as the time required for the output envelope to reach 0.57 times the final steady-state level. Recovery time is measured by reducing the input signal amplitude by a 6-dB step to 72.5 mV and is defined as the time required for the output envelope to settle to 1.5 times the final steady-state level.

The attack and recovery times are determined by an internal resistor, R_{EXP}, and the external capacitor, C_{EXP}, connected to ETC and 0 V, V_{SS}.

Attack time = $0.173 \times C_{ETC} \times R_{EXP}$

Recovery time = $0.693 \times C_{ETC} \times R_{EXP}$

RXSW

RXSW is a 4-input switch block that provides a selection between the call-tone input terminal (CTI), the expander output (externally capacitively coupled to terminal RXVI), the expander-bypass path (for testing), and the output from the DTMF generator as the input to the volume-control block. The control bits are <$RXSW_1$ and $RXSW_0$>.

To simplify the connection of a digital signal for a *User Alert* tone (typically between 200 Hz and 400 Hz), no internal bias is provided for the CTI input. If an ac-coupled signal is applied to CTI, an external bias resistor (typical value is 100 kΩ) is required and should be connected between CTI and V_{MID}.

volume control

This block provides output level adjustment to implement a user-adjustable level control via control bits <VOL_3 – VOL_0>.

LSSW

The loudspeaker control switch block (LSSW) allows selection between either SP1 or SP2 outputs, muting, or differential drive of both terminals via control bits <LS_1 – LS_0>.

PRINCIPLES OF OPERATION

receive path – data/SAT

The demodulated signal from the receiver is input to the TCM8010-50 at the RXIN terminal. This signal, containing voice, data, and SAT components, is processed and antialias filtered by the RXTRIM block.

receive data path – data comparator

The signal from RXTRIM is applied to the data comparator block, which has defined threshold levels. The data signal is Manchester encoded at 10 kbit/s for AMPS mode and at 8 kbit/s for TACS mode. Detected data appears at RXDO. This signal path is enabled in the standby mode.

receive SAT path – RX SAT filter

The RX SAT filter block uses a fourth-order Butterworth bandpass filter centered at 6 kHz to separate received SAT signals from the voice signal. The output of the bandpass filter is routed to an input of the SATSW block and to the SAT comparator block.

receive SAT path – SATSW

SATSW is a 2-input switch block that selects between the output of the RX SAT filter and an external SAT source (applied to terminal TXSA) via control bit <ISAT>.

receive SAT path – SAT comparator

The SAT comparator block recovers the SAT signal and has defined hysteresis levels for improved noise immunity. The output is routed to terminal RXSO. An internal switch, controlled by bit <SATDIG>, bypasses the SAT comparator, applying the output from the RX SAT filter block directly to terminal RXSO.

digital interface

The TCM8010-50 is controlled by a 3-wire digital interface, consisting of a clock signal (DCLK), a chip select ($\overline{CS}$), and a bidirectional data line (DATA). The logic signal present on DATA is written into the device on the rising edge of DCLK when $\overline{CS}$ is low. Serial messages to and from the device contain a read/write bit, an address field, and a data word. Results from the ADC are read back using the serial interface, and the DCLK signal is used to drive the converter. Test access to analog and digital sections of the device are provided using the serial interface.

write operations

A timing diagram for a write operation to the device is shown in Figure 14. In this case, the read/write bit is set to 1, followed by a 3-bit address word, (A2–A0), and a 10-bit data word (D9–D0). Data shifts into the device on the rising edge of DCLK and is transferred to internal registers on the falling edge of the fourteenth clock pulse after $\overline{CS}$ goes low. If $\overline{CS}$ returns high before this time, no transfer takes place and the input interface is reset.

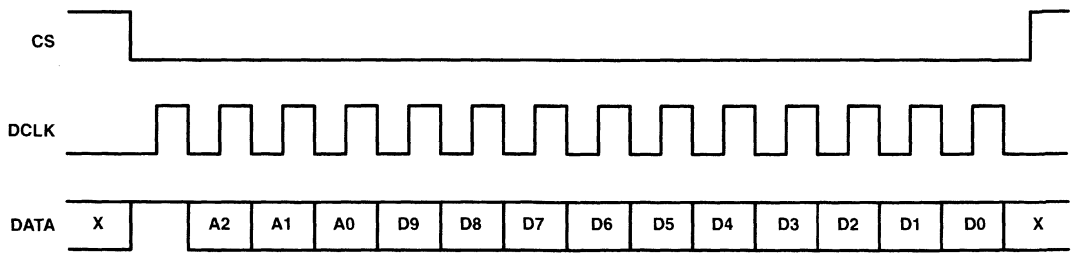


Figure 14. Write-Operation Timing

PRINCIPLES OF OPERATION

control words

Table 1 shows control-word and configuration assignments for the device. Table 2 shows control-word descriptions, Table 3 shows test modes, and Table 4 details DTMF control words.

Table 1. Control-Word and Configuration Assignments

	A_2	A_1	A_0	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Word 0	0	0	0	STBY	MD_1	MD_0	ISAT	SATDIG	DACX2	CKSEL	$CKRT_2$	$CKRT_1$	$CKRT_0$
Word 1	0	0	1	$TXSW_1$	$TXSW_0$	TXSAT	TXDAT	TXVOX	$TXATT_1$	$TXATT_0$	DACON	LS_1	LS_0
Word 2	0	1	0	MICSEL	$MICT_3$	$MICT_2$	$MICT_1$	$MICT_0$	TXT_4	TXT_3	TXT_2	TXT_1	TXT_0
Word 3	0	1	1	LIM_2	LIM_1	LIM_0	SAT_3	SAT_2	SAT_1	SAT_0	1	0	0
Word 4	1	0	0	RXT_3	RXT_2	RXT_1	RXT_0	$RXSW_1$	$RXSW_0$	VOL_3	VOL_2	VOL_1	VOL_0
Word 5	1	0	1	DTSK	$DTTR_3$	$DTTR_2$	$DTTR_1$	$DTTR_0$	0	0	0	$TEST_1$	$TEST_0$
Word 6	1	1	0	$DACAD_1$	$DACAD_0$	DAC_7	DAC_6	DAC_5	DAC_4	DAC_3	DAC_2	DAC_1	DAC_0
Word 7	1	1	1	—	—	—	—	—	—	$DTMF_3$	$DTMF_2$	$DTMF_1$	$DTMF_0$

Table 2. Control-Word Descriptions

	DESCRIPTION
Word 0	STBY = Standby select: 0 = Standby, 1 = Active MD_1 – MD_0 = Mode select: 00 = AMPS, 01 = Undefined, 10 = TACS, 11 = Undefined ISAT = SAT select: 0 = External, 1 = Internal SATDIG = Digital/Analog RX SAT: 0 = Digital, 1 = Analog DACX2 = DAC range select: 0 = 0 – $V_{DD}/2$, 1 = 0 – V_{DD} CKSEL = Clock source select: 0 = Oscillator, 1 = Sinusoidal input $CKRT_2$ – $CKRT_0$ = Clock rate select: 000 = 3.58 MHz, 001 = 7.16 MHz, 010 = 10.74 MHz, 011 = 14.32 MHz, 100 = 2.56 MHz, 101 = 10.24 MHz, 110 = 12.80 MHz, 111 = 15.36 MHz
Word 1	$TXSW_1$ – $TXSW_0$ = TX Voice select: 00 = Mute, 01 = Compressor O/P, 10 = Compressor bypass, 11 = DTMF TXSAT = TX SAT enable: 0 = Mute, 1 = Enable TXDAT = TX Wideband data enable: 0 = Mute, 1 = Enable TXVOX = TX Voice enable: 0 = Mute, 1 = Enable $TXATT_1$ – $TXATT_0$ = TX attenuation: 00 = 0 dB, 01 = 8 dB, 10 = dB, 11 = 24 dB DACON = DACS on select in standby: 0 = Off, 1 = On LS_1 – LS_0 = Loudspeaker configuration: 00 = Mute, 01 = SP2 enable, 10 = SP1 enable, 11 = Differential
Word 2	MICSEL = Microphone select: 0 = M1, 1 = M2 $MICT_3$ – $MICT_0$ = Microphone trim: 0000 = minimum gain, 1111 = maximum gain TXT_4 – TXT_0 = TX Deviation trim: 00000 = minimum gain, 11111 = maximum gain
Word 3	LIM_2 – LIM_0 = Deviation limiter adjust: 000 = minimum deviation, 111 = maximum deviation SAT_3 – SAT_0 = TXSAT adjust: 0000 = minimum, 1111 = maximum D_0 – D_1 = 0, D_2 = 1
Word 4	RXT_3 – RXT_0 = RX input adjust: 0000 = minimum, 1111 = maximum $RXSW_1$ – $RXSW_0$ = RX switch control: 00 = CT input, 01 = Expander O/P, 10 = Expander bypass, 11 = DTMF VOL_3 – VOL_0 = RX path audio volume control: 0000 = minimum, 1111 = maximum
Word 5	DTSK = DTMF Skew enable: 0 = disabled, 1 = enabled $DTTR_3$ – $DTTR_0$ = DTMF adjust: 0000 = minimum, 1111 = maximum $TEST_1$ – $TEST_0$ = Test mode: (see Table 3) D_2 – D_4 = 0
Word 6	$DACAD_1$ – $DACAD_0$ = DAC address: 00 = DAC 1, 01 = DAC 2, 10 = DAC 3, 11 = all DACs
Word 7	$DTMF_3$ – $DTMF_0$ = DTMF control: (see Table 4)

PRINCIPLES OF OPERATION

Table 3. Test Modes (to Word 5)

SATDIG	$TEST_1$	$TEST_0$	MODE	OUTPUT AT RXDO	OUTPUT AT RXSO
X	0	0	Normal		
0	0	1	Digital Test	Digital DTMF High Tone	Digital DTMF Low Tone
1	1	0	Analog Test A	Rx Data (analog)	Limiter Output (dc)
1	1	1	Analog Test B	Bandgap Output	Tx Data (analog)
0	1	0	Other States	Rx Data (digital)	Rx SAT (digital)
0	1	1	Other States	Digital DTMF High Tone	Digital DTMF Low Tone
1	0	1	Other States	Digital DTMF High Tone	RXSAT (analog)

Table 4. DTMF Control (to Word 7)

$DTMF_3$	$DTMF_2$	$DTMF_1$	$DTMF_0$	KEY	LOW TONE Hz	HIGH TONE Hz
0	0	0	0	1	697	1209
0	0	0	1	4	770	1209
0	0	1	0	7	852	1209
0	0	1	1	*	941	1209
0	1	0	0	2	697	1336
0	1	0	1	5	770	1336
0	1	1	0	8	852	1336
0	1	1	1	0	941	1336
1	0	0	0	3	697	1477
1	0	0	1	6	770	1477
1	0	1	0	9	852	1477
1	0	1	1	#	941	1477
1	1	0	0	—	697	Off
1	1	0	1	—	Off	1209
1	1	1	0	—	Off	1477
1	1	1	1	—	Off	Off

PRINCIPLES OF OPERATION

read operations

A timing diagram of a read operation, which outputs ADC results from the device, is shown in Figure 15. The first bit driven into the device is a logic 0, followed by a 3-bit address word. The device then assumes control of the DATA line on the falling edge of the fifth clock pulse after $\overline{CS}$ goes low. The conversion result is output MSB first, with the MSB being output on the falling edge of the seventh clock pulse after $\overline{CS}$ goes low. Control of the DATA line is released (returned to input mode), when $\overline{CS}$ goes high.

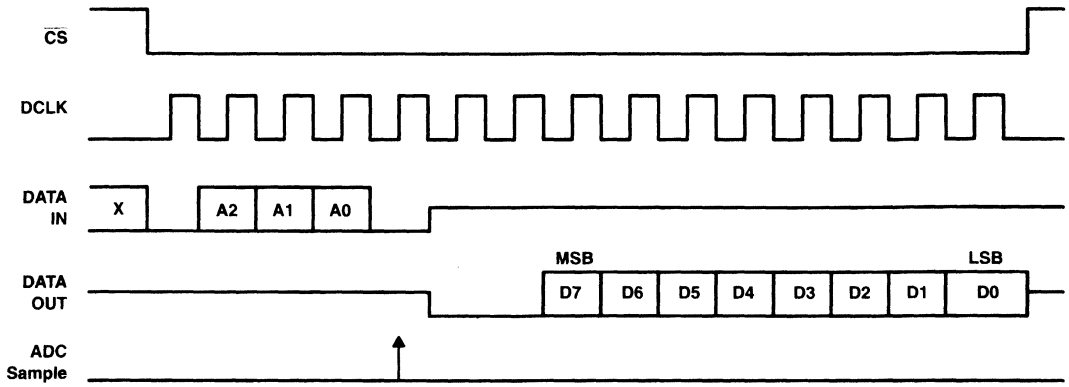


Figure 15. Read-Operation Timing

Table 5 details the decoding of the three address bits.

Table 5. Address Bit Decoding

A2	A1	A0	REFERENCE	MEASUREMENT
0	0	0	Band gap	V_{MID}
0	0	1	Band gap	ADC1
0	1	0	Band gap	ADC2

additional functions

The following paragraphs detail some additional functions of the TCM8010-50.

digital-to-analog converters

Three 8-bit, voltage-output DACs are provided, with outputs on terminals DAC1, DAC2, and DAC3. The output range of each converter is from 0 V to $V_{DD}/2$ or 0 V to V_{DD} with an LSB step size of $V_{DD}/256$ or $V_{DD}/2 \times 1/256$ as selected by <DACX2>. All DAC outputs can either go to 0 V in standby mode or be active on depending on the state of control bit <DACON>. For correct operation of all of the TCM8010-50, < DACON > must be set to 0 in active mode. Previously written values are restored to the DAC outputs on entry to active mode. <$DACAD_1$–$DACAD_0$> selects which DAC is being addressed, and <DAC_7–DAC_0> sets the output voltage.

PRINCIPLES OF OPERATION

analog-to-digital converter

The TCM8010-50 contains an 8-bit ADC with a 3-channel analog-input multiplexer. This allows conversion of signals on ADC1, ADC2, and V_{MID}. An internal band gap voltage reference multiplied by two is used when measuring ADC1, ADC2, and V_{MID}.

Fifteen periods of DCLK are required to complete a conversion.

DTMF generator

The DTMF generator produces the seven standard tones with a frequency accuracy of ±1%. The desired DTMF signal is selected by <$DTMF_3$–$DTMF_0$>. A switchable preemphasis or skew between the low and high tone groups is provided for TACS operation and is selected by bit <DTSK>.

DTMF signal levels scale directly with supply voltage. A 4-bit trim is provided to allow adjustment of DTMF amplitude to meet system specifications and allow flexibility for user-generated call-tone type signals (<$DTTR_3$–$DTTR_0$>). When DTMF is selected in the transmit or receive paths, typical voice signals are attenuated by 50 dB.

clock and supply

Power supply and clock considerations are covered in the following paragraphs.

supply voltage

Specifications are given for a supply voltage of 5 V. Signal levels such as SAT, DATA, and DTMF are derived from this. Other parameters such as the compressor and expander unity-gain levels are also dependent on the supply voltage.

supply current

The TCM8010-50 has two basic operating modes: standby and active. In the standby mode, only the receive data path is enabled and current consumption is less than 2 mA. There is also the option of keeping the DACs powered up in the standby mode, depending on the setting of <DACON>. In the active mode, all functional blocks are powered up and the current consumption is less than 12 mA.

crystal oscillator and clock interface

The clock signal for the device can be generated by the internal oscillator block using an external crystal connected to the XT0 and XT1 terminals. Or, an external 0.5-V (minimum) peak sinusoidal clock signal can be applied to XT1. The external clock signal or the crystal can be one of eight frequencies, selected by control bits <$CKRT_2$–$CKRT_0$>. Crystal or external clock operation is selected by <CKSEL>.

TCM8030
BASEBAND PROCESSOR FOR ANALOG CELLULAR TELEPHONES

SLWS033 – JUNE 1996

- **Single Chip Audio and Data Processor for AMPS/EAMPS/NAMPS/TACS/ETACS/JTACS and NTACS**
- **2.7-V to 5.5-V Operation**
- **Multiple Power-Saving Modes**
- **On-Chip Compander**
- **Automatic Frequency Control**
- **Microphone Preamplifiers**
- **32-Ω Earpiece Driver**
- **Simple Serial Interface**
- **User-Configurable Interrupt Structure**
- **Independent Watchdog Timer**
- **8-Bit Programmable Timer**
- **Software-Selectable RX/TX Automute**
- **Digitally-Controlled Gains and Signal Selection or Muting**
- **Three 8-Bit DACs with Output Buffers**
- **DTMF Generator**
- **Arbitration Processing**
- **Two 8-bit Programmable Expansion I/O Ports**
- **Operation From Internal Oscillator, External Clock, or External TCXO**

description

The TCM8030 baseband processor for analog cellular telephones provides all the baseband signal processing required for any of the following standards for mobile and hand-portable cellular telephones: AMPS (Advanced Mobile telephone Service); EAMPS (Extended Advanced Mobile telephone Service); NAMPS (Narrow-Band Advanced Mobile telephone Service); TACS (Total Access Communication System); ETACS (Extended Total Access Communication System); JTACS (Japanese Total Access Communication System), and NTACS (North-American Total Access Communication System).

The analog section of the TCM8030 performs all filtering required for the speech, data, SAT (supervisory audio tone), and ST (signaling tone) paths. It has an integrated, CCITT (International Telegraph and Telephone Consultative Committee)-compatible compander as well as microphone preamplifiers and a differential, 32-Ω earpiece driver to complete the full integration of the baseband audio signal paths.

The digital section of the device implements the data transceiving, data processing, and SAT functions, including data recovery, majority voting, BCH (Bose-Chaudhuri-Hocquenghem) decoding, BCH encoding, TX (transmission) frame assembly, and SAT generation, detection, and regeneration. The TCM8030 supports both narrow-band standards, NTACS and NAMPS, with full implementation of the narrowband data, and DSAT (digital supervisory audio tone) and DST (digital signaling tone) filtering and processing functions. An on-chip, AFC (automatic frequency control) circuit also facilitates narrow-band operation. Communication with the microcontroller is achieved through a simple 4-wire serial interface.

In addition to these basic signal processing requirements, the TCM8030, integrates many of the ancillary functions required in a typical FM cellular telephone. Included are three 8-bit DACs (digital-to-analog converters), a DTMF (dual-tone multiple-frequency) generator, an 8-bit programmable counter/timer, an independent watchdog timer, two 8-bit microcontroller expansion ports, and a 4-bit keyboard interrupt port. Clock operation is through a pin-selectable on-chip crystal-referenced oscillator, an external clock source, or an external TCXO (temperature-controlled crystal oscillator).

PRODUCT PREVIEW

Caution. These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

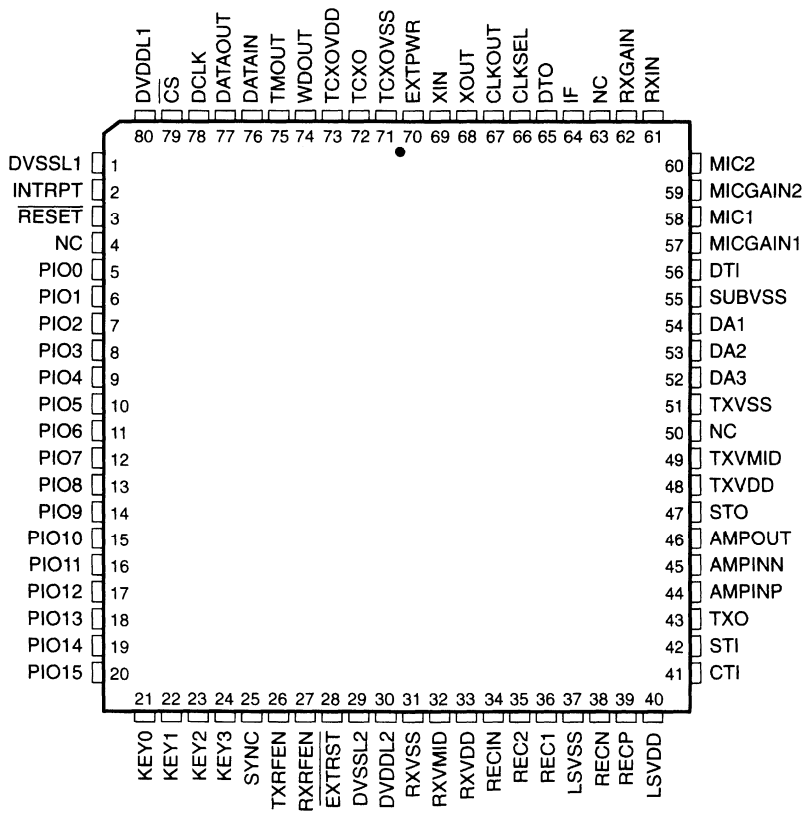
description (continued)

The TCM8030 is designed for ultra low-power applications and is manufactured using a low-power CMOS process. It operates from a single 2.7-V to 5.5-V supply and has five power-saving modes in addition to normal operation. The TCM8030 also features a total power-down mode in which the TCM8030 waits for the user to press the power-on key located on the telephone keyboard. Also implemented are two features that extend idle mode operation time.

One feature enables a reduction in the duty cycle of the microcontroller, and the other feature periodically shuts down the RF receiver. These features reduce the system power consumption to a minimum during idle mode and significantly increase the telephone standby time.

The gain and signal selection paths are software configurable so that all audio trimming functions can be achieved without manual intervention during telephone calibration on the production line. This production-time reduction feature, together with its high level of integration and low-power design, makes the TCM8030 an ideal solution for FM analog cellular telephones.

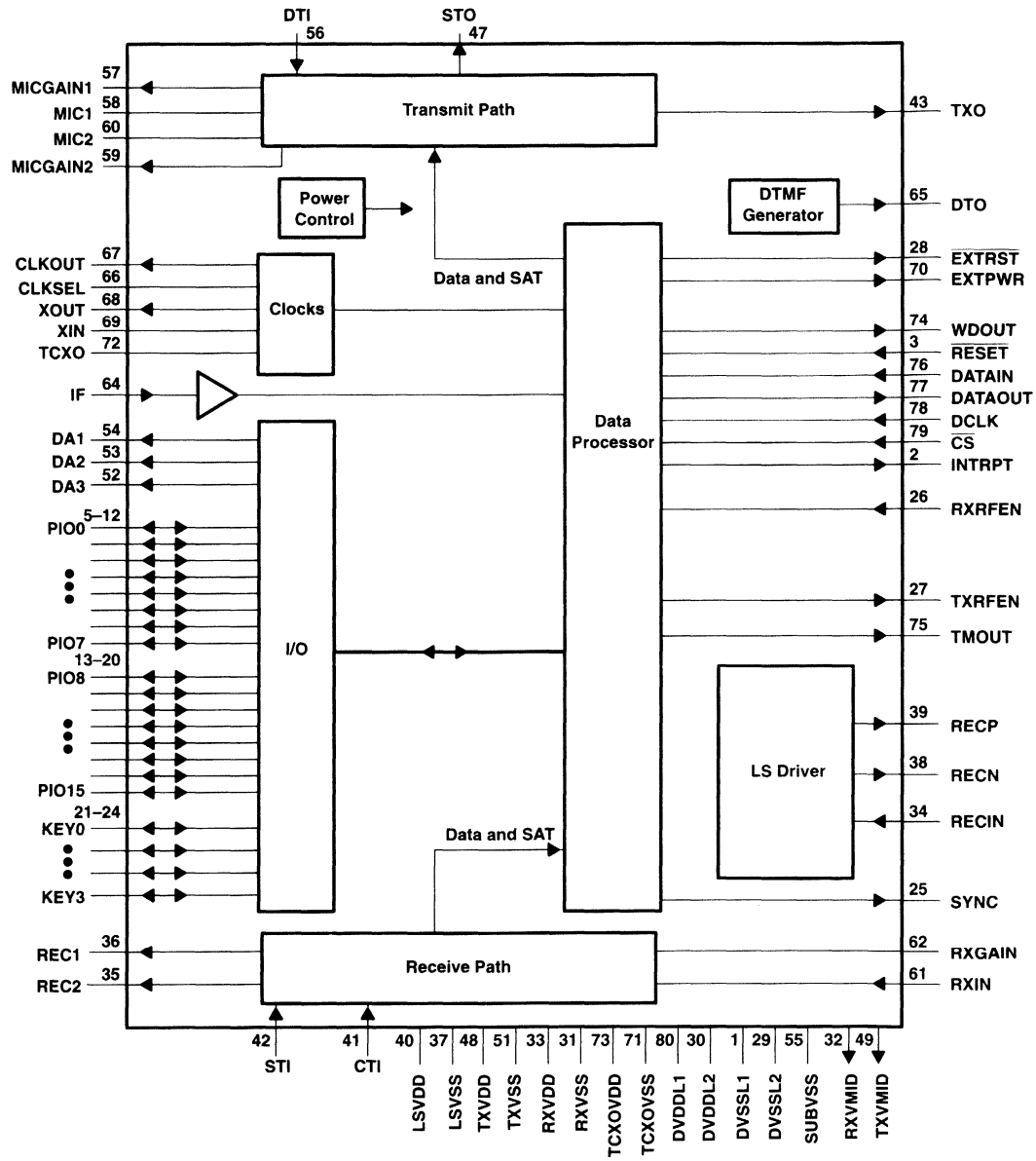
QFP PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCT PREVIEW

functional block diagram



PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AMPINN	45	I	Operational amplifier inverting input — uncommitted (analog)
AMPINP	44	I	Operational amplifier non inverting input — uncommitted (analog)
AMPOUT	46	O	Operational amplifier output — uncommitted (analog)
CTI	41	I	Call tone input (analog)
CLKSEL	66	I	Clock source select (digital)
CLKOUT	67	O	Clock output (digital)
$\overline{CS}$	79	I	Chip select input, active low (digital)
DA1 – DA3	52–54	O	Digital-to-analog converter output (analog)
DATAIN	76	I	Data input (digital)
DATAOUT	77	O	Data output (digital)
DCLK	78	I	Data clock input (digital)
DTI	56	I	Transmit DTMF input (analog)
DTO	65	O	DTMF generator output (analog)
DVDDL1, DVDDL2	80, 30		Digital power supply No. 1 and No. 2
DVSSL1, DVSSL2	1, 29		Digital ground No. 1 and No. 2
$\overline{EXTRST}$	28	O	Reset output to the rest of the telephone (used in total power-down mode) (digital)
EXTPWR	70	O	Power-on enable to the rest of the telephone (used in total-power-down mode) (digital)
IF	64	I	Input from second IF to AFC circuit (analog)
INTRPT	2	O	Interrupt output (digital)
KEY0 – KEY3	21–24	I/O	Keyboard interrupt inputs or programmable I/O ports (digital)
LSVDD	40		Loudspeaker power supply
LSVSS	37		Loudspeaker ground
MIC1, MIC2	58, 60	I	Microphone amplifier No. 1 and No. 2 input (analog)
MICGAIN1 MICGAIN2	57, 59	O	Microphone amplifier No. 1 and 2 output (analog)
PIO0 – PIO15	5–20	I/O	Programmable input or output port 0 through 15 (digital)
REC1, REC2	35, 36	O	Receive output No. 1 and No. 2 (analog)
RECIN	34	I	Earpiece amplifier input (analog)
RECN	38	O	Earpiece amplifier differential outputs, negative (analog)
RECP	39	O	Earpiece amplifier differential outputs, positive (analog)
$\overline{RESET}$	3	I	Reset input, active low (digital)
RXIN	61	I	Receive amplifier input (analog)
RXGAIN	62	O	Receive amplifier output gain (analog)
RXRFEN	27	O	RXRF enable output from RXRF idle mode logic (digital)
RXVDD	33		Receive-analog power supply
RXVMID	32	O	Receive-analog mid-supply voltage
RXVSS	31		Receive-analog ground
SYNC	25	O	Frame sync (digital)
STI	42	I	Sidetone input (analog)
STO	47	O	Sidetone output (analog)
SUBVSS	55		Substrate ground connection

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
TCXO	72	I	Input from TCXO to input buffer, AFC, and clock circuits (digital)
TCXOVDD	73		XTALOSC and TCXO input buffer power supply
TCXOVSS	71		XTALOSC and TCXO input buffer ground
TMOUT	75	O	Counter / timer output (digital)
TXO	43	O	Transmit output (analog)
TXRFEN	26	O	Transmit RF enable output from arbitration logic (digital)
TXVDD	48		Transmit analog supply
TXVMID	49	O	TX analog mid-supply voltage
TXVSS	51		Transmit analog ground
WDOUT	74	O	Watchdog timer output (digital)
XIN	69	I	Clock input or input connection for external crystal
XOUT	68	O	External crystal output connection

absolute maximum ratings over operating free-air temperature range (see Note 1)†

Supply voltage range, V_{DD}, V_{SS} . . . . . – 0.5V to 6.0V
Input voltage range, any input, V_I . . . . . – 0.5 to V_{DD} + 0.5V
Output voltage range (includes open drain outputs), any output, V_O . . . . . – 0.5 to V_{DD} + 0.5V
Operating free-air temperature range, T_A . . . . . – 30°C to 70°C
Continuous total power dissipation at (or below) T_A = 25°C . . . . . .
Storage temperature range, T_{stg} . . . . . – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	2.7	3	3.8	V
Operating free-air temperature range, T_A	–30		70	°C
Operating junction temperature, T_J	–30		70	°C
Output load resistance at MICGAIN1 and MICGAIN2	10	50		kΩ
Output load capacitance at MICGAIN1 and MICGAIN2			20	pF
Output load resistance at RXGAIN	47			kΩ
Output load capacitance at RXGAIN			20	pF
Load resistance, DACx	30			kΩ
Load capacitance, DACx			50	pF
Output load to GND at DTO	100			kΩ
Output load resistance at AMPOUT	47			kΩ
Output load capacitance at AMPOUT			20	pF
Output load at REC1/REC2	500			Ω

PRODUCT PREVIEW

electrical characteristics over recommended range of supply voltages and operating conditions (unless otherwise noted)

supply current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DD(A)}$	Analog supply current	Full operation		25		mA
$I_{DD(D)}$	Digital supply current	Full operation		0.5	1	mA
$I_{DD(PM1)}$	Power mode No. 1	Total power-down mode		41		µA
$I_{DD(PM2)}$	Power mode No. 2	Shut-down mode		340		µA
$I_{DD(PM3)}$	Power mode No. 3	Idle mode		2.2		mA
$I_{DD(PM4)}$	Power mode No. 4	Tone mode		5		mA
$I_{DD(PM5)}$	Power mode No. 5	Full operation, DTMF off		22		mA
$I_{DD(PM6)}$	Power mode No. 6	Full operation, DTMF on		25		mA

digital I/Os

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 1 mA	$V_{DD}-0.4$		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA		$V_{SS}+0.4$	V
V_{IT+}	Positive-going input threshold voltage			$0.7\ V_{DD}$	V
V_{IT-}	Negative-going input threshold voltage		$0.3\ V_{DD}$		V
V_{hys}	Hysteresis ($V_{IT+} - V_{IT-}$)		$0.1\ V_{DD}$	$0.3\ V_{DD}$	V
I_{OZ}	High-impedance output current	$V_I = V_{DD}$ or V_{SS}		±10	µA
I_{IL}	Low-level input current	$V_I = V_{SS}$		−1	µA
I_{IH}	High-level input current	$V_I = V_{DD}$		1	µA

transmit path specifications (see Figure 14)

MIC1 and MIC2

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Unity gain frequency			1.5	2.5	MHz
Input current at MIC1 and MIC2			1		µA
Input noise, psophometric weighting	R_{in} = 50 kΩ			0.1	mVrms
Open loop voltage amplification		70	80		dB
Close loop voltage amplification			15	26	dB

VOICE and DTMF (V/D) trim, MIC1 to TXO

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Positive trim range	Code FH			3.75	dB
Negative trim range	Code 0H	−4.3			dB
Step size			0.5		dB
0 dB tolerance	Code 8H		0.5		dB

COMPRESSOR, MIC1 to TXO

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Unity gain level			−24.43		dBV
Linearity				±1	dB
Attack time (see Note 2)		2.4	3	3.6	ms
Recovery time (see Note 3)		10.8	13.5	16.2	ms

NOTES: 2. Time taken for the output to settle to 1.5 times the final value with a 6-dB input step
3. Time taken for the output to settle to 0.75 times the final value with a −6-dB input step

PRODUCT PREVIEW

LIMITER, MIC1 to TXO

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum output signal, AMPS/TACS	Code Fh, max deviation		740		mVpp
Positive trim range	Code Fh			2.6	dB
Negative trim range	Code 0h	–4.6			dB
Step size			0.43		dB
0 dB tolerance	Code Ah		0		dB
Distortion, AMPS/NAMPS/TACS	2/3 of max output signal			3%	

TXTRIM, MIC1 to TXO

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Positive trim range	Code 1Fh		4.1		dB
Negative trim range	Code 0h	–4.4			dB
Step size			0.2		dB
0 dB Tolerance	Code 10h		0		dB

transmit path, MIC1 to TXO

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TXSUM mute attenuation		f = 1 kHz at MIC1	50	80		dB
Distortion, AMPS/NAMPS/TACS		2/3 of max output signal			3%	
Noise, Compressor enabled,	AMPS and TACS	MIC1/MIC2=V_{MID}			2.3	mVrms
	NAMPS				1	mVrms
Crosstalk in TXSW		f = 1 kHz	50			dB
Crosstalk RX and TX Path MIC1/REC1, RXIN grounded		f = 1 kHz at 100 mV	50			dB

transmit data, at TXO

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output level	AMPS/TACS			580		mVpp
	NAMPS/NTACS			29		mVpp
Harmonic distortion				3.3%		

TX-DAT Trim at TXO

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Positive trim range	Code Fh			1.8	dB
Negative trim range	Code 0h	–2.3			dB
Step size			0.6		dB
0 dB tolerance	Code 4h		0.5		dB

transmit SAT at TXO

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output level	AMPS/TACS					mVrms
Harmonic distortion						

transmit SAT TRIM at TXO

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Positive trim range	Code 7h			2.3	dB
Negative trim range	Code 0h	–2.4			dB
Step size			0.3		dB
0 dB tolerance	Code 8h		0.5		dB

PRODUCT PREVIEW

receive path specifications (see Figure 14)

RXAMP

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Unity gain frequency			1.5		MHz
Input current			1		µA
Input noise psophometrically weighted	Rin = 50 kΩ			0.1	mVrms
Open-loop voltage amplification		70	80		dB
Closed-loop voltage amplification			15	26	dB

RXTRIM, RXGAIN to REC1

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Positive trim range	Code Fh			3.7	dB
Negative trim range	Code 0h	−4.3			dB
Step size			0.5		dB
0 dB Tolerance	Code 8h		0.5		dB

Audio Expander, RXGAIN to REC1

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Unity gain level			690		mVpp
Linearity				±2	dB
Attack time (see Note 4)		2.4	3	3.6	ms
Recovery time (see Note 5)		10.8	13.5	16.2	ms

NOTES: 4. Time taken for the output to settle to 0.57 times the final value with a 6-dB input step
5. Time taken for the output to settle to 1.5 times the final value with a −6-dB input step

receiver path, RXGAIN to REC1

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REC1SW mute attenuation			50		dB
Crosstalk between REC1/REC2			36		dB
Distortion at REC1/REC2 Expander enabled	RX_{IN} 400 mV, f=1kHz, No load		0.01%		
Noise at REC1/REC2 Expander bypassed	RX_{IN} = VMID, psophometric weighting		0.02		mVrms
Voice mute attenuation	RX_{IN} = 400 mV, 1kHz	50	80		dB
Output voltage at REC1/REC2	R_L = 500 Ω	1.5			Vpp

VOL CTRL, RXGAIN to REC1

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Positive range	Code Fh			16.5	dB
Negative range	Code 0h	−20			dB
Step size			2.5		dB
0 dB Tolerance	Code 8h		0.5		

LS DRIVER at RECP and RECN

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Open loop voltage amplification			70		dB
Unity gain frequency			1.5		MHz
Differential output level	V_{DD} = 3 V		0.8		Vp-p
Distortion			0.12%		
Input load resistance			150		Ω

PRODUCT PREVIEW

receive data detect

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Level at RXGAIN	NAMPS			–27.68		dBV
	NTACS			–25.65		dBV
	TACS, JTACS			–6.53		dBV
	AMPS			–6.43		dBV
Must not detect level				–25.51		dBV
Must detect level				–19.49		dBV

receive SAT detect

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Level at RXGAIN	TACS, JTACS			–17.95		dBV
	AMPS			–18.56		dBV
Must not detect level				–37.43		dBV
Must detect level				–30.49		dBV

miscellaneous block specifications (see Figure 14)

digital-to-analog converters DAC1, DAC2, and DAC3

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DACx output voltage	Code 255	V_{DD} –0.05			V
DACx zero code DC offset	Code 0		0	0.05	V
Differential nonlinearity	Codes 5 – 250	–1		1	LSB
Integral nonlinearity	Codes 5 – 250	–1		1	LSB
Conversion time			3		ms

DTMF GEN

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DTO output level low	AMPS			270		mVrms
697 Hz				270		mVrms
770 Hz				270		mVrms
852 Hz				270		mVrms
941 Hz				270		mVrms
DTO output level high	AMPS			270		mVrms
1150 Hz				270		mVrms
1209 Hz				270		mVrms
1336 Hz				270		mVrms
1477 Hz				270		mVrms
1633 Hz				270		mVrms
2048 Hz				270		mVrms

PRODUCT PREVIEW

AMP7

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Unity gain frequency			1.5		MHz
Input current			1		μA
Input noise, psophometric weighting	R_{in} = 50 kΩ			0.1	mVrms
Open-loop voltage amplification		70	83		dB
Closed-loop voltage amplification			15	26	dB
Harmonic Distortion			0.01%		

timing requirements over recommended ranges of operating conditions (see Figure 1)

		MIN	NOM	MAX	UNIT
t_{su1}	Setup time, $\overline{CS}$ to DCLK↑	≥200			ns
t_{su2}	Setup time, DATAIN before DCLK↑	≥200			ns
t_h	Hold time, DATAIN after DCLK↑	≥200			ns
t_d	Delay time, DCLK↑ to $\overline{CS}$↓ (start of next cycle)	≥1000			ns
DCLK				≤1	MHz

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

Figure 1 shows the write timing diagram for the microcontroller interface. The read timing diagram for the microcontroller interface is shown in Figure 2. Refer to microcontroller interface operation for a detailed description.

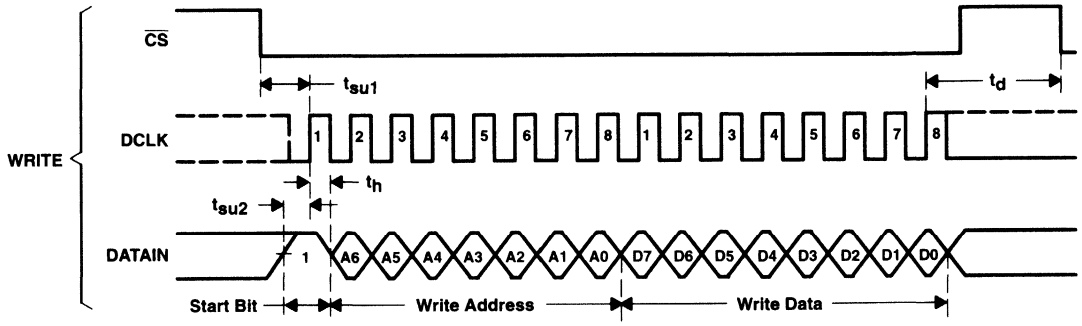


Figure 1. Microcontroller Interface Write Timing Diagram

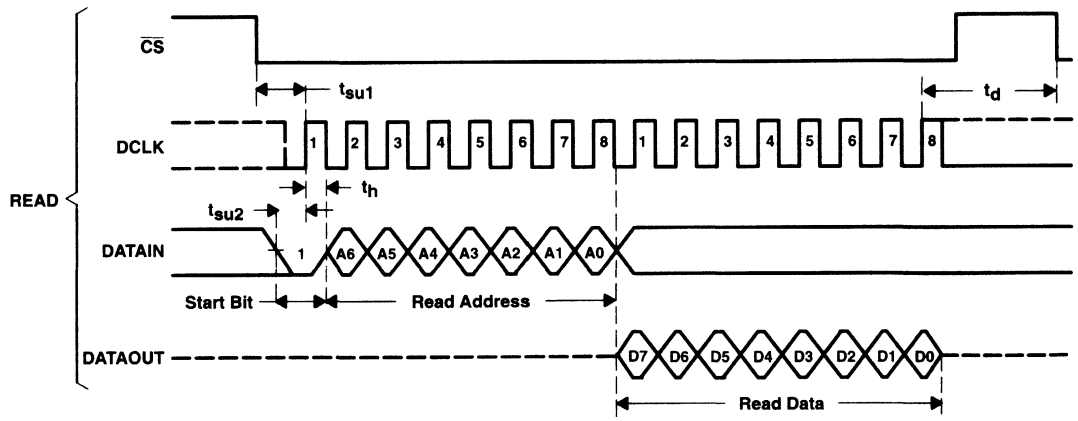


Figure 2. Microcontroller Interface Read Timing Diagram

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

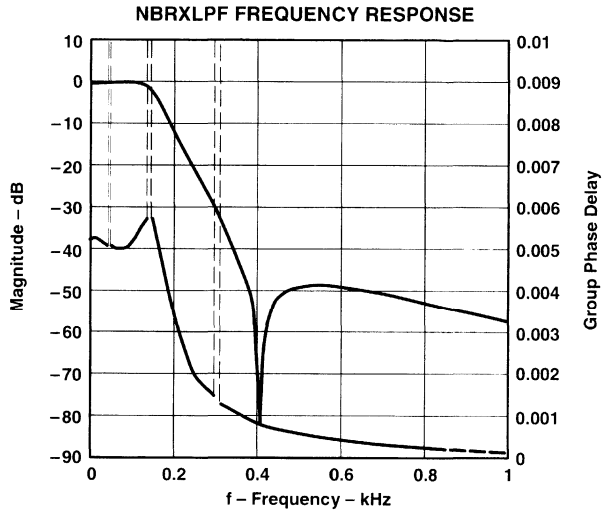


Figure 3

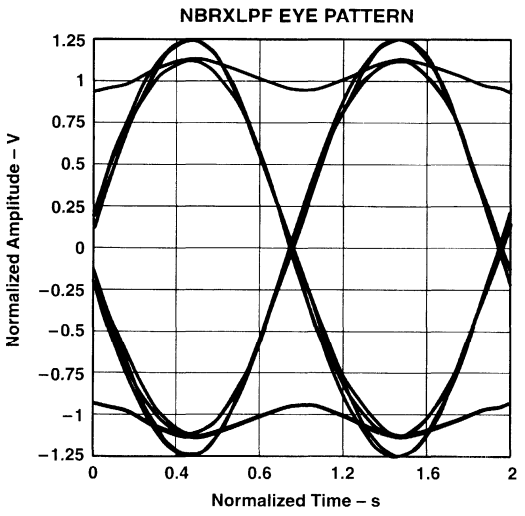


Figure 4

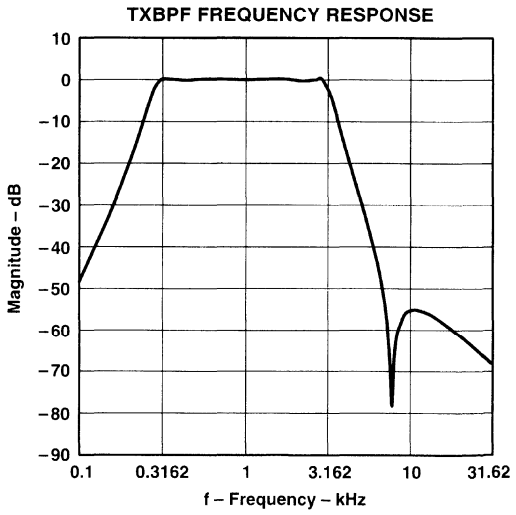


Figure 5

TYPICAL CHARACTERISTICS

TXBPF FREQUENCY RESPONSE

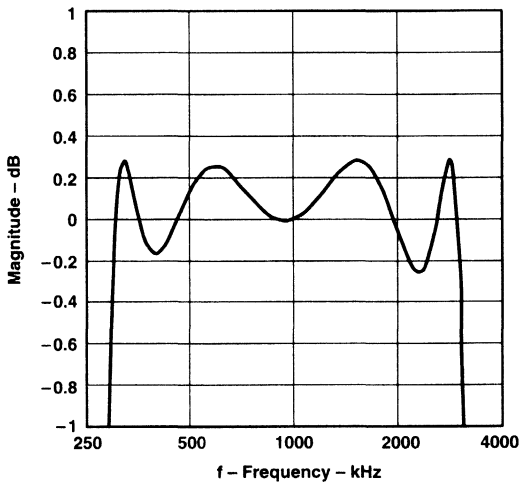


Figure 6

TXDATLPF AND TXSUMLPF COMBINED RESPONSE

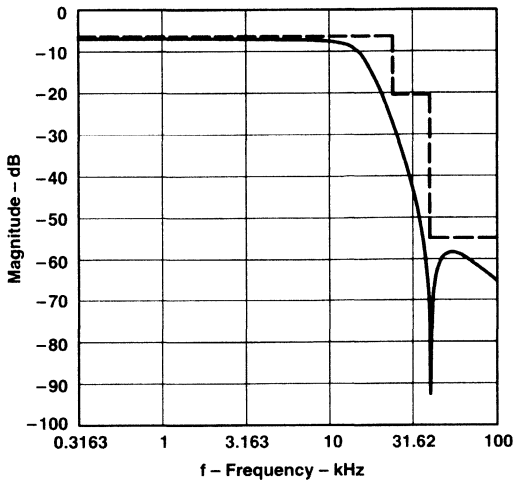


Figure 7

EYE PATTERN FOR TXDALPF AND TXSUMLPF COMBINED (NARROWBAND)

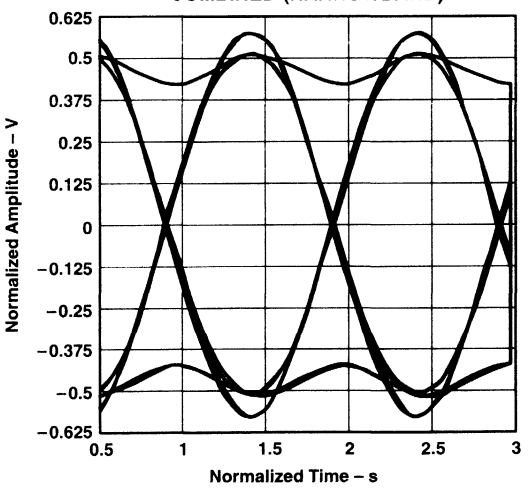


Figure 8

TXLPF FREQUENCY RESPONSE

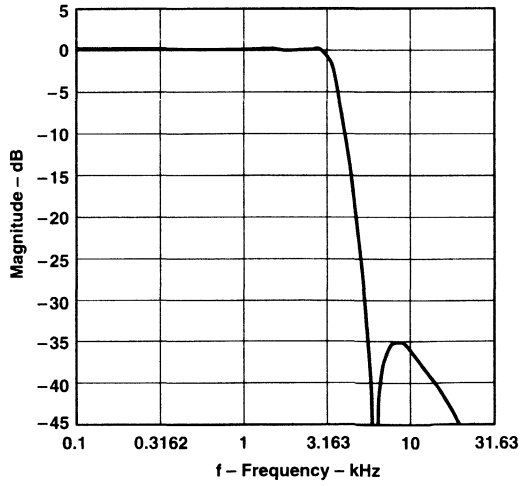


Figure 9

PRODUCT PREVIEW

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

TXLPF FEQUENCY RESPONSE

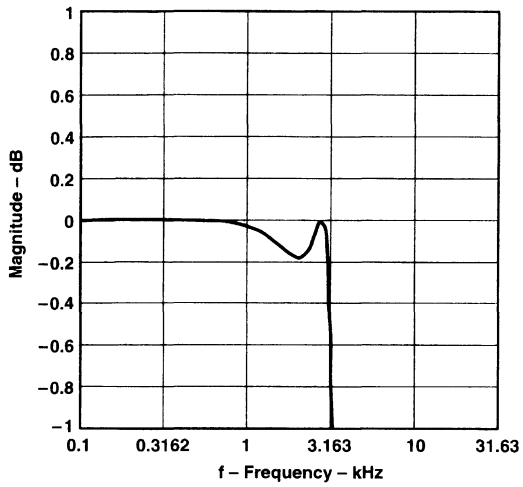


Figure 10

TXSATBPF RESPONSE PROFILE

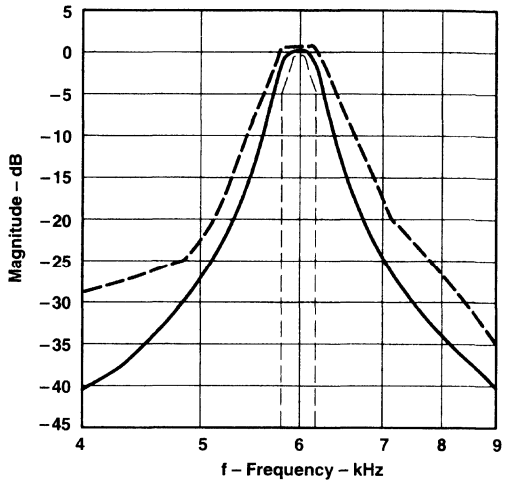


Figure 11

TXSUMLPF FREQUENCY RESPONSE

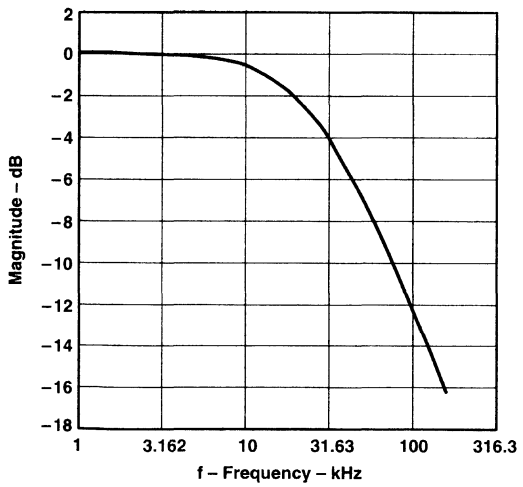


Figure 12

TXSUMLPF FREQUENCY RESPONSE

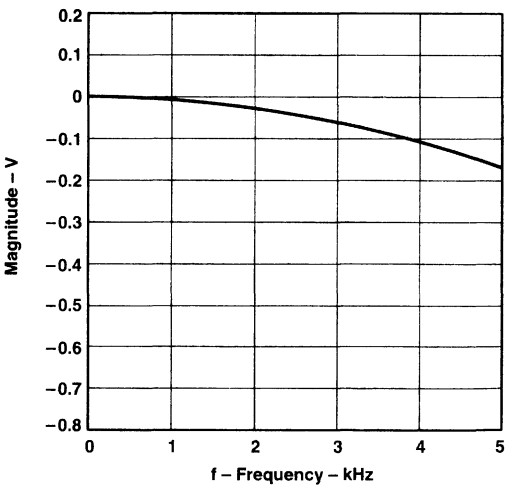


Figure 13

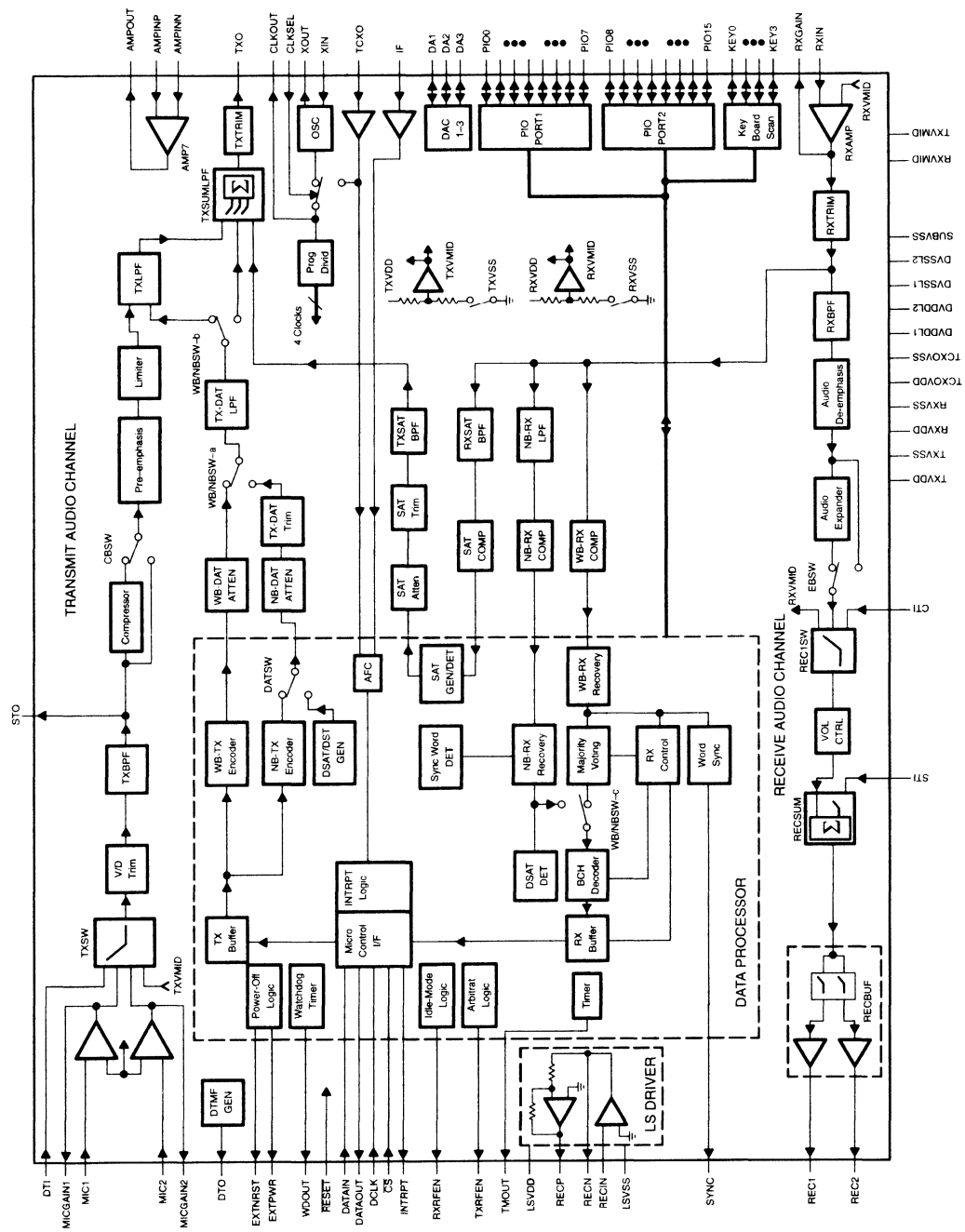


Figure 14. TCM8030 Detailed Functional Block Diagram

PRODUCT PREVIEW

PRINCIPLES OF OPERATION

overview

The TCM8030, has two main analog paths for transmit and receive, a digital data processor with associated filters, comparator and routing switches, data I/O, and other functions that include audio power amplifiers, an uncommitted operational amplifier, and DTMF generator as shown in Figure 14. In addition, separate power control functions are provided to maximize system power efficiency.

A block diagram of the receive audio path is shown in Figure 15. A pair of external gain setting resistors (R1, R2) adjust the input sensitivity to suit system requirements. A second digitally programmable gain trim is provided in the next stage (RXTRIM) followed by a BPF (band-pass filter). The output of the filter drives both the Data/SAT paths and the audio de-emphasis block.

The audio expander can be bypassed for testing and linear functions. Switch REC1SW allows either transmit loopback, the audio expander output, or the DTMF call tone (CTI) to be selected and then fed to the digitally-programmable volume control (VOL CTRL).

The receive summing block, RECSUM, can sum (or not sum) the sidetone (STI) with the audio signal based on a software command. The final stage in this path is a pair of configurable output buffers that can drive a piezo speaker or other light load. A separate loudspeaker driver block (LS DRIVER) is discussed later (see Figure 17).

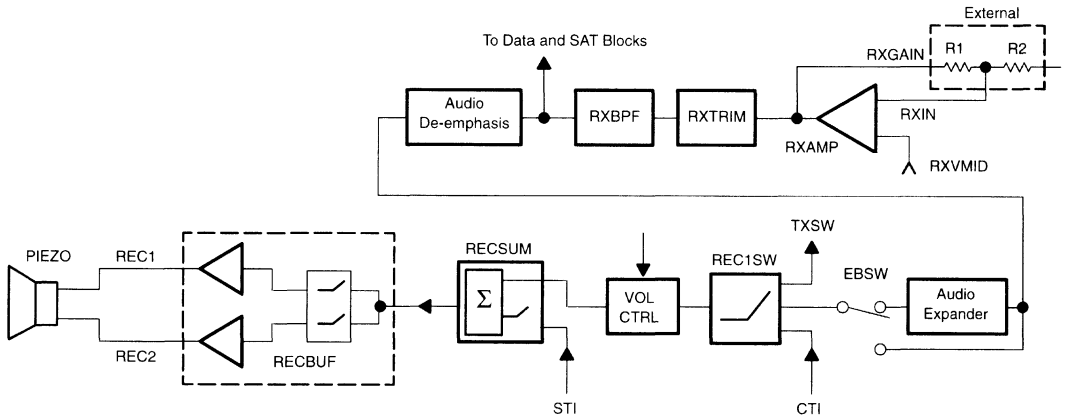


Figure 15. Receiver Audio-Path Block Diagram

PRINCIPLES OF OPERATION

overview (continued)

The block diagram for the transmit audio path is shown in Figure 16. Here, a choice of inputs can be selected under software control using the transmit switch (TXSW). The MIC1 and MIC2 inputs have operational amplifiers that can be configured with external gain setting resistors: R1/R2 and R3/R4. A selectable DTMF signaling input (DTI) is provided, together with a programmable DTMF generator that has an independent output (DTO).

A programmable voice/DTMF gain-trim stage V/D trim drives the transmit band-pass filter, TXBPF. The output of TXBPF goes to the sidetone output (STO) and the audio compressor. A bypass switch, CBSW, is provided to bypass the compressor for DTMF tones and other uncompressed functions (i.e., testing).

The audio pre-emphasis and (deviation) limiter blocks then drive the transmit low-pass filter, TXLPF. This attenuates the harmonics caused by limiting the signal. Some data transmission modes use the TXLPF route, which inverts the signal. This calls for the data signal polarity to be reinverted either by using the inversion set/reset bits or by external means.

The transmit sum and low-pass filter block, TXSUMLPF, can select voice, data, or SAT signals and sum them together. It also provides a continuous-time filter that removes high-frequency products. The final stage is the transmit gain-trim stage that drives the output terminal, TXO.

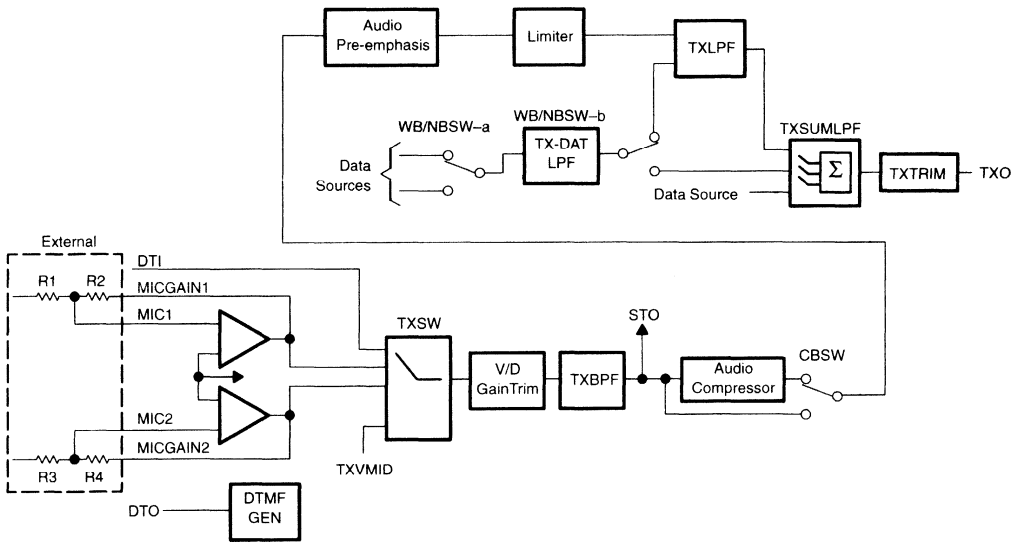


Figure 16. Transmit Audio-Path Block Diagram

PRODUCT PREVIEW

overview (continued)

Miscellaneous functional blocks are shown in Figure 17. The LS DRIVER block provides the capability to drive loudspeakers. Gain is set with the external resistor pair R1/R2. An uncommitted operational amplifier (AMP7) is provided and a pair of gain-set resistors (R3/R4) are shown connected externally.

A separate mid-rail voltage source is provided for both the receive and transmit paths. Each is deselected when its part of the circuit is powered down.

A programmable divide, PROG DIVID, can be programmed to divide the oscillator signal (or external clock) into four separate internal clocking signals. The oscillator block requires only a crystal (XTAL) and a pair of capacitors for operation. Alternatively, an external clock can be connected at XIN, or TCXO can be selected as required. A triple DAC is also provided for oscillator trim functions. Used in conjunction with the AFC control in the data processor block (see Figure 18), this permits lower stability oscillators to be used successfully, thus saving system costs.

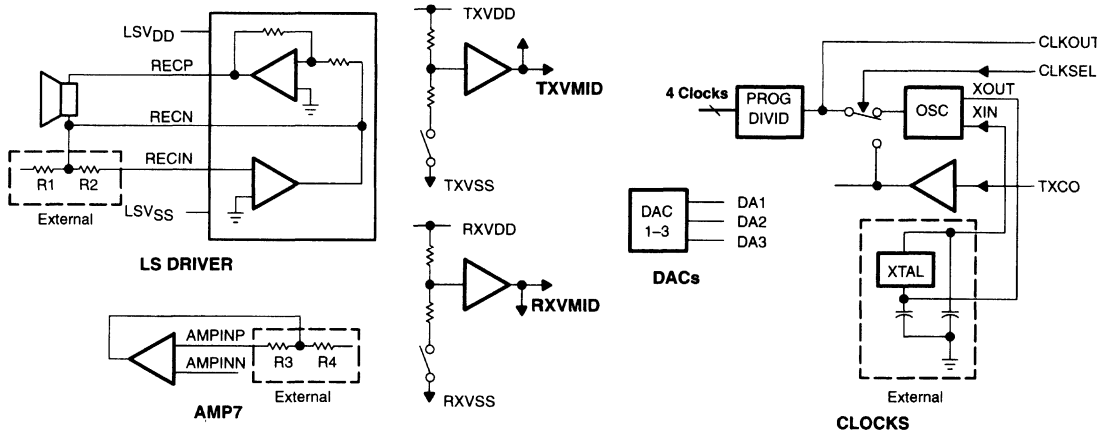


Figure 17. Miscellaneous Functional Block Diagrams

PRINCIPLES OF OPERATION

overview (continued)

The data processor, Figure 18, provides a large number of functions for processing cellular data streams and controlling the other functions of the TCM8030.

Power-off and idle-mode logic is provided, together with both standard and watchdog timers. Incoming (RX) data is selected according to standard (for example, WB/NB) and processed through filters/comparators to comply with the standard. After majority voting and BCH decoding, the data is buffered and applied to the microcontroller interface. On the transmit side, data is placed in the TX buffer after selecting the appropriate encoder. The encoded data goes through its attenuator/trim stage to the transmit data lowpass filter (TXDAT LPF) and is switched into the transmit (TX) audio path.

SAT is recovered from the RX audio path through a filter and comparator and fed to the data processor detector/regenerator. Regenerated TXSAT goes through programmable attenuator/trim stages to the band-pass filter that feeds the TX path.

Digital supervisory audio tone (DSAT) is detected through the NB data recovery block. The regenerated signal is sent through the normal NBDAT path to the transmit path.

The microprocessor interface is a simple serial shift register function, using DATAIN, DATAOUT, DATACLK, and $\overline{CS}$, and has an interrupt output (INTRPT). This interface allows the TCM8030 to communicate with the microcontroller that is operating the telephone.

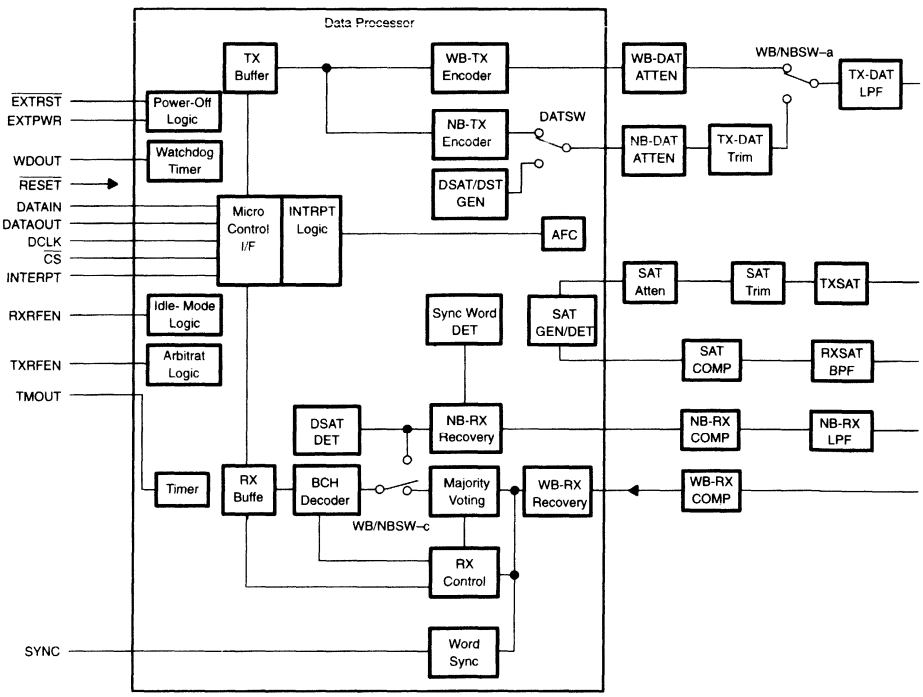


Figure 18. Data Processor Block Diagram

PRODUCT PREVIEW

PRINCIPLES OF OPERATION

audio processing functions — receive path

The TCM8030 audio receive path is composed of the following circuits, as shown in Figure 14. A brief functional description is given for each circuit listed.

RXAMP

The receive amplifier circuit (RXAMP) receives its input from terminal RXIN. A portion of the RXAMP output is applied through terminal RXGAIN to a pair of external resistors that set the stage gain. The RXAMP noninverting input is internally connected to the internal RXVMID reference signal.

RXTRIM

The receive trim (RXTRIM) stage is provided to compensate for FM discriminator variations. This block also includes a switched-capacitor filter to perform antialiasing.

RXBPF

The receive band-pass-filter (RXBPF) is a switched-capacitor filter with a passband of 300 Hz to 3 kHz.

AUDIO DE-EMPHASIS

As the audio frequency increases, the audio deemphasis circuit decreases the signal gain at a rate of 6 dB per octave across 300 Hz to 3 KHz.

AUDIO EXPANDER

The audio expander circuit provides an output level change of 2 dB for an input signal level change of 1 dB.

EBSW

The audio expander bypass switch (EBSW) permits the routing of the received audio around the audio expander circuit during testing.

REC1SW

The receive 1 switch (REC1SW) selects one of three inputs: the output from the audio expander (or bypassed expander), the CTI (DTMF) input, or it selects RXVMID to mute the channel.

VOL CTRL

The volume control (VOL CTRL) circuit can be programmed to provide a nominal gain of –20 dB to +17.5 dB.

RECSUM

The receiver summing circuit and switch (RECSUM) provides the means for adding the sidetone input (STI) into the receive audio path.

RECBUF

The receive buffer (RECBUF) switches in or mutes two output buffers independently, or connects these buffers in differential mode so that a piezo speaker can be connected to REC1 and REC2 terminals. Independent control of the two audio outputs allows one to be used for external handsfree operation.

LS DRIVER

The loud speaker driver (LS DRIVER) circuit is a selectable differential or single-ended output earpiece power amplifier. It is used to drive a 32-Ω dynamic earpiece (or a piezo earpiece).

PRINCIPLES OF OPERATION

audio processing functions — transmit path

The TCM8030 audio transmit path is composed of the following circuits as shown in Figure 14. A brief functional description is given for each circuit listed.

MIC1, MIC2

A pair of single-ended microphone amplifiers accept two input signals (MIC1 and MIC2). Output from each amplifier is fed back through terminals MICGAIN1 and MICGAIN2 and applied to an external resistor to set the gain for each individual amplifier.

TXSW

The transmit switch (TXSW) permits selecting one of four transmit audio sources. TXSW can select either the voice signal from MICAMP1 or MICAMP2, or the input from the DTI terminal (which has been connected externally to the DTMF generator). The path can also be muted by connecting the switch to the internal reference TXVMID signal.

V/D TRIM

The voice and DTMF (V/D Trim) circuit contains an antialiasing filter to process the audio signal before it is applied to the transmit band-pass filter. This circuit block also provides a means to trim the voice and DTMF signal levels.

TXBPF

The transmit band-pass filter (TXBPF) circuit is a switched-capacitor band-pass filter that passes only the transmit-audio frequencies from 300 Hz to 3 kHz.

COMPRESSOR

The compressor circuit compresses the audio signal and outputs a signal that changes by1 dB for an input signal change of 2 dB.

CBSW

The compressor bypass switch (CBSW) permits routing the audio signal around the compressor circuit when testing the audio channel or for passing DTMF signals.

PRE-EMPHASIS

As audio frequency increases, the preemphasis circuit increases the signal gain at a rate of 6 dB per octave across the 300Hz to 3KHz audio passband.

LIMITER

The LIMITER circuit limits the transmit signal deviation within an acceptable range.

TXLPF

This circuit is a transmission low-pass switched-capacitor filter (TXLPF). It removes harmonics caused by the (deviation) limiter. Linear phase design prevents overshoots. This circuit is also used in the narrow-band mode to filter switched-capacitor output noise from TXDATLPF.

TXSUMLPF

The transmit summing and low-pass filter circuit (TXSUMLPF) selectively sums voice, data, or SAT into the audio output. It also includes a low-pass switched-capacitor filter to reduce spurious output emissions above 10 kHz.

PRINCIPLES OF OPERATION

TXTRIM

The transmit trim stage (TXTRIM) trims the FM deviation transmitting ST or wide-band data prior to its output on the TXO terminal stage. This stage has a continuous second-order smoothing filter that removes noise.

data processing functions — receive path

The TCM8030 data receive path is composed of the following circuits as shown in Figure 14. A brief functional description is given for each circuit listed.

WB – RX COMP

This wide-band receive comparator circuit (WB-RXCOMP) features built-in hysteresis to reject noise.

WB – RX RECOVERY

This circuit performs the wide-band receive data recovery function (WB-RX RECOVERY), including dotting.

WORD SYNC

This circuit performs frame synchronization (WORD SYNC) recovery for the wide-band data channel.

NB-RXLPF

The narrow-band receive-data and low-pass filter circuit (NB-RXLPF) contains a low-pass switched-capacitor filter for filtering DSAT and audio signals. This circuit also includes a decimating antialias stage at the input.

NB – RX COMP

The narrow-band receive and DSAT comparator circuit (NB-RXCOMP) features built-in hysteresis to reject noise.

NB – RX RECOVERY

The narrow band data and DSAT recovery circuit (NB-RX RECOVERY) recovers the narrow-band data and DSAT components for application to the BCH decoder circuit.

SYNC WORD DET

The sync word detect circuit (Sync Word DET) detects the narrow-band data sync word.

DSAT DET

The digital supervisory audio tone detector circuit (DSAT DET) monitors the narrow-band receive recovery data for the DSAT signal.

MAJORITY VOTING

All 40 receive-data bits are individually majority voted in the wide-band and narrow-band data majority voting circuit. The number of repeats used can be read using the microcontroller interface.

BCH DECODER

The wide-band and narrow-band BCH decoder stage can correct up to two errors in the received signal and give a 4-bit-error-correction status report.

RX BUFFER

The receive buffer (RX BUFFER) stage provides a buffer for both wide-band and narrow-band received data.

RX CONTROL

The receive control (RX CONTROL) functional block controls the wide-band/narrow-band receive data recovery and decoding stages and splits the time-multiplexed busy/idle bits, chooses word A or B, and starts majority voting and error correction when required.

PRINCIPLES OF OPERATION

ARBITRAT LOGIC

The arbitration logic circuit (ARBITRAT LOGIC) arbitrates the wide-band data busy/idle bits majority voting and outputs the result to the TXRFEN terminal.

IDLE-MODE LOGIC

The idle-mode logic circuit senses the microcontroller unit (MCU) idle mode and receive RF (RXRF) idle mode functions and applies an enable signal to output terminal RXRFEN to control internal power mode.

data processing functions — transmit path

The data processing functions associated with the TCM8030 transmit path are performed by the following circuits illustrated in Figure 14. A brief functional description is given for each circuit listed.

TX BUFFER

The transmit buffer (TXBUFFER) buffers both narrow-band and wide-band data that is loaded from the five transmit dataword registers.

WB – TX Encoder

The wide-band transmit data encoder circuit (WB – TX Encoder) receives the data from the transmit buffer and performs all the necessary operations for both the reverse control channel (RECC) and reverse voice channel (RVC) data transmission. BCH parity bits are calculated and added to the data along with word sync and dotting. The wide-band signaling tone, ST, is generated when required.

NB – TX Encoder

The narrow-band transmit data encoder circuit (NB – TX Encoder) calculates the BCH encoding parity bits from the data in the transmit buffer and adds the 30-bit sync word to synchronize the transmission of RVC data to the DSAT.

DATSW

The digital audio tone switch (DATSW) selects either narrow-band data or the output from the DSAT/DST GEN stage for application to the NB – DAT ATTEN stage. Operation of the DATSW is controlled by the value in bits 5 and 6 of the operational control word C1. When bits 5 and 6 are 0, the switch connects to the NB – TX Encoder input. See topic, address 00 — operational control word (C1) topic for detailed information about control word C1.

WB/NBSW-a, -b and -c

The (wide-band, narrow-band) switches WB/NBSW-a through -c are ganged together to select either narrow-band (NAMPS) or wide-band (AMPS) transmission operation. The switch position is controlled by the value in bit 1 of the operational control word. See topic, address 00 — operational control word (C1) for detailed information about the control word C1.

DSAT/DST GEN

The digital supervisory audio tone/digital sinaling tone generator (DSAT/DST GEN) circuit generates the narrow-band DSAT and DST signals.

NB – DAT ATTEN AND WB – DAT ATTEN

These two circuits are fixed narrow-band and wide-band data attenuators (NB – DAT ATTEN AND WB – DAT ATTEN that set the correct data signal levels.

TXDAT TRIM

The transmit data trim circuit (TXDAT TRIM) trims the DSAT, DST, and narrow-band data levels.

PRINCIPLES OF OPERATION

TX-DAT LPF

The transmit data low-pass filter circuit (TX-DAT LPF) provides low-pass switched-capacitor filtering of the DSAT, DST, and transmitted narrow-band and wide-band data to minimize output harmonics and achieve correct narrow-band transmitted data eye pattern.

SAT processing functions — receive path

The processing of the supervisory audio tone (SAT) is the TCM8030 receive path is performed by the following circuits shown in Figure 14. A brief functional description is given for each circuit listed.

RXSAT BPF

The receive SAT band-pass filter (RXSAT BPF) is a switched-capacitor filter.

SAT COMP

The supervisory audio tone comparator (SAT COMP) circuit slices the received SAT signal before sending it to the SAT GEN/DET circuit and contains built-in hysteresis to aid in noise rejection.

SAT processing functions — transmit path

The supervisory audio tone processing functions associated with the TCM8030 transmit path are performed by the following circuits illustrated in Figure 14. A brief functional description is given for each circuit listed.

SAT GEN/DET

The supervisory audio tone generator and detect (SAT GEN/DET) circuit is primarily a transponding digital phase-locked loop (PLL) circuit. It is used in wide-band mode only. This circuit is an enhanced design that improves SAT sensitivity. SAT outputs can also be programmed without a SAT input when testing the telephone.

SAT ATTEN

The supervisory audio tone attenuator (SAT ATTEN) circuit consists of a fixed attenuator and is used to set the correct TX SAT signal level.

SAT TRIM

The supervisory audio tone trim (SAT TRIM) circuit sets the wide-band SAT trim level. Output from this circuit is applied to the TXSATBPF antialias filter.

TXSAT BPF

The transmit band-pass filter (TXSAT BPF) circuit is a switched-capacitor band-pass filter that performs antialiasing.

Clocks

The crystal oscillator and programmable dividers (OSC and PROG DIVID) circuits generate internal clocks and also an external clock output on the CLKOUT terminal.

PRINCIPLES OF OPERATION

OSC and PROG DIVID

The TCM8030 can be clocked from one of three sources as selected by the CLKSEL terminal as follows:

1. Internal crystal oscillator (XTALOSC), crystal connected between terminals XIN and XOUT. In this mode the crystal used must be 5.12 MHz. (CLKSEL=LOW).
2. External square wave frequency with a standard CMOS logic level input applied to terminal XIN. (CLKSEL=LOW).
3. External TCXO sine wave with an amplitude at least 0.5 V peak-to-peak applied to terminal TCXO (CLKSEL=HIGH).

When the CLKSEL terminal is high in mode 3, an external TCXO is selected. When CLKSEL is low, then the clock source is the internal crystal oscillator when a crystal is connected between terminals XIN and XOUT in mode 1 or when an external squarewave frequency is applied to terminal XIN in mode 2.

In modes 2 and 3, any of the frequencies in Table 1 can be used.

When the device is being tested, mode 2 is used with a 10 MHz, full CMOS logic-level external clock.

The state of the CLKSEL terminal is also used to route either the TCXO frequency signal source (CLKSEL=1) or the internal oscillator/external squarewave frequency signal source (CLKSEL=0) through a divide-by-two counter to the CLKOUT terminal. Bit 3 of (CLKOUTSEL) is used to place the CLKOUT terminal in a Hi-Z state when an external clock is not needed.

When modes 1 or 2 are used as the master clock for the TCM8030 using an internal crystal oscillator or external square wave source, the AFC circuit functions with the TCXO operating at any frequency less than 20 MHz. When mode 3 is used as the master clock for the TCM8030, the external TCXO frequency must be one of the frequencies associated with CKRT(bits 0–2) as shown in Table 1.

Frequency divider circuits derive the internal clocks, 2.56 MHz to the data processor and 1.28 MHz, and 320 kHz, 160 kHz, and 10 kHz to the audio processor.

The internal oscillator XTALOSC, TXCO input clock recovery circuit TCXOAMP, and internal dividers, PROGDIV share their own dedicated power supply terminals so the amount of crosstalk from the rest of the circuit (and hence the clock jitter) is minimized.

All the clock circuits are powered down in the TCM8030 total power-down mode, but in all other modes, the clock output on CLKOUT is active when CLKOUTSEL is 0.

The first 3 bits of the CLKSRC register specifiy the master clock input or crystal frequency, and bit 3 of CLKSRC controls the output of a clock signal on CLKOUT, as shown in Table 1.

PRINCIPLES OF OPERATION

OSC and PROG DIVID (continued)

Table 1. Master Clock Input Frequency and CLKOUT Select

BIT 2 CKRT2	BIT 1 CKRT1	BIT 0 CKRT0	BIT 3 CLKOUTSEL	FREQUENCY SELECTED	TERMINAL CLKOUT
0	0	0	X	5.12 MHz†	X
0	0	1	X	7.68 MHz	X
0	1	0	X	10.24 MHz	X
0	1	1	X	12.8 MHz	X
1	0	0	X	15.36 MHz	X
1	0	1	X	17.92 MHz	X
1	1	0	X	‡	X
1	1	1	X	‡	X
X	X	X	0	X	Active
X	X	X	1	X	Hi-Z

† When using the internal crystal oscillator, 5.12 MHz must be selected and a 5.12 MHz crystal must be connected between terminals XIN and XOUT.
‡ CKRT(bits 0–2) = 110 and 111 not allowed.

The clocking scheme is summarized in Figure 19.

PRINCIPLES OF OPERATION

OSC and PROG DIVID (continued)

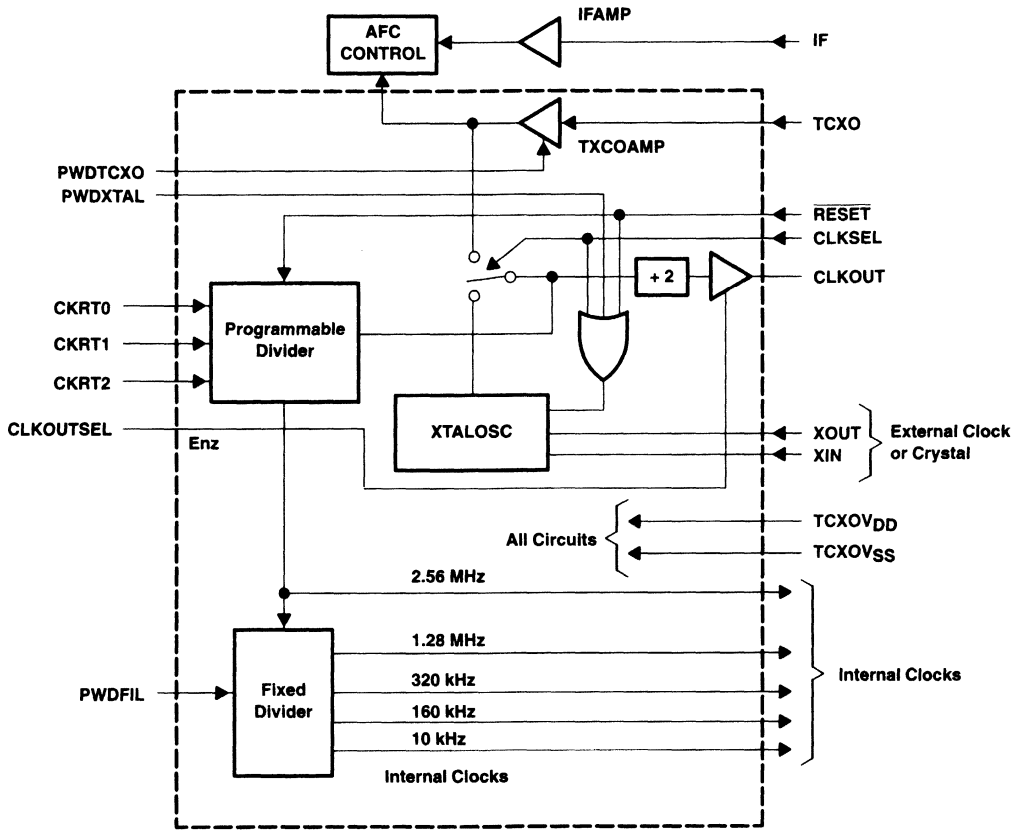


Figure 19. TCM8030 Clocking Scheme Functional Block Diagram

PRODUCT PREVIEW

PRINCIPLES OF OPERATION

POWER MODES

The power off logic circuitry implements six modes in which various functions of the TCM8030 are powered off. These modes are selected by control word 4. In power-down mode, all internal circuits, including the crystal oscillator (XTALOSC) are disabled.

total power-down mode

In this mode, power is still applied to the TCM8030 but, the device is in total power-down mode. All circuits including clock, bias circuits, PIOs, and the watchdog timer are powered down and the TCM8030 is stopped so it draws only minimal-leakage current. The EXTPWR output terminal is low to disable the power supply to the rest of the telephone (including the MCU). The $\overline{\text{EXTRST}}$ terminal also is active-low during total power-down mode and the TCM8030 microcontroller interface is disabled.

It is intended that the TCM8030 be the only device in the telephone with its power supply enabled in this mode. Static power-up logic implemented using one of the keyboard interrupt ports waits for the power-on key to be pressed. After the power-on key is pressed, the TCM8030 exits total power-down mode, reactivates the oscillator, enables the regulators to the rest of the telephone (using the EXTPWR enable signal), and holds $\overline{\text{EXTRST}}$ terminal low for 0.1 to 0.2 seconds to allow the rest of the telephone to power up reset when the system is stable.

The TCM8030 is placed in total-power-down mode by writing 02 hexadecimal to C4(bits4:0). (Both of the bits C4 (bits 1–0) must be toggled with this write). The security bit, C4.1, reduces the probability that the total power-down mode is entered erroneously, for example, by RFI (radio frequency interference).

The independent analog circuits IFAMP, AMP7, and DAC1-3 are also powered down in total power-down mode independently of the status of their own power-down control bits in register AUXPE (write address 30).

The total power-down mode is used in the cellular telephone system from the first connection of the battery as follows:

1. Power is applied for the first time when the battery is connected. Only the TCM8030 has its power supply connected initially and powers up in shutdown mode, enabling its clock, such as XTALOSC, when selected by CLKSEL terminal and immediately setting the EXTPWR high.
2. The powerup clear to TCM8030 ($\overline{\text{RESET}}$ input) is held low (active) during the operation of the external power-on-reset (RC) circuit. This causes $\overline{\text{EXTRST}}$ to also be low (active).
3. When the external power-on-reset is complete, the TCM8030 MCU interface is enabled and the MCU starts its boot routine. Because TCM8030 INTRPT terminal is not set to 1, the MCU knows that it was reset by a powerup from a battery connect. (In this situation the telephone should appear to be OFF until the power-on key is pressed.) The MCU then writes to the TCM8030 to:
   - Enable a keypad interrupt on the appropriate key terminal. This requires four writes to TCM8030 registers:
     - PI3INT (write address 1C) to enable the terminal interrupt
     - PI3PULL (write address 1B) to enable or disable the pullup as required
     - PIOC3 (write address 19) to set direction as input
     - IE2 (write address 06) to enable interrupts from the PIO3 and keypad port
   - Set the C4 (bits 4–0) to 01h to enter total power down mode

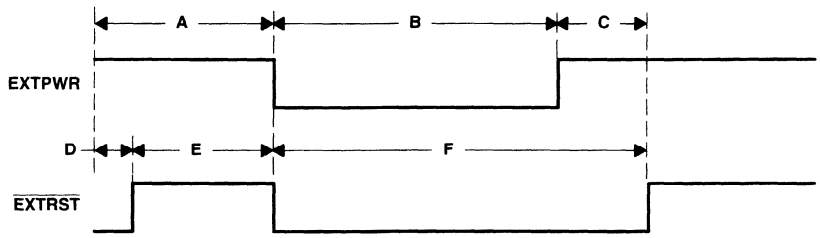
PRINCIPLES OF OPERATION

total power-down mode (continued)

The MCU must first enable the keypad port terminal connected to the power-on key before entering total power-down mode. If this is not done, only $\overline{\text{RESET}}$ to the TCM8030 reenables it.

4. At this point the clock stops, EXTPWR goes low (inactive), $\overline{\text{EXTRST}}$ goes active low, and the MCU and other parts of the system power off, waiting for the power-on key to be pressed.
5. The user presses the power-on key and this is sensed on one of the KEY inputs. Asynchronous logic, which does not need the clock, reads the power-on key and forces the TCM8030 back into shutdown mode and turns EXTPWR back on. The TCM8030 event register also records the fact that a keypad interrupt has been received.
6. EXTPWR going high powers up the microcontroller and after a timed interval of between 0.1 second and 0.2 second plus the XTALOSC warm-up time, $\overline{\text{EXTRST}}$ is released, allowing the rest of the system to power up reset when the system is stable. The MCU then executes its boot routine.
7. At this time the INTRPT terminal from the TCM8030 is active and the the microcontroller checks the TCM8030 event register and finds that it has been awakened by a keypad event, such as the power-on key was pressed. This means that the microcontroller starts initializing the entire system appropriately.

Figure 20 summarizes the TCM8030 power sequence.



NOTES: A. A battery is connected and power is applied the first time. (TCM8030 powers up in shutdown mode.)
B. The TCM8030 is waiting for power key to be pressed.
C. The microcontroller powers up and $\overline{\text{EXTRST}}$ is released after 0.1 to 0.2 second delay (plus XTALOSC warmup time).
D. $\overline{\text{RESET}}$ low during the power up-reset mode.
E. Power-up reset cycle starts, and microcontroller enables keypad interrupts. TCM8030 enters the total power-down mode.
F. A keypad sense power-on event, such as the power-on key, is pressed. EXTPWR is re-enabled, after 0.1 to 0.2 seconds timer times out (plus XTALOSC the warm up time).

Figure 20. Summary of TCM8030 Power-Up Events

shutdown mode

The microcontroller interface, all three PIOs, clock, bias circuits, and the watchdog timer blocks remain operational in the shutdown mode. The shutdown mode can be used, when the telephone is switched on but is not able to receive calls, for example, while the battery is being recharged. The microcontroller interface may be used to access all internal registers during shutdown mode, but the microcontroller can not issue commands for addresses 08h to 0Eh.

PRINCIPLES OF OPERATION

idle mode

In addition to the circuits that are operational in shutdown mode, the wide-band receive data path is enabled in this mode. This corresponds to the telephone being in idle mode, on a forward control channel (FOCC). Two submodes are also implemented within the idle mode to further minimize power consumption within the telephone. First, the MCU idle submode (see description for register E2 in read address map – read address 06, Table 39) enables the MCU to go to sleep when no new messages are received, and the RXRF idle submode (see description for register RXRFTIM in write address map – write address 20, Table 2 in detailed description — Write Address Map) allows the RF receiver to be powered down when it is not needed.

tone mode

In addition to the circuits in shutdown mode, the DTMF generator, and the section of the RX audio path following the CTI input are powered up in this mode. This mode can be used when the telephone is powered up and the user interface, such as the key pad and user memories, is enabled but the telephone is not in communication with the base station.

full operation mode, (DTMF TX off)

All circuits except the DTMF generator are on. This mode corresponds to a telephone conversation in progress.

full operation mode, (DTMF TX on)

All circuits are on. This mode is enabled for a DTMF tone to be transmitted during a telephone conversation.

miscellaneous functions

There are several circuits within the TCM8030 that perform specific functions given in Figure 14. These circuits are listed below along with a brief functional description.

TXVMID and RXVMID

The TXVMID and RXVMID functional blocks are separate receive and transmit analog reference voltage generators. The circuits contain resistive dividers fed from analog voltage supplies. The outputs are buffered and then decoupled externally to provide an accurate, quiet, mid-rail reference for internal audio circuits.

AFC

The AFC (automatic frequency controller) circuit receives one input from an external TCXO (temperature-compensated oscillator) and another input from the receiver second IF (intermediate frequency) stage. The counters in this block then process the inputs and provide a count that can be read using the microcontroller interface.

DAC 1 – 3

The DACs 1 – 3 are each 8-bit linear digital-to-analog converters.

AMP7

AMP 7 is an uncommitted operational amplifier.

DTMF GEN

The dual-tone multifrequency generator (DTMF GEN) circuit generates the tones for pushbutton dialing and provides the user-alert tone.

TIMER

The timer circuit is a programmable 8-bit count-down timer. The timer can either countdown once or cycle continuously. When the count reaches zero, the output changes state.

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WATCHDOG TIMER

The watchdog timer circuit is started by a write to a location in the microcontroller interface. If the location is not written to again within the timeout period, the watchdog timer times out and its output changes state. This change in output resets the telephone microcontroller.

PIO PORT 1 AND PIO PORT 2

PIO port 1 and PIO port 2 are two 8-bit wide programmable ports. Each line of each port can be individually programmed to be either an input or an output.

KEYBOARD SCAN

The KEYBOARD SCAN port is a 4-bit port that accepts inputs from a keyboard and generates interrupts to the microcontroller. The port can also be reconfigured as a general purpose I/O (input/output) port. One I/O terminals connected to the telephone ON/OFF key supplies a wakeup signal that terminates the total power-down mode.

MICRO CONTRL I/F and INTRPT LOGIC

All wide-band and narrow-band data communications are transmitted to and received from the telephone microcontroller using the microcontroller interface (MICRO CONTRL I/F) circuitry. Internal data, command, and interrupt registers are programmed using write operations. Other internal data, status, and interrupt registers are monitored using read operations.

microcontroller interface operation

Sampling of input data occurs on the rising edge of DCLK, and changes in output data occur on the falling edge. DCLK may begin and end in either the high or low state. Operation of the microcontroller interface may be achieved in software using the microcontroller general purpose I/O terminals. Alternatively, it may be noted that the timing diagram, shown in Figure 21, is compatible with a 2-byte transfer using a peripheral having an SPI (serial peripheral interface) when operating in CPOL = 1 and CPHA = 1 modes. This timing is also compatible with clock-synchronous transfers from the general-purpose 8-bit UART (universal asynchronous receiver-transmitter), when an additional microcontroller I/O port is used to generate the $\overline{CS}$ signal. In the latter case, the duration of the eighth clock pulse shown can be increased, so that two consecutive 8-bit writes can be used for a TCM8030 write operation, or a consecutive 8-bit write and an 8-bit read can be used for a TCM8030 read operation.

The DATAOUT terminal has a 3-state driver and normally presents a high impedance, as indicated in Figure 2. This allows the both the DATAIN and the DATAOUT pins to be connected to a bidirectional microcontroller pin.

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write

For a write operation, the $\overline{CS}$ input is taken low and data on DATAIN is clocked into the TCM8030 on each rising edge of DCLK, Figure 21. The input sequence is start bit (logic 1), 7-bit address, and then eight bits of data.

The address and data to be written to control the TCM8030 and to transmit Manchester-encoded signals are detailed in the write address map given in Table 2. Eight bits of data are always written to the interface and the data is right justified.

For those write operations to addresses that have less than eight significant data bits, it is necessary to supply the full complement of eight data clock cycles on DCLK, although the state of DATAIN during these nonsignificant write data clock cycles is not important.

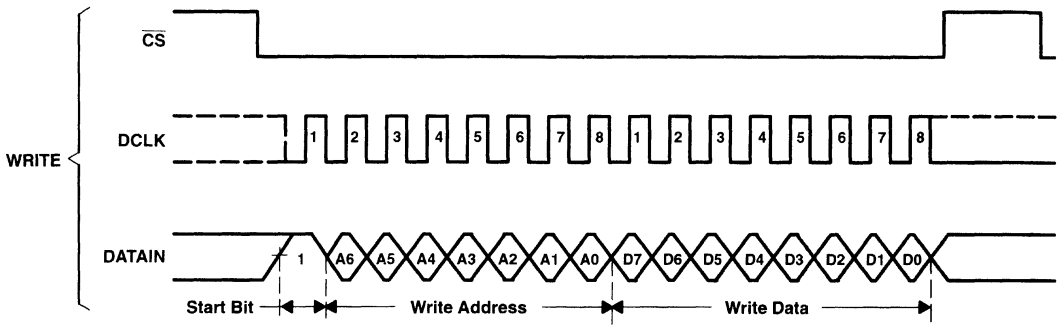

Figure 21. Microcontroller Interface Write Timing Diagram

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detailed description — write address map

Table 2. Write Address Map

HEXADECIMAL ADDRESS (7 BITS)	NAME	REGISTER NAME	FUNCTION	NO. OF SIGNIFICANT BITS	DEFAULT VALUE (HEX)
00	Control word 1	C1	Operational control word	8	00
01	Control word 2	C2	DCC/SAT/DSAT control word	7	00
02	Control word 3	C3	Signal polarity selection	4	0
03	Control word 4	C4	Master power-enables	5	1
04	Control word 5	C5	FOCC/FVC optional modes	4	0
05	Interrupt control word 1	IE1	Interrupt enables	7	00
06	Interrupt control word 2	IE2	Interrupt enables	8	00
07	Not used				
08	Commence TX	TXSTART	Commence TX command	0	–
09	Start watchdog	WDSTART	Start/Restart watchdog	0	–
0A	Abort TX	TXABORT	Abort TX command	0	–
0B	Clear TX buffer	TXCLEAR	Clear TX buffer command	0	–
0C	Restart frame sync	FRAMESYNC	Restarted frame sync command	0	–
0D	Reset	RST	Reset chip command	0	–
0E	Reset arbitration	ARBITRST	Reset arbitration	0	–
0F	Not used				
10	TX data word 0	TXD0	TX data bits 35 – 28	8	00
11	TX data word 1	TXD1	TX data bits 27 – 20	8	00
12	TX data word 2	TXD2	TX data bits 19 – 12	8	00
13	TX data word 3	TXD3	TX data bits 11 – 4	8	00
14	TX data word 4	TXD4	TX data bits 3 – 0 (LSBs)	4	0
15	PIO1 control word	PIOC1	PIO1 direction selection	8	00
16	PIO1 output word	PO1	PIO1 values for outputs	8	00
17	PIO2 control word	PIOC2	PIO2 direction selection	8	00
18	PIO2 output word	PO2	PIO2 values for outputs	8	00
19	PIO3 control word	PIOC3	PIO3 direction selection	4	0
1A	PIO3 output word	PO3	PIO3 values for outputs	4	0
1B	PIO3 pullup control	PI3PULL	PIO3 input pullup enable	4	F

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Table 2. Write Address Map (continued)

HEXADECIMAL ADDRESS (7 BITS)	NAME	REGISTER NAME	FUNCTION	NO. OF SIGNIFICANT BITS	DEFAULT VALUE (HEX)
1C	PIO3 interrupt control	PI3INT	Enable event monitoring on PI3, set sense of input	8	00
1D – 1F	Not used				
20	RXRF idle mode timer	RXRFTIM	RXRFTIM, RF power-saving duration	6	2B
21	Counter / timer coef.	TIMER	Coefficient and start command	8	00
22	Mismatch	FRAMEMIS	Frame mismatch coefficient — wide-band	3	05
23	FOCC dotting	FCCDOT	Detect coefficient — wide-band	4	07
24	FVC dotting	FVCDOT	Detect coefficient — wide-band	7	1D
25	Narrow band error coef.	NBCOEF	Allowed narrow-band errors	7	00
26	SAT coef.	SATCOEF	SAT lock determination — wide-band	6	3F
27 – 2D	Not used				
2E	Dataprocessor test control 1	DTEST1	Dataprocessor test control	1	0
30	Auxiliary power enables	AUXPE	Power enables DACs, IFAMP, AMP7 and LSDRIVER	6	00
31	Clock source frequency select	CLKSRC	Frequency of external clock source, and CLKOUT 3-state enable	4	08
32	Receive audio path config	RXCFG	Receive audio path switch settings	8	00
33	Transmit audio path config	TXCFG	Transmit audio path switch settings	6	00
34	Microphone and TX DTMF trim	VDTRIM	Voice and DTMF trim gain setting	4	08
35	Limiter trim	LIMITER	Limiter gain setting	4	0A
36	Transmit SAT trim	SATTRIM	Transmit SAT trim gain setting	4	08
37	Transmit data trim	TXDATRIM	Transmit Data trim gain setting	3	04
38	Transmit trim	TXTRIM	Final TX trim gain setting	5	10
39	Receive trim	RXTRIM	Receive trim gain setting	4	08
3A	Volume control	VOLCTRL	Loudspeaker volume control	4	08
3B	DTMF control	DTMFCTRL	DTMF frequency setting	7	3F
3C	Analog test modes	ATEST	Analog test mode control	4	0
3D – 3F	Not used				
40	DAC range select	DACRANGE	DAC range setting	3	0
41	DAC1 data	DAC1DAT	DAC1 input data code	8	0
42	DAC2 data	DAC2DAT	DAC2 input data code	8	0
43	DAC3 data	DAC3DAT	DAC3 input data code	8	0
44	AFC control	AFCCTRL	AFC control	5	00

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detailed description — write address map (continued)

In the following description for write address registers, a bit position within a register is identified by prefixing the bit number with its register name. For example, bit 6 of control word 1 in write address 00 is identified as C1.6.

address 00 — operational control word 1 (C1)

Control word C1 is composed of eight bits. When a C1 bit is set to 1, the functions shown in Table 3 are performed (function performed when bit is reset to 0).

Table 3. Control Word 1 (C1) Definition

BIT	FUNCTION
0	AMPS/(TACS)
1	Narrow-band mode/(wide-band mode)
2	Voice channel operation (RVC)/(Control channel operation RECC)
3	Receive FOCC B-word/(receive FOCC A-word)
4	Enable automatic arbitration logic. RXRFEN goes low, TXOUT is disabled on arbitration fail.
5	Enable SATOUT output — wide-band Enable DSAT/DST output — narrow-band
6	Enable Signaling Tone (ST) generation — wide-band Enable Digital Signaling Tone (DST) generation — narrow-band
7	Timer continuously cycles/(stops when it reaches 00 count)

transmit mode operation

Bits C1.1, C1.2, C1.5 and C1.6 of operational control word 1 (C1) in write address 00, together with the control word TXSUM control bits TXVEN, TXDEN, and TXSEN (write address 33), control the transmit mode of the TCM8030 as shown in Table 4. No other combination of these control bits should be used.

Table 4. Transmit Signal Selection

TXCFG.3 (TXVEN)	TXCFG.4 (TXDEN)	TXCFG.5 (TXSEN)	C1.1 (NB not WB)	C1.2 (RVC not RECC)	C1.5 (SAT/ DSAT	C1.6 (ST/DST)	TRANSMITTED SIGNAL AT TXO TERMINAL
0	0	0	X	X	X	X	Transmitter muted at TXSUM
0	1	0	X	0	X	X	Wide-band data on RECC
1	1	0	0	1	0	0	Wide-band data on RVC
1	1	0	0	1	0	1	ST and voice on RVC mixed together at TXSUM
1	0	1	0	1	1	0	SAT and voice on RVC mixed together at TXSUM
1	1	1	0	1	1	1	ST and SAT and voice on RVC mixed together at TXSUM
1	0	0	1	1	0	0	Narrow-band data and voice on RVC mixed together at TXSUM
1	0	0	1	1	1	1	DST and voice on RVC mixed together at TXSUM
1	0	0	1	1	1	0	DSAT and voice on RVC mixed together at TXSUM

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arbitration

Table 5 defines how arbitration is controlled and how the RXRFEN terminal is used

Table 5. Operational Control Word 1, Bit 4 Definition C1.4

C1.4 (write addr 00)	ARBITRATION	RXRFEN TERMINAL
0	Software controlled Arbitration failure indicated by event bit E1.2 (read address 05) and status bit S1.2 (read address 00)	Always inactive — sense set by C3.2 (write address 02)
1	Hardware controlled (RF amplifier directly switched off using TXRFEN terminal and TXOUT disabled on arbitration failure. Also arbitration failure still indicated by event bit E1.2 (read address 05) and status bit S1.2 (read address 00))	Used for arbitration circuit. Terminal goes active on arbitration failure. Only returns high after Reset Arbitration command — sense set by C3.2 (write address 02)

address 01 — DCC/SAT/DSAT Control Word (C2)

Control word C2 is seven bits wide. When a C2 bit is set to 1, the functions shown in Table 6 are performed.

Table 6. Control Word 2 (C2) Definition

BIT	FUNCTION
0	Digital color code 1st bit (DCC)
1	Digital color code 2nd bit (DCC)
2	SAT color code 1st bit (SCC) — wide-band
3	SAT color code 2nd bit (SCC) — wide-band
4	DSAT color code 1st bit (DSCC) — narrow-band
5	DSAT color code 2nd bit (DSCC) — narrow-band
6	DSAT color code 3rd bit (DSCC) — narrow-band
7	Not used

digital color codes (DCC)

The DCC control bits result in the sequences shown in Table 7 being included in the transmitted RECC message.

Table 7. Digital Color Codes — narrow-band

CONTROL WORD 2		TRANSMITTED CODE
BIT 1	BIT 0	
0	0	0000000
0	1	0011111
1	0	1100011
1	1	1111100

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SAT and DSAT circuit operation

SAT reception — wide-band

A digital phase-locked loop locks onto the received SAT signal when it is in the frequency band corresponding to the SAT color code (SCC) bits as shown in Table 8.

Table 8. SAT Color Codes — Wide-band

CONTROL WORD 2		SAT FREQUENCY BAND
BIT 3	BIT 2	
0	0	5955 Hz < f < 5985 Hz
0	1	5985 Hz < f < 6015 Hz
1	0	6015 Hz < f < 6045 Hz
1	1	Transmit test

When the input frequency is not in the expected band, the invalid SAT status flag, S1.6 (read address 00) is set. Note that the SAT status flag is high when the SAT circuit is initialized. Initialization occurs when entering wide-band voice channel mode and also when control word 2 is rewritten; however, the phase of the regenerated SAT is not disturbed.

The associated event flag E1.6 (read address 05) is set when the SAT status changes from valid to invalid, when it changes from invalid to valid, and also on the first SAT evaluation after initialization. This event generates an interrupt if the mask bit IE1.6 (write address 05) is set.

SAT lock status is evaluated over a 0.1 second interval to avoid the occurrence when the reference and input signals are only temporarily in phase. A programmable coefficient, SATCOEF in write address 26, controls the evaluation of lock status.

SAT transmission — wide-band

The SAT circuit always generates a valid SAT within the band defined by the written SCC, independently of the received signal. The microcontroller must turn off the SAT by resetting bit = 0 of C1.5 (write address 00), after a lost SAT event occurs. The exact SAT frequency transmitted depends on the state of the SAT comparator output:

1. When a SAT is received that is outside the the SCC band, the transmitted SAT is within ±15 Hz of the center frequency of the band. It is not steady. Typically it alternates between +15 Hz and –15 Hz.
2. When no SAT signal is received at all and the SAT comparator output is at logic 0, the transmitted SAT is within the range ±1 Hz of the SCC center frequency. This situation is detected and the invalid SAT flag is set high.

Because a valid SAT within the SCC band is always transmitted, all three SAT frequencies can be generated during the production test of the telephone simply by writing the correct bits in C2.2+3 SCC as shown in Table 8. When there is no received signal, the SAT output is within ±1 Hz of the SCC center frequency. In addition, when SCC is set to 11, a 6-kHz test frequency is generated that is unaffected by any received signal and does not attempt to lock onto it.

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DSAT reception — narrow-band

In narrow-band mode (C1.1 = 1, write address 00) the received signal is continuously compared with the DSAT word corresponding to the DSAT Color Code (DSCC) bits as shown in Table 9.

Table 9. DSAT Color Codes — Narrow-band

CONTROL WORD 2			DSAT WORD
BIT 6	BIT 5	BIT 4	
0	0	0	2556CB
0	0	1	255B2B
0	1	0	256A9B
0	1	1	25AD4D
1	0	0	26AB2B
1	0	1	26B2AD
1	1	0	2969AB
1	1	1	AAAAAA

A DSAT word is regarded as correctly detected and the receiver is locked onto the voice channel when the number of errors is less than or equal to that written to the NBCOEF register (write address 25). When the DSAT is not detected, the invalid DSAT status flag, S1.6 read address 00, is set to 1. The DSAT status flag is high when the DSAT circuit is initialized. The DSAT circuit is initialized after entering narrow-band mode and also whenever C2 is written. The associated event flag E1.6 (read address 05) is set whenever the status has changed from valid to invalid or from invalid to valid, and also after the first evaluation, which takes place 0.12 seconds after the circuit is initialized. This event generates an interrupt when the mask bit IE1.6 (write address 05) has been set.

The base station stops DSAT transmission when data is transmitted. The effect of this on DSAT determination is discussed in topic MRI (mobile-reported interference) operation and read address 25 narrow-band error rate (NBERRS).

DSAT transmission — narrow-band

The DSAT circuit always generates the DSAT corresponding to the DSCC, independently of the received DSAT. It is up to the microcontroller to turn the DSAT off by writing 0 to C1.5 (write address 00) after a lost DSAT event occurs.

Control bit C1.6 (write address 00) determines whether DSAT or DST is output. When this bit is set high, DST is generated instead of DSAT. DST is simply the inverted DSAT. The transition from DSAT to DST and vice-versa only takes place at specific places in the code sequence, as defined by the NAMPS/NTACS specifications. The switching point is handled automatically.

During the production test of the telephone, all DSATs can be transmitted even when no DSAT is received.

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address 02 — signal polarity selection (C3)

The signal polarity selection control word (C3) is four bits wide. The functions when bit positions are set high or low are shown in Table 10.

Table 10. Signal Polarity Selection Control Word (C3) Definition

BIT	FUNCTION
0	When cleared 0, = normal logic: RXIN data zero = logic low, RXIN data one = logic high When set to 1, = inverted logic: RXIN data zero = logic high, RXIN data one = logic low
1	When cleared 0, = normal logic: TXO data zero = logic low, TXO data one = logic high When set to 1, = inverted logic: TXO data zero = logic high, TXO data one = logic low
2	When cleared 0, = TXRFEN and RXRFEN are active high (high = arbitration failure/RXRF idle mode active)† When set to 1, = TXRFEN and RXRFEN are active low (low = arbitration failure/RXRF idle mode active)†
3	When cleared 0, = INTRPT is active high (high = interrupt valid) When set to 1, = INTRPT is active low (low =interrupt valid)
4–7	Not used

† TXRFEN and RXRFEN have open-drain output drivers. These terminals have active pulldowns, and require external pullups.

address 03 — master power enables (C4)

This register controls the operation of the different power modes as shown in Table 11. When a bit in this register is set to 1, a section of the TCM8030 is powered up. After a $\overline{\text{RESET}}$, only bit 0 is enabled so that the device is initially in shutdown mode. To disable sections of the TCM8030, a 0 is written to the appropriate bit.

Table 11. Master Power Enables (C4) Definition

BIT	FUNCTION
0	Power up of CLOCK (TCXOAMP, XTALOSC and PROGDIV). When clock is powered down (0 in this bit), all circuits in the data processor and PIO ports are also off. Only the keypad port remains active to receive an external power key-press. Reset state is 1 so that the TCM8030 powers up in shutdown mode.
1	Security bit. Reset to 0. It must always be the inverse of C4.0 and must be set to 1 at same time as C4.0 is reset to 0 to enter total power-down mode.
2	FOCC data reception enabled. Reset to 0.
3	DTMF generator and DTMF receive path enabled. Reset to 0.
4	Transmission circuits for speech, data, SAT/DSAT, and ST/DST, and receive circuit for speech enabled, reset to 0.
5–7	Not used

TCM8030 power modes

The following bits should be written to register C4 to specify one of the six TCM8030 power modes as shown in Table 12.

Table 12. Power Modes (C4) Definition

C4.4	C4.3	C4.2	C4.1	C4.0	POWER MODE
0	0	0	1	0	Total power-down mode
0	0	0	0	1	Shutdown mode
0	0	1	0	1	Idle mode
0	1	0	0	1	Tone mode
1	0	1	0	1	Full operation mode, DTMF TX off
1	1	1	0	1	Full operation mode, DTMF TX on

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independent circuits

The IFAMP, DACs 1 – 3, and AMP7 blocks can be individually powered down as described for the auxiliary power enable (AUXPE) register (write address 30). These bits are overidden and all circuits powered down in total power-down mode.

address 04 — FOCC/FVC optional controls (C5)

The FOCC/FVC operational control word C5 is four bits wide. The function of each bit depends on its value (0 or 1) as shown in Table 13.

Table 13. Operational Control Word 5 (C5) Definition

BIT	FUNCTION
0	0 = One busy/idle bit examined to detect busy/idle status 1 = Two busy/idle bits examined to detect busy/idle status
1	0 = Maximum of eleven FVC word repeats used — wide-band 1 = Maximum of five FVC word repeats used — wide-band
2	0 = Auto muting is enabled when transmitting and receiving a message on voice channel — wide-band 1 = Auto muting is disabled when transmitting and receiving a message on voice channel — wide-band
3	0 = RXRF idle mode disabled 1 = RXRF idle mode enabled
4–7	Not used

address 05 — interrupt control word 1 (IE1)

The interrupt control word 1 (IE1) is seven bits wide. The function of each bit when set to 1 is as shown in Table 14.

Table 14. Interrupt Control Word 1 (IE1) Definition

BIT	FUNCTION
0	RX data available
1	TX buffer available
2	Arbitration failure
3	TX sequence completed
4	Change of RECC busy/idle status
5	Counter/timer reaches zero state
6	Wide-band SAT/narrow-band DSAT status changed
7	Not used

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address 06 — interrupt control word 2 (IE2)

The interrupt control word 2 (IE2) is eight bits wide. The function of each bit when set to 1 is shown in Table 15.

Table 15. Interrupt Control Word 2 (IE2) Definition

BIT	FUNCTION
0	FOCC data changed, (different from previously received word)
1	FVC dotting detected — wide-band
2	FVC frame sync achieved (wide-band word sync/narrow-band sync word received)
3	Change of FOCC frame sync status
4	Change of RXRF idle mode power-saving status
5	NRZ error count register (NBERRS) updated — narrow-band
6	PI03 input port signal sensed
7	AFC has reached terminal count

address 08 — commence TX (TXSTART)

A write operation (the data is not significant) to this address transfers data from the transmit buffer to the transmit encoder and starts the encoding and transmission of the data.

address 09 — start watchdog (WDSTART)

A write operation (the data is not significant) to this address starts one cycle of the watchdog timer. Unless restarted, the watchdog times out in 1.5 to 1.6 seconds. Timeout is indicated by the WDOUT output terminal going low for 100 ms. The TXRFEN terminal is also disabled until the next chip reset or WDSTART command occurs.

The WDSTART command should be given at intervals of 1.4 seconds or less.

address 0A — abort TX (TXABORT)

A write operation (the data is not significant) to this address immediately stops a transmission sequence that is in progress.

address 0B — clear TX buffer (TXCLEAR)

A write operation (the data is not significant) to this address clears the contents of the transmit buffer. This prevents the contents from being transmitted from the end of the transmission of a word that is currently in progress (known as following on).

address 0C — restart frame sync (FRAMESYNC)

A write operation (the data is not significant) resets the data recovery circuit to achieve bit synchronization to the received data. It can be used when the telephone switches to a new forward control channel (FOCC) to reduce the time taken to acquire bit synchronization. The data recovery circuit does not have to wait until it has detected loss of bit synchronization to change to fast-lock mode.

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address 0D — reset (RST)

A write operation (the data is not significant) to this address performs a chip reset. Its function is identical to that of the $\overline{\text{RESET}}$ input terminal, except that it does not affect the WDOUT terminal. The default values listed in the write address map are loaded.

address 0E — reset arbitration (ARBITRST)

A write operation (the data is not significant) to this address resets the arbitration circuit. After an arbitration failure, this command must be sent to re-enable the transmission of data.

address 10 — TX data word 0 (TXD0)

This register contains the transmitted data bits 35 to 28 (bit 35 is the MSB).

address 11 — TX data word 1 (TXD1)

This register contains the transmitted data bits 27 to 20 (bit 27 is the MSB).

address 12 — TX data word 2 (TXD2)

This register contains the transmitted data bits 19 to 12 (bit 19 is the MSB).

address 13 — TX data word 3 (TXD3)

This register contains the transmitted data bits 11 to 4 (bit 11 is the MSB).

address 14 — TX data word 4 (TXD4)

This register contains the transmitted transmit data word 4, bits 4–7 as shown in Table 16.

Table 16. Transmit Data Word 4 (TXD4) Definition

BIT	FUNCTION
3 – 0	Not used
4	TX data bit 0
5	TX data bit 1
6	TX data bit 2
7	TX data bit 3

The data to be transmitted is written to 5 addresses (10 – 14), and this loads the transmit buffer. Data word TXD4 is the least significant byte and should be written last.

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address 15,17,19 — PIO control words (PIOC1, PIOC2, PIOC3)

These control words select whether the individual terminals of the port are configured as inputs or used as outputs as shown in Table 17.

Table 17. PIO Control Words (PIO C1,2,3) Definition

VALUE	CORRESPONDING TERMINAL FUNCTION
0	Input
1	Output

The eight terminals (four for PIO3) of the port are configured as inputs by default.

address 16,18,1A — PIO output words (PO1, PO2, PO3)

This sets the state of the PIO terminals that are configured as outputs.

address 1B — PIO3 pullup enables (PI3PULL)

When set to 1, bits 0 to 3 of this register activate a small pullup transistor. The pullup allows the inputs to be driven by open-drain drivers. After reset, the ports are configured as inputs and the PIO3 pullups are enabled.

address 1C — PIO3 interrupt control (PI3INT)

Table 18. PIO3 Interrupt Control (PI3INT, bits 3–0) Definition

PI3INT BIT(0–3)	FUNCTION
0	PIO3 operates as normal port
1	Signal sensed on PI3INT causes interrupt when IE2.6 is high. (Note: The port may still be read at address 20 in this mode)

Table 19. PIO3 Interrupt Control (PI3INT bits 7–4) Definition

PI3INT BIT(4–7)	FUNCTION
0	Active low interrupt
1	Active high interrupt

address 20 — RXRF idle mode timer (RXRFTIM)

Writing to this 6-bit address sets the duration of RXRF idle (RF receiver powered down) mode. In RXRF idle mode, the RF receiver may be powered down for part of the FOCC data frame using the RXRFEN terminal. This should only be used in good signal conditions when multiple repeats of the word are not required.

The default value of 2Bh ensures that the receiver has five bit periods within which to power up before the start of the dotting sequence of the next frame. For AMPS, a bit period is 0.1 ms; for TACS, it is 0.125 ms. The timer is clocked at the bit rate divided by 8. For example, RFRXTIM = 2 A allows the receiver up to 15 additional 8-bit periods in which to stabilize before the start of dotting.

address 21 — counter / timer coef (TIMER)

Writing to this address sets the count length and starts the counter. The timer counts in units of 12.8 ms, giving a maximum time interval of 3.264 seconds (255 counts). A TMZERO terminal and status bit S1.5 indicate the timer status. When the timer is counting, TMZERO and S1.5 are low, but when the timer reaches zero, they go high and stay high until TIMER is written again unless C1.7 is high, to indicate recycling mode. In recycling mode, the timer automatically reloads the count coefficient and starts the count again so TMZERO and S1.5 is only low for 12.8 ms. In the recirculating mode, with timer set to 255, the output would be low for 255 counts and high for 1 count, giving an overall period of 256 counts.

The timer can be stopped either by a chip reset or by writing 00 to TIMER. This causes TMZERO signal and S1.5 to stay low. (Note that after sending the start command there is a latency of 12.8 ms before the timer is loaded.)

When IE1.5 (write address 05) is set, an interrupt is generated when the counter reaches zero.

address 22 — mismatch wide-band (FRAMEMIS)

This is the number of invalid wide-band word syncs that are allowed during data recovery on both FVC and FOCC before bit synchronization with the dotting pattern is restarted.

address 23 — FOCC dotting coefficient (FCCDOT) — wide-band

This is a coefficient for the data recovery circuit and sets how much of the dotting preamble of the FOCC data is required before it is accepted that bit synchronization has been achieved . It applies only to wide-band mode.

address 24 — FVC dotting coefficient (FVCDOT) — wide-band

This is a coefficient for the data recovery circuit and sets how much of the dotting preamble of the FVC data is required before it is accepted that bit synchronization has been achieved. It applies only to wide-band mode.

address 25 — allowed narrow-band errors (NBCOEF) — narrow-band

This register defines how many errors are allowed in the detection of the DSAT and SYNC words as shown in Table 20. When errors are received in a DSAT word that exceed the error threshold, the DSAT is assumed to be lost and the event bit E1.6 (change in DSAT status) is set. When a SYNC word is transmitted, but the number of errors exceeds the error threshold, then the SYNC word and the data following it are not recognized. Even when the SYNC word is correctly detected, a bad DSAT status is reported. This is cleared when 24 bits of DSAT have been received following the data word (up to 1.6 seconds from the time the DSAT went bad).

Table 20. Narrow-Band Error Coefficient Setting

BITS	FUNCTION	DEFAULT	MAXIMUM BIT ERRORS ALLOWED	MAXIMUM BIT ERRORS RECOMMENDED
0 – 3	DSATERRS	0	6	3
3	Not used	–	–	–
6 – 4	SYNCERRS	0	6	4
7	Not used	–	–	–

The two error coefficients are initialized to 0 on reset. They may be set to any value up to and including 6. It is recommended, however, that the DSAT and SYNC word-error thresholds do not exceed 3 and 4, respectively, as these values correspond to the maximum bit error rates documented in the NAMPS specification.

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address 26 — SAT lock determination (SATCOEF) — wide-band

The SAT PLL attempts to lock onto the incoming signal when it is a coherent signal within ±15 Hz of the SCC center frequency. SAT lock is determined over a 0.1-second interval, during which time there is approximately 600 cycles of the regenerated SAT. The input and output signals are compared, and when they are out-of-phase an error counter is incremented. When the counter reaches the value defined by SATCOEF (Table 21), an invalid SAT is indicated immediately on status bit S1.6 (read address 00). When the counter does not reach the threshold by the end of the 0.1-second period, a valid SAT is indicated.

When the received SAT is different from the SCC, lock cannot not be obtained. The input and reference signals beat in and out of phase. They are out of phase 50% of the time, so approximately 300 errors can be expected. The absence of a signal is also detected. The number of times that the input is held high or low for a whole cycle is counted, halved, and then added to the error counter.

To allow a safety margin, the error counter only goes up to the default error threshold of 255. It should not be necessary to lower the threshold; however, some programmability has been provided. The lower nibble of error threshold is hardwired to Fh and the upper nibble can be programmed using the SATCOEF register. It is also possible to enable/disable the counting of the two error types that have been discussed.

Table 21. SAT Lock Control Definition

SATCOEF BIT	FUNCTION	DEFAULT
0 – 3	Errors required to loose lock (ms nibble)	Fh
4	Phase error counting enabled	1
5	No-signal error counting enabled	1

address 2E — data processor test control 1 (DTEST1)

To facilitate production testing of the data processor, PIO ports 1 and 2 can be used to control and observe internal blocks. Port directions must be set as input and output respectively by writing to the direction control register PIO C1 and PIO C2 (write addresses 15 and 17).

To select a test mode, set the appropriate bit of the test register to 1 as defined in Table 22. When more than one test mode is selected, then control using PIO1 affects all test modes simultaneously, but data can be observed from one test mode only. The selected test mode that is the least significant bit of DTEST1 is the one that is observed on PIO2.

Table 22. TCM8030 Data Processor Test Modes

DTEST1 BIT	TEST MODE
0	Reserved
1	Reserved
2	Data Recovery Observation
3 – 7	Reserved

The detailed description of each test mode is shown in Table 23.

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Table 23. Data Recovery Observation (DTEST1.2 = 1)

PIO2 BIT	INFORMATION OBSERVED ON PIO2 OUTPUTS WHEN DTEST1.0 IS SET TO 1
0	NRZ narrow-band data and wide-band data before Manchester decoding. (e.g., Manchester-encoded 1 is seen as 0 followed by 1)
1	NRZ clock — 200 Hz (narrow-band); 16 kHz (TACS); 20 kHz (AMPS).
2	Decoded Manchester data. (e.g., 01 or 10 input sequences output as 1 or 0)
3	Clock — 100 Hz (narrow-band), 8 kHz (TACS), 10kHz (AMPS)
4 – 7	Reserved

address 30 — auxiliary power enables (AUXPE)

This register is used to independently enable (bit is set to 1) or power down (bit is set to 0) the DACs, AMP7 (uncommitted op amp), IFAMP, and LS DRIVER blocks as shown in Table 24.

Table 24. Auxiliary Power Enables (AUXPE) Definition

BIT	NAME	FUNCTION
0	DAC1EN	DAC1 enable
1	DAC2EN	DAC2 enable
2	DAC3EN	DAC3 enable
3	AMP7EN	AMP7 (uncommitted op amp enable)
4	IFAMPEN	IFAMP enable
5	LSDRIVEREN	LSDRIVER enable. The LS driver is powered off independently when both bits C4.3 and C4.4 are low (see write address 3). Differential or single-ended operation is selected by bit RXCFG.7, write address 32.

address 31 — clock source frequency select (CLKSRC)

The TCM8030 can be clocked from one of the following frequency sources selected by the first three bits in the CLKSRC register as shown in Table 25 (refer to Table 1 also).

Table 25. External Clock and Crystal Frequency Select

BIT	NAME	FREQUENCY
0	CKRT0	CKRT (bits 2–0) = 000: 5.12 MHz, 001: 7.68 MHz, 010: 10.24 MHz, 011: 12.80 MHz 100: 15.36 MHz, 101: 17.92 MHz, 110: not allowed, 111: not allowed
1	CKRT1	
2	CKRT2	
3	CLKOUTSEL	When cleared to 0 the CLKOUT terminal active; when set to 1: CLKOUT terminal = hi-Z

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address 32 — receive-audio path configuration (RXCFG)

The RXCFG register configures the receive audio path switches. The receive audio path is automuted at REC1SW during the reception of wide-band data on FVC when automuting is enabled with a 0 to C5.2 (write address 4) as shown in Table 26.

Table 26. Receive-Audio Path Configuration (RXCFG) Control

BIT	NAME	FUNCTION
0	EBSW	Expander bypass switch. 0 = Expander connected, 1 = Expander bypassed
1	REC1SW0	Receive path switch REC1SW = 00: Mute 11: forbidden 10: CTI input 01: Expander (or bypassed Expander) output
2	REC1SW1	
3	RECSUM	Side-tone switch and summing block (RECSUM) = 0: STI switched out 1: STI summed in
4	RECBUF0	REC1 and REC2 configuration (REC2SW) = 00: REC1 mute, REC2 mute 01: REC1 connected, REC2 mute 10: REC1 mute, REC2 connected 11: REC1 and REC2 differential
5	RECBUF1	
6	LSOPBIAS	Independent loudspeaker VMID output bias control on RECN and RECP terminals. 1 = RECN and RECP outputs are biased to VMID internally, 0 = RECN and RECP outputs must be biased externally. Note that in power-off mode, the LS output biases are automatically switched off.
7	DIFFSIGSEL	LSDRIVER differential/single-ended control 0: single-ended output (Only RECN output active, RECP output powered down), 1: RECN and RECP form differential outputs

address 33 — transmit-audio path configuration (TXCFG)

The TXCFG register is six bits wide and configures the transmit-audio path switches as shown in Table 27. The audio transmit path is automuted at the TXSUM functional block during the transmission of wide-band data on RVC, when automuting is enabled with a 0 written to C5.2 (write address 4).

Refer to Table 2 at write address 00 to configure different transmit modes using the last three bits in this register and the control bits in operational control word 1 (C1), write address 0.

Table 27. Transmit-Audio Path Configuration (TXCFG) Control

BIT	NAME	FUNCTION
0	TXSW0	TX audio source. TXSW = 11: DTI 10: AMP2 Select 01: AMP1 Select 00: Mute
1	TXSW1	
2	CBSW	Compressor bypass 0: Compressor connected 1: Compressor bypassed
3	TXVEN	TX voice enable at TXSUM, 0 = Mute, 1 = Enable
4	TXDEN	TX data enable at TXSUM, 0 = Mute, 1 = Enable
5	TXSEN	TX SAT enable at TXSUM, 0 = Mute, 1 = Enable

address 34 — microphone and TX DTMF trim (VDTRIM)

The VDTRIM register is four bits wide and sets the VDTRIM stage gain for microphone and/or TX DTMF level trim as shown in Table 28.

Table 28. Microphone and TXDTMF Trim (VDTRIM) Adjust

VD3	VD2	VD1	VD0	NOMINAL GAIN (dB)
0	0	0	0	−4.30
0	0	0	1	−3.74
0	0	1	0	−3.20
0	0	1	1	−2.65
0	1	0	0	−2.12
0	1	0	1	−1.58
0	1	1	0	−1.06
0	1	1	1	−0.53
1	0	0	0	0
1	0	0	1	0.53
1	0	1	0	1.05
1	0	1	1	1.58
1	1	0	0	2.12
1	1	0	1	2.65
1	1	1	0	3.14
1	1	1	1	3.74

address 35 — limiter trim (LIMITER)

The LIMITER register is four bits wide and sets the limiter deviation as shown in Table 29.

Table 29. Limiter Trim Adjust

LIM3	LIM2	LIM1	LIM0	DIFFERENCE FROM NOMINAL LIMIT LEVEL (dB)
0	0	0	0	−5
0	0	0	1	−4.5
0	0	1	0	−4
0	0	1	1	−3.5
0	1	0	0	−3
0	1	0	1	−2.5
0	1	1	0	−2
0	1	1	1	−1.5
1	0	0	0	−1
1	0	0	1	−0.5
1	0	1	0	0
1	0	1	1	0.5
1	1	0	0	1
1	1	0	1	1.5
1	1	1	0	2
1	1	1	1	2.5

address 36 — transmit SAT trim (SAT TRIM)

The SAT TRIM register is four bits wide and sets the SAT TRIM gain as shown in Table 30.

Table 30. Transmit SAT TRIM Adjust

SAT3	SAT2	SAT1	SAT0	NOMINAL GAIN (dB)
0	0	0	0	−2.28
0	0	0	1	−1.97
0	0	1	0	−1.67
0	0	1	1	−1.36
0	1	0	0	−1.06
0	1	0	1	−0.76
0	1	1	0	−0.45
0	1	1	1	−0.15
1	0	0	0	0.15
1	0	0	1	0.45
1	0	1	0	0.76
1	0	1	1	1.06
1	1	0	0	1.36
1	1	0	1	1.67
1	1	1	0	1.97
1	1	1	1	2.29

address 37 — transmit data trim (TXDATRIM)

The TXDATRIM register is three bits wide and sets the TX data trim levels as shown in Table 31.

Table 31. Transmit Data Trim (DXDATRIM) Adjust

DAT2	DAT1	DAT0	NOMINAL GAIN (dB)
0	0	0	−2.28
0	0	1	−1.82
0	1	0	−1.21
0	1	1	−0.6
1	0	0	0
1	0	1	0.6
1	1	0	1.21
1	1	1	1.82

address 38 — transmit trim (TXTRIM)

The TXTRIM register is five bits wide and sets the TXTRIM stage gain, the final stage in the TX path as shown in Table 32.

Table 32. Transmit Trim (TXTRIM) Adjust

TXT4	TXT3	TXT2	TXT1	TXT0	NOMINAL GAIN (dB)
0	0	0	0	0	−4.37
0	0	0	0	1	−4.08
0	0	0	1	0	−3.8
0	0	0	1	1	−3.5
0	0	1	0	0	−3.24
0	0	1	0	1	−2.97
0	0	1	1	0	−2.7
0	0	1	1	1	−2.42
0	1	0	0	0	−2.15
0	1	0	0	1	−1.88
0	1	0	1	0	−1.61
0	1	0	1	1	−1.34
0	1	1	0	0	−1.07
0	1	1	0	1	−0.8
0	1	1	1	0	−0.54
0	1	1	1	1	−0.27
1	0	0	0	0	0
1	0	0	0	1	0.27
1	0	0	1	0	0.53
1	0	0	1	1	0.8
1	0	1	0	0	1.07
1	0	1	0	1	1.34
1	0	1	1	0	1.61
1	0	1	1	1	1.88
1	1	0	0	0	2.15
1	1	0	0	1	2.42
1	1	0	1	0	2.69
1	1	0	1	1	2.97
1	1	1	0	0	3.24
1	1	1	0	1	3.52
1	1	1	1	0	3.8
1	1	1	1	1	4.08

address 39 — receive trim (RXTRIM)

The RXTRIM register is four bits wide and sets the RX TRIM stage gain as shown in Table 33.

Table 33. Receive Trim (RXTRIM) Adjust

RXT3	RXT2	RXT1	RXT0	NOMINAL GAIN (dB)
0	0	0	0	−4.3
0	0	0	1	−3.74
0	0	1	0	−3.2
0	0	1	1	−2.65
0	1	0	0	−2.12
0	1	0	1	−1.58
0	1	1	0	−1.06
0	1	1	1	−0.53
1	0	0	0	0
1	0	0	1	0.53
1	0	1	0	1.05
1	0	1	1	1.58
1	1	0	0	2.12
1	1	0	1	2.65
1	1	1	0	3.14
1	1	1	1	3.74

address 3A — loudspeaker volume control (VOL CTRL)

The VOL CTRL register is four bits wide and sets the loudspeaker volume as shown in Table 34.

Table 34. Loud Speaker Volume Control (VOL CTRL) Adjust

VOL3	VOL2	VOL1	VOL0	NOMINAL GAIN (dB)
0	0	0	0	−20
0	0	0	1	−17.5
0	0	1	0	−15
0	0	1	1	−12.5
0	1	0	0	−10
0	1	0	1	−7.5
0	1	1	0	−5
0	1	1	1	−2.5
1	0	0	0	0
1	0	0	1	2.5
1	0	1	0	5
1	0	1	1	7.5
1	1	0	0	10
1	1	0	1	12.5
1	1	1	0	15
1	1	1	1	17.5

address 3B — DTMF control (DTMFCTRL)

The DTMFCTRL register is six bits wide. Bits 0 through 4 select the DTMF generator output as shown in Table 35.

Table 35. DTMF Tone Output Control

KEY	DTMF4	DTMF3	DTMF2	DTMF1	DTMF0	LOW TONE (Hz)	HIGH TONE (Hz)
1	0	0	0	0	0	697	1209
2	0	0	0	0	1	697	1336
3	0	0	0	1	0	697	1477
4	0	0	0	1	1	770	1209
5	0	0	1	0	0	770	1336
6	0	0	1	0	1	770	1477
7	0	0	1	1	0	852	1209
8	0	0	1	1	1	852	1336
9	0	1	0	0	0	852	1477
*	0	1	0	0	1	941	1209
0	0	1	0	1	0	941	1336
#	0	1	0	1	1	941	1477
–	0	1	1	0	0	697	1150
–	0	1	1	0	1	770	1150
–	0	1	1	1	0	852	1150
–	0	1	1	1	1	941	1150
–	1	0	0	0	0	697	Off
–	1	0	0	0	1	770	Off
–	1	0	0	1	0	852	Off
–	1	0	0	1	1	941	Off
–	1	0	1	0	0	Off	1150
–	1	0	1	0	1	Off	1209
–	1	0	1	1	0	Off	1336
–	1	0	1	1	1	Off	1477
–	1	1	0	0	0	Off	1633
–	1	1	0	0	1	Off	2048
–	1	1	0	1	0	Off	Off
–	1	1	0	1	1	Off	Off
–	1	1	1	0	0	Off	Off
–	1	1	1	0	1	Off	Off
–	1	1	1	1	0	Off	Off
–	1	1	1	1	1	Off	Off

Bit 5 of the DTMF, control word 1 bits 0 and 1, selects DTMF mode control. The levels of the DTMF tones and a 2-dB level skew between the high tones and low tones is set according to the control bits as shown in Table 36.

Table 36. DTMF Mode Control

CONTROL WORD 1 (WRITE ADDR 0) BIT 0	CONTROL WORD 1 (WRITE ADDR 0) BIT 1	DTMF CONTROL WORD (WRITE ADDR 3B) BIT 5 MODCTRL	SYSTEM	SIGNAL LEVEL AT DTO (3 V SUPPLY) PER TONE	SIGNAL LEVEL AT DTO (3 V SUPPLY) BOTH TONES
TACS	WB	0	JTACS levels (skew off)	0.8 Vpp	1.6 Vpp
TACS	WB	1	ETACS levels (skew on)	0.756 Vpp low tones, 0.956 Vpp high tones	1.512 Vpp low tones, 1.912 Vpp high tones
TACS	NB	0	NTACS levels (skew off)	0.867 Vpp	1.734 Vpp
TACS	NB	1	Not allowed	–	–
AMPS	WB	0	AMPS levels (skew off)	1 Vpp	2 Vpp
AMPS	WB	1	Not allowed	–	–
AMPS	NB	0	NAMPS levels (skew off)	1 Vpp	2 Vpp
AMPS	NB	1	Not allowed	–	–

address 3C — analog test modes (ATEST)

To facilitate testing of the TCM8030, the REC1 and REC2 outputs can be reconfigured to observe internal analog signals. This register is reset to 0000 and should not be written to during normal operation.

address 40 — DAC range select (DACRANGE)

The DACRANGE register is three bits wide and sets the range of each DAC (address 41 – 43) as shown in Table 37.

Each DAC can be independently set to full or half range. For full range, the step size is TXVDD/256 and for half range the step size is TXVDD/512. Register AUXPE, at address 30, is used to independently power up or down each DAC. Each DAC has its own address to which the conversion word is written as described in the following paragraphs.

Table 37. DAC Range Select (DACRANGE) Definition

BIT	NAME	FUNCTION
0	DAC1X0	DAC1 range select. 0 = TXVDD/2, 1 = TXVDD
1	DAC2X1	DAC2 range select. 0 = TXVDD/2, 1 = TXVDD
2	DAC3X2	DAC3 range select. 0 = TXVDD/2, 1 = TXVDD

address 41 — DAC1 data (DAC1DAT)

Input data register for the first DAC (DAC1).

address 42 — DAC2 data (DAC2DAT)

Input data register for the second DAC (DAC2).

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address 43 — DAC3 data (DAC3DAT)

Input data register for the third DAC (DAC3).

address 44 — AFC control (AFCCTRL)

The AFCCTRL register is five bits wide. The first four bits set the AFC cycle and the fifth bit, AFCSTART, starts an AFC measurement cycle as shown in Table 38.

Table 38. AFC Control

BIT	NAME	FUNCTION
0	AFCTERM0	AFCTERM (bits 3–0) = 4 bits set terminal count of AFC cycle
1	AFCTERM1	
2	AFCTERM2	
3	AFCTERM3	
4	AFCSTART	AFC start/stop. When AFCST = 1: start AFC count, when AFCST = 0: stop AFC count.

The AFC measurement cycle begins when the AFCSTART bit (bit 4) is set. When the TCXO count reaches the terminal value set by the AFCTERM (bits 0–4) bits, the count is stopped, the AFC event bit E2.7 (read address 06) is set, and when the AFC interrupt mask bit IE2.7 (write address 06) has been set, an interrupt is generated. The microcontroller can then read the 20-bit terminal count of the IF–2 counter at AFCIF1, AFCIF2, and AFCIF3 (read addresses 43 to 45).

The start bit AFCSTART is reset automatically when the terminal value is reached. When AFCSTART is low the counter is stopped — not reset. Reading the terminal count when AFCSTART is low causes the counters to reset after the read of AFCIF3. Reading the counters when AFCSTART is high does not cause a reset, but the serial reading process means the data may not be reliable.

Note also that IFAMP must be powered-up with bit AUXPE.4 set (write address 30) before the AFC function can start.

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read

Figure 22 shows the microcontroller read timing diagram.

For a read operation, the start bit is bit 0. Following the seven address bits, the DATAOUT terminal is enabled and the output data is updated on each falling edge of DCLK. The DATAOUT terminal returns to a high impedance state when $\overline{CS}$ goes high. During the read operation, 8 bits of data are output on DATAOUT in the order bit 7 to bit 0. The address and meaning of the data read from the TCM8030 using the microcontroller interface is shown in the read address map (Table 39.) The data is right justified.

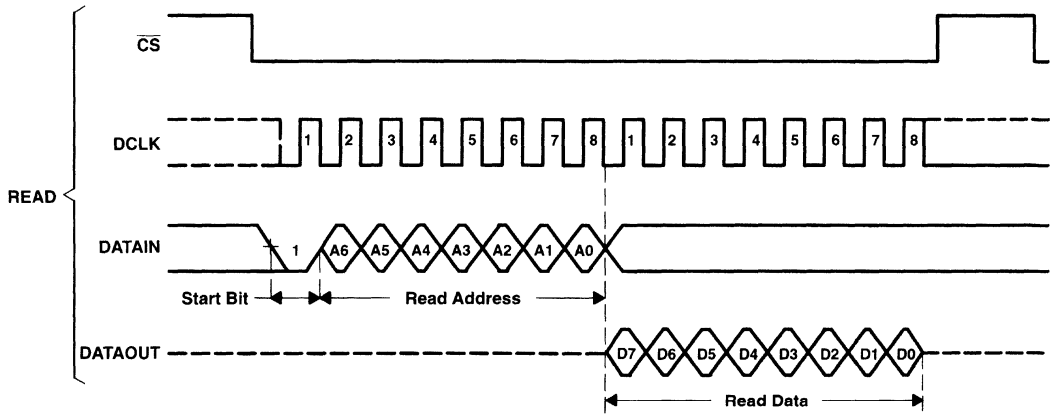

Figure 22. Microcontroller Interface Read Timing Diagram

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Table 39. Read Address Map

HEXA-DECIMAL ADDRESS (7 BITS)	NAME	REGISTER NAME	FUNCTION	NUMBER OF SIGNIFICANT BITS
00	Status word 1	S1	Status word 1	7
01	Status word 2	S2	Status word 2	5
02 – 04	Not used			
05	Event register 1	E1	Event register 1	7
06	Event register 2	E2	Event register 2	8
07 – 0F	Not used			
10	RX data word 0	RXD0	RX bits 27 – 20	8
11	RX data word 1	RXD1	RX bits 19 – 12	8
12	RX data word 2	RXD2	RX bits 11 – 4	8
13	RX data word 3 (Bits 7 – 4)	RXD3	RX bits 3 – 0 and error correction status	8
14 – 15	Not used			
16	PIO1 status word	PI1	State of PIO1 terminals	8
18	PIO2 status word	PI2	State of PIO2 terminals	8
1A	PIO3 status word	PI3	State of PIO3 terminals	4
1B – 21	Not used			
22	RX repeat count	RXRPT	Number of word repeats used for the majority voting — wide-band	4
26 – 42	Not used			
25	Narrow band error rate	NBERRS	Number of DSAT and SYNC bit errors in the last 200 received bits — narrow-band	8
43	AFC term count most significant nibble	AFCIF1	Termination count of IF–2, most significant byte	8
44	AFC term count middle byte	AFCIF2	Termination count of IF–2, middle byte	8
45	AFC term count least significant byte	AFCIF3	Termination count of IF–2, least significant nibble	4

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detailed description — read address map

In the following descriptions for the read address registers, a bit position within a register is identified by prefixing the bit number with its register name. For example, bit 1 of event register 1 (read address 05) is identified as: E1.1.

address 00 — status word 1 register (S1)

The S1 register is seven bits wide and the status of each bit, when it is set to 1, is shown in Table 40.

Table 40. Status Word 1 (S1) Definition

BIT	STATUS
0	RX data available
1	TX buffer available
2	Most recent TX aborted OR arbitration-wide-band failure
3	TX encoder active
4	RECC busy (not idle)
5	Counter/timer at zero state
6	Received wide-band SAT /narrow-band DSAT does not match the value defined in register C2. This bit is initially high during the first evaluation.

address 01 — status word 2 register (S2)

The S2 register is eight bits wide and the status of each bit, when it is set to 1, is shown in Table 41.

Table 41. Status Word 2 (S2) Definition

BIT	STATUS
0	Last two FOCC words differ
1	Not Used
2	FVC message being received
3	In FOCC frame sync
4	RXRF idle mode power saving active
5	Not Used
6	Not Used
7	Not Used

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address 05 — event register 1 (E1)

The E1 register is seven bits wide and the status of each bit, when it is set to 1, is shown in Table 42.

Table 42. Event Register 1 (E1) Definition

BIT	STATUS SINCE PREVIOUS READ OF THIS WORD
0	RX data available
1	TX buffer available
2	Arbitration failure
3	TX sequence completed
4	Change of FOCC busy/idle status
5	Counter/timer reaches zero state
6	Wide-band SAT/narrow-band DSAT status changed. This always changes after the first evaluation.

These flags indicate which event(s) have occurred since the previous read, regardless of their associated interrupt control bits. Event registers are cleared following a read. Since there are two registers, the following protocol takes place:

1. The microcontroller addresses E1.
2. The INTRPT terminal goes low, the contents of both interrupt registers are transferred to buffers and the registers are cleared and are then ready to catch new events.
3. The serial microcontroller interface clocks out the buffered event information.
4. Any new events are caught in the main interrupt register; however, at this time INTRPT remains low.
5. The microcontroller addresses E2.
6. The buffered E2 information, caught in step 2, is clocked out.
7. Once the read is completed, INTRPT goes high if any interrupts occurred during steps 2 through 6. The event register now contains all the events that occurred during the read process.

NOTE

Always read both E1 and then E2 in order. Reading only E1 results in the events being queued until E2 is eventually read.

address 06 — event register 2 (E2)

The E2 register is eight bits wide and the status of each bit, when it is set to 1, is shown in Table 43.

Table 43. Event Register 2 (E2) Definition

BIT	STATUS SINCE PREVIOUS READ OF THIS WORD
0	FOCC data changed value
1	FVC dotting detected — wide-band
2	FVC frame sync achieved (wide-band word sync/narrow-band sync word)
3	Change of FOCC frame sync status
4	Change of RXRF idle mode power-saving status
5	NRZ error count register (NBERRS) updated — narrow-band
6	PIO3 input port-sensed signal
7	AFC has reached terminal count

These flags indicate which event(s) have occurred since the previous read, regardless of their associated interrupt control bits. E2 can only be read after E1 because of the protocol for queuing and clearing events (see the description for address 02).

Priorities for the events in registers E1 and E2, shown in Table 42 and Table 43, are handled inside the TCM8030. Interrupt priorities are handled in software.

MCU idle mode processing

This idle mode processing feature is in addition to RXRF idle mode. It allows the use of microcontroller power-saving modes.

Operation is achieved by masking out the RX1 data available event, by writing 0 to IE1.0 (write address 05) and writing a 1 to the FOCC data change event, IE2.0 (write address 06).

The TCM8030 generates an interrupt only when the received word changes from its previous value. This means that no interrupt is generated (after the first word) during the reception of a stream of words that are the same. This extended time between interrupts allows the microcontroller to spend more time in sleep mode.

This feature may be implemented after the reception of a CFM (control filler message). It is likely that several more CFMs are received, so the microcontroller can enter idle mode processing and subsequently enter sleep mode.

No interpretation of messages is done, however. The interrupt is generated based on a bit-for-bit comparison of the current word and the previous one. Continuously repeated single words are handled, but repeated multiword messages are not supported.

SYNC terminal

This terminal goes high in FVC mode (C1.2 = 1, write address 00) while a message is being received. It also goes high in FOCC mode (C1.2 = 0, write address 00) while the data processor is in sync with the control channel.

address 10 — RX data word 0 (RXD0)

This register contains the error-corrected received data bits 27 to 20 (bit 27 is MSB).

PRINCIPLES OF OPERATION

address 11 — RX data word 1 (RXD1)

This register contains the error-corrected received data bits 19 to 12 (bit 19 is MSB).

address 12 — RX data word 2 (RXD2)

This register contains the error-corrected received data bits 11 to 4 (bit 11 is MSB).

address 13 — RX data word 3 (RXD3)

This register contains the error-corrected received data bits 3 to 0 and the error correction status as shown in Table 44.

Table 44. RX Data Word 3 (RXD3) Definition

BIT	STATUS
3 – 0	Received data decode status (see Table 45)
4	RX data bit 0
5	RX data bit 1
6	RX data bit 2
7	RX data bit 3

The received data error correction status is contained in bits 0 – 3, with 16 possible status conditions as shown in Table 45.

Table 45. RX Data Word 3 (RXD3) Error Correction Status Definition

RECEIVED DATA WORD 3				DECODE STATUS
BIT 3	BIT 2	BIT 1	BIT 0	
0	0	0	0	No errors detected
0	0	0	1	One error detected in parity bits
0	0	1	0	Two errors detailed in parity bits
0	0	1	1	Not used
0	1	0	0	One error corrected in data
0	1	0	1	One error corrected in data, one error detected in parity bits
0	1	1	0	Not used
0	1	1	1	Not used
1	0	0	0	Two errors corrected in data
1	0	0	1	Not used
1	0	1	0	Not used
1	0	1	1	Not used
1	1	0	0	More than two erasures† occurred — up to two data bits corrected.
1	1	0	1	More than two erasures† occurred — one error detected in parity bits and up to one data bit corrected.
1	1	1	0	More than two erasures† occurred — two errors in parity bits detected.
1	1	1	1	More than two errors detected — data not corrected.

† A bit erasure occurs when, over valid repeats , the bit is detected an equal number of times as a 1 and as a 0.

PRODUCT PREVIEW

addresses 16,18, 1A — PIO status words (PI1, PI2, PI3)

These addresses monitor the states of PIO1, PIO2, and PIO3 terminals.

address 22 — RX repeat count — wide-band

The received repeat count gives the number of repeats of the received word that were actually used, using the bit-wise majority voting circuit to generate the received data.

address 25 — narrow-band error rate (NBERRS)

This register is provided to assist in implementing the mobile reported interference function required by the NAMPS specification.

MRI (mobile-reported interference) operation

The NBERRS register contains the total errors detected in the 200 NRZ bits of DSAT and sync word that were received up until the latest update. The NBERRS register is updated once for each group of 100 received NRZ bits. At the same time as this update, the event E2.5 (read address 06) is triggered. When the interrupt bit IE2.5 (write address 06) has been set, then an interrupt is generated. The microcontroller can then read the NBERRS register to determine the error rate over the last 200 NRZ bits.

While the sync word is being received, the DSAT error checking reports a large number of errors. The errors are eliminated automatically (subtracted out) once the whole word is successfully received, and the error register is incremented by the number of sync-word errors. When a complete data word is received, the DSAT continues as if it were never interrupted, that is, during data reception the reference DSAT generator phase is advanced every NRZ clock cycle even when there is no DSAT output.

Error counting begins when 24 bits of NRZ data have been received. The total-error count contained in these twenty-fourth bits determines the DSAT status. However, the NBERRS error counting mechanism only considers the twenty-fourth bit. After this initialization period, the error counting mechanism functions regardless of DSAT status. For example, when bad DSAT status is indicated, the reference DSAT generator maintains its original phase and continues to perform error accumulation on each bit as it is received. After only 1.6 seconds (the time taken for a sync word, data word, and 24 bits of DSAT) the DSAT generator phase is rotated to find a best fit with the received data. Having found the best fit, the received bit is tested against the reference bit to see whether the error count needs to be incremented.

The rest of the MRI function is done in software. This consists of comparing the narrow-band error rate with the threshold setting that has been communicated by a control message to the mobile unit. When this threshold setting is exceeded, a MRI order is generated from the mobile to the base station over the RVC.

The microcontroller must:

1. Read the NBERRS register after an NBERRS update interrupt.
2. Integrate as required, many NBERRS readings over time to get an averaged result.
3. Determine when the error rate has gone above the threshold.
4. Generate an MRI order, when threshold has been exceeded, on the RVC by sending a correct data word to the TCM8030.

The MRI circuit always operates on FVC in narrow-band mode. MRI interrupts can be enabled or disabled by setting or resetting the interrupt mask bit IE2.5 (write address 06). Therefore, no MRI start/stop bit is provided. The NBERRS count is reinitialized when the narrow-band mode (C1.1, write address 00) and FVC (C1.2, write address 00) bits change from any other state to binary 11. Hence, no MRI clear bit is provided.

PRINCIPLES OF OPERATION

address 43 — AFC terminal count MS byte (AFCIF1)

This register contains the most significant byte (bits 12 –19 stored in locations 0–7) of the IF-2 counter in the AFC block.

address 44 — AFC terminal count middle byte (AFCIF2)

This register contains the middle byte (bits 4–11 stored in locations 0 – 7) of the IF-2 counter in the AFC block.

address 45 — AFC terminal count lower byte (AFCIF3)

This register contains the lower nibble (bits 0–3 stored in locations 4 –7 respectively) of the IF-2 counter in the AFC block as shown in Table 46.

Table 46. AFC Terminal Count Lower Byte (AFCIF3) Definition

BIT	STATUS
4	AFC, IF-2 counter bit 0
5	AFC, IF-2 counter bit 1
6	AFC, IF-2 counter bit 2
7	AFC, IF-2 counter bit 3

The AFC terminal counter should be read MS byte first and LS nibble last. After a reading of the LS nibble has occurred, both the TCXO counter and the AFC counter are automatically reset.

PRODUCT PREVIEW

APPLICATIONS INFORMATION

suggested trim sequence

The TCM8030 is designed so that no manual trims are required. All levels can be adjusted to meet system requirements and to compensate for production tolerances by writing to the digital interface. The data required is stored in a nonvolatile memory by the microcontroller in the telephone. When the telephone is turned on, an initialization routine writes this calibration data to the TCM8030.

The sequence of adjustments is detailed in the following procedure. Steps 1 – 6 adjust the transmit path and step 7 adjusts the receive path.

1. TXTRIM
   a. Set the TX DAT TRIM to nominal = 100.
   b. Set the TCM8030 to transmit signaling tone.
   c. Adjust the TXTRIM register to set the frequency deviation to that required by the system.
2. TXSAT
   a. Turn the signaling tone off and turn on the SAT path.
   b. Set the TCM8030 to generate its own SAT tone of 6000 Hz.
   c. Adjust the SATTRIM register to give the required frequency deviation.
3. VDTRIM
   a. Mute the signaling tone and SAT.
   b. Inject an audio signal at the desired level into the microphone preamplifier, MICAMP2.
   c. Adjust the VDTRIM register to set the frequency deviation. This also adjusts the TX DTMF level.
4. LIMITER TRIM
   a. Increase the audio signal level by 20 dB, typically.
   b. Adjust LIMITER register to produce the required maximum deviation.
5. DTMF Trim

   The DTMF level is set by external resistors between the DTO output and the DTI input (TX side) and CTI input (RX side). There is no independent DTMF trim register on the TCM8030.
6. TX NARROW BAND DATA (NTACS or NAMPS)

   The narrow-band data transmission level can be adjusted using the TXDATRIM register.
7. RXTRIM
   a. Input a modulated signal to the telephone
   b. Adjust the RXTRIM register to produce the required signal level at REC1 and REC2.

APPLICATIONS INFORMATION

muting the audio paths

Both the transmit path as well as the receive path can be muted at two locations within the TCM8030. Muting is accomplished by writing 00h to the associated transmit receive configuration register.

transmit

Writing 00 (hex) to register TXCFG (address 33) mutes the TX path. The path is actually muted at TXSW and TXSUM by connection to TXVMID.

receive

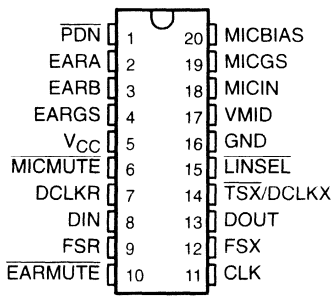
Writing 00 (hex) to register RXCFG (address 32) mutes the RX path. The path is actually muted at REC1SW and RECBUF by connection to RXVMID.

6 Voice-Band Audio Processors

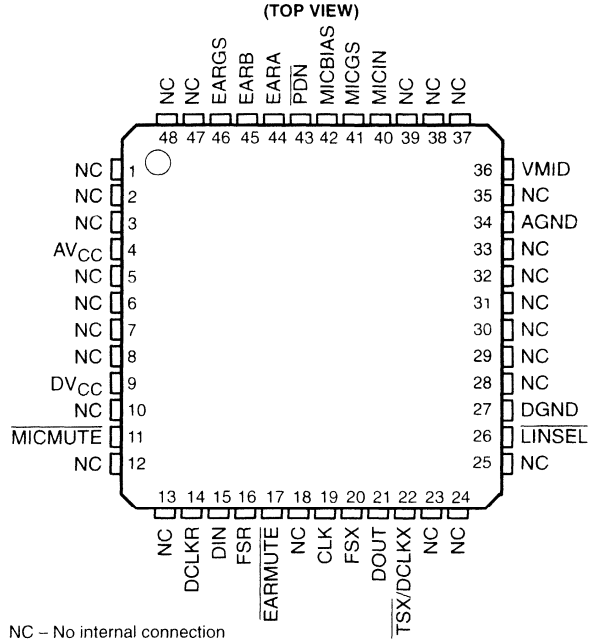
- Single 5-V Operation
- Low Power Consumption:
  - Operating Mode . . . 40 mW Typ
  - Standby Mode . . . 5 mW Typ
  - Power-Down Mode . . . 3 mW Typ
- Combined A/D, D/A, and Filters
- Extended Variable-Frequency Operation
  - Sample Rates up to 16 kHz
  - Pass-Band up to 7.2 kHz
- Electret Microphone Bias Reference Voltage Available
- Drive a Piezo Speaker Directly
- Compatible With All Digital Signal Processors (DSPs)
- Selectable Between 8-Bit Companded and 13-Bit (Dynamic Range) Linear Conversion:
  - TCM320AC36 . . . μ-Law and Linear Modes
  - TCM320AC37 . . . A-Law and Linear Modes
- Programmable Volume Control in Linear Mode
- 300 Hz – 3.6 kHz Passband with Specified Master Clock
- Designed for Standard 2.048-MHz Master Clock for U.S. Analog, U.S. Digital, CT2, DECT, GSM, and PCS Standards for Hand-Held Battery-Powered Telephones

description

DW OR N PACKAGE
(TOP VIEW)



PT PACKAGE
(TOP VIEW)



NC – No internal connection

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

VBAP is a trademark of Texas Instruments Incorporated.

description

The TCM320AC36 and TCM320AC37 voice-band audio processor (VBAP) integrated circuits are designed to perform the transmit encoding (A/D conversion) and receive decoding (D/A conversion) together with transmit and receive filtering for voice-band communications systems. Cellular telephone systems are targeted in particular; however, these integrated circuits can function in other systems including digital audio, telecommunications, and data acquisition.

These devices are pin-selectable for either of two modes, companded and linear, providing data in two formats. In the companded mode, data is transmitted and received in 8-bit words. In the linear mode, 13 bits of data, and either three bits of gain-setting control data, or three zero bits of padding to create a 16-bit word, are sent and received.

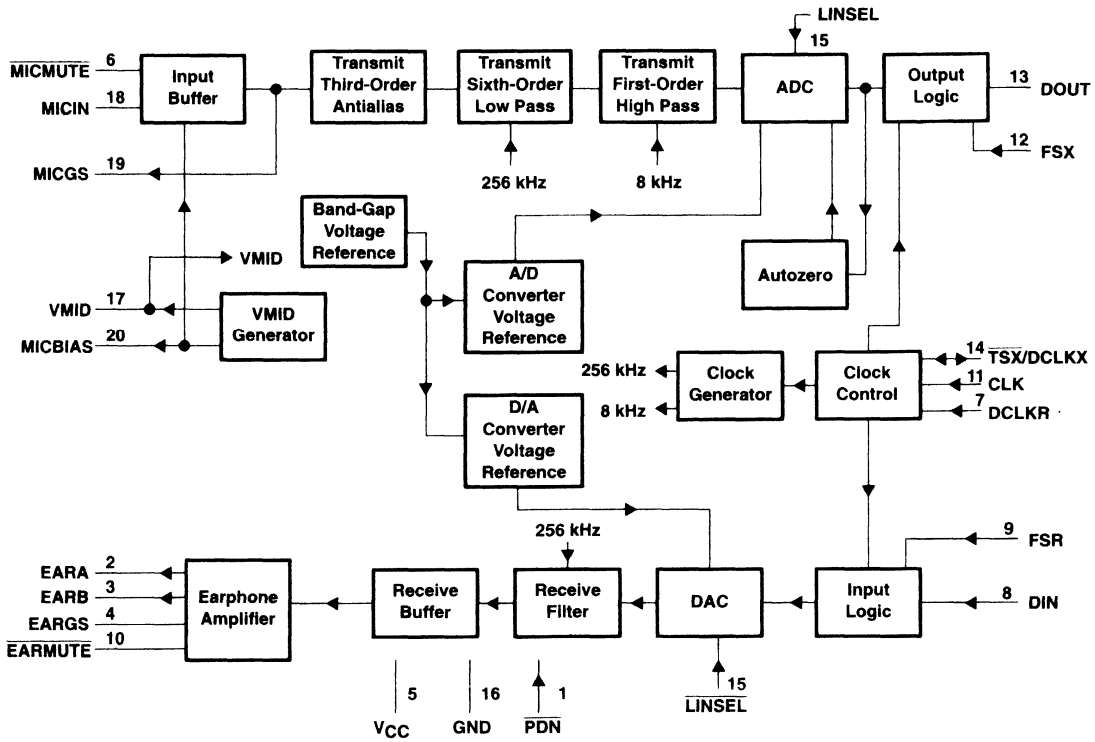
The transmit section is designed to interface directly with an electret microphone element. The microphone input signal (MICIN) is buffered and amplified with provision for setting the amplifier gain to accommodate a range of signal input levels. The amplified signal is passed through antialiasing and band-pass filters. The filtered signal is then applied to the input of a compressing analog-to-digital converter (COADC) when companded mode is selected. Otherwise, the analog-to-digital converter performs a linear conversion. The resulting data is then clocked out of DOUT as a serial data stream.

The receive section takes a frame of serial data on DIN and converts it to analog through an expanding digital-to-analog converter (EXDAC) when the companded mode is selected; otherwise, a linear conversion is performed. The analog signal then passes through switched capacitor filters, which provide out-of-band rejection, (sin x)/x correction functions, and smoothing. The filtered signal is sent to the earphone amplifier. The earphone amplifier has a differential output with adjustable gain and is designed to minimize static power dissipation.

A single on-chip high-precision band-gap circuit generates all voltage references, eliminating the need for external reference voltages. An internal reference voltage equal to $V_{CC}/2$, VMID, is used to develop the midlevel virtual ground for all the amplifier circuits and the microphone bias circuit. Another reference voltage, MICBIAS, can supply bias current for the microphone.

The TCM320AC3xC devices are characterized for operation from 0°C to 70°C. The TCM320AC3xI devices are characterized for operation from −40°C to 85°C.

functional block diagram



Terminal numbers shown are for the DW and N packages.

Terminal Functions

TERMINAL NAME	TERMINAL NO. DW, N	TERMINAL NO. PT	I/O	DESCRIPTION
AGND	—	34		Ground return for all internal analog circuits
AV_{CC}	—	4		5-V supply voltage for all internal analog circuits
CLK	11	19	I	Clock input. In the fixed-data-rate mode, CLK is the master clock input as well as the transmit and receive data clock input . In the variable-data-rate mode, CLK is the master clock input only (digital).
DCLKR	7	14	I	Selection of fixed- or variable-data-rate operation. When DCLKR is connected to V_{CC}, the device operates in the fixed-data-rate mode. When DCLKR is not connected to V_{CC}, the device operates in the variable-data-rate mode and DCLKR becomes the receive data clock (digital).
DGND	—	27		Ground return for all internal digital circuits
DIN	8	15	I	Receive data input. Input data is clocked in on consecutive negative transitions of the receive data clock, which is CLK for a fixed data rate and DCLKR for a variable data rate (digital).
DOUT	13	21	O	Transmit data output. Transmit data is clocked out on consecutive positive transitions of the transmit data clock, which is CLK for a fixed data rate and DCLKX for a variable data rate (digital).
DV_{CC}	—	9		5-V supply voltage for all internal digital circuits
EARA	2	44	O	Earphone output. EARA forms a differential drive when used with the EARB signal (analog).
EARB	3	45	O	Earphone output. EARB forms a differential drive when used with the EARA signal (analog).
EARGS	4	46	I	Earphone gain set input of feedback signal for the earphone output. The ratio of an external potential divider network connected across EARA and EARB adjusts the power amplifier gain. Maximum gain occurs when EARGS is connected to EARB. Minimum gain occurs when EARGS is connected to EARA. Earphone frequency response correction is performed using an RC approach (analog).
$\overline{\text{EARMUTE}}$	10	17	I	Earphone output mute control signal. When $\overline{\text{EARMUTE}}$ is low, the output amplifier is disabled and no audio is sent to the earphone (digital).
FSR	9	16	I	Frame-synchronization clock input for the receive channel. In the variable-data-rate mode, this signal must remain high for the duration of the time slot. The receive channel enters the standby condition when FSR is TTL-low for five frames or longer. The device enters a production test-mode condition when either FSR or FSX is held high for five frames or longer (digital).
FSX	12	20	I	Frame synchronization clock input for the transmit channel. FSX operates independently of FSR, but also in an analogous manner to FSR. The transmit channel enters the standby condition when FSX is low for five frames or longer. The device enters a production test-mode condition when either FSX or FSR is held high for five frames or longer (digital).
GND	16	—		Ground return for all internal circuits
$\overline{\text{LINSEL}}$	15	26	I	Linear selection input. When low, $\overline{\text{LINSEL}}$ selects linear coding/decoding. When high, $\overline{\text{LINSEL}}$ selects companded coding/decoding. Companding code on the 'AC36 is μ-law, and companding code on the 'AC37 is A-law (digital).
MICBIAS	20	42	O	Microphone bias. MICBIAS voltage for the electret microphone is equal to VMID.
MICGS	19	41	O	Output of the internal microphone amplifier. MICGS is used as the feedback to set the microphone amplifier gain. If sidetone is required, it is accomplished by connecting a series network between MICGS and EARGS (analog).
MICIN	18	40	I	Microphone input. Electret microphone input to the internal microphone amplifier (analog)
$\overline{\text{MICMUTE}}$	6	11	I	Microphone input mute control signal. When $\overline{\text{MICMUTE}}$ is active (low), zero code is transmitted (dig.).
$\overline{\text{PDN}}$	1	43	I	Power-down input. When $\overline{\text{PDN}}$ is low, the device powers down to reduce power consumption (digital).
$\overline{\text{TSX}}$/DCLKX	14	22	I/O	Transmit time slot strobe (active-low output) or data clock (input) for the transmit channel. In the fixed-data-rate mode, $\overline{\text{TSX}}$/DCLKX is an open-drain output that pulls to ground and is used as an enable signal for a 3-state buffer. In the variable-data-rate mode, DCLKX becomes the transmit data clock input (digital).
V_{CC}	5	—		5-V supply voltage for all internal circuits
VMID	17	36	O	$V_{CC}/2$ bias voltage reference. A pair of external, low-leakage, high-frequency capacitors (1 μF and 470 pF) should be connected between VMID and ground for filtering.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.3 V to 7 V
Output voltage range at DOUT, V_O ..... −0.3 V to 7 V
Input voltage range at DIN, V_I ..... −0.3 V to 7 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: C suffix ..... 0°C to 70°C
I suffix ..... −40°C to 85°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage value is with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW
PT	1075 mW	7.1 mW/°C	756 mW	649 mW

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
Supply voltage, V_{CC} (see Note 3)		4.5	5.5	V
High-level input voltage, V_{IH}		2.2		V
Low-level input voltage, V_{IL}			0.8	V
Load resistance between EARA and EARB, R_L (see Note 4)		600		Ω
Load capacitance between EARA and EARB, C_L (see Note 4)			113	nF
Operating free-air temperature, T_A	TCM320AC36C, TCM320AC37C	0	70	°C
	TCM320AC36I, TCM320AC37I	−40	85	

NOTES: 2. To avoid possible damage to these CMOS devices and resulting reliability problems, the power-up sequence detailed in the system reliability features paragraph should be followed.
3. Voltages at analog inputs, outputs, and V_{CC} are with respect to GND.
4. R_L and C_L should not be applied simultaneously.

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted)

supply current, f_{DCLKR} or f_{DCLKX} = 2.048 MHz, outputs not loaded, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
I_{CC}	Supply current from V_{CC}	Operating	$\overline{PDN}$ is high with CLK signal present		9.9	mA
		Power down	$\overline{PDN}$ is low for 500 µs		0.85	
		Standby – both	$\overline{PDN}$ is high with FSX and FSR held low		2	
		Standby – one	$\overline{PDN}$ is high with either FSX or FSR pulsing with the other held low		6	

digital interface

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	DOUT	I_{OH} = –3.2 mA, V_{CC} = 5 V	2.4	4.6		V
V_{OL}	Low-level output voltage		I_{OL} = 3.2 mA, V_{CC} = 5 V		0.2	0.4	V
I_{IH}	High-level input current, any digital input		V_I = 2.2 V to V_{CC}			10	µA
I_{IL}	Low-level input current, any digital input		V_I = 0 to 0.8 V			10	µA
C_i	Input capacitance				5		pF
C_o	Output capacitance				5		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

microphone interface

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IO}	Input offset voltage at MICIN		V_I = 0 to 5 V			±5	mV
I_{IB}	Input bias current at MICIN					±200	nA
B_1	Unity-gain bandwidth, open loop at MICIN				1		MHz
C_i	Input capacitance at MICIN				5		pF
A_V	Large-signal voltage amplification at MICGS				10000		V/V
I_{O}max	Maximum output current	VMID		1			µA
		MICBIAS (source only)		1			mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

speaker interface

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{O(PP)}$	AC output voltage				3	Vpp
V_{OO}	Output offset voltage at EARA, EARB (single-ended)	Relative to GND			80	mVpk
$I_{I(lkg)}$	Input leakage current at EARGS	V_I = 0.5 V to (V_{CC} – 0.5) V			±200	nA
I_{O}max	Maximum output current	R_L = 600 Ω			±5	mA
r_o	Output resistance at EARA, EARB			1		Ω
	Gain change	$\overline{EARMUTE}$ low, max level when muted	–80			dB

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

transmit gain and dynamic range, companded mode (μ-law or A-law) or linear mode selected, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted) (see Notes 5 and 6)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit reference-signal level (0 dB) (see Note 7)	Companded mode selected, μ-law ('AC36)		0.982	Vrms
	Companded mode selected, A-law ('AC37)		0.985	
	Linear mode selected ('AC36 and 'AC37)		1.001	
Overload-signal level (MICIN at unity gain)	Companded mode selected, μ-law ('AC36)		4	Vpp
	Companded mode selected, A-law ('AC37)		4	
	Linear mode selected ('AC36 and 'AC37)		4	
Absolute gain error	0-dB input signal		±1	dB
Gain error with input level relative to gain at −10 dBm0	MICIN to DOUT at 3 dBm0 to −36 dBm0		±0.5	dB
	MICIN to DOUT at −37 dBm0 to −40 dBm0		±1	
	MICIN to DOUT at −41 dBm0 to −50 dBm0		±1.5	dB
	MICIN to DOUT at −51 dBm0 to −55 dBm0		±2	dB
Gain variation	V_{CC} ±10%, T_A = 0°C to 70°C		±0.5	dB

NOTES: 5. Unless otherwise noted, the analog input is 0 dB, 1020-Hz sine wave, where 0 dB is defined as the zero-reference point of the channel under test.
6. The input amplifier is set for inverting unity gain.
7. The reference-signal level, which is input to the transmit channel, is defined as a value 3 dB below the full-scale value of 2 V.

transmit filter transfer, companded mode (μ-law or A-law) or linear mode selected, over recommended ranges of supply voltage and free-air temperature, CLK = 2.048 MHz, FSX = 8 kHz (see Note 6)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to input signal gain at 1.02 kHz	Input amplifier set for unity gain, noninverting maximum gain output signal at MICIN is 0 dB	f_{MICIN} = 50 Hz	−10	0	dB
		f_{MICIN} = 200 Hz	−1.8	0	
		f_{MICIN} = 300 Hz to 3 kHz		±0.15	
		f_{MICIN} = 3.3 kHz	−0.35	0.04	
		f_{MICIN} = 3.4 kHz	−1	−0.1	
		f_{MICIN} = 4 kHz		−14	
		f_{MICIN} ≥4.6 kHz		−32	

NOTE 6. The input amplifier is set for inverting unity gain.

transmit idle channel noise and distortion, companded mode with μ-law or A-law selected, over recommended ranges of supply voltage and operating free-air temperature (see Note 8)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise, psophometrically weighted	MICIN connected to MICGS through a 10-kΩ resistor		−71	dB0p
Transmit noise, C-message weighted	MICIN connected to MICGS through a 10-kΩ resistor		10	dBrnC0
Transmit signal-to-distortion ratio with sine-wave input	MICIN to DOUT at 0 dBm0 to −17 dBm0	36		dB
	MICIN to DOUT at −18 dBm0 to −23 dBm0	34		
	MICIN to DOUT at −24 dBm0 to −29 dBm0	30		
	MICIN to DOUT at −30 dBm0 to −35 dBm0	24		
	MICIN to DOUT at −36 dBm0 to −45 dBm0	16		
Intermodulation distortion, 2-tone CCITT method, composite power level −13 dBm0	CCITT G.712 (7.1), R2	49		dB
	CCITT G.712 (7.2), R3	51		

NOTE 8: Transmit noise, linear mode: 200 μVrms is equivalent to −74 dB (referenced to device 0-dB level).

transmit idle channel noise and distortion, linear mode selected, over recommended ranges of supply voltage and operating free-air temperature (see Notes 6 and 8)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise	MICIN connected to MICGS through a 10-kΩ resistor		200	μVrms
Transmit signal-to-distortion ratio with sine-wave input	MICIN to DOUT at 0 dBm0 to –6 dBm0	50		dB
	MICIN to DOUT at –7 dBm0 to –12 dBm0	48		
	MICIN to DOUT at –13 dBm0 to –18 dBm0	40		
	MICIN to DOUT at –19 dBm0 to –24 dBm0	35		
	MICIN to DOUT at –25 dBm0 to –40 dBm0	20		
	MICIN to DOUT at –41 dBm0 to –45 dBm0	18		

NOTES: 6. The input amplifier is set for inverting unity gain.
8. Transmit noise, linear mode: 200 μVrms is equivalent to –74 dB (referenced to device 0-dB level).

receive gain and dynamic range, companded mode (μ-law or A-law) or linear mode selected, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted) (see Notes 9 and 10)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive reference-signal level (0 dB) (see Note 11)	Companded mode selected, μ-law ('AC36)		0.736	Vrms
	Companded mode selected, A-law ('AC37)		0.739	
	Linear mode selected ('AC36 and 'AC37)		0.751	
Overload-signal level	Companded mode selected, μ-law ('AC36)		3	Vpp
	Companded mode selected, A-law ('AC37)		3	
	Linear mode selected ('AC36 and 'AC37)		3	
Absolute gain error	0-dB input signal		±1	dB
Gain error with output level relative to gain at –10 dBm0	DIN to EARA and EARB at 3 dBm0 to –36 dBm0		±0.5	dB
	DIN to EARA and EARB at –37 dBm0 to –40 dBm0		±1	
	DIN to EARA and EARB at –41 dBm0 to –50 dBm0		±1.5	
	DIN to EARA and EARB at –51 dBm0 to –55 dBm0		±2	
Gain variation	V_{CC} ±10%, T_A = 0°C to 70°C		±0.5	dB

NOTES: 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.
10. Unless otherwise noted, the digital input is a word stream generated by passing a 0-dB sine wave at 1020 Hz through an ideal encoder, where 0 dB is defined as the zero reference.
11. This reference-signal level is measured at the speaker output of the receive channel with the gain of the output speaker amplifier set to unity.

receive filter transfer, companded mode (μ-law or A-law) or linear mode selected, over recommended ranges of supply voltage and operating free-air temperature, FSR = 8 kHz (see Note 9)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	DIN = 0 dBm0	f_{DIN} = < 200 Hz		0.15	dB
		f_{DIN} = 200 Hz	–0.5	0.15	
		f_{DIN} = 300 Hz to 3 kHz		±0.15	
		f_{DIN} = 3.3 kHz	–0.35	0.03	
		f_{DIN} = 3.4 kHz	–1	–0.18	
		f_{DIN} = 4 kHz		–14	
		f_{DIN} = > 4.6 kHz		–30	

NOTE 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.

receive idle channel noise and distortion, companded mode with μ-law or A-law selected, over recommended ranges of supply voltage and operating free-air temperature (see Note 9)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive noise, psophometrically weighted	DIN = 11010101 (A-law)		−75	dB0p
Receive noise, C-message weighted	DIN = 11111111 (μ-law)		5	dBrnc0
Receive signal-to-distortion ratio with sine-wave input	DIN to EARA and EARB at 0 dBm0 to −18 dBm0	36		dB
	DIN to EARA and EARB at −19 dBm0 to −24 dBm0	34		
	DIN to EARA and EARB at −25 dBm0 to −30 dBm0	30		
	DIN to EARA and EARB at −31 dBm0 to −38 dBm0	23		
	DIN to EARA and EARB at −39 dBm0 to −45 dBm0	17		

NOTE 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.

receive idle channel noise and distortion, linear mode selected, over recommended ranges of supply voltage and operating free-air temperature (see Notes 9 and 12)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive noise	DIN = 00000000		200	μVrms
Receive signal-to-distortion ratio with sine-wave input	DIN to EARA and EARB at 0 dBm0 to −6 dBm0	50		dB
	DIN to EARA and EARB at −7 dBm0 to −12 dBm0	48		
	DIN to EARA and EARB at −13 dBm0 to −18 dBm0	38		
	DIN to EARA and EARB at −19 dBm0 to −24 dBm0	32		
	DIN to EARA and EARB at −25 dBm0 to −40 dBm0	18		
	DIN to EARA and EARB at −41 dBm0 to −45 dBm0	15		
Intermodulation, 2-tone CCITT distortion method, composite power level −13 dBm0	CCITT G.712 (7.1), R2	50		dB
	CCITT G.712 (7.2), R3	54		

NOTES: 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.
12. Receive noise, linear mode: 200 μVrms is equivalent to −71 dB (referenced to device 0-dB level).

power supply rejection and crosstalk attenuation over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Supply voltage rejection, transmit channel	Idle channel, supply signal = 100 mVrms, f = 0 to 30 kHz (measured at DOUT)		−30		dB
Supply voltage rejection, receive channel	Idle channel, supply signal = 100 mVrms, EARGS connected to EARB, f = 0 to 30 kHz (measured differentially between EARA and EARB)		−30		dB
Crosstalk attenuation, transmit-to-receive (differential)	MICIN = 0 dB, f = 1.02 kHz, unity transmit gain, EARGS connected to EARB, measured differentially between EARA and EARB	68			dB
Crosstalk attenuation, receive-to-transmit	DIN = 0 dBm0, f = 1.02 kHz, unity transmit gain, measured at DOUT	68			dB

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

timing requirements

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figure 1 through Figure 4)

		MIN	NOM†	MAX	UNIT
t_t	Transition time, CLK and DCLKX/DCLKR			10	ns
	Duty cycle, CLK	45%	50%	55%	
	Duty cycle, DCLKX/DCLKR	45%	50%	55%	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 2)

		MIN	MAX	UNIT
$t_{su(FSX)}$	Setup time, FSX high before CLK↓	20	468	ns
$t_{h(FSX)}$	Hold time, FSX high after CLK↓	20	468	ns

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 1)

		MIN	MAX	UNIT
$t_{su(FSR)}$	Setup time, FSR high before CLK↓	20	468	ns
$t_{h(FSR)}$	Hold time, FSR high after CLK↓	20	468	ns
$t_{su(DIN)}$	Setup time, DIN high or low before CLK↓	20		ns
$t_{h(DIN)}$	Hold time, DIN high or low after CLK↓	20		ns

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see Figure 4)

		MIN	MAX	UNIT
$t_{su(FSX)}$	Setup time, FSX high before DCLKX↓	40	$t_{c(DCLKX)}-40$	ns
$t_{h(FSX)}$	Hold time, FSX high after DCLKX↓	35	$t_{c(DCLKX)}-35$	ns

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see Figure 3)

		MIN	MAX	UNIT
$t_{su(FSR)}$	Setup time, FSR high before DCLKR↓	40		ns
$t_{h(FSR)}$	Hold time, FSR high after DCLKR↓	35	$t_{c(DCLKR)}-35$	ns
$t_{su(DIN)}$	Setup time, DIN high or low before DCLKR↓	30		ns
$t_{h(DIN)}$	Hold time, DIN high or low after DCLKR↓	30		ns

switching characteristics

propagation delay times over recommended ranges of operating conditions, fixed-data-rate mode, C_L = 0 to 10 pF (see Figure 2)

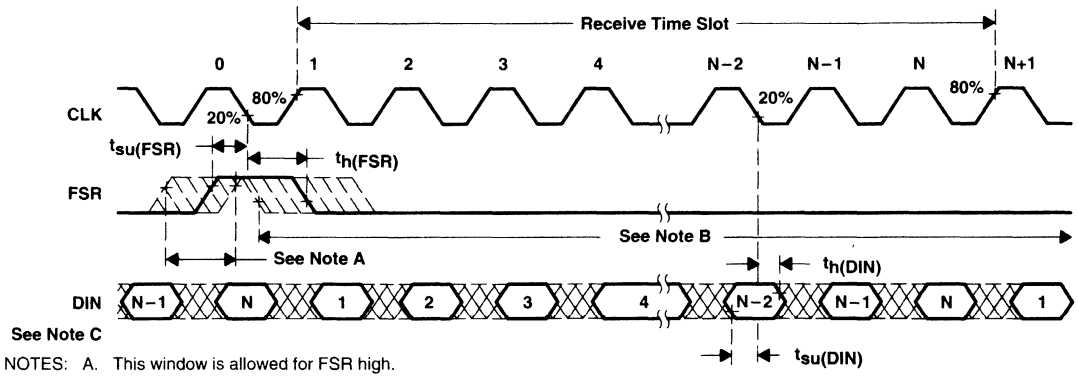
	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	From CLK bit 1 high to DOUT bit 1 valid			35	ns
t_{pd2}	From CLK high to DOUT valid, bits 2 to n			35	ns
t_{pd3}	From CLK bit n low to DOUT bit n Hi-Z		30		ns
t_{pd4}	From CLK bit 1 high to $\overline{TSX}$ active (low)	R_{pullup} = 1.24 kΩ		40	ns
t_{pd5}	From CLK bit n low to $\overline{TSX}$ inactive (high)	R_{pullup} = 1.24 kΩ	30		ns

propagation delay times over recommended ranges of operating conditions, variable-data-rate mode (see Figure 4)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{pd6}	FSX high to DOUT bit 1 valid	C_L = 0 to 10 pF		30	ns
t_{pd7}	DCLKX high to DOUT valid, bits 2 to n	C_L = 0 to 10 pF		40	ns
t_{pd8}	FSX low to DOUT bit n Hi-Z		20		ns

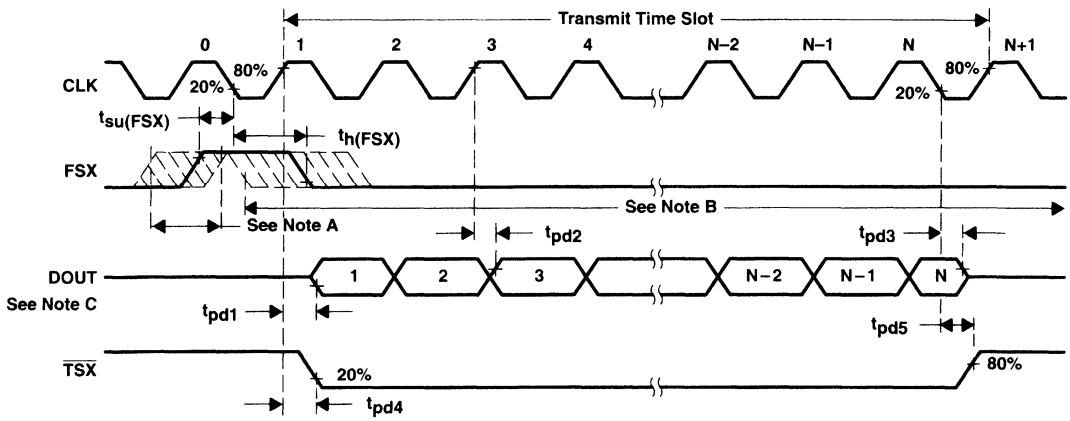
PARAMETER MEASUREMENT INFORMATION

All timing parameters are referenced to V_{IH} and V_{IL}. Bit 1 = MSB (most significant bit) and is clocked in first on DIN or clocked out first on DOUT. Bit n = LSB (least significant bit) and is clocked in last on DIN or is clocked out last on DOUT. N = 8 for the companded mode, and N = 16 for the linear mode.



NOTES: A. This window is allowed for FSR high.
B. This window is allowed for FSR low.
C. Transitions are measured at 50%.

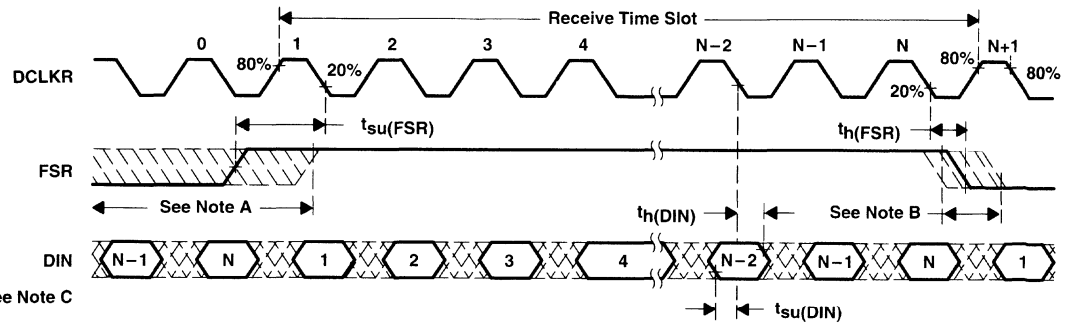
Figure 1. Fixed-Data Rate Mode, Receive Side Timing Diagram



NOTES: A. This window is allowed for FSX high.
B. This window is allowed for FSX low ($t_{h(FSX)}$ max determined by data collision considerations).
C. Transitions are measured at 50%.

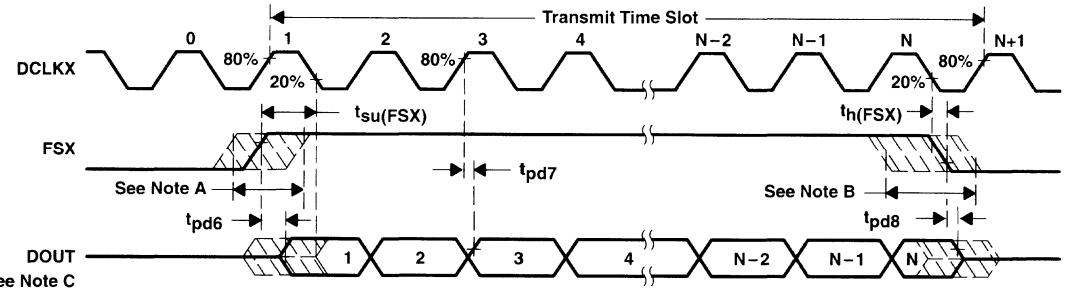
Figure 2. Fixed-Data Rate Mode, Transmit Side Timing Diagram

PARAMETER MEASUREMENT INFORMATION



NOTES: A. This window is allowed for FSR high ($t_{su(FSR)}$ max determined by data collision considerations).
B. This window is allowed for FSR low.
C. Transitions are measured at 50%.

Figure 3. Variable-Data Rate Mode, Receive Side Timing Diagram



NOTES: A. This window is allowed for FSX high.
B. This window is allowed for FSX low without data repetition.
C. Transitions are measured at 50%.

Figure 4. Variable-Data Rate Mode, Transmit Side Timing Diagram

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PRINCIPLES OF OPERATION

general

system reliability features

The device should be powered up and initialized as follows:

1. Apply GND.
2. Apply V_{CC}.
3. Connect all clocks.
4. Apply TTL high to $\overline{PDN}$.
5. Apply synchronizing pulses to FSX and/or FSR.

Even though the VBAP is heavily protected against latch-up, it is still possible to cause it to latch up under certain improper power conditions. To help ensure that latch-up does not occur, a reverse-biased Schottky diode (with a forward voltage drop of less than or equal to 0.4 V — 1N5711 or equivalent) should be connected between V_{CC} (power supply) and GND.

On the transmit channel, digital outputs DOUT and $\overline{TSX}$ are held in the high-impedance state for approximately four frames (500 µs) after power up or application of V_{CC}. After this delay, DOUT, $\overline{TSX}$, and signaling are functional and occur in the correct time slot. The analog circuits on the transmit side require approximately 60 ms to reach their equilibrium value due to the autozero circuit settling time. To further enhance system integrity, DOUT and $\overline{TSX}$ are placed in the high-impedance state after an interruption of CLK.

power-down and standby operations

To minimize power consumption, a power-down mode and three standby modes are provided.

For power down, an external low signal is applied to $\overline{PDN}$. In the absence of a signal, $\overline{PDN}$ is internally pulled up to a high logic level and the device remains active. In the power-down mode, the average power consumption is reduced to 3 mW.

Three standby modes give the user the option of placing the entire device on standby, placing only the transmit channel on standby, or placing only the receive channel on standby. To place the entire device on standby, both FSX and FSR are held low. For transmit-only operation (receive channel on standby), FSX is pulsing and FSR is held low. For receive-only operation (transmit section on standby), FSR is pulsing and FSX is held low. When the entire device is in standby mode, power consumption is reduced to 5 mW. See Table 1 for power-down and standby procedures.

PRINCIPLES OF OPERATION

Table 1. Power-Down and Standby Procedures

DEVICE STATUS	PROCEDURE	TYPICAL POWER CONSUMPTION	DIGITAL OUTPUT STATUS
Power on	$\overline{PDN}$ = high, FSX = pulses, FSR = pulses	40 mW	Digital outputs active but not loaded
Power down	$\overline{PDN}$ = low, FSX, FSR = X†	3 mW	$\overline{TSX}$ and DOUT in the high-impedance state
Entire device on standby mode	FSX = low, FSR = low, $\overline{PDN}$ = high	5 mW	$\overline{TSX}$ and DOUT in the high-impedance state
Only transmit channel in standby mode	FSX = low, FSR = pulses, $\overline{PDN}$ = high	20 mW	$\overline{TSX}$ and DOUT in the high-impedance state within five frames
Only receive channel in standby mode	FSR = low, FSX = pulses, $\overline{PDN}$ = high	20 mW	Digital outputs active but not loaded

† X = don't care

fixed-data-rate timing

Fixed-data-rate timing is selected by connecting DCLKR to V_{CC} and uses the master clock (CLK), frame synchronization clocks (FSX and FSR), and the $\overline{TSX}$ output. FSX and FSR are inputs that set the sampling frequency. Data is transmitted on DOUT on the positive transitions of CLK following the rising edge of FSX. Data is received on DIN on the falling edges of CLK following FSR. A D/A conversion is performed on the received digital word, and the resulting analog sample is held on an internal sample-and-hold capacitor until transferred to the receive filter. The data word is eight bits long in the companded mode and 16 bits long in the linear mode.

variable-data-rate timing

Variable-data-rate timing is selected by connecting DCLKR to the receive data clock. In this mode, the master clock (CLK) controls the switched-capacitor filters, while data transfer into DIN and out of DOUT is controlled by DCLKR and DCLKX respectively. This allows the data to be transferred in and out of the device at any rate up to the frequency of the master clock. DCLKR and DCLKX must be synchronous with CLK.

While the FSX input is high, data is transmitted from DOUT on consecutive positive transitions of DCLKX. Similarly, while the FSR input is high, the data word is received at DIN on consecutive negative transitions of DCLKR. The transmitted data word at DOUT is repeated in all remaining time slots in the frame as long as DCLKX is pulsed and FSX is held high. This feature, which allows the data word to be transmitted more than once per frame, is available only with variable-data-rate timing.

asynchronous operations

To avoid crosstalk problems associated with special interrupt circuits, the design includes separate converters, filters, and voltage references on the transmit and receive sides to allow completely independent operation of the two channels. In either timing mode, the master clock, data clock, and time-slot strobe must be synchronized at the beginning of each frame.

precision voltage references

A precision band-gap reference voltage is generated internally and is used to supply all the references required for operation of both the transmit and receive channels. The gain in each channel is trimmed during the manufacturing process. This ensures very accurate, stable gain performance over variations in supply voltage and device temperature.

PRINCIPLES OF OPERATION

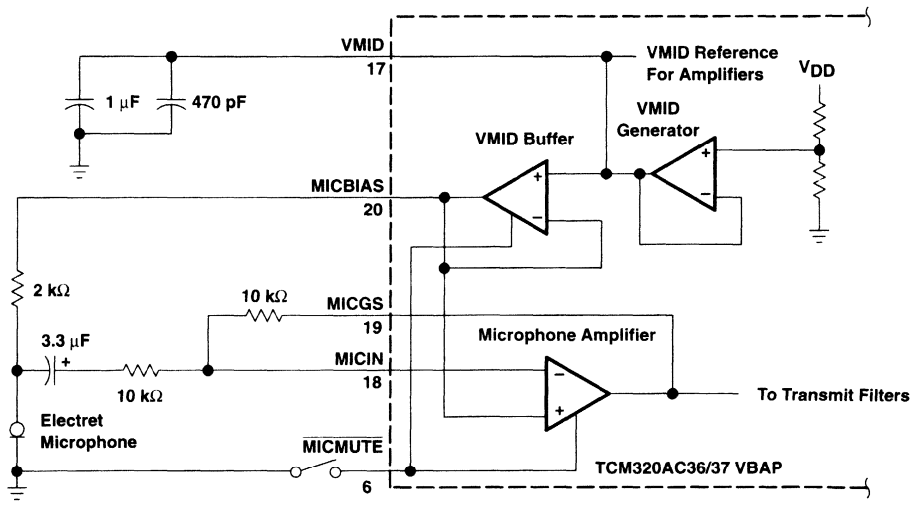
conversion laws

The TCM320AC36 provides μ-law companding operation that approximates the CCITT G.711 recommendation. The TCM320AC37 provides A-law companding operation that approximates the CCITT G.711 recommendation. The linear mode of operation uses a 13-bit two's-complement format and is the same for both the TCM320AC36 and the TCM320AC37.

transmit operation

microphone input

The microphone input amplifier is designed specifically to interface to electret-type microphone elements, as shown in Figure 5. The VMID buffer circuit provides a voltage (MICBIAS) equal to 1/2 V_{CC} as a reference for the microphone amplifier and a bias voltage to the electret microphone. The microphone amplifier output (MICGS) is used in conjunction with a feedback network and applied to the amplifier inverting input (MICIN) to set the amplifier gain. In the companded mode, when the MICIN signal level decreases to a level near the noise floor, the VBAP mutes the signal and outputs zero bits while continuing to monitor the signal level. When the input level once again exceeds the noise threshold, the mute is released and normal operation resumes. Input hysteresis is provided to ensure noiseless transitions in to and out of the muted condition. VMID appears at a terminal to provide a place to filter the VMID voltage.



NOTE A: Terminal numbers shown are for the DW and N packages.

Figure 5. Typical Microphone Interface

microphone mute function

The $\overline{\text{MICMUTE}}$ input causes the digital circuitry to transmit all zero code on DOUT.

transmit filter

A low-pass antialiasing section is included on the device and achieves a 35-dB attenuation at the sampling frequency. No external components are required to provide the necessary antialiasing function for the switched-capacitor section of the transmit filter.

PRINCIPLES OF OPERATION

encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample-and-hold capacitor. The encoder performs an A/D conversion on a switched-capacitor array. Digital data representing the sample is transmitted on the first 8 or 16 data clock cycles of the next frame.

The autozero circuit corrects for dc offset on the input signal to the encoder using the sign-bit averaging technique. The sign bit from the encoder output is long-term averaged and subtracted from the input to the encoder.

data word structure

The data word is eight bits long in the companded mode and all eight bits represent one audio data sample. The sign bit is the first bit transmitted.

The data word is 16 bits long in the linear mode. The first 13 bits comprise the audio data sample, and the last three bits form the volume control word in the receive direction (DIN) and are zero pad bits in the transmit direction (DOUT). The sign bit is transmitted first.

receive operation

decoding

In the companded mode, the serial data word is received at DIN on the first eight clock cycles in fixed-data rate and on the last eight clock cycles in variable-data rate. In the linear mode, the serial data word is received at DIN on the first 13 clock cycles. D/A conversion is performed, and the corresponding analog sample is held on an internal sample-and-hold capacitor. This sample is transferred to the receive filter.

receive filter

The receive section of the filter provides pass-band flatness and stop-band rejection that approximates both the AT&T D3/D4 specification and CCITT recommendation G.712 when operated at the recommended frequencies. The filter contains the required compensation for the (sin x)/x response of such decoders.

receive buffer

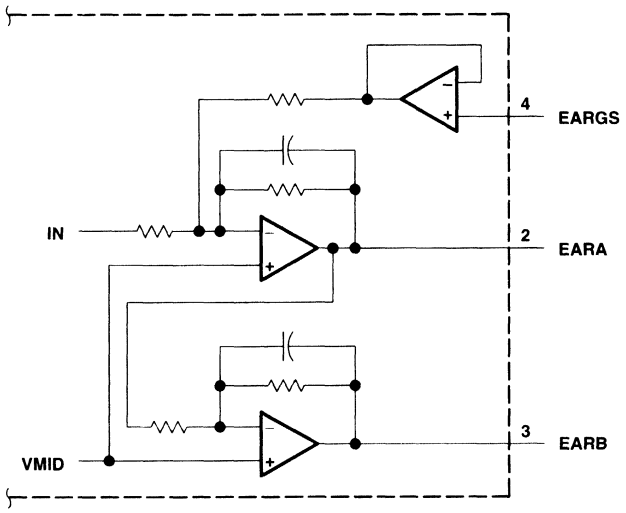
The receive buffer contains the volume control.

earphone amplifier

The earphone audio-output amplifier has a balanced output, as shown in Figure 6, to allow maximum flexibility in output configuration. The output amplifier is designed to directly drive a piezo earphone in the differential configuration without any additional external components. The output can also be used to drive a single-ended load with the output signal voltage centered around $V_{CC}/2$.

The receive-channel output level can be adjusted between specified limits by connecting an external resistor network to EARGS.

PRINCIPLES OF OPERATION



NOTE A: Terminal numbers shown are for the DW and N packages.

Figure 6. Earphone Audio-Output Amplifier Configuration and Internal Gain-Setting Network

receive data format

In the companded mode, eight bits of data are received. The sign bit is the first bit received (see Table 2).

In the linear mode, 16 bits of data are received. The first 13 bits are the D/A code, and the remaining three bits form the volume control word (see Table 2). The volume control function is actually an attenuation control in which the first bit received is the most significant. The maximum volume occurs when all three volume control bits are zero. Eight levels of attenuation are selectable in 3-dB steps, giving a maximum attenuation of 21 dB when all bits are 1s. The volume control bits are not latched into the VBAP and must be present in each received data word.

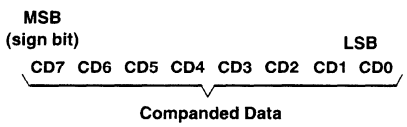
PRINCIPLES OF OPERATION

Table 2. Receive-Data Bit Definitions

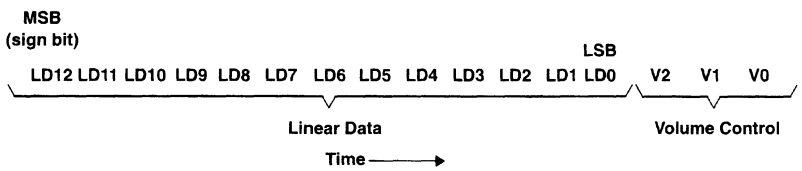
BIT NO.	COMPANDED MODE	LINEAR MODE
0	CD7	LD12
1	CD6	LD11
2	CD5	LD10
3	CD4	LD9
4	CD3	LD8
5	CD2	LD7
6	CD1	LD6
7	CD0	LD5
8	–	LD4
9	–	LD3
A	–	LD2
B	–	LD1
C	–	LD0
D	–	V2
E	–	V1
F	–	V0

Volume control and other control bits always follow the PCM data in time:

Companded Mode:



Linear Mode:



where:

CD7–CD0 = Data word when in companded mode
LD12–LD0 = Data word when in linear mode
V2, V1, V0 = Volume (attenuation control) 000 = maximum volume, 3 dBm0
111 = minimum volume, –18 dBm0

APPLICATION INFORMATION

output gain set design considerations (see Figure 7)

EARA and EARB are low-impedance complementary outputs. The voltages at the nodes are:

V_{O+} at EARA
V_{O-} at EARB
$V_{OD} = V_{O+} - V_{O-}$ (total differential response)

R1 and R2 are a gain-setting resistor network with the center tap connected to EARGS.

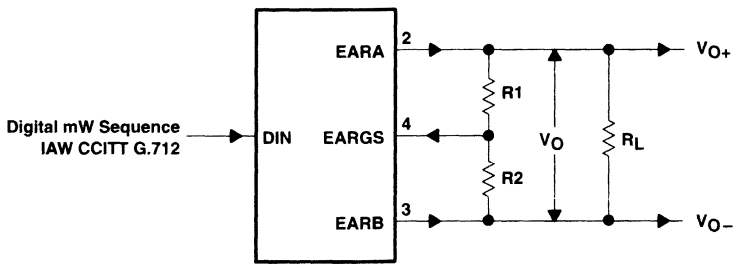
A value greater than 10 kΩ and less than 100 kΩ for R1 + R2 is recommended because of the following:

The parallel combination R1 + R2 and R_L sets the total loading. The total capacitance at EARGS and the parallel combination of R1 and R2 define a time constant that has to be minimized to avoid inaccuracies.

V_A represents the maximum available digital mW output response (V_A = 0.751 Vrms).

$$V_{OD} = A \times V_A$$

$$\text{where } A = \frac{1 + (R1/R2)}{4 + (R1/R2)}$$



NOTE A: Terminal numbers shown are for the DW and N packages.

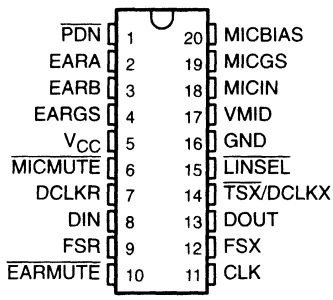
Figure 7. Gain-Setting Configuration

higher clock frequencies and sample rates

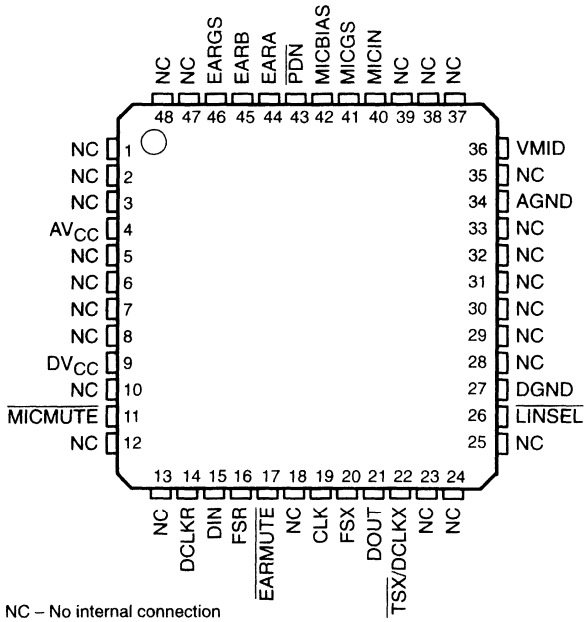
The VBAP is designed to work with sample rates up to 16 kHz where the frequency of the frame sync determines the sampling frequency. However, there is a fundamental requirement to maintain the ratio of the master clock frequency, f_{CLK}, to the frame sync frequency, f_{FSR}/f_{FSX}. This ratio for the VBAP is 2.048 MHz/8 kHz, or 256 master clocks per frame sync. For example, to operate the VBAP at a sampling rate of f_{FSR} and f_{FSX} equal to 16 kHz, f_{CLK} must be 256 times 16 kHz, or 4.096 MHz. If the VBAP is operated above an 8-kHz sample rate, however, it is expected that the performance becomes somewhat degraded. Exact parametric specifications for rates up to 16-kHz sample rate are not specified at this time.

- Single 5-V Operation
- Low Power Consumption:
  - Operating Mode . . . 40 mW Typ
  - Standby Mode . . . 5 mW Typ
  - Power-Down Mode . . . 3 mW Typ
- Combined A/D, D/A, and Filters
- Extended Variable-Frequency Operation
  - Sample Rates up to 16 kHz
  - Pass-Band up to 7.2 kHz
- Electret Microphone Bias Reference Voltage Available
- Drive a Piezo Speaker Directly
- Compatible With All Digital Signal Processors (DSPs)
- Selectable Between 8-Bit Companded and 13-Bit (Dynamic Range) Linear Conversion:
  - TCM320AC38 . . . μ-Law and Linear Modes
  - TCM320AC39 . . . A-Law and Linear Modes
- Programmable Volume Control in Linear Mode
- 300 Hz – 3.6 kHz Passband with Specified Master Clock
- Designed for Standard 2.6-MHz Master Clock for GSM and PCS Standards for Hand-Held Battery-Powered Telephones

DW OR N PACKAGE
(TOP VIEW)



PT PACKAGE
(TOP VIEW)



NC – No internal connection

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

VBAP is a trademark of Texas Instruments Incorporated.

description

The TCM320AC38 and TCM320AC39 voice-band audio processor (VBAP) integrated circuits are designed to perform the transmit encoding (A/D conversion) and receive decoding (D/A conversion) together with transmit and receive filtering for voice-band communications systems. Cellular telephone systems are targeted in particular; however, these integrated circuits can function in other systems including digital audio, telecommunications, and data acquisition.

These devices are pin-selectable for either of two modes, companded and linear, providing data in two formats. In the companded mode, data is transmitted and received in 8-bit words. In the linear mode, 13 bits of data and either three bits of gain-setting control data, or three zero bits of padding to create a 16-bit word, are sent and received.

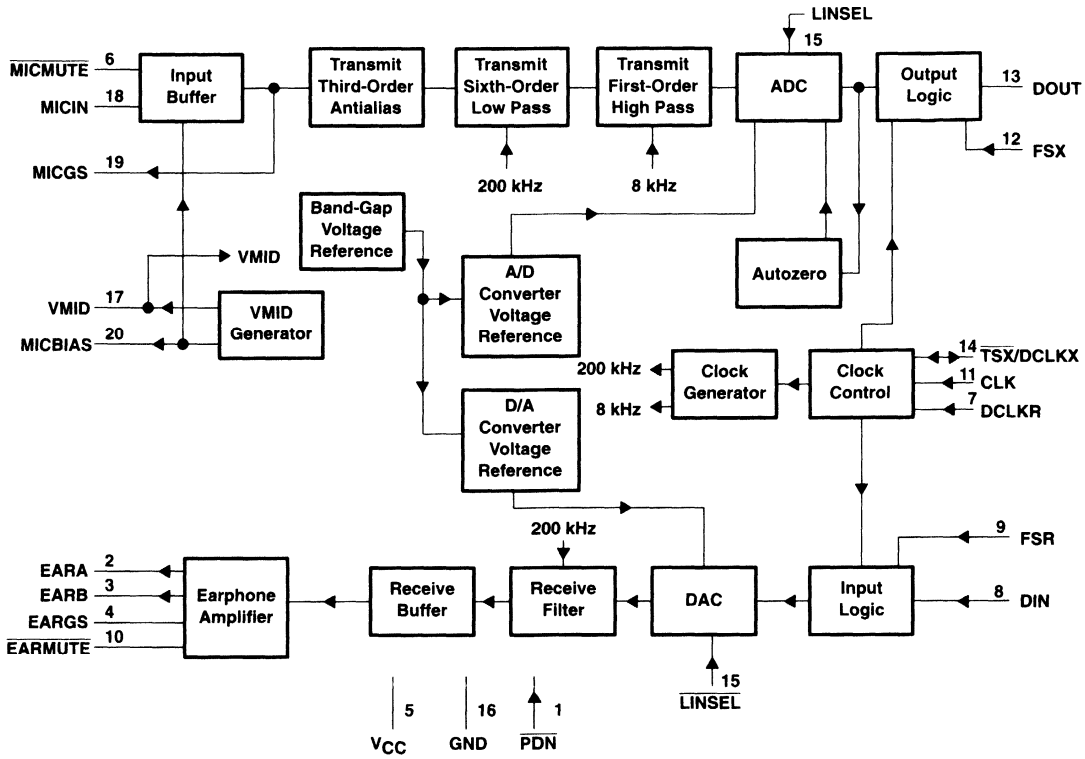
The transmit section is designed to interface directly with an electret microphone element. The microphone input signal (MICIN) is buffered and amplified with provision for setting the amplifier gain to accommodate a range of signal input levels. The amplified signal is passed through antialiasing and band-pass filters. The filtered signal is then applied to the input of a compressing analog-to-digital converter (COADC) when companded mode is selected. Otherwise, the analog-to-digital converter performs a linear conversion. The resulting data is then clocked out of DOUT as a serial data stream.

The receive section takes a frame of serial data on DIN and converts it to analog through an expanding digital-to-analog converter (EXDAC) when the companded mode is selected; otherwise, a linear conversion is performed. The analog signal then passes through switched capacitor filters, which provide out-of-band rejection, (sin x)/x correction functions, and smoothing. The filtered signal is sent to the earphone amplifier. The earphone amplifier has a differential output with adjustable gain and is designed to minimize static power dissipation.

A single on-chip high-precision band-gap circuit generates all voltage references, eliminating the need for external reference voltages. An internal reference voltage equal to $V_{CC}/2$, VMID, is used to develop the midlevel virtual ground for all the amplifier circuits and the microphone bias circuit. Another reference voltage, MICBIAS, can supply bias current for the microphone.

The TCM320AC3xC devices are characterized for operation from 0°C to 70°C. The TCM320AC3xI devices are characterized for operation from −40°C to 85°C.

functional block diagram



Terminal numbers shown are for the DW and N packages.

Terminal Functions

TERMINAL NAME	TERMINAL NO. DW, N	TERMINAL NO. PT	I/O	DESCRIPTION
AGND	—	34		Ground return for all internal analog circuits
AV_{CC}	—	4		5-V supply voltage for all internal analog circuits
CLK	11	19	I	Clock input. In the fixed-data-rate mode, CLK is the master clock input as well as the transmit and receive data clock input . In the variable-data-rate mode, CLK is the master clock input only (digital).
DCLKR	7	14	I	Selection of fixed- or variable-data-rate operation. When DCLKR is connected to V_{CC}, the device operates in the fixed-data-rate mode. When DCLKR is not connected to V_{CC}, the device operates in the variable-data-rate mode and DCLKR becomes the receive data clock (digital).
DGND	—	27		Ground return for all internal digital circuits
DIN	8	15	I	Receive data input. Input data is clocked in on consecutive negative transitions of the receive data clock, which is CLK for a fixed data rate and DCLKR for a variable data rate (digital).
DOUT	13	21	O	Transmit data output. Transmit data is clocked out on consecutive positive transitions of the transmit data clock, which is CLK for a fixed data rate and DCLKX for a variable data rate (digital).
DV_{CC}	—	9		5-V supply voltage for all internal digital circuits
EARA	2	44	O	Earphone output. EARA forms a differential drive when used with the EARB signal (analog).
EARB	3	45	O	Earphone output. EARB forms a differential drive when used with the EARA signal (analog).
EARGS	4	46	I	Earphone gain set input of feedback signal for the earphone output. The ratio of an external potential divider network connected across EARA and EARB adjusts the power amplifier gain. Maximum gain occurs when EARGS is connected to EARB. Minimum gain occurs when EARGS is connected to EARA. Earphone frequency response correction is performed using an RC approach (analog).
$\overline{\text{EARMUTE}}$	10	17	I	Earphone output mute control signal. When $\overline{\text{EARMUTE}}$ is low, the output amplifier is disabled and no audio is sent to the earphone (digital).
FSR	9	16	I	Frame-synchronization clock input for the receive channel. In the variable-data-rate mode, this signal must remain high for the duration of the time slot. The receive channel enters the standby condition when FSR is TTL-low for five frames or longer. The device enters a production test-mode condition when either FSR or FSX is held high for five frames or longer (digital).
FSX	12	20	I	Frame synchronization clock input for the transmit channel. FSX operates independently of FSR, but also in an analogous manner to FSR. The transmit channel enters the standby condition when FSX is low for five frames or longer. The device enters a production test-mode condition when either FSX or FSR is held high for five frames or longer (digital).
GND	16	—		Ground return for all internal circuits
$\overline{\text{LINSEL}}$	15	26	I	Linear selection input. When low, $\overline{\text{LINSEL}}$ selects linear coding/decoding. When high, $\overline{\text{LINSEL}}$ selects companded coding/decoding. Companding code on the 'AC38 is μ-law, and companding code on the 'AC39 is A-law (digital).
MICBIAS	20	42	O	Microphone bias. MICBIAS voltage for the electret microphone is equal to VMID.
MICGS	19	41	O	Output of the internal microphone amplifier. MICGS is used as the feedback to set the microphone amplifier gain. If sidetone is required, it is accomplished by connecting a series network between MICGS and EARGS (analog).
MICIN	18	40	I	Microphone input. Electret microphone input to the internal microphone amplifier (analog)
$\overline{\text{MICMUTE}}$	6	11	I	Microphone input mute control signal. When $\overline{\text{MICMUTE}}$ is active (low), zero code is transmitted (dig.).
$\overline{\text{PDN}}$	1	43	I	Power-down input. When $\overline{\text{PDN}}$ is low, the device powers down to reduce power consumption (digital).
$\overline{\text{TSX}}$/DCLKX	14	22	I/O	Transmit time slot strobe (active-low output) or data clock (input) for the transmit channel. In the fixed-data-rate mode, $\overline{\text{TSX}}$/DCLKX is an open-drain output that pulls to ground and is used as an enable signal for a 3-state buffer. In the variable-data-rate mode, DCLKX becomes the transmit data clock input (digital).
V_{CC}	5	—		5-V supply voltage for all internal circuits
VMID	17	36	O	$V_{CC}/2$ bias voltage reference. A pair of external, low-leakage, high-frequency capacitors (1 μF and 470 pF) should be connected between VMID and ground for filtering.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.3 V to 7 V
Output voltage range at DOUT, V_O ..... −0.3 V to 7 V
Input voltage range at DIN, V_I ..... −0.3 V to 7 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: C suffix ..... 0°C to 70°C
I suffix ..... −40°C to 85°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage value is with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW
PT	1075 mW	7.1 mW/°C	756 mW	649 mW

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
Supply voltage, V_{CC} (see Note 3)		4.5	5.5	V
High-level input voltage, V_{IH}		2.2		V
Low-level input voltage, V_{IL}			0.8	V
Load resistance between EARA and EARB, R_L (see Note 4)		600		Ω
Load capacitance between EARA and EARB, C_L (see Note 4)			113	nF
Operating free-air temperature, T_A	TCM320AC38C, TCM320AC39C	0	70	°C
	TCM320AC38I, TCM320AC39I	−40	85	

NOTES: 2. To avoid possible damage to these CMOS devices and resulting reliability problems, the power-up sequence detailed in the system reliability features paragraph should be followed.
3. Voltages at analog inputs, outputs, and V_{CC} are with respect to GND.
4. R_L and C_L should not be applied simultaneously.

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted)

supply current, f_{DCLKR} or f_{DCLKX} = 2.6 MHz, outputs not loaded, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
I_{CC}	Supply current from V_{CC}	Operating	$\overline{PDN}$ is high with CLK signal present		9.9	mA
		Power down	$\overline{PDN}$ is low for 500 µs		0.85	
		Standby – both	$\overline{PDN}$ is high with FSX and FSR held low		2	
		Standby – one	$\overline{PDN}$ is high with either FSX or FSR pulsing with the other held low		6	

digital interface

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	DOUT	I_{OH} = –3.2 mA, V_{CC} = 5 V	2.4	4.6		V
V_{OL}	Low-level output voltage		I_{OL} = 3.2 mA, V_{CC} = 5 V		0.2	0.4	V
I_{IH}	High-level input current, any digital input		V_I = 2.2 V to V_{CC}			10	µA
I_{IL}	Low-level input current, any digital input		V_I = 0 to 0.8 V			10	µA
C_i	Input capacitance				5		pF
C_o	Output capacitance				5		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

microphone interface

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IO}	Input offset voltage at MICIN		V_I = 0 to 5 V			±5	mV
I_{IB}	Input bias current at MICIN					±200	nA
B_1	Unity-gain bandwidth, open loop at MICIN				1		MHz
C_i	Input capacitance at MICIN				5		pF
A_V	Large-signal voltage amplification at MICGS				10000		V/V
I_{O}max	Maximum output current	VMID		1			µA
		MICBIAS (source only)		1			mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

speaker interface

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{O(PP)}$	AC output voltage				3	Vpp
V_{OO}	Output offset voltage at EARA, EARB (single-ended)	Relative to GND			80	mVpk
$I_{I(lkg)}$	Input leakage current at EARGS	V_I = 0.5 V to (V_{CC} – 0.5) V			±200	nA
I_{O}max	Maximum output current	R_L = 600 Ω			±5	mA
r_o	Output resistance at EARA, EARB			1		Ω
	Gain change	$\overline{EARMUTE}$ low, max level when muted	–80			dB

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

transmit gain and dynamic range, companded mode (μ-law or A-law) or linear mode selected, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted) (see Notes 5 and 6)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit reference-signal level (0 dB) (see Note 7)	Companded mode selected, μ-law ('AC38)		0.982	Vrms
	Companded mode selected, A-law ('AC39)		0.985	
	Linear mode selected ('AC38 and 'AC39)		1.001	
Overload-signal level (MICIN at unity gain)	Companded mode selected, μ-law ('AC38)		4	Vpp
	Companded mode selected, A-law ('AC39)		4	
	Linear mode selected ('AC38 and 'AC39)		4	
Absolute gain error	0-dB input signal		±1	dB
Gain error with input level relative to gain at –10 dBm0	MICIN to DOUT at 3 dBm0 to –36 dBm0		±0.5	dB
	MICIN to DOUT at –37 dBm0 to –40 dBm0		±1	
	MICIN to DOUT at –41 dBm0 to –50 dBm0		±1.5	dB
	MICIN to DOUT at –51 dBm0 to –55 dBm0		±2	dB
Gain variation	V_{CC} ±10%, T_A = 0°C to 70°C		±0.5	dB

NOTES: 5. Unless otherwise noted, the analog input is 0 dB, 1020-Hz sine wave, where 0 dB is defined as the zero-reference point of the channel under test.
6. The input amplifier is set for inverting unity gain.
7. The reference-signal level, which is input to the transmit channel, is defined as a value 3 dB below the full-scale value of 2 V.

transmit filter transfer, companded mode (μ-law or A-law) or linear mode selected, over recommended ranges of supply voltage and free-air temperature, CLK = 2.6 MHz, FSX = 8 kHz (see Note 6)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to input signal gain at 1.02 kHz	Input amplifier set for unity gain, noninverting maximum gain output signal at MICIN is 0 dB	f_{MICIN} = 50 Hz	–10	0	dB
		f_{MICIN} = 200 Hz	–1.8	0	
		f_{MICIN} = 300 Hz to 3 kHz		±0.15	
		f_{MICIN} = 3.3 kHz	–0.35	0.04	
		f_{MICIN} = 3.4 kHz	–1	–0.1	
		f_{MICIN} = 4 kHz		–14	
		f_{MICIN} ≥4.6 kHz		–32	

NOTE 6. The input amplifier is set for inverting unity gain.

transmit idle channel noise and distortion, companded mode with μ-law or A-law selected, over recommended ranges of supply voltage and operating free-air temperature (see Note 8)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise, psophometrically weighted	MICIN connected to MICGS through a 10-kΩ resistor		–71	dB0p
Transmit noise, C-message weighted	MICIN connected to MICGS through a 10-kΩ resistor		10	dBrnC0
Transmit signal-to-distortion ratio with sine-wave input	MICIN to DOUT at 0 dBm0 to –17 dBm0	36		dB
	MICIN to DOUT at –18 dBm0 to –23 dBm0	34		
	MICIN to DOUT at –24 dBm0 to –29 dBm0	30		
	MICIN to DOUT at –30 dBm0 to –35 dBm0	24		
	MICIN to DOUT at –36 dBm0 to –45 dBm0	16		
Intermodulation distortion, 2-tone CCITT method, composite power level –13 dBm0	CCITT G.712 (7.1), R2	49		dB
	CCITT G.712 (7.2), R3	51		

NOTE 8: Transmit noise, linear mode: 200 μVrms is equivalent to –74 dB (referenced to device 0-dB level).

transmit idle channel noise and distortion, linear mode selected, over recommended ranges of supply voltage and operating free-air temperature (see Notes 6 and 8)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise	MICIN connected to MICGS through a 10-kΩ resistor		200	μVrms
Transmit signal-to-distortion ratio with sine-wave input	MICIN to DOUT at 0 dBm0 to –6 dBm0	50		dB
	MICIN to DOUT at –7 dBm0 to –12 dBm0	48		
	MICIN to DOUT at –13 dBm0 to –18 dBm0	40		
	MICIN to DOUT at –19 dBm0 to –24 dBm0	35		
	MICIN to DOUT at –25 dBm0 to –40 dBm0	20		
	MICIN to DOUT at –41 dBm0 to –45 dBm0	18		

NOTES: 6. The input amplifier is set for inverting unity gain.
8. Transmit noise, linear mode: 200 μVrms is equivalent to –74 dB (referenced to device 0-dB level).

receive gain and dynamic range, companded mode (μ-law or A-law) or linear mode selected, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted) (see Notes 9 and 10)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive reference-signal level (0 dB) (see Note 11)	Companded mode selected, μ-law ('AC38)		0.736	Vrms
	Companded mode selected, A-law ('AC39)		0.739	
	Linear mode selected ('AC38 and 'AC39)		0.751	
Overload-signal level	Companded mode selected, μ-law ('AC38)		3	Vpp
	Companded mode selected, A-law ('AC39)		3	
	Linear mode selected ('AC38 and 'AC39)		3	
Absolute gain error	0-dB input signal		±1	dB
Gain error with output level relative to gain at –10 dBm0	DIN to EARA and EARB at 3 dBm0 to –36 dBm0		±0.5	dB
	DIN to EARA and EARB at –37 dBm0 to –40 dBm0		±1	
	DIN to EARA and EARB at –41 dBm0 to –50 dBm0		±1.5	
	DIN to EARA and EARB at –51 dBm0 to –55 dBm0		±2	
Gain variation	V_{CC} ±10%, T_A = 0°C to 70°C		±0.5	dB

NOTES: 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.
10. Unless otherwise noted, the digital input is a word stream generated by passing a 0-dB sine wave at 1020 Hz through an ideal encoder, where 0 dB is defined as the zero reference.
11. This reference-signal level is measured at the speaker output of the receive channel with the gain of the output speaker amplifier set to unity.

receive filter transfer, companded mode (μ-law or A-law) or linear mode selected, over recommended ranges of supply voltage and operating free-air temperature, FSR = 8 kHz (see Note 9)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	DIN = 0 dBm0	f_{DIN} = < 200 Hz		0.15	dB
		f_{DIN} = 200 Hz	–0.5	0.15	
		f_{DIN} = 300 Hz to 3 kHz		±0.15	
		f_{DIN} = 3.3 kHz	–0.35	0.03	
		f_{DIN} = 3.4 kHz	–1	–0.18	
		f_{DIN} = 4 kHz		–14	
		f_{DIN} = > 4.6 kHz		–30	

NOTE 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.

receive idle channel noise and distortion, companded mode (μ-law or A-law selected) over recommended ranges of supply voltage and operating free-air temperature (see Note 9)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive noise, psophometrically weighted	DIN = 11010101 (A-law)		−75	dB0p
Receive noise, C-message weighted	DIN = 11111111 (μ-law)		5	dBrnc0
Receive signal-to-distortion ratio with sine-wave input	DIN to EARA and EARB at 0 dBm0 to −18 dBm0	36		dB
	DIN to EARA and EARB at −19 dBm0 to −24 dBm0	34		
	DIN to EARA and EARB at −25 dBm0 to −30 dBm0	30		
	DIN to EARA and EARB at −31 dBm0 to −38 dBm0	23		
	DIN to EARA and EARB at −39 dBm0 to −45 dBm0	17		

NOTE 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.

receive idle channel noise and distortion, linear mode selected, over recommended ranges of supply voltage and operating free-air temperature (see Notes 9 and 12)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive noise	DIN = 00000000		200	μVrms
Receive signal-to-distortion ratio with sine-wave input	DIN to EARA and EARB at 0 dBm0 to −6 dBm0	50		dB
	DIN to EARA and EARB at −7 dBm0 to −12 dBm0	48		
	DIN to EARA and EARB at −13 dBm0 to −18 dBm0	38		
	DIN to EARA and EARB at −19 dBm0 to −24 dBm0	32		
	DIN to EARA and EARB at −25 dBm0 to −40 dBm0	18		
	DIN to EARA and EARB at −41 dBm0 to −45 dBm0	15		
Intermodulation, 2-tone CCITT distortion method, composite power level −13 dBm0	CCITT G.712 (7.1), R2	50		dB
	CCITT G.712 (7.2), R3	54		

NOTES: 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.
12. Receive noise, linear mode: 200 μVrms is equivalent to −71 dB (referenced to device 0-dB level).

power supply rejection and crosstalk attenuation over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Supply voltage rejection, transmit channel	Idle channel, supply signal = 100 mVrms, f = 0 to 30 kHz (measured at DOUT)		−30		dB
Supply voltage rejection, receive channel	Idle channel, supply signal = 100 mVrms, EARGS connected to EARB, f = 0 to 30 kHz (measured differentially between EARA and EARB)		−30		dB
Crosstalk attenuation, transmit-to-receive (differential)	MICIN = 0 dB, f = 1.02 kHz, unity transmit gain, EARGS connected to EARB, measured differentially between EARA and EARB	68			dB
Crosstalk attenuation, receive-to-transmit	DIN = 0 dBm0, f = 1.02 kHz, unity transmit gain, measured at DOUT	68			dB

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

timing requirements

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figure 1 through Figure 4)

		MIN	NOM†	MAX	UNIT
t_t	Transition time, CLK and DCLKX/DCLKR			10	ns
	Duty cycle, CLK	45%	50%	55%	
	Duty cycle, DCLKX/DCLKR	45%	50%	55%	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 2)

		MIN	MAX	UNIT
$t_{su(FSX)}$	Setup time, FSX high before CLK↓	20	468	ns
$t_{h(FSX)}$	Hold time, FSX high after CLK↓	20	468	ns

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 1)

		MIN	MAX	UNIT
$t_{su(FSR)}$	Setup time, FSR high before CLK↓	20	468	ns
$t_{h(FSR)}$	Hold time, FSR high after CLK↓	20	468	ns
$t_{su(DIN)}$	Setup time, DIN high or low before CLK↓	20		ns
$t_{h(DIN)}$	Hold time, DIN high or low after CLK↓	20		ns

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see Figure 4)

		MIN	MAX	UNIT
$t_{su(FSX)}$	Setup time, FSX high before DCLKX↓	40	$t_{c(DCLKX)}-40$	ns
$t_{h(FSX)}$	Hold time, FSX high after DCLKX↓	35	$t_{c(DCLKX)}-35$	ns

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see Figure 3)

		MIN	MAX	UNIT
$t_{su(FSR)}$	Setup time, FSR high before DCLKR↓	40		ns
$t_{h(FSR)}$	Hold time, FSR high after DCLKR↓	35	$t_{c(DCLKR)}-35$	ns
$t_{su(DIN)}$	Setup time, DIN high or low before DCLKR↓	30		ns
$t_{h(DIN)}$	Hold time, DIN high or low after DCLKR↓	30		ns

switching characteristics

propagation delay times over recommended ranges of operating conditions, fixed-data-rate mode, C_L = 0 to 10 pF (see Figure 2)

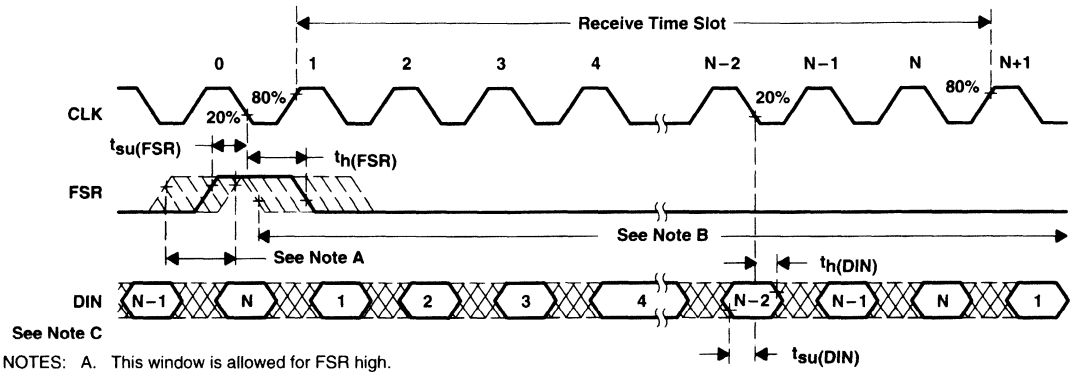
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	From CLK bit 1 high to DOUT bit 1 valid			35	ns
t_{pd2}	From CLK high to DOUT valid, bits 2 to n			35	ns
t_{pd3}	From CLK bit n low to DOUT bit n Hi-Z		30		ns
t_{pd4}	From CLK bit 1 high to $\overline{TSX}$ active (low)	R_{pullup} = 1.24 kΩ		40	ns
t_{pd5}	From CLK bit n low to $\overline{TSX}$ inactive (high)	R_{pullup} = 1.24 kΩ	30		ns

propagation delay times over recommended ranges of operating conditions, variable-data-rate mode (see Figure 4)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd6}	FSX high to DOUT bit 1 valid	C_L = 0 to 10 pF		30	ns
t_{pd7}	DCLKX high to DOUT valid, bits 2 to n	C_L = 0 to 10 pF		40	ns
t_{pd8}	FSX low to DOUT bit n Hi-Z		20		ns

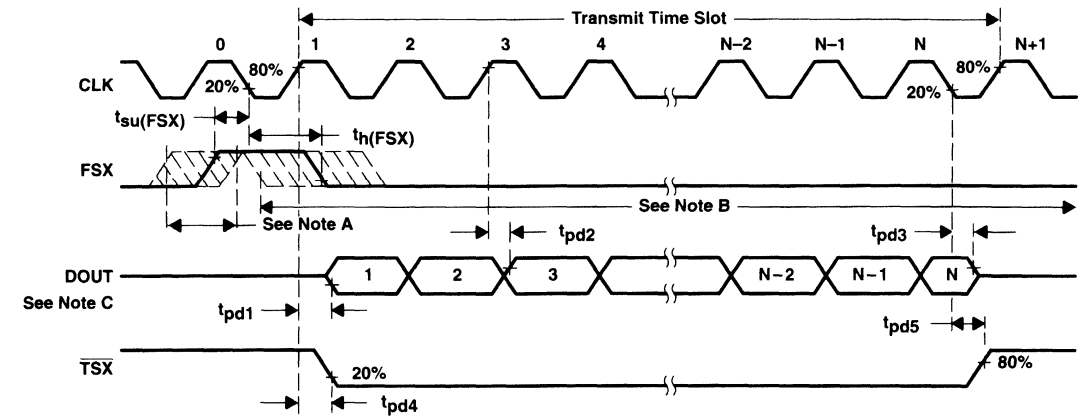
PARAMETER MEASUREMENT INFORMATION

All timing parameters are referenced to V_{IH} and V_{IL}. Bit 1 = MSB (most significant bit) and is clocked in first on DIN or clocked out first on DOUT. Bit n = LSB (least significant bit) and is clocked in last on DIN or is clocked out last on DOUT. N = 8 for the companded mode, and N = 16 for the linear mode.



NOTES: A. This window is allowed for FSR high.
B. This window is allowed for FSR low.
C. Transitions are measured at 50%.

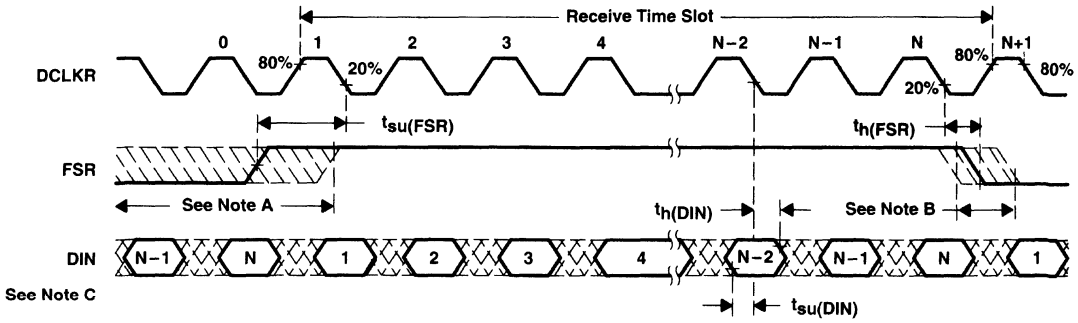
Figure 1. Fixed-Data Rate Mode, Receive Side Timing Diagram



NOTES: A. This window is allowed for FSX high.
B. This window is allowed for FSX low ($t_{h(FSX)}$ max determined by data collision considerations).
C. Transitions are measured at 50%.

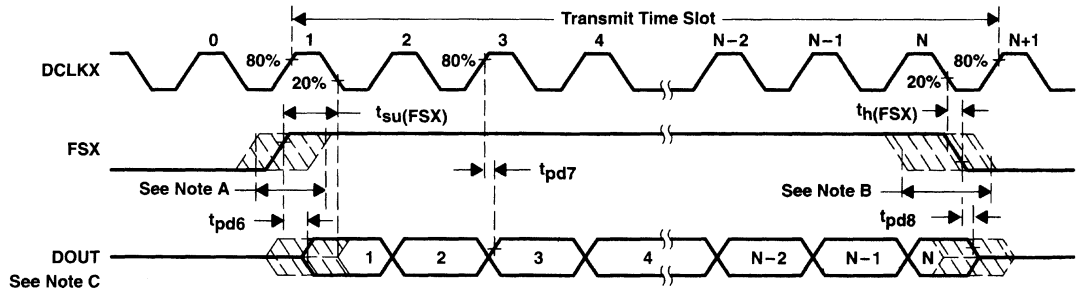
Figure 2. Fixed-Data Rate Mode, Transmit Side Timing Diagram

PARAMETER MEASUREMENT INFORMATION



NOTES: A. This window is allowed for FSR high ($t_{su(FSR)}$ max determined by data collision considerations).
B. This window is allowed for FSR low.
C. Transitions are measured at 50%.

Figure 3. Variable-Data Rate Mode, Receive Side Timing Diagram



NOTES: A. This window is allowed for FSX high.
B. This window is allowed for FSX low without data repetition.
C. Transitions are measured at 50%.

Figure 4. Variable-Data Rate Mode, Transmit Side Timing Diagram

PRINCIPLES OF OPERATION

general

system reliability features

The device should be powered up and initialized as follows:

1. Apply GND.
2. Apply V_{CC}.
3. Connect all clocks.
4. Apply TTL high to $\overline{PDN}$.
5. Apply synchronizing pulses to FSX and/or FSR.

Even though the VBAP is heavily protected against latch-up, it is still possible to cause it to latch up under certain improper power conditions. To help ensure that latch-up does not occur, a reverse-biased Schottky diode (with a forward voltage drop of less than or equal to 0.4 V — 1N5711 or equivalent) should be connected between V_{CC} (power supply) and GND.

On the transmit channel, digital outputs DOUT and $\overline{TSX}$ are held in the high-impedance state for approximately four frames (500 µs) after power up or application of V_{CC}. After this delay, DOUT, $\overline{TSX}$, and signaling are functional and occur in the correct time slot. The analog circuits on the transmit side require approximately 60 ms to reach their equilibrium value due to the autozero circuit settling time. To further enhance system integrity, DOUT and $\overline{TSX}$ are placed in the high-impedance state after an interruption of CLK.

power-down and standby operations

To minimize power consumption, a power-down mode and three standby modes are provided.

For power down, an external low signal is applied to $\overline{PDN}$. In the absence of a signal, $\overline{PDN}$ is internally pulled up to a high logic level and the device remains active. In the power-down mode, the average power consumption is reduced to 3 mW.

Three standby modes give the user the option of placing the entire device on standby, placing only the transmit channel on standby, or placing only the receive channel on standby. To place the entire device on standby, both FSX and FSR are held low. For transmit-only operation (receive channel on standby), FSX is pulsing and FSR is held low. For receive-only operation (transmit section on standby), FSR is pulsing and FSX is held low. When the entire device is in standby mode, power consumption is reduced to 5 mW. See Table 1 for power-down and standby procedures.

PRINCIPLES OF OPERATION

Table 1. Power-Down and Standby Procedures

DEVICE STATUS	PROCEDURE	TYPICAL POWER CONSUMPTION	DIGITAL OUTPUT STATUS
Power on	$\overline{PDN}$ = high, FSX = pulses, FSR = pulses	40 mW	Digital outputs active but not loaded
Power down	$\overline{PDN}$ = low, FSX, FSR = X†	3 mW	$\overline{TSX}$ and DOUT in the high-impedance state
Entire device on standby mode	FSX = low, FSR = low, $\overline{PDN}$ = high	5 mW	$\overline{TSX}$ and DOUT in the high-impedance state
Only transmit channel in standby mode	FSX = low, FSR = pulses, $\overline{PDN}$ = high	20 mW	$\overline{TSX}$ and DOUT in the high-impedance state within five frames
Only receive channel in standby mode	FSR = low, FSX = pulses, $\overline{PDN}$ = high	20 mW	Digital outputs active but not loaded

† X = don't care

fixed-data-rate timing

Fixed-data-rate timing is selected by connecting DCLKR to V_{CC} and uses the master clock (CLK), frame synchronization clocks (FSX and FSR), and the $\overline{TSX}$ output. FSX and FSR are inputs that set the sampling frequency. Data is transmitted on DOUT on the positive transitions of CLK following the rising edge of FSX. Data is received on DIN on the falling edges of CLK following FSR. A D/A conversion is performed on the received digital word, and the resulting analog sample is held on an internal sample-and-hold capacitor until transferred to the receive filter. The data word is eight bits long in the companded mode and 16 bits long in the linear mode.

variable-data-rate timing

Variable-data-rate timing is selected by connecting DCLKR to the receive data clock. In this mode, the master clock (CLK) controls the switched-capacitor filters, while data transfer into DIN and out of DOUT is controlled by DCLKR and DCLKX respectively. This allows the data to be transferred in and out of the device at any rate up to the frequency of the master clock. DCLKR and DCLKX must be synchronous with CLK.

While the FSX input is high, data is transmitted from DOUT on consecutive positive transitions of DCLKX. Similarly, while the FSR input is high, the data word is received at DIN on consecutive negative transitions of DCLKR. The transmitted data word at DOUT is repeated in all remaining time slots in the frame as long as DCLKX is pulsed and FSX is held high. This feature, which allows the data word to be transmitted more than once per frame, is available only with variable-data-rate timing.

asynchronous operations

To avoid crosstalk problems associated with special interrupt circuits, the design includes separate converters, filters, and voltage references on the transmit and receive sides to allow completely independent operation of the two channels. In either timing mode, the master clock, data clock, and time-slot strobe must be synchronized at the beginning of each frame.

precision voltage references

A precision band-gap reference voltage is generated internally and is used to supply all the references required for operation of both the transmit and receive channels. The gain in each channel is trimmed during the manufacturing process. This ensures very accurate, stable gain performance over variations in supply voltage and device temperature.

PRINCIPLES OF OPERATION

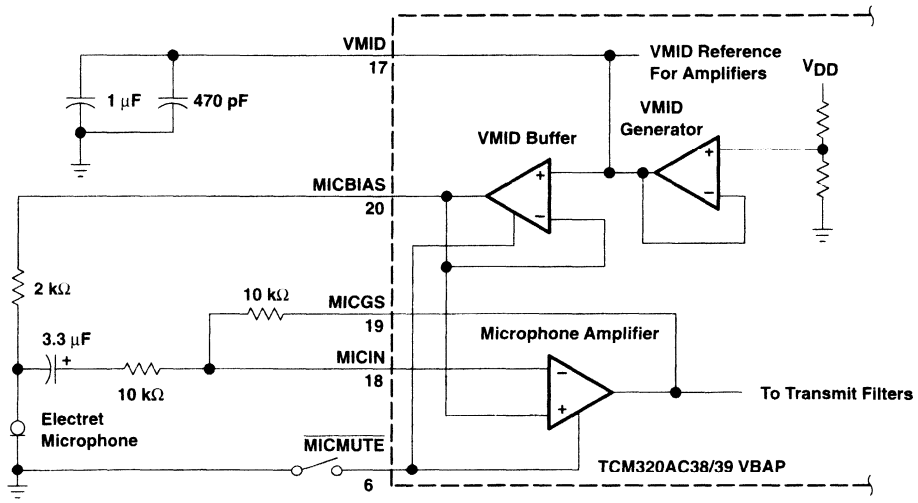
conversion laws

The TCM320AC38 provides μ-law companding operation that approximates the CCITT G.711 recommendation. The TCM320AC39 provides A-law companding operation that approximates the CCITT G.711 recommendation. The linear mode of operation uses a 13-bit two's-complement format and is the same for both the TCM320AC38 and the TCM320AC39.

transmit operation

microphone input

The microphone input amplifier is designed specifically to interface to electret-type microphone elements, as shown in Figure 5. The VMID buffer circuit provides a voltage (MICBIAS) equal to 1/2 V_{CC} as a reference for the microphone amplifier and a bias voltage to the electret microphone. The microphone amplifier output (MICGS) is used in conjunction with a feedback network and applied to the amplifier inverting input (MICIN) to set the amplifier gain. In the companded mode, when the MICIN signal level decreases to a level near the noise floor, the VBAP mutes the signal and outputs zero bits while continuing to monitor the signal level. When the input level once again exceeds the noise threshold, the mute is released and normal operation resumes. Input hysteresis is provided to ensure noiseless transitions in to and out of the muted condition. VMID appears at a terminal to provide a place to filter the VMID voltage.



NOTE A: Terminal numbers shown are for the DW and N packages.

Figure 5. Typical Microphone Interface

microphone mute function

The $\overline{\text{MICMUTE}}$ input causes the digital circuitry to transmit all zero code on DOUT.

transmit filter

A low-pass antialiasing section is included on the device and achieves a 35-dB attenuation at the sampling frequency. No external components are required to provide the necessary antialiasing function for the switched-capacitor section of the transmit filter.

PRINCIPLES OF OPERATION

encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample-and-hold capacitor. The encoder performs an A/D conversion on a switched-capacitor array. Digital data representing the sample is transmitted on the first 8 or 16 data clock cycles of the next frame.

The autozero circuit corrects for dc offset on the input signal to the encoder using the sign-bit averaging technique. The sign bit from the encoder output is long-term averaged and subtracted from the input to the encoder.

data word structure

The data word is eight bits long in the companded mode and all eight bits represent one audio data sample. The sign bit is the first bit transmitted.

The data word is 16 bits long in the linear mode. The first 13 bits comprise the audio data sample, and the last three bits form the volume control word in the receive direction (DIN) and are zero pad bits in the transmit direction (DOUT). The sign bit is transmitted first.

receive operation

decoding

In the companded mode, the serial data word is received at DIN on the first eight clock cycles in fixed-data rate and on the last eight clock cycles in variable-data rate. In the linear mode, the serial data word is received at DIN on the first 13 clock cycles. D/D conversion is performed, and the corresponding analog sample is held on an internal sample-and-hold capacitor. This sample is transferred to the receive filter.

receive filter

The receive section of the filter provides pass-band flatness and stop-band rejection that approximates both the AT&T D3/D4 specification and CCITT recommendation G.712 when operated at the recommended frequencies. The filter contains the required compensation for the (sin x)/x response of such decoders.

receive buffer

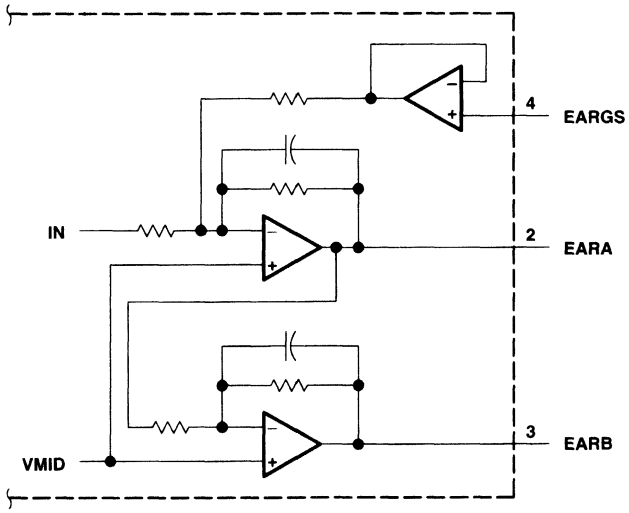
The receive buffer contains the volume control.

earphone amplifier

The earphone audio-output amplifier has a balanced output, as shown in Figure 6, to allow maximum flexibility in output configuration. The output amplifier is designed to directly drive a piezo earphone in the differential configuration without any additional external components. The output can also be used to drive a single-ended load with the output signal voltage centered around $V_{CC}/2$.

The receive-channel output level can be adjusted between specified limits by connecting an external resistor network to EARGS.

PRINCIPLES OF OPERATION



NOTE A: Terminal numbers shown are for the DW and N packages.

Figure 6. Earphone Audio-Output Amplifier Configuration and Internal Gain-Setting Network

receive data format

In the companded mode, eight bits of data are received. The sign bit is the first bit received (see Table 2).

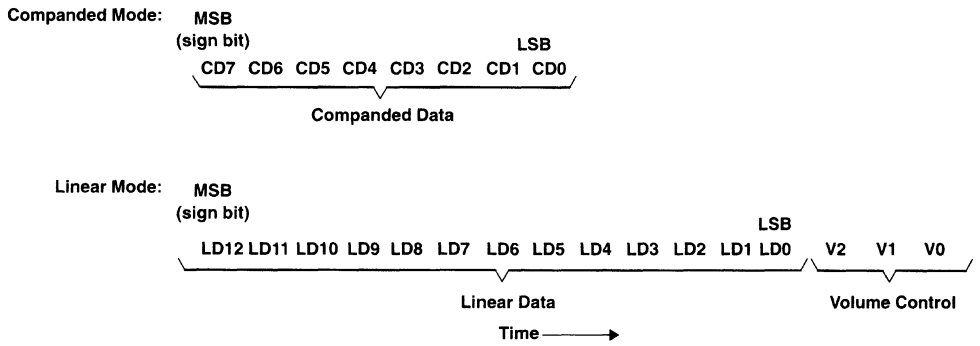
In the linear mode, 16 bits of data are received. The first 13 bits are the D/A code, and the remaining three bits form the volume control word (see Table 2). The volume control function is actually an attenuation control in which the first bit received is the most significant. The maximum volume occurs when all three volume control bits are zero. Eight levels of attenuation are selectable in 3-dB steps, giving a maximum attenuation of 21 dB when all bits are 1s. The volume control bits are not latched into the VBAP and must be present in each received data word.

PRINCIPLES OF OPERATION

Table 2. Receive-Data Bit Definitions

BIT NO.	COMPANDED MODE	LINEAR MODE
0	CD7	LD12
1	CD6	LD11
2	CD5	LD10
3	CD4	LD9
4	CD3	LD8
5	CD2	LD7
6	CD1	LD6
7	CD0	LD5
8	–	LD4
9	–	LD3
A	–	LD2
B	–	LD1
C	–	LD0
D	–	V2
E	–	V1
F	–	V0

Volume control and other control bits always follow the PCM data in time:



where:

CD7–CD0 = Data word when in companded mode
LD12–LD0 = Data word when in linear mode
V2, V1, V0 = Volume (attenuation control) 000 = maximum volume, 3 dBm0
111 = minimum volume, –18 dBm0

APPLICATION INFORMATION

output gain set design considerations (see Figure 7)

EARA and EARB are low-impedance complementary outputs. The voltages at the nodes are:

V_{O+} at EARA
V_{O-} at EARB
$V_{OD} = V_{O+} - V_{O-}$ (total differential response)

R1 and R2 are a gain-setting resistor network with the center tap connected to EARGS.

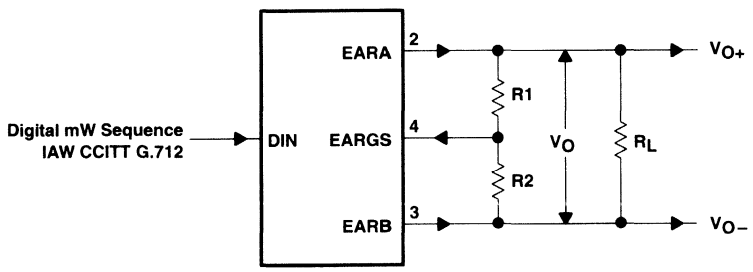
A value greater than 10 kΩ and less than 100 kΩ for R1 + R2 is recommended because of the following:

The parallel combination R1 + R2 and R_L sets the total loading. The total capacitance at EARGS and the parallel combination of R1 and R2 define a time constant that has to be minimized to avoid inaccuracies.

V_A represents the maximum available digital mW output response (V_A = 0.751 Vrms).

$$V_{OD} = A \times V_A$$

$$\text{where } A = \frac{1 + (R1/R2)}{4 + (R1/R2)}$$



NOTE A: Terminal numbers shown are for the DW and N packages.

Figure 7. Gain-Setting Configuration

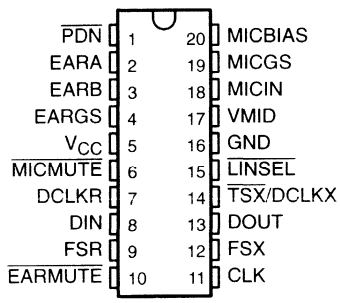
higher clock frequencies and sample rates

The VBAP is designed to work with sample rates up to 16 kHz where the frequency of the frame sync determines the sampling frequency. However, there is a fundamental requirement to maintain the ratio of the master clock frequency, f_{CLK}, to the frame sync frequency, f_{FSR}/f_{FSX}. This ratio for the VBAP is 2.6 MHz/8 kHz, or 325 master clocks per frame sync. For example, to operate the VBAP at a sampling rate of f_{FSR} and f_{FSX} equal to 16 kHz, f_{CLK} must be 325 times 16 kHz, or 5.2 MHz. If the VBAP is operated above an 8-kHz sample rate, however, it is expected that the performance becomes somewhat degraded. Exact parametric specifications for rates up to 16-kHz sample rate are not specified at this time.

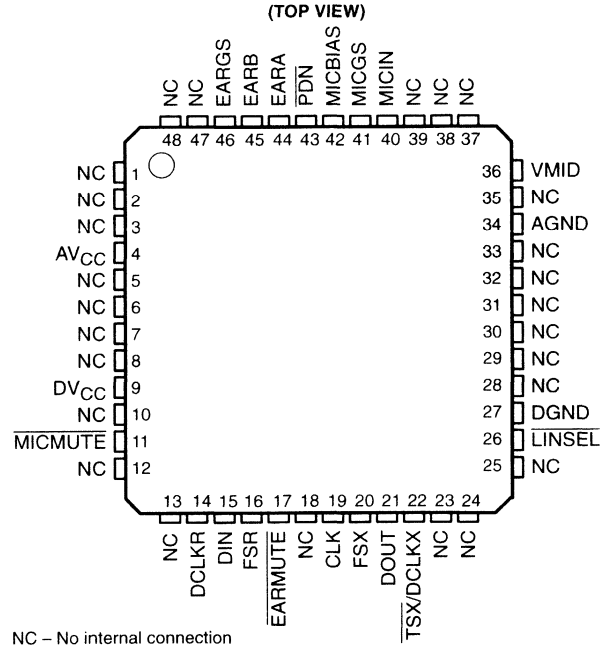
- Single 5-V Operation
- Low Power Consumption:
  - Operating Mode . . . 40 mW Typ
  - Standby Mode . . . 5 mW Typ
  - Power-Down Mode . . . 3 mW Typ
- Combined A/D, D/A, and Filters
- Extended Variable-Frequency Operation
  - Sample Rates up to 16 kHz
  - Pass-Band up to 7.2 kHz
- Electret Microphone Bias Reference Voltage Available
- Drive a Piezo Speaker Directly
- Compatible With All Digital Signal Processors (DSPs)
- Selectable Between 8-Bit Companded and 13-Bit (Dynamic Range) Linear Conversion:
  - TCM320AC56 . . . μ-Law and Linear Modes
  - TCM320AC57 . . . A-Law and Linear Modes
- Programmable Volume Control in Linear Mode
- 300 Hz – 3.6 kHz Passband with Specified Master Clock
- Designed for Standard 2.048-MHz Master Clock for U.S. Analog, U.S. Digital, and CT2, DECT, GSM, and PCS Standards for Hand-Held Battery-Powered Telephones

description

DW OR N PACKAGE
(TOP VIEW)



PT PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCT PREVIEW

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

VBAP is a trademark of Texas Instruments Incorporated.

description

The TCM320AC56 and TCM320AC57 voice-band audio processor (VBAP) integrated circuits are designed to perform the transmit encoding (A/D conversion) and receive decoding (D/A conversion) together with transmit and receive filtering for voice-band communications systems. Cellular telephone systems are targeted in particular; however, these integrated circuits can function in other systems including digital audio, telecommunications, and data acquisition.

These devices are pin-selectable for either of two modes, companded and linear, providing data in two formats. In the companded mode, data is transmitted and received in 8-bit words. In the linear mode, 13 bits of data, and either three bits of gain-setting control data, or three zero bits of padding to create a 16-bit word, are sent and received.

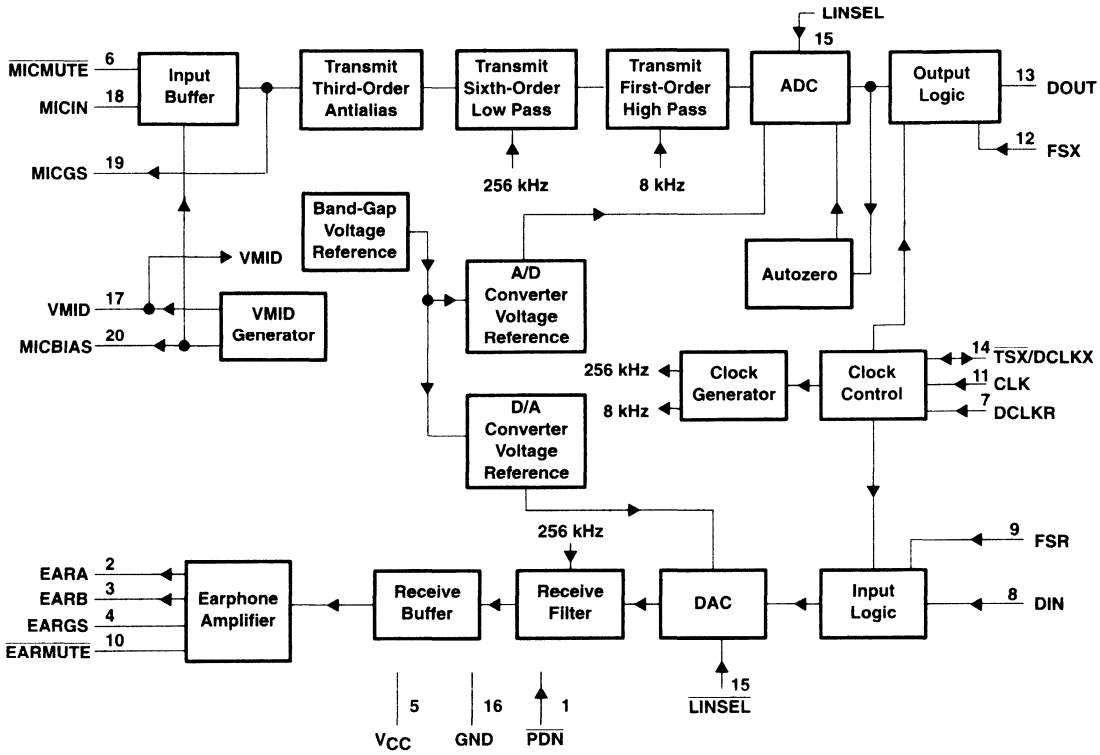
The transmit section is designed to interface directly with an electret microphone element. The microphone input signal (MICIN) is buffered and amplified with provision for setting the amplifier gain to accommodate a range of signal input levels. The amplified signal is passed through antialiasing and band-pass filters. The filtered signal is then applied to the input of a compressing analog-to-digital converter (COADC) when companded mode is selected. Otherwise, the analog-to-digital converter performs a linear conversion. The resulting data is then clocked out of DOUT as a serial data stream.

The receive section takes a frame of serial data on DIN and converts it to analog through an expanding digital-to-analog converter (EXDAC) when the companded mode is selected; otherwise, a linear conversion is performed. The analog signal then passes through switched capacitor filters, which provide out-of-band rejection, (sin x)/x correction functions, and smoothing. The filtered signal is sent to the earphone amplifier. The earphone amplifier has a differential output with adjustable gain and is designed to minimize static power dissipation.

A single on-chip high-precision band-gap circuit generates all voltage references, eliminating the need for external reference voltages. An internal reference voltage equal to $V_{CC}/2$, VMID, is used to develop the midlevel virtual ground for all the amplifier circuits and the microphone bias circuit. Another reference voltage, MICBIAS, can supply bias current for the microphone.

The TCM320AC5xC devices are characterized for operation from 0°C to 70°C. The TCM320AC5xI devices are characterized for operation from –40°C to 85°C.

functional block diagram



Terminal numbers shown are for the DW and N packages.

PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	TERMINAL NO. DW, N	TERMINAL NO. PT	I/O	DESCRIPTION
AGND	—	34		Ground return for all internal analog circuits
AV_{CC}	—	4		5-V supply voltage for all internal analog circuits
CLK	11	19	I	Clock input. In the fixed-data-rate mode, CLK is the master clock input as well as the transmit and receive data clock input . In the variable-data-rate mode, CLK is the master clock input only (digital).
DCLKR	7	14	I	Selection of fixed- or variable-data-rate operation. When DCLKR is connected to V_{CC}, the device operates in the fixed-data-rate mode. When DCLKR is not connected to V_{CC}, the device operates in the variable-data-rate mode and DCLKR becomes the receive data clock (digital).
DGND	—	27		Ground return for all internal digital circuits
DIN	8	15	I	Receive data input. Input data is clocked in on consecutive negative transitions of the receive data clock, which is CLK for a fixed data rate and DCLKR for a variable data rate (digital).
DOUT	13	21	O	Transmit data output. Transmit data is clocked out on consecutive positive transitions of the transmit data clock, which is CLK for a fixed data rate and DCLKX for a variable data rate (digital).
DV_{CC}	—	9		5-V supply voltage for all internal digital circuits
EARA	2	44	O	Earphone output. EARA forms a differential drive when used with the EARB signal (analog).
EARB	3	45	O	Earphone output. EARB forms a differential drive when used with the EARA signal (analog).
EARGS	4	46	I	Earphone gain set input of feedback signal for the earphone output. The ratio of an external potential divider network connected across EARA and EARB adjusts the power amplifier gain. Maximum gain occurs when EARGS is connected to EARB. Minimum gain occurs when EARGS is connected to EARA. Earphone frequency response correction is performed using an RC approach (analog).
$\overline{\text{EARMUTE}}$	10	17	I	Earphone output mute control signal. When $\overline{\text{EARMUTE}}$ is low, the output amplifier is disabled and no audio is sent to the earphone (digital).
FSR	9	16	I	Frame-synchronization clock input for the receive channel. In the variable-data-rate mode, this signal must remain high for the duration of the time slot. The receive channel enters the standby condition when FSR is TTL-low for five frames or longer. The device enters a production test-mode condition when either FSR or FSX is held high for five frames or longer (digital).
FSX	12	20	I	Frame synchronization clock input for the transmit channel. FSX operates independently of FSR, but also in an analogous manner to FSR. The transmit channel enters the standby condition when FSX is low for five frames or longer. The device enters a production test-mode condition when either FSX or FSR is held high for five frames or longer (digital).
GND	16	—		Ground return for all internal circuits
$\overline{\text{LINSEL}}$	15	26	I	Linear selection input. When low, $\overline{\text{LINSEL}}$ selects linear coding/decoding. When high, $\overline{\text{LINSEL}}$ selects companded coding/decoding. Companding code on the 'AC56 is μ-law, and companding code on the 'AC57 is A-law (digital).
MICBIAS	20	42	O	Microphone bias. MICBIAS voltage for the electret microphone is equal to VMID.
MICGS	19	41	O	Output of the internal microphone amplifier. MICGS is used as the feedback to set the microphone amplifier gain. If sidetone is required, it is accomplished by connecting a series network between MICGS and EARGS (analog).
MICIN	18	40	I	Microphone input. Electret microphone input to the internal microphone amplifier (analog)
$\overline{\text{MICMUTE}}$	6	11	I	Microphone input mute control signal. When $\overline{\text{MICMUTE}}$ is active (low), zero code is transmitted (dig.).
$\overline{\text{PDN}}$	1	43	I	Power-down input. When $\overline{\text{PDN}}$ is low, the device powers down to reduce power consumption (digital).
$\overline{\text{TSX}}$/DCLKX	14	22	I/O	Transmit time slot strobe (active-low output) or data clock (input) for the transmit channel. In the fixed-data-rate mode, $\overline{\text{TSX}}$/DCLKX is an open-drain output that pulls to ground and is used as an enable signal for a 3-state buffer. In the variable-data-rate mode, DCLKX becomes the transmit data clock input (digital).
V_{CC}	5	—		5-V supply voltage for all internal circuits
VMID	17	36	O	$V_{CC}/2$ bias voltage reference. A pair of external, low-leakage, high-frequency capacitors (1 μF and 470 pF) should be connected between VMID and ground for filtering.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.3 V to 7 V
Output voltage range at DOUT, V_O ..... −0.3 V to 7 V
Input voltage range at DIN, V_I ..... −0.3 V to 7 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: C suffix ..... 0°C to 70°C
I suffix ..... −40°C to 85°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage value is with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW
PT	1075 mW	7.1 mW/°C	756 mW	649 mW

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
Supply voltage, V_{CC} (see Note 3)		4.5	5.5	V
High-level input voltage, V_{IH}		2.2		V
Low-level input voltage, V_{IL}			0.8	V
Load resistance between EARA and EARB, R_L (see Note 4)		600		Ω
Load capacitance between EARA and EARB, C_L (see Note 4)			113	nF
Operating free-air temperature, T_A	TCM320AC56C, TCM320AC57C	0	70	°C
	TCM320AC56I, TCM320AC57I	−40	85	

NOTES: 2. To avoid possible damage to these CMOS devices and resulting reliability problems, the power-up sequence detailed in the system reliability features paragraph should be followed.
3. Voltages at analog inputs, outputs, and V_{CC} are with respect to GND.
4. R_L and C_L should not be applied simultaneously.

PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted)

supply current, f_{DCLKR} or f_{DCLKX} = 2.048 MHz, outputs not loaded, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
I_{CC}	Supply current from V_{CC}	Operating	$\overline{PDN}$ is high with CLK signal present		9.9	mA
		Power down	$\overline{PDN}$ is low for 500 µs		0.85	
		Standby – both	$\overline{PDN}$ is high with FSX and FSR held low		2	
		Standby – one	$\overline{PDN}$ is high with either FSX or FSR pulsing with the other held low		6	

digital interface

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	DOUT	I_{OH} = –3.2 mA, V_{CC} = 5 V	2.4	4.6		V
V_{OL}	Low-level output voltage		I_{OL} = 3.2 mA, V_{CC} = 5 V		0.2	0.4	V
I_{IH}	High-level input current, any digital input		V_I = 2.2 V to V_{CC}			10	µA
I_{IL}	Low-level input current, any digital input		V_I = 0 to 0.8 V			10	µA
C_i	Input capacitance				5		pF
C_o	Output capacitance				5		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

microphone interface

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IO}	Input offset voltage at MICIN		V_I = 0 to 5 V			±5	mV
I_{IB}	Input bias current at MICIN					±200	nA
B_1	Unity-gain bandwidth, open loop at MICIN				1		MHz
C_i	Input capacitance at MICIN				5		pF
A_V	Large-signal voltage amplification at MICGS				10000		V/V
I_{O}max	Maximum output current	VMID		1			µA
		MICBIAS (source only)		1			mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

speaker interface

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{O(PP)}$	AC output voltage				3	Vpp
V_{OO}	Output offset voltage at EARA, EARB (single-ended)	Relative to GND			80	mVpk
$I_{I(lkg)}$	Input leakage current at EARGS	V_I = 0.5 V to (V_{CC} – 0.5) V			±200	nA
I_{O}max	Maximum output current	R_L = 600 Ω			±5	mA
r_o	Output resistance at EARA, EARB			1		Ω
	Gain change	$\overline{EARMUTE}$ low, max level when muted	–80			dB

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

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transmit gain and dynamic range, companded mode (μ-law or A-law) or linear mode selected, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted) (see Notes 5 and 6)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit reference-signal level (0 dB) (see Note 7)	Companded mode selected, μ-law ('AC56)		0.982	Vrms
	Companded mode selected, A-law ('AC57)		0.985	
	Linear mode selected ('AC56 and 'AC57)		1.001	
Overload-signal level (MICIN at unity gain)	Companded mode selected, μ-law ('AC56)		4	Vpp
	Companded mode selected, A-law ('AC57)		4	
	Linear mode selected ('AC56 and 'AC57)		4	
Absolute gain error	0-dB input signal		±1	dB
Gain error with input level relative to gain at −10 dBm0	MICIN to DOUT at 3 dBm0 to −36 dBm0		±0.5	dB
	MICIN to DOUT at −37 dBm0 to −40 dBm0		±1	
	MICIN to DOUT at −41 dBm0 to −50 dBm0		±1.5	dB
	MICIN to DOUT at −51 dBm0 to −55 dBm0		±2	dB
Gain variation	V_{CC} ±10%, T_A = 0°C to 70°C		±0.5	dB

NOTES: 5. Unless otherwise noted, the analog input is 0 dB, 1020-Hz sine wave, where 0 dB is defined as the zero-reference point of the channel under test.
6. The input amplifier is set for inverting unity gain.
7. The reference-signal level, which is input to the transmit channel, is defined as a value 3 dB below the full-scale value of 2 V.

transmit filter transfer, companded mode (μ-law or A-law) or linear mode selected, over recommended ranges of supply voltage and free-air temperature, CLK = 2.048 MHz, FSX = 8 kHz (see Note 6)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to input signal gain at 1.02 kHz	Input amplifier set for unity gain, noninverting maximum gain output signal at MICIN is 0 dB	f_{MICIN} = 50 Hz	−10	0	dB
		f_{MICIN} = 200 Hz	−1.8	0	
		f_{MICIN} = 300 Hz to 3 kHz		±0.15	
		f_{MICIN} = 3.3 kHz	−0.35	0.04	
		f_{MICIN} = 3.4 kHz	−1	−0.1	
		f_{MICIN} = 4 kHz		−14	
		f_{MICIN} ≥4.6 kHz		−32	

NOTE 6. The input amplifier is set for inverting unity gain.

transmit idle channel noise and distortion, companded mode with μ-law or A-law selected, over recommended ranges of supply voltage and operating free-air temperature (see Note 8)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise, psophometrically weighted	MICIN connected to MICGS through a 10-kΩ resistor		−71	dB0p
Transmit noise, C-message weighted	MICIN connected to MICGS through a 10-kΩ resistor		10	dBrnC0
Transmit signal-to-distortion ratio with sine-wave input	MICIN to DOUT at 0 dBm0 to −17 dBm0	36		dB
	MICIN to DOUT at −18 dBm0 to −23 dBm0	34		
	MICIN to DOUT at −24 dBm0 to −29 dBm0	30		
	MICIN to DOUT at −30 dBm0 to −35 dBm0	24		
	MICIN to DOUT at −36 dBm0 to −45 dBm0	16		
Intermodulation distortion, 2-tone CCITT method, composite power level −13 dBm0	CCITT G.712 (7.1), R2	49		dB
	CCITT G.712 (7.2), R3	51		

NOTE 8: Transmit noise, linear mode: 200 μVrms is equivalent to −74 dB (referenced to device 0-dB level).

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transmit idle channel noise and distortion, linear mode selected, over recommended ranges of supply voltage and operating free-air temperature (see Notes 6 and 8)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise	MICIN connected to MICGS through a 10-kΩ resistor		200	μVrms
Transmit signal-to-distortion ratio with sine-wave input	MICIN to DOUT at 0 dBm0 to –6 dBm0	50		dB
	MICIN to DOUT at –7 dBm0 to –12 dBm0	48		
	MICIN to DOUT at –13 dBm0 to –18 dBm0	40		
	MICIN to DOUT at –19 dBm0 to –24 dBm0	35		
	MICIN to DOUT at –25 dBm0 to –40 dBm0	20		
	MICIN to DOUT at –41 dBm0 to –45 dBm0	18		

NOTES: 6. The input amplifier is set for inverting unity gain.
8. Transmit noise, linear mode: 200 μVrms is equivalent to –74 dB (referenced to device 0-dB level).

receive gain and dynamic range, companded mode (μ-law or A-law) or linear mode selected, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted) (see Notes 9 and 10)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive reference-signal level (0 dB) (see Note 11)	Companded mode selected, μ-law ('AC56)		0.736	Vrms
	Companded mode selected, A-law ('AC57)		0.739	
	Linear mode selected ('AC56 and 'AC57)		0.751	
Overload-signal level	Companded mode selected, μ-law ('AC56)		3	Vpp
	Companded mode selected, A-law ('AC57)		3	
	Linear mode selected ('AC56 and 'AC57)		3	
Absolute gain error	0-dB input signal		±1	dB
Gain error with output level relative to gain at –10 dBm0	DIN to EARA and EARB at 3 dBm0 to –36 dBm0		±0.5	dB
	DIN to EARA and EARB at –37 dBm0 to –40 dBm0		±1	
	DIN to EARA and EARB at –41 dBm0 to –50 dBm0		±1.5	
	DIN to EARA and EARB at –51 dBm0 to –55 dBm0		±2	
Gain variation	V_{CC} ±10%, T_A = 0°C to 70°C		±0.5	dB

NOTES: 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.
10. Unless otherwise noted, the digital input is a word stream generated by passing a 0-dB sine wave at 1020 Hz through an ideal encoder, where 0 dB is defined as the zero reference.
11. This reference-signal level is measured at the speaker output of the receive channel with the gain of the output speaker amplifier set to unity.

receive filter transfer, companded mode (μ-law or A-law) or linear mode selected, over recommended ranges of supply voltage and operating free-air temperature, FSR = 8 kHz (see Note 9)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	DIN = 0 dBm0	f_{DIN} = < 200 Hz		0.15	dB
		f_{DIN} = 200 Hz	–0.5	0.15	
		f_{DIN} = 300 Hz to 3 kHz		±0.15	
		f_{DIN} = 3.3 kHz	–0.35	0.03	
		f_{DIN} = 3.4 kHz	–1	–0.18	
		f_{DIN} = 4 kHz		–14	
		f_{DIN} = > 4.6 kHz		–30	

NOTE 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.

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receive idle channel noise and distortion, companded mode with μ-law or A-law selected, over recommended ranges of supply voltage and operating free-air temperature (see Note 9)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive noise, psophometrically weighted	DIN = 11010101 (A-law)		–75	dB0p
Receive noise, C-message weighted	DIN = 11111111 (μ-law)		5	dBrnc0
Receive signal-to-distortion ratio with sine-wave input	DIN to EARA and EARB at 0 dBm0 to –18 dBm0	36		dB
	DIN to EARA and EARB at –19 dBm0 to –24 dBm0	34		
	DIN to EARA and EARB at –25 dBm0 to –30 dBm0	30		
	DIN to EARA and EARB at –31 dBm0 to –38 dBm0	23		
	DIN to EARA and EARB at –39 dBm0 to –45 dBm0	17		

NOTE 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.

receive idle channel noise and distortion, linear mode selected, over recommended ranges of supply voltage and operating free-air temperature (see Notes 9 and 12)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive noise	DIN = 00000000		200	μVrms
Receive signal-to-distortion ratio with sine-wave input	DIN to EARA and EARB at 0 dBm0 to –6 dBm0	50		dB
	DIN to EARA and EARB at –7 dBm0 to –12 dBm0	48		
	DIN to EARA and EARB at –13 dBm0 to –18 dBm0	38		
	DIN to EARA and EARB at –19 dBm0 to –24 dBm0	32		
	DIN to EARA and EARB at –25 dBm0 to –40 dBm0	18		
	DIN to EARA and EARB at –41 dBm0 to –45 dBm0	15		
Intermodulation, 2-tone CCITT distortion method, composite power level –13 dBm0	CCITT G.712 (7.1), R2	50		dB
	CCITT G.712 (7.2), R3	54		

NOTES: 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.
12. Receive noise, linear mode: 200 μVrms is equivalent to –71 dB (referenced to device 0-dB level).

power supply rejection and crosstalk attenuation over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Supply voltage rejection, transmit channel	Idle channel, supply signal = 100 mVrms, f = 0 to 30 kHz (measured at DOUT)		–30		dB
Supply voltage rejection, receive channel	Idle channel, supply signal = 100 mVrms, EARGS connected to EARB, f = 0 to 30 kHz (measured differentially between EARA and EARB)		–30		dB
Crosstalk attenuation, transmit-to-receive (differential)	MICIN = 0 dB, f = 1.02 kHz, unity transmit gain, EARGS connected to EARB, measured differentially between EARA and EARB	68			dB
Crosstalk attenuation, receive-to-transmit	DIN = 0 dBm0, f = 1.02 kHz, unity transmit gain, measured at DOUT	68			dB

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

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timing requirements

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figure 1 through Figure 4)

		MIN	NOM†	MAX	UNIT
t_t	Transition time, CLK and DCLKX/DCLKR			10	ns
	Duty cycle, CLK	45%	50%	55%	
	Duty cycle, DCLKX/DCLKR	45%	50%	55%	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 2)

		MIN	MAX	UNIT
$t_{su(FSX)}$	Setup time, FSX high before CLK↓	20	468	ns
$t_{h(FSX)}$	Hold time, FSX high after CLK↓	20	468	ns

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 1)

		MIN	MAX	UNIT
$t_{su(FSR)}$	Setup time, FSR high before CLK↓	20	468	ns
$t_{h(FSR)}$	Hold time, FSR high after CLK↓	20	468	ns
$t_{su(DIN)}$	Setup time, DIN high or low before CLK↓	20		ns
$t_{h(DIN)}$	Hold time, DIN high or low after CLK↓	20		ns

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see Figure 4)

		MIN	MAX	UNIT
$t_{su(FSX)}$	Setup time, FSX high before DCLKX↓	40	$t_{c(DCLKX)}-40$	ns
$t_{h(FSX)}$	Hold time, FSX high after DCLKX↓	35	$t_{c(DCLKX)}-35$	ns

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see Figure 3)

		MIN	MAX	UNIT
$t_{su(FSR)}$	Setup time, FSR high before DCLKR↓	40		ns
$t_{h(FSR)}$	Hold time, FSR high after DCLKR↓	35	$t_{c(DCLKR)}-35$	ns
$t_{su(DIN)}$	Setup time, DIN high or low before DCLKR↓	30		ns
$t_{h(DIN)}$	Hold time, DIN high or low after DCLKR↓	30		ns

switching characteristics

propagation delay times over recommended ranges of operating conditions, fixed-data-rate mode, C_L = 0 to 10 pF (see Figure 2)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	From CLK bit 1 high to DOUT bit 1 valid			35	ns
t_{pd2}	From CLK high to DOUT valid, bits 2 to n			35	ns
t_{pd3}	From CLK bit n low to DOUT bit n Hi-Z		30		ns
t_{pd4}	From CLK bit 1 high to $\overline{TSX}$ active (low)	R_{pullup} = 1.24 kΩ		40	ns
t_{pd5}	From CLK bit n low to $\overline{TSX}$ inactive (high)	R_{pullup} = 1.24 kΩ	30		ns

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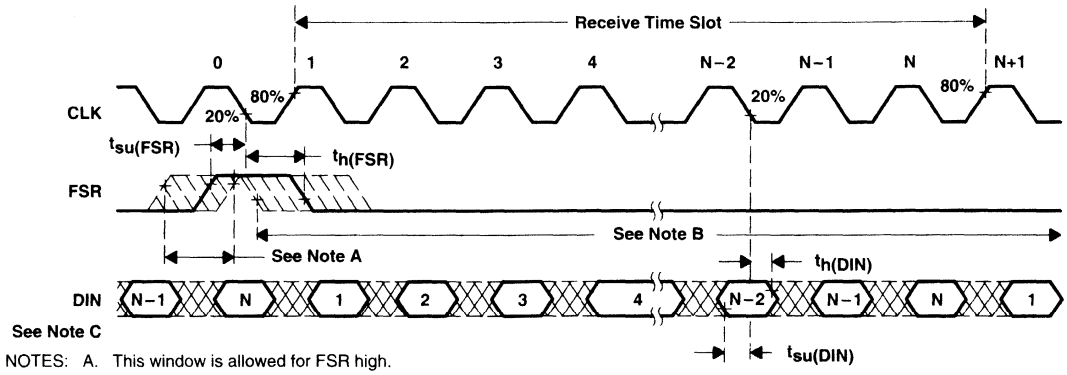
propagation delay times over recommended ranges of operating conditions, variable-data-rate mode (see Figure 4)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd6}	FSX high to DOUT bit 1 valid	C_L = 0 to 10 pF		30	ns
t_{pd7}	DCLKX high to DOUT valid, bits 2 to n	C_L = 0 to 10 pF		40	ns
t_{pd8}	FSX low to DOUT bit n Hi-Z		20		ns

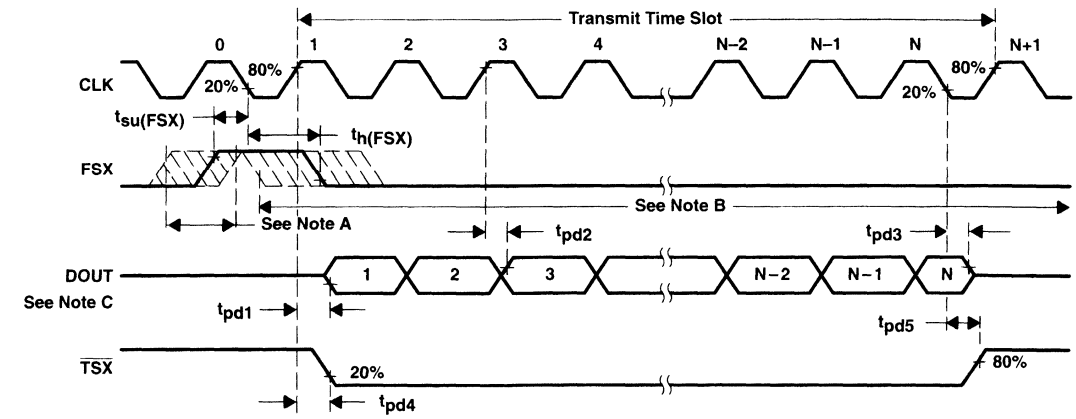
PARAMETER MEASUREMENT INFORMATION

All timing parameters are referenced to V_{IH} and V_{IL}. Bit 1 = MSB (most significant bit) and is clocked in first on DIN or clocked out first on DOUT. Bit n = LSB (least significant bit) and is clocked in last on DIN or is clocked out last on DOUT. N = 8 for the companded mode, and N = 16 for the linear mode.



NOTES: A. This window is allowed for FSR high.
B. This window is allowed for FSR low.
C. Transitions are measured at 50%.

Figure 1. Fixed-Data Rate Mode, Receive Side Timing Diagram



NOTES: A. This window is allowed for FSX high.
B. This window is allowed for FSX low ($t_{h(FSX)}$ max determined by data collision considerations).
C. Transitions are measured at 50%.

Figure 2. Fixed-Data Rate Mode, Transmit Side Timing Diagram

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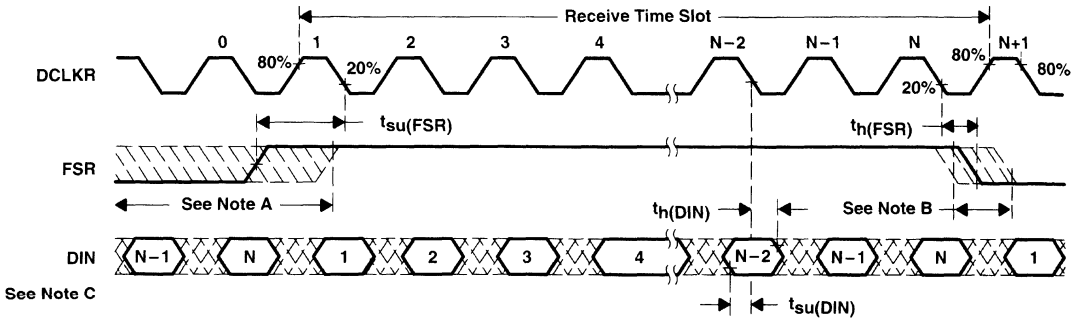
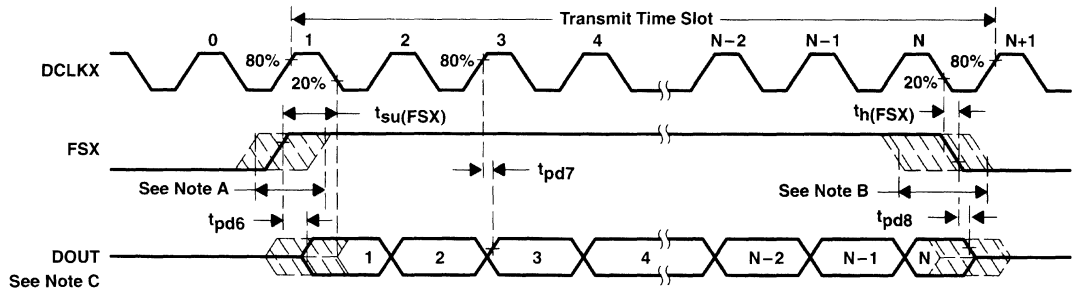
PARAMETER MEASUREMENT INFORMATION



NOTES: A. This window is allowed for FSR high ($t_{su(FSR)}$ max determined by data collision considerations).
B. This window is allowed for FSR low.
C. Transitions are measured at 50%.

Figure 3. Variable-Data Rate Mode, Receive Side Timing Diagram



NOTES: A. This window is allowed for FSX high.
B. This window is allowed for FSX low without data repetition.
C. Transitions are measured at 50%.

Figure 4. Variable-Data Rate Mode, Transmit Side Timing Diagram

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PRINCIPLES OF OPERATION

general

system reliability features

The device should be powered up and initialized as follows:

1. Apply GND.
2. Apply V_{CC}.
3. Connect all clocks.
4. Apply TTL high to $\overline{PDN}$.
5. Apply synchronizing pulses to FSX and/or FSR.

Even though the VBAP is heavily protected against latch-up, it is still possible to cause it to latch up under certain improper power conditions. To help ensure that latch-up does not occur, a reverse-biased Schottky diode (with a forward voltage drop of less than or equal to 0.4 V — 1N5711 or equivalent) should be connected between V_{CC} (power supply) and GND.

On the transmit channel, digital outputs DOUT and $\overline{TSX}$ are held in the high-impedance state for approximately four frames (500 μs) after power up or application of V_{CC}. After this delay, DOUT, $\overline{TSX}$, and signaling are functional and occur in the correct time slot. The analog circuits on the transmit side require approximately 60 ms to reach their equilibrium value due to the autozero circuit settling time. To further enhance system integrity, DOUT and $\overline{TSX}$ are placed in the high-impedance state after an interruption of CLK.

power-down and standby operations

To minimize power consumption, a power-down mode and three standby modes are provided.

For power down, an external low signal is applied to $\overline{PDN}$. In the absence of a signal, $\overline{PDN}$ is internally pulled up to a high logic level and the device remains active. In the power-down mode, the average power consumption is reduced to 3 mW.

Three standby modes give the user the option of placing the entire device on standby, placing only the transmit channel on standby, or placing only the receive channel on standby. To place the entire device on standby, both FSX and FSR are held low. For transmit-only operation (receive channel on standby), FSX is pulsing and FSR is held low. For receive-only operation (transmit section on standby), FSR is pulsing and FSX is held low. When the entire device is in standby mode, power consumption is reduced to 5 mW. See Table 1 for power-down and standby procedures.

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PRINCIPLES OF OPERATION

Table 1. Power-Down and Standby Procedures

DEVICE STATUS	PROCEDURE	TYPICAL POWER CONSUMPTION	DIGITAL OUTPUT STATUS
Power on	$\overline{PDN}$ = high, FSX = pulses, FSR = pulses	40 mW	Digital outputs active but not loaded
Power down	$\overline{PDN}$ = low, FSX, FSR = X†	13 mW	$\overline{TSX}$ and DOUT in the high-impedance state
Entire device on standby mode	$\overline{FSX}$ = low, $\overline{FSR}$ = low, $\overline{PDN}$ = high	5 mW	$\overline{TSX}$ and DOUT in the high-impedance state
Only transmit channel in standby mode	$\overline{FSX}$ = low, FSR = pulses, $\overline{PDN}$ = high	20 mW	$\overline{TSX}$ and DOUT in the high-impedance state within five frames
Only receive channel in standby mode	$\overline{FSR}$ = low, $\overline{FSX}$ = pulses, $\overline{PDN}$ = high	20 mW	Digital outputs active but not loaded

† X = don't care

PRODUCT PREVIEW

fixed-data-rate timing

Fixed-data-rate timing is selected by connecting $\overline{DCLKR}$ to V_{CC} and uses the master clock (CLK), frame synchronization clocks (FSX and FSR), and the $\overline{TSX}$ output. FSX and FSR are inputs that set the sampling frequency. Data is transmitted on DOUT on the positive transitions of CLK following the rising edge of FSX. Data is received on DIN on the falling edges of CLK following FSR. A D/A conversion is performed on the received digital word, and the resulting analog sample is held on an internal sample-and-hold capacitor until transferred to the receive filter. The data word is eight bits long in the companded mode and 16 bits long in the linear mode.

variable-data-rate timing

Variable-data-rate timing is selected by connecting DCLKR to the receive data clock. In this mode, the master clock (CLK) controls the switched-capacitor filters, while data transfer into DIN and out of DOUT is controlled by DCLKR and DCLKX respectively. This allows the data to be transferred in and out of the device at any rate up to the frequency of the master clock. DCLKR and DCLKX must be synchronous with CLK.

While the FSX input is high, data is transmitted from DOUT on consecutive positive transitions of DCLKX. Similarly, while the FSR input is high, the data word is received at DIN on consecutive negative transitions of DCLKR. The transmitted data word at DOUT is repeated in all remaining time slots in the frame as long as DCLKX is pulsed and FSX is held high. This feature, which allows the data word to be transmitted more than once per frame, is available only with variable-data-rate timing.

asynchronous operations

To avoid crosstalk problems associated with special interrupt circuits, the design includes separate converters, filters, and voltage references on the transmit and receive sides to allow completely independent operation of the two channels. In either timing mode, the master clock, data clock, and time-slot strobe must be synchronized at the beginning of each frame.

precision voltage references

A precision band-gap reference voltage is generated internally and is used to supply all the references required for operation of both the transmit and receive channels. The gain in each channel is trimmed during the manufacturing process. This ensures very accurate, stable gain performance over variations in supply voltage and device temperature.

PRINCIPLES OF OPERATION

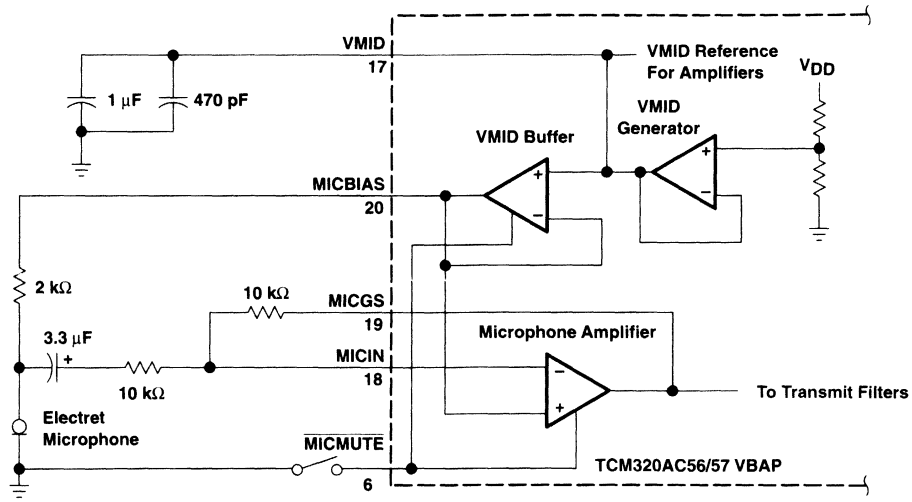
conversion laws

The TCM320AC56 provides μ-law companding operation that approximates the CCITT G.711 recommendation. The TCM320AC57 provides A-law companding operation that approximates the CCITT G.711 recommendation. The linear mode of operation uses a 13-bit two's-complement format and is the same for both the TCM320AC56 and the TCM320AC57.

transmit operation

microphone input

The microphone input amplifier is designed specifically to interface to electret-type microphone elements, as shown in Figure 5. The VMID buffer circuit provides a voltage (MICBIAS) equal to 1/2 V_{CC} as a reference for the microphone amplifier and a bias voltage to the electret microphone. The microphone amplifier output (MICGS) is used in conjunction with a feedback network and applied to the amplifier inverting input (MICIN) to set the amplifier gain. VMID appears at a terminal to provide a place to filter the VMID voltage.



NOTE A: Terminal numbers shown are for the DW and N packages.

Figure 5. Typical Microphone Interface

microphone mute function

The $\overline{\text{MICMUTE}}$ input causes the digital circuitry to transmit all zero code on DOUT.

transmit filter

A low-pass antialiasing section is included on the device and achieves a 35-dB attenuation at the sampling frequency. No external components are required to provide the necessary antialiasing function for the switched-capacitor section of the transmit filter.

PRODUCT PREVIEW

PRINCIPLES OF OPERATION

encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample-and-hold capacitor. The encoder performs an A/D conversion on a switched-capacitor array. Digital data representing the sample is transmitted on the first 8 or 16 data clock cycles of the next frame.

The autozero circuit corrects for dc offset on the input signal to the encoder using the sign-bit averaging technique. The sign bit from the encoder output is long-term averaged and subtracted from the input to the encoder.

data word structure

The data word is eight bits long in the companded mode and all eight bits represent one audio data sample. The sign bit is the first bit transmitted.

The data word is 16 bits long in the linear mode. The first 13 bits comprise the audio data sample, and the last three bits form the volume control word in the receive direction (DIN) and are zero pad bits in the transmit direction (DOUT). The sign bit is transmitted first.

receive operation

decoding

In the companded mode, the serial data word is received at DIN on the first eight clock cycles in fixed-data rate and on the last eight clock cycles in variable-data rate. In the linear mode, the serial data word is received at DIN on the first 13 clock cycles. D/A conversion is performed, and the corresponding analog sample is held on an internal sample-and-hold capacitor. This sample is transferred to the receive filter.

receive filter

The receive section of the filter provides pass-band flatness and stop-band rejection that approximates both the AT&T D3/D4 specification and CCITT recommendation G.712 when operated at the recommended frequencies. The filter contains the required compensation for the (sin x)/x response of such decoders.

receive buffer

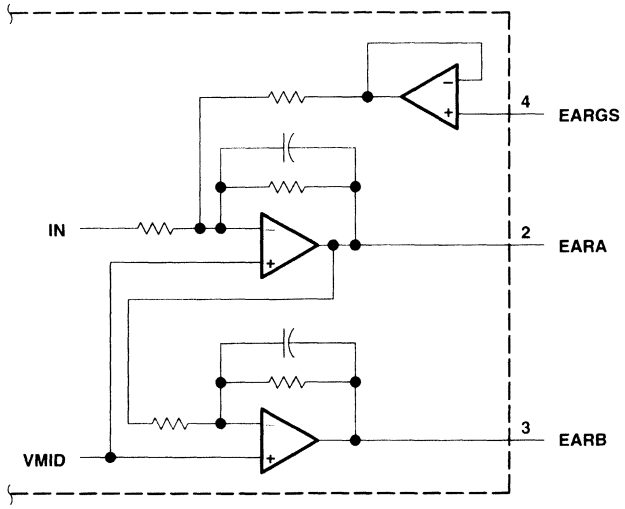
The receive buffer contains the volume control.

earphone amplifier

The earphone audio-output amplifier has a balanced output, as shown in Figure 6, to allow maximum flexibility in output configuration. The output amplifier is designed to directly drive a piezo earphone in the differential configuration without any additional external components. The output can also be used to drive a single-ended load with the output signal voltage centered around $V_{CC}/2$.

The receive-channel output level can be adjusted between specified limits by connecting an external resistor network to EARGS.

PRINCIPLES OF OPERATION



NOTE A: Terminal numbers shown are for the DW and N packages.

Figure 6. Earphone Audio-Output Amplifier Configuration and Internal Gain-Setting Network

receive data format

In the companded mode, eight bits of data are received. The sign bit is the first bit received (see Table 2).

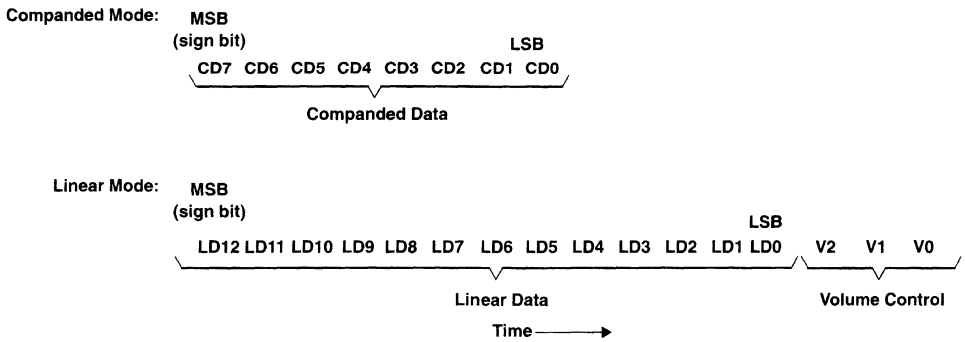
In the linear mode, 16 bits of data are received. The first 13 bits are the D/A code, and the remaining three bits form the volume control word (see Table 2). The volume control function is actually an attenuation control in which the first bit received is the most significant. The maximum volume occurs when all three volume control bits are zero. Eight levels of attenuation are selectable in 3-dB steps, giving a maximum attenuation of 21 dB when all bits are 1s. The volume control bits are not latched into the VBAP and must be present in each received data word.

PRINCIPLES OF OPERATION

Table 2. Receive-Data Bit Definitions

BIT NO.	COMPANDED MODE	LINEAR MODE
0	CD7	LD12
1	CD6	LD11
2	CD5	LD10
3	CD4	LD9
4	CD3	LD8
5	CD2	LD7
6	CD1	LD6
7	CD0	LD5
8	–	LD4
9	–	LD3
A	–	LD2
B	–	LD1
C	–	LD0
D	–	V2
E	–	V1
F	–	V0

Volume control and other control bits always follow the PCM data in time:



where:

CD7–CD0 = Data word when in companded mode
LD12–LD0= Data word when in linear mode
V2, V1, V0 = Volume (attenuation control) 000 = maximum volume, 3 dBm0
111 = minimum volume, –18 dBm0

PRODUCT PREVIEW

APPLICATION INFORMATION

output gain set design considerations (see Figure 7)

EARA and EARB are low-impedance complementary outputs. The voltages at the nodes are:
V_{O+} at EARA
V_{O-} at EARB
$V_{OD} = V_{O+} - V_{O-}$ (total differential response)

R1 and R2 are a gain-setting resistor network with the center tap connected to EARGS.

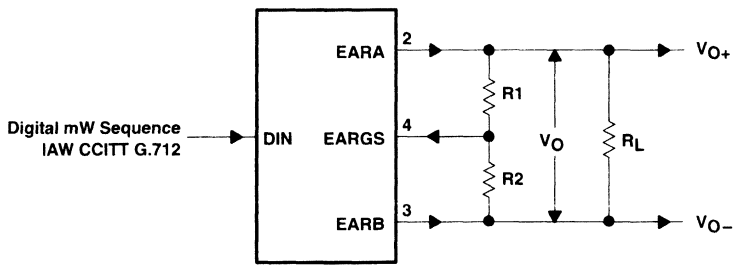
A value greater than 10 kΩ and less than 100 kΩ for R1 + R2 is recommended because of the following:

The parallel combination R1 + R2 and R_L sets the total loading. The total capacitance at EARGS and the parallel combination of R1 and R2 define a time constant that has to be minimized to avoid inaccuracies.

V_A represents the maximum available digital mW output response (V_A = 0.751 Vrms).

$$V_{OD} = A \times V_A$$

$$\text{where } A = \frac{1 + (R1/R2)}{4 + (R1/R2)}$$



NOTE A: Terminal numbers shown are for the DW and N packages.

Figure 7. Gain-Setting Configuration

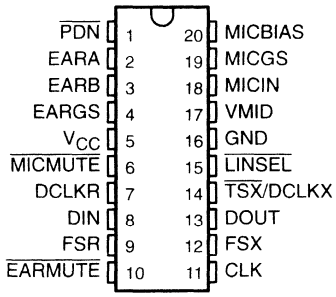
higher clock frequencies and sample rates

The VBAP is designed to work with sample rates up to 16 kHz where the frequency of the frame sync determines the sampling frequency. However, there is a fundamental requirement to maintain the ratio of the master clock frequency, f_{CLK}, to the frame sync frequency, f_{FSR}/f_{FSX}. This ratio for the VBAP is 2.048 MHz/8 kHz, or 256 master clocks per frame sync. For example, to operate the VBAP at a sampling rate of f_{FSR} and f_{FSX} equal to 16 kHz, f_{CLK} must be 256 times 16 kHz, or 4.096 MHz. If the VBAP is operated above an 8-kHz sample rate, however, it is expected that the performance becomes somewhat degraded. Exact parametric specifications for rates up to 16-kHz sample rate are not specified at this time.

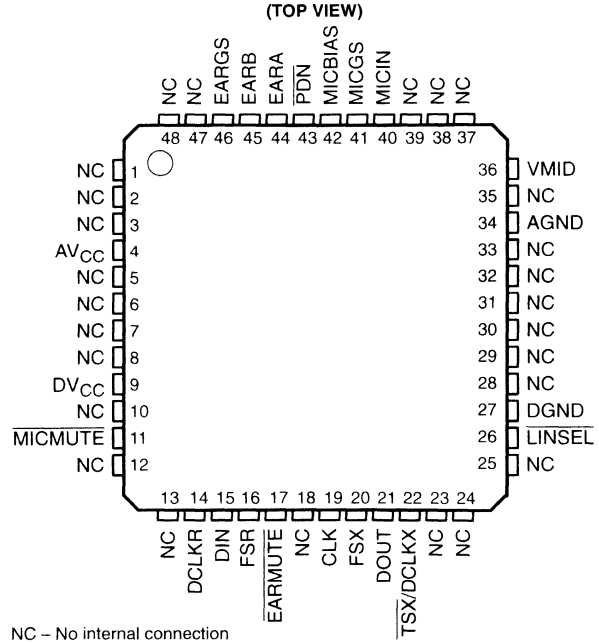
PRODUCT PREVIEW

- **Single 3-V Operation**
- **Low Power Consumption:**
  - **Operating Mode . . . 20 mW Typ**
  - **Standby Mode . . . 5 mW Typ**
  - **Power-Down Mode . . . 2 mW Typ**
- **Combined A/D, D/A, and Filters**
- **Extended Variable-Frequency Operation**
  - **Sample Rates up to 16 kHz**
  - **Pass-Band up to 7.2 kHz**
- **Electret Microphone Bias Reference Voltage Available**
- **Drive a Piezo Speaker Directly**
- **Compatible With All Digital Signal Processors (DSPs)**
- **Selectable Between 8-Bit Companded and 13-Bit (Dynamic Range) Linear Conversion:**
  - **TLV320AC36 . . . μ-Law and Linear Modes**
  - **TLV320AC37 . . . A-Law and Linear Modes**
- **Programmable Volume Control in Linear Mode**
- **300 Hz – 3.6 kHz Passband with Specified Master Clock**
- **Designed for Standard 2.048-MHz Master Clock for U.S. Analog, U.S. Digital, CT2, DECT, GSM, and PCS Standards for Hand-Held Battery-Powered Telephones**

DW OR N PACKAGE
(TOP VIEW)



PT PACKAGE
(TOP VIEW)



NC – No internal connection

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

VBAP is a trademark of Texas Instruments Incorporated.

description

The TLV320AC36 and TLV320AC37 voice-band audio processor (VBAP) integrated circuits are designed to perform the transmit encoding (A/D conversion) and receive decoding (D/A conversion) together with transmit and receive filtering for voice-band communications systems. Cellular telephone systems are targeted in particular; however, these integrated circuits can function in other systems including digital audio, telecommunications, and data acquisition.

These devices are pin-selectable for either of two modes, companded and linear, providing data in two formats. In the companded mode, data is transmitted and received in 8-bit words. In the linear mode, 13 bits of data, and either three bits of gain-setting control data, or three zero bits of padding to create a16-bit word, are sent and received.

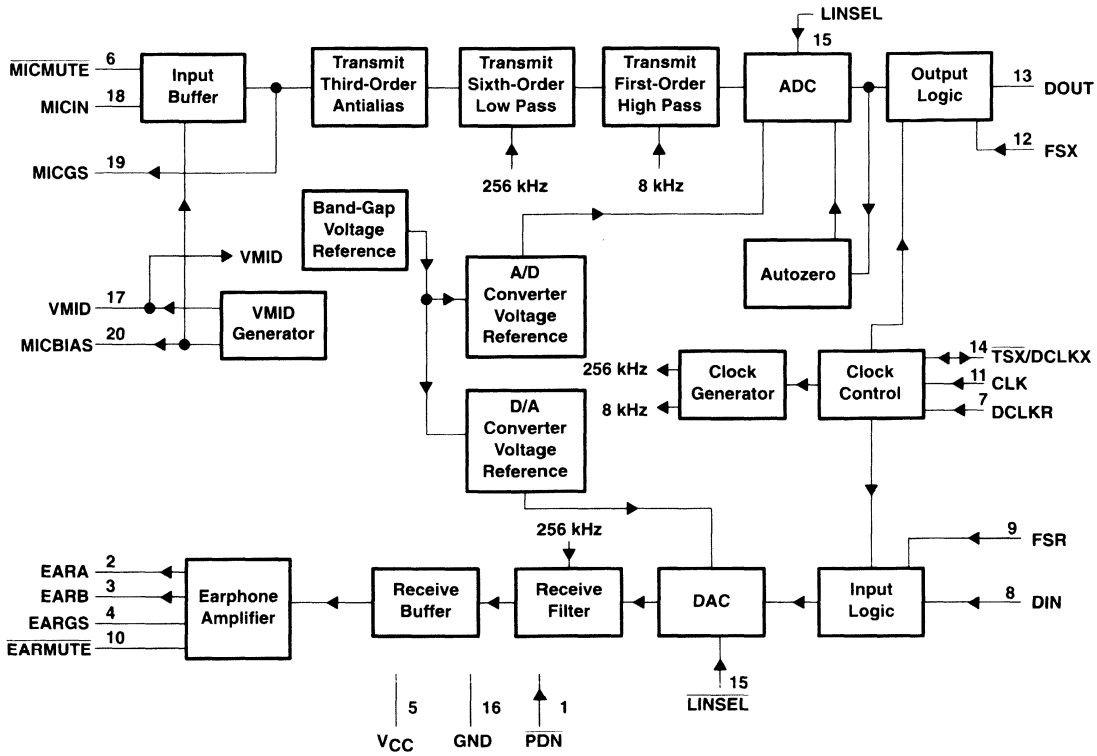
The transmit section is designed to interface directly with an electret microphone element. The microphone input signal (MICIN) is buffered and amplified with provision for setting the amplifier gain to accommodate a range of signal input levels. The amplified signal is passed through antialiasing and band-pass filters. The filtered signal is then applied to the input of a compressing analog-to-digital converter (COADC) when companded mode is selected. Otherwise, the analog-to-digital converter performs a linear conversion. The resulting data is then clocked out of DOUT as a serial data stream.

The receive section takes a frame of serial data on DIN and converts it to analog through an expanding digital-to-analog converter (EXDAC) when the companded mode is selected; otherwise, a linear conversion is performed. The analog signal then passes through switched capacitor filters, which provide out-of-band rejection, (sin x)/x correction functions, and smoothing. The filtered signal is sent to the earphone amplifier. The earphone amplifier has a differential output with adjustable gain and is designed to minimize static power dissipation.

A single on-chip high-precision band-gap circuit generates all voltage references, eliminating the need for external reference voltages. An internal reference voltage equal to $V_{CC}/2$, VMID, is used to develop the midlevel virtual ground for all the amplifier circuits and the microphone bias circuit. Another reference voltage, MICBIAS, can supply bias current for the microphone.

The TLV320AC3xC devices are characterized for operation from 0°C to 70°C. The TLV320AC3xI devices are characterized for operation from −40°C to 85°C.

functional block diagram



NOTE A: Terminal numbers shown are for the DW and N packages.

Terminal Functions

TERMINAL NAME	NO. DW, N	NO. PT	I/O	DESCRIPTION
AGND	—	34		Ground return for all internal analog circuits
AV_{CC}	—	4		3-V supply voltage for all internal analog circuits
CLK	11	19	I	Clock input. In the fixed-data-rate mode, CLK is the master clock input as well as the transmit and receive data clock input . In the variable-data-rate mode, CLK is the master clock input only (digital).
DCLKR	7	14	I	Selection of fixed- or variable-data-rate operation. When DCLKR is connected to V_{CC}, the device operates in the fixed-data-rate mode. When DCLKR is not connected to V_{CC}, the device operates in the variable-data-rate mode and DCLKR becomes the receive data clock (digital).
DGND	—	27		Ground return for all internal digital circuits
DIN	8	15	I	Receive data input. Input data is clocked in on consecutive negative transitions of the receive data clock, which is CLK for a fixed data rate and DCLKR for a variable data rate (digital).
DOUT	13	21	O	Transmit data output. Transmit data is clocked out on consecutive positive transitions of the transmit data clock, which is CLK for a fixed data rate and DCLKX for a variable data rate (digital).
DV_{CC}	—	9		3-V supply voltage for all internal digital circuits
EARA	2	44	O	Earphone output. EARA forms a differential drive when used with the EARB signal (analog).
EARB	3	45	O	Earphone output. EARB forms a differential drive when used with the EARA signal (analog).
EARGS	4	46	I	Earphone gain set input of feedback signal for the earphone output. The ratio of an external potential divider network connected across EARA and EARB adjusts the power amplifier gain. Maximum gain occurs when EARGS is connected to EARB. Minimum gain occurs when EARGS is connected to EARA. Earphone frequency response correction is performed using an RC approach (analog).
$\overline{\text{EARMUTE}}$	10	17	I	Earphone output mute control signal. When $\overline{\text{EARMUTE}}$ is low, the output amplifier is disabled and no audio is sent to the earphone (digital).
FSR	9	16	I	Frame-synchronization clock input for the receive channel. In the variable-data-rate mode, this signal must remain high for the duration of the time slot. The receive channel enters the standby condition when FSR is TTL-low for five frames or longer. The device enters a production test-mode condition when either FSR or FSX is held high for five frames or longer (digital).
FSX	12	20	I	Frame synchronization clock input for the transmit channel. FSX operates independently of FSR, but also in an analogous manner to FSR. The transmit channel enters the standby condition when FSX is low for five frames or longer. The device enters a production test-mode condition when either FSX or FSR is held high for five frames or longer (digital).
GND	16	—		Ground return for all internal circuits
$\overline{\text{LINSEL}}$	15	26	I	Linear selection input. When low, $\overline{\text{LINSEL}}$ selects linear coding/decoding. When high, $\overline{\text{LINSEL}}$ selects companded coding/decoding. Companding code on the 'AC36 is μ-law, and companding code on the 'AC37 is A-law (digital).
MICBIAS	20	42	O	Microphone bias. MICBIAS voltage for the electret microphone is equal to VMID.
MICGS	19	41	O	Output of the internal microphone amplifier. MICGS is used as the feedback to set the microphone amplifier gain. If sidetone is required, it is accomplished by connecting a series network between MICGS and EARGS (analog).
MICIN	18	40	I	Microphone input. Electret microphone input to the internal microphone amplifier (analog)
$\overline{\text{MICMUTE}}$	6	11	I	Microphone input mute control signal. When $\overline{\text{MICMUTE}}$ is active (low), zero code is transmitted (dig.).
$\overline{\text{PDN}}$	1	43	I	Power-down input. When $\overline{\text{PDN}}$ is low, the device powers down to reduce power consumption (digital).
$\overline{\text{TSX}}$/DCLKX	14	22	I/O	Transmit time slot strobe (active-low output) or data clock (input) for the transmit channel. In the fixed-data-rate mode, $\overline{\text{TSX}}$/DCLKX is an open-drain output that pulls to ground and is used as an enable signal for a 3-state buffer. In the variable-data-rate mode, DCLKX becomes the transmit data clock input (digital).
V_{CC}	5	—		3-V supply voltage for all internal circuits
VMID	17	36	O	$V_{CC}/2$ bias voltage reference. A pair of external, low-leakage, high-frequency capacitors (1 μF and 470 pF) should be connected between VMID and ground for filtering.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.3 V to 5.5 V
Output voltage range at DOUT, V_O . . . . . −0.3 V to 5.5 V
Input voltage range at DIN, V_I . . . . . −0.3 V to 5.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: C suffix . . . . . 0°C to 70°C
I suffix . . . . . −40°C to 85°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage value is with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW
PT	1075 mW	7.1 mW/°C	756 mW	649 mW

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
Supply voltage, V_{CC} (see Note 3)		2.7	3.3	V
High-level input voltage, V_{IH}		2.2		V
Low-level input voltage, V_{IL}			0.8	V
Load resistance between EARA and EARB, R_L (see Note 4)		600		Ω
Load capacitance between EARA and EARB, C_L (see Note 4)			50	nF
Operating free-air temperature, T_A	TLV320AC36C, TLV320AC37C	0	70	°C
	TLV320AC36I, TLV320AC37I	−40	85	

NOTES: 2. To avoid possible damage to these CMOS devices and resulting reliability problems, the power-up sequence detailed in the system reliability features paragraph should be followed.
3. Voltages at analog inputs, outputs, and V_{CC} are with respect to GND.
4. R_L and C_L should not be applied simultaneously.

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted)

supply current, f_{DCLKR} or f_{DCLKX} = 2.048 MHz, outputs not loaded, V_{CC} = 3 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
I_{CC}	Supply current from V_{CC}	Operating	$\overline{PDN}$ is high with CLK signal present		7.5	mA
		Power down	$\overline{PDN}$ is low for 500 µs		0.75	
		Standby – both	$\overline{PDN}$ is high with FSX and FSR held low		2	
		Standby – one	$\overline{PDN}$ is high with either FSX or FSR pulsing with the other held low		4.5	

digital interface

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	DOUT	I_{OH} = –3.2 mA, V_{CC} = 3 V	2.4	2.8		V
V_{OL}	Low-level output voltage		I_{OL} = 3.2 mA, V_{CC} = 3 V		0.2	0.4	V
I_{IH}	High-level input current, any digital input		V_I = 2.2 V to V_{CC}			10	µA
I_{IL}	Low-level input current, any digital input		V_I = 0 to 0.8 V			10	µA
C_i	Input capacitance				5		pF
C_o	Output capacitance				5		pF

† All typical values are at V_{CC} = 3 V, T_A = 25°C.

microphone interface

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IO}	Input offset voltage at MICIN		V_I = 0 to 3 V			±5	mV
I_{IB}	Input bias current at MICIN					±200	nA
B_1	Unity-gain bandwidth, open loop at MICIN‡				1.5		MHz
C_i	Input capacitance at MICIN				5		pF
A_V	Large-signal voltage amplification at MICGS				10000		V/V
I_{O}max	Maximum output current	VMID		3			µA
		MICBIAS (source only)		1			mA

† All typical values are at V_{CC} = 3 V, T_A = 25°C.
‡ The frequency of the first pole is 100 Hz.

speaker interface

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{O(PP)}$	AC output voltage				3§	Vpp
V_{OO}	Output offset voltage at EARA, EARB (single-ended)	Relative to GND			80	mVpk
$I_{I(lkg)}$	Input leakage current at EARGS	V_I = 0.5 V to (V_{CC} – 0.5) V			±200	nA
I_{O}max	Maximum output current	R_L = 600 Ω			±2.5	mA
r_o	Output resistance at EARA, EARB			1		Ω
	Gain change	$\overline{EARMUTE}$ low, max level when muted	–60			dB

† All typical values are at V_{CC} = 3 V, T_A = 25°C.
§ 2.5 V_{pp} when V_{CC} is 2.7 V.

transmit gain and dynamic range, companded mode (μ-law or A-law) or linear mode selected, V_{CC} = 3 V, T_A = 25°C (unless otherwise noted) (see Notes 5 and 6)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit reference-signal level (0 dB) (see Note 7)	Companded mode selected, μ-law ('AC36)		0.614	Vrms
	Companded mode selected, A-law ('AC37)		0.616	
	Linear mode selected ('AC36 and 'AC37)		0.626	
Overload-signal level (MICIN at unity gain)	Companded mode selected, μ-law ('AC36)		2.5	Vpp
	Companded mode selected, A-law ('AC37)		2.5	
	Linear mode selected ('AC36 and 'AC37)		2.5	
Absolute gain error	0-dB input signal		±1	dB
Gain error with input level relative to gain at −10 dBm0	MICIN to DOUT at 3 dBm0 to −40 dBm0		±0.5	dB
	MICIN to DOUT at −41 dBm0 to −50 dBm0		±1.5	dB
	MICIN to DOUT at −51 dBm0 to −55 dBm0		±2	dB
Gain variation	V_{CC} ±10%, T_A = 0°C to 70°C		±0.5	dB

NOTES: 5. Unless otherwise noted, the analog input is 0 dB, 1020-Hz sine wave, where 0 dB is defined as the zero-reference point of the channel under test.
6. The input amplifier is set for inverting unity gain.
7. The reference-signal level, which is input to the transmit channel, is defined as a value 3 dB below the full-scale value of 2 V.

transmit filter transfer, companded mode (μ-law or A-law) or linear mode selected, over recommended ranges of supply voltage and free-air temperature, CLK = 2.048 MHz, FSX = 8 kHz (see Note 6)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to input signal gain at 1.02 kHz	Input amplifier set for unity gain, noninverting maximum gain output signal at MICIN is 0 dB	f_{MICIN} = 50 Hz	−10	0	dB
		f_{MICIN} = 200 Hz	−2.8	0	
		f_{MICIN} = 300 Hz to 3 kHz		±0.25	
		f_{MICIN} = 3.3 kHz	−0.55	0.2	
		f_{MICIN} = 3.4 kHz	−1	−0.1	
		f_{MICIN} = 4 kHz		−14	
		f_{MICIN} ≥ 4.6 kHz		−32	

NOTE 6. The input amplifier is set for inverting unity gain.

transmit idle channel noise and distortion, companded mode with μ-law or A-law selected, over recommended ranges of supply voltage and operating free-air temperature (see Note 8)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise, psophometrically weighted	MICIN connected to MICGS through a 10-kΩ resistor		−72	dB0p
Transmit noise, C-message weighted	MICIN connected to MICGS through a 10-kΩ resistor		10	dBrnC0
Transmit signal-to-distortion ratio with sine-wave input	MICIN to DOUT at 0 dBm0 to −24 dBm0	36		dB
	MICIN to DOUT at −25 dBm0 to −30 dBm0	34		
	MICIN to DOUT at −31 dBm0 to −38 dBm0	30		
	MICIN to DOUT at −39 dBm0 to −40 dBm0	24		
	MICIN to DOUT at −41 dBm0 to −45 dBm0	20		
Intermodulation distortion, 2-tone CCITT method, composite power level −13 dBm0	CCITT G.712 (7.1), R2	49		dB
	CCITT G.712 (7.2), R3	51		

NOTE 8: Transmit noise, linear mode: 200 μVrms is equivalent to −74 dB (referenced to device 0-dB level).

transmit idle channel noise and distortion, linear mode selected, over recommended ranges of supply voltage and operating free-air temperature (see Notes 6 and 8)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise	MICIN connected to MICGS through a 10-kΩ resistor		200	μVrms
Transmit signal-to-distortion ratio with sine-wave input	MICIN to DOUT at 0 dBm0 to −10 dBm0	46		dB
	MICIN to DOUT at −11 dBm0 to −12 dBm0	44		
	MICIN to DOUT at −13 dBm0 to −18 dBm0	40		
	MICIN to DOUT at −19 dBm0 to −24 dBm0	35		
	MICIN to DOUT at −25 dBm0 to −40 dBm0	20		
	MICIN to DOUT at −41 dBm0 to −45 dBm0	18		

NOTES: 6. The input amplifier is set for inverting unity gain.
8. Transmit noise, linear mode: 200 μVrms is equivalent to −74 dB (referenced to device 0-dB level).

receive gain and dynamic range, companded mode (μ-law or A-law) or linear mode selected, V_{CC} = 3 V, T_A = 25°C (unless otherwise noted) (see Notes 9 and 10)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive reference-signal level (0 dB) (see Note 11)	Companded mode selected, μ-law ('AC36)		0.736	Vrms
	Companded mode selected, A-law ('AC37)		0.739	
	Linear mode selected ('AC36 and 'AC37)		0.751	
Overload-signal level	Companded mode selected, μ-law ('AC36)		3	Vpp
	Companded mode selected, A-law ('AC37)		3	
	Linear mode selected ('AC36 and 'AC37)		3	
Absolute gain error	0-dB input signal		±1	dB
Gain error with output level relative to gain at −10 dBm0	DIN to EARA and EARB at 3 dBm0 to −38 dBm0		±0.5	dB
	DIN to EARA and EARB at −39 dBm0 to −50 dBm0		±1.5	
	DIN to EARA and EARB at −51 dBm0 to −55 dBm0		±2	
Gain variation	V_{CC} ±10%, T_A = 0°C to 70°C		±0.5	dB

NOTES: 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.
10. Unless otherwise noted, the digital input is a word stream generated by passing a 0-dB sine wave at 1020 Hz through an ideal encoder, where 0 dB is defined as the zero reference.
11. This reference-signal level is measured at the speaker output of the receive channel with the gain of the output speaker amplifier set to unity.

receive filter transfer, companded mode (μ-law or A-law) or linear mode selected, over recommended ranges of supply voltage and operating free-air temperature, FSR = 8 kHz (see Note 9)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	DIN = 0 dBm0	f_{DIN} = < 200 Hz		0.25	dB
		f_{DIN} = 200 Hz	−0.5	0.25	
		f_{DIN} = 300 Hz to 3 kHz		±0.25	
		f_{DIN} = 3.3 kHz	−0.55	0.2	
		f_{DIN} = 3.4 kHz	−1	−0.1	
		f_{DIN} = 4 kHz		−14	
		f_{DIN} = > 4.6 kHz		−30	

NOTE 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.

receive idle channel noise and distortion, companded mode with μ-law or A-law selected, over recommended ranges of supply voltage and operating free-air temperature (see Note 9)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive noise, psophometrically weighted	DIN = 11010101 (A-law)		–72	dB0p
Receive noise, C-message weighted	DIN = 11111111 (μ-law)		8	dBrnc0
Receive signal-to-distortion ratio with sine-wave input	DIN to EARA and EARB at 0 dBm0 to –18 dBm0	36		dB
	DIN to EARA and EARB at –19 dBm0 to –24 dBm0	34		
	DIN to EARA and EARB at –25 dBm0 to –30 dBm0	30		
	DIN to EARA and EARB at –31 dBm0 to –38 dBm0	23		
	DIN to EARA and EARB at –39 dBm0 to –45 dBm0	17		

NOTE 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.

receive idle channel noise and distortion, linear mode selected, over recommended ranges of supply voltage and operating free-air temperature (see Notes 9 and 12)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive noise	DIN = 00000000		200	μVrms
Receive signal-to-distortion ratio with sine-wave input	DIN to EARA and EARB at 0 dBm0 to –12 dBm0	46		dB
	DIN to EARA and EARB at –13 dBm0 to –18 dBm0	38		
	DIN to EARA and EARB at –19 dBm0 to –24 dBm0	32		
	DIN to EARA and EARB at –25 dBm0 to –40 dBm0	18		
	DIN to EARA and EARB at –41 dBm0 to –45 dBm0	15		
Intermodulation, 2-tone CCITT distortion method, composite power level –13 dBm0	CCITT G.712 (7.1), R2	50		dB
	CCITT G.712 (7.2), R3	54		

NOTES: 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.

12. Receive noise, linear mode: 200 μVrms is equivalent to –71 dB (referenced to device 0-dB level).

power supply rejection and crosstalk attenuation over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Supply voltage rejection, transmit channel	Idle channel, supply signal = 100 mVrms, f = 0 to 30 kHz (measured at DOUT)		–30		dB
Supply voltage rejection, receive channel	Idle channel, supply signal = 100 mVrms, EARGS connected to EARB, f = 0 to 30 kHz (measured differentially between EARA and EARB)		–30		dB
Crosstalk attenuation, transmit-to-receive (differential)	MICIN = 0 dB, f = 1.02 kHz, unity transmit gain, EARGS connected to EARB, measured differentially between EARA and EARB	50			dB
Crosstalk attenuation, receive-to-transmit	DIN = 0 dBm0, f = 1.02 kHz, unity transmit gain, measured at DOUT	50			dB

† All typical values are at V_{CC} = 3 V, T_A = 25°C.

timing requirements

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figure 1 through Figure 4)

		MIN	NOM†	MAX	UNIT
t_t	Transition time, CLK and DCLKX/DCLKR			10	ns
	Duty cycle, CLK	45%	50%	55%	
	Duty cycle, DCLKX/DCLKR	45%	50%	55%	

† All typical values are at V_{CC} = 3 V, T_A = 25°C.

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 2)

		MIN	MAX	UNIT
$t_{su(FSX)}$	Setup time, FSX high before CLK↓	20	468	ns
$t_{h(FSX)}$	Hold time, FSX high after CLK↓	20	468	ns

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 1)

		MIN	MAX	UNIT
$t_{su(FSR)}$	Setup time, FSR high before CLK↓	20	468	ns
$t_{h(FSR)}$	Hold time, FSR high after CLK↓	20	468	ns
$t_{su(DIN)}$	Setup time, DIN high or low before CLK↓	20		ns
$t_{h(DIN)}$	Hold time, DIN high or low after CLK↓	20		ns

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see Figure 4)

		MIN	MAX	UNIT
$t_{su(FSX)}$	Setup time, FSX high before DCLKX↓	40	$t_{c(DCLKX)}-40$	ns
$t_{h(FSX)}$	Hold time, FSX high after DCLKX↓	35	$t_{c(DCLKX)}-35$	ns

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see Figure 3)

		MIN	MAX	UNIT
$t_{su(FSR)}$	Setup time, FSR high before DCLKR↓	40		ns
$t_{h(FSR)}$	Hold time, FSR high after DCLKR↓	35	$t_{c(DCLKR)}-35$	ns
$t_{su(DIN)}$	Setup time, DIN high or low before DCLKR↓	30		ns
$t_{h(DIN)}$	Hold time, DIN high or low after DCLKR↓	30		ns

switching characteristics

propagation delay times over recommended ranges of operating conditions, fixed-data-rate mode, C_L = 0 to 10 pF (see Figure 2)

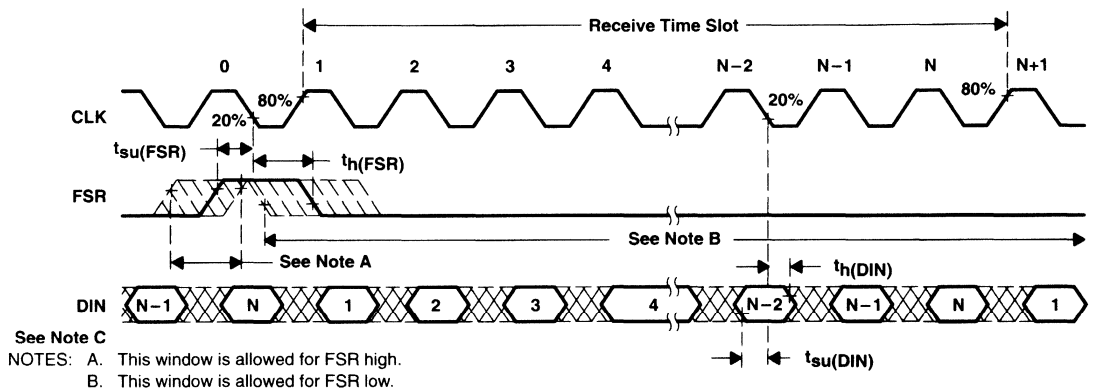
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	From CLK bit 1 high to DOUT bit 1 valid			35	ns
t_{pd2}	From CLK high to DOUT valid, bits 2 to n			35	ns
t_{pd3}	From CLK bit n low to DOUT bit n Hi-Z		30		ns
t_{pd4}	From CLK bit 1 high to $\overline{TSX}$ active (low)	R_{pullup} = 1.24 kΩ		40	ns
t_{pd5}	From CLK bit n low to $\overline{TSX}$ inactive (high)	R_{pullup} = 1.24 kΩ	30		ns

propagation delay times over recommended ranges of operating conditions, variable-data-rate mode (see Figure 4)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd6}	FSX high to DOUT bit 1 valid	C_L = 0 to 10 pF		30	ns
t_{pd7}	DCLKX high to DOUT valid, bits 2 to n	C_L = 0 to 10 pF		40	ns
t_{pd8}	FSX low to DOUT bit n Hi-Z		20		ns

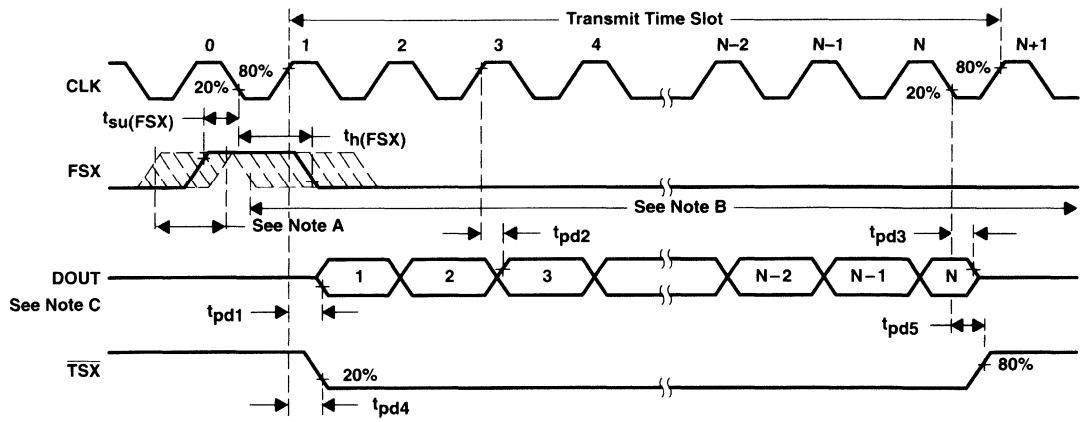
PARAMETER MEASUREMENT INFORMATION

All timing parameters are referenced to V_{IH} and V_{IL}. Bit 1 = MSB (most significant bit) and is clocked in first on DIN or clocked out first on DOUT. Bit n = LSB (least significant bit) and is clocked in last on DIN or is clocked out last on DOUT. N = 8 for the companded mode, and N = 16 for the linear mode.



NOTES: A. This window is allowed for FSR high.
B. This window is allowed for FSR low.
C. Transitions are measured at 50%.

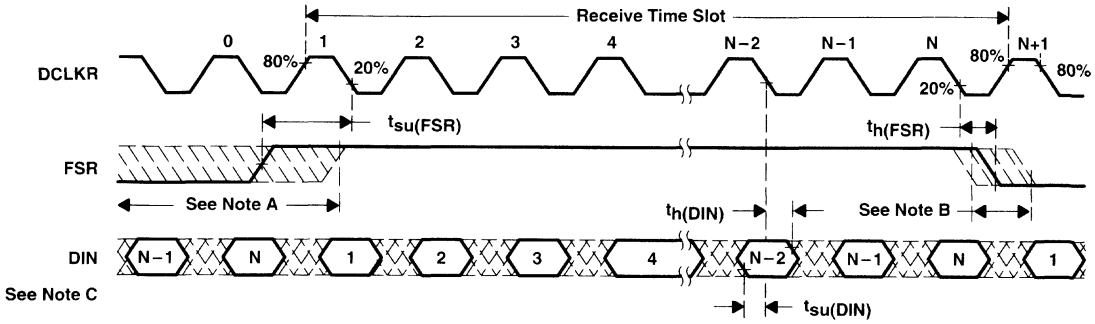
Figure 1. Fixed-Data Rate Mode, Receive Side Timing Diagram



NOTES: A. This window is allowed for FSX high.
B. This window is allowed for FSX low ($t_{h(FSX)}$ max determined by data collision considerations).
C. Transitions are measured at 50%.

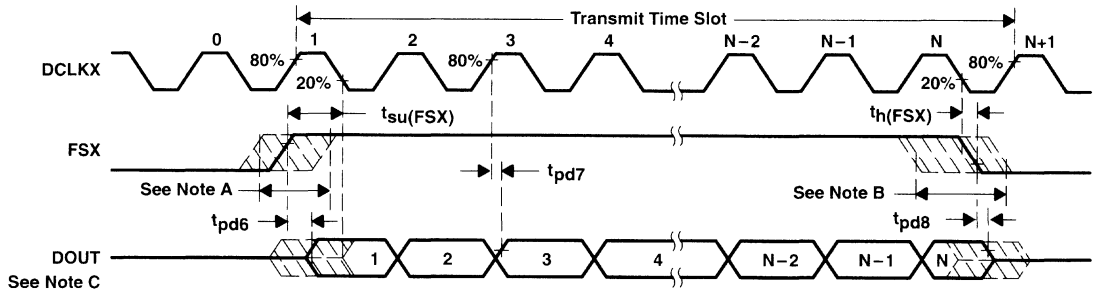
Figure 2. Fixed-Data Rate Mode, Transmit Side Timing Diagram

PARAMETER MEASUREMENT INFORMATION



NOTES: A. This window is allowed for FSR high ($t_{su(FSR)}$ max determined by data collision considerations).
B. This window is allowed for FSR low.
C. Transitions are measured at 50%.

Figure 3. Variable-Data Rate Mode, Receive Side Timing Diagram



NOTES: A. This window is allowed for FSX high.
B. This window is allowed for FSX low without data repetition.
C. Transitions are measured at 50%.

Figure 4. Variable-Data Rate Mode, Transmit Side Timing Diagram

PRINCIPLES OF OPERATION

general

system reliability features

The device should be powered up and initialized as follows:

1. Apply GND.
2. Apply V_{CC}.
3. Connect all clocks.
4. Apply TTL high to $\overline{PDN}$.
5. Apply synchronizing pulses to FSX and/or FSR.

Even though the VBAP is heavily protected against latch-up, it is still possible to cause it to latch up under certain improper power conditions. To help ensure that latch-up does not occur, a reverse-biased Schottky diode (with a forward voltage drop of less than or equal to 0.4 V — 1N5711 or equivalent) should be connected between V_{CC} (power supply) and GND.

On the transmit channel, digital outputs DOUT and $\overline{TSX}$ are held in the high-impedance state for approximately four frames (500 μs) after power up or application of V_{CC}. After this delay, DOUT, $\overline{TSX}$, and signaling are functional and occur in the correct time slot. The analog circuits on the transmit side require approximately 60 ms to reach their equilibrium value due to the autozero circuit settling time. To further enhance system integrity, DOUT and $\overline{TSX}$ are placed in the high-impedance state after an interruption of CLK.

power-down and standby operations

To minimize power consumption, a power-down mode and three standby modes are provided.

For power down, an external low signal is applied to $\overline{PDN}$. In the absence of a signal, $\overline{PDN}$ is internally pulled up to a high logic level and the device remains active. In the power-down mode, the average power consumption is reduced to 2 mW.

Three standby modes give the user the option of placing the entire device on standby, placing only the transmit channel on standby, or placing only the receive channel on standby. To place the entire device on standby, both FSX and FSR are held low. For transmit-only operation (receive channel on standby), FSX is pulsing and FSR is held low. For receive-only operation (transmit section on standby), FSR is pulsing and FSX is held low. When the entire device is in standby mode, power consumption is reduced to 5 mW. See Table 1 for power-down and standby procedures.

PRINCIPLES OF OPERATION

Table 1. Power-Down and Standby Procedures

DEVICE STATUS	PROCEDURE	TYPICAL POWER CONSUMPTION	DIGITAL OUTPUT STATUS
Power on	$\overline{PDN}$ = high, FSX = pulses, FSR = pulses	20 mW	Digital outputs active but not loaded
Power down	$\overline{PDN}$ = low, FSX, FSR = X†	2 mW	$\overline{TSX}$ and DOUT in the high-impedance state
Entire device on standby mode	FSX = low, FSR = low, $\overline{PDN}$ = high	5 mW	$\overline{TSX}$ and DOUT in the high-impedance state
Only transmit channel in standby mode	FSX = low, FSR = pulses, $\overline{PDN}$ = high	10 mW	$\overline{TSX}$ and DOUT in the high-impedance state within five frames
Only receive channel in standby mode	FSR = low, FSX = pulses, $\overline{PDN}$ = high	10 mW	Digital outputs active but not loaded

† X = don't care

fixed-data-rate timing

Fixed-data-rate timing is selected by connecting DCLKR to V_{CC} and uses the master clock (CLK), frame synchronization clocks (FSX and FSR), and the $\overline{TSX}$ output. FSX and FSR are inputs that set the sampling frequency. Data is transmitted on DOUT on the positive transitions of CLK following the rising edge of FSX. Data is received on DIN on the falling edges of CLK following FSR. A D/A conversion is performed on the received digital word, and the resulting analog sample is held on an internal sample-and-hold capacitor until transferred to the receive filter. The data word is eight bits long in the companded mode and 16 bits long in the linear mode.

variable-data-rate timing

Variable-data-rate timing is selected by connecting DCLKR to the receive data clock. In this mode, the master clock (CLK) controls the switched-capacitor filters, while data transfer into DIN and out of DOUT is controlled by DCLKR and DCLKX respectively. This allows the data to be transferred in and out of the device at any rate up to the frequency of the master clock. DCLKR and DCLKX must be synchronous with CLK.

While the FSX input is high, data is transmitted from DOUT on consecutive positive transitions of DCLKX. Similarly, while the FSR input is high, the data word is received at DIN on consecutive negative transitions of DCLKR. The transmitted data word at DOUT is repeated in all remaining time slots in the frame as long as DCLKX is pulsed and FSX is held high. This feature, which allows the data word to be transmitted more than once per frame, is available only with variable-data-rate timing.

asynchronous operations

To avoid crosstalk problems associated with special interrupt circuits, the design includes separate converters, filters, and voltage references on the transmit and receive sides to allow completely independent operation of the two channels. In either timing mode, the master clock, data clock, and time-slot strobe must be synchronized at the beginning of each frame.

precision voltage references

A precision band-gap reference voltage is generated internally and is used to supply all the references required for operation of both the transmit and receive channels. The gain in each channel is trimmed during the manufacturing process. This ensures very accurate, stable gain performance over variations in supply voltage and device temperature.

PRINCIPLES OF OPERATION

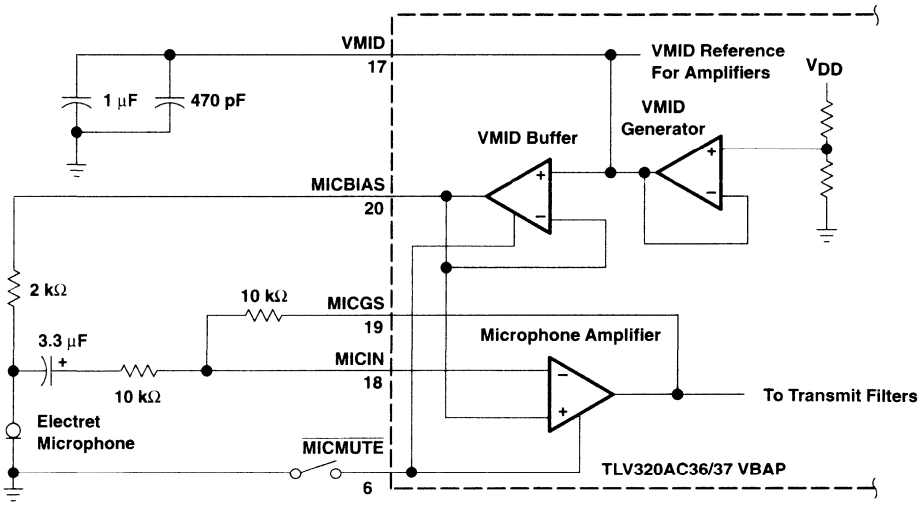
conversion laws

The TLV320AC36 provides μ-law companding operation that approximates the CCITT G.711 recommendation. The TLV320AC37 provides A-law companding operation that approximates the CCITT G.711 recommendation. The linear mode of operation uses a 13-bit two's-complement format and is the same for both the TLV320AC36 and the TLV320AC37.

transmit operation

microphone input

The microphone input amplifier is designed specifically to interface to electret-type microphone elements, as shown in Figure 5. The VMID buffer circuit provides a voltage (MICBIAS) equal to 1/2 V_{CC} as a reference for the microphone amplifier and a bias voltage to the electret microphone. The microphone amplifier output (MICGS) is used in conjunction with a feedback network and applied to the amplifier inverting input (MICIN) to set the amplifier gain. In the companded mode, when the MICIN signal level decreases to a level near the noise floor, the VBAP mutes the signal and outputs zero bits while continuing to monitor the signal level. When the input level once again exceeds the noise threshold, the mute is released and normal operation resumes. Input hysteresis is provided to ensure noiseless transitions in to and out of the muted condition. VMID appears at a terminal to provide a place to filter the VMID voltage.



NOTE A: Terminal numbers shown are for the DW and N packages.

Figure 5. Typical Microphone Interface

microphone mute function

The $\overline{\text{MICMUTE}}$ input causes the digital circuitry to transmit all zero code on DOUT.

transmit filter

A low-pass antialiasing section is included on the device and achieves a 35-dB attenuation at the sampling frequency. No external components are required to provide the necessary antialiasing function for the switched-capacitor section of the transmit filter.

PRINCIPLES OF OPERATION

encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample-and-hold capacitor. The encoder performs an A/D conversion on a switched-capacitor array. Digital data representing the sample is transmitted on the first 8 or 16 data clock cycles of the next frame.

The autozero circuit corrects for dc offset on the input signal to the encoder using the sign-bit averaging technique. The sign bit from the encoder output is long-term averaged and subtracted from the input to the encoder.

data word structure

The data word is eight bits long in the companded mode and all eight bits represent one audio data sample. The sign bit is the first bit transmitted.

The data word is 16 bits long in the linear mode. The first 13 bits comprise the audio data sample, and the last three bits form the volume control word in the receive direction (DIN) and are zero pad bits in the transmit direction (DOUT). The sign bit is transmitted first.

receive operation

decoding

In the companded mode, the serial data word is received at DIN on the first eight clock cycles in fixed-data rate and on the last eight clock cycles in variable-data rate. In the linear mode, the serial data word is received at DIN on the first 13 clock cycles. D/A conversion is performed, and the corresponding analog sample is held on an internal sample-and-hold capacitor. This sample is transferred to the receive filter.

receive filter

The receive section of the filter provides pass-band flatness and stop-band rejection that approximates both the AT&T D3/D4 specification and CCITT recommendation G.712 when operated at the recommended frequencies. The filter contains the required compensation for the (sin x)/x response of such decoders.

receive buffer

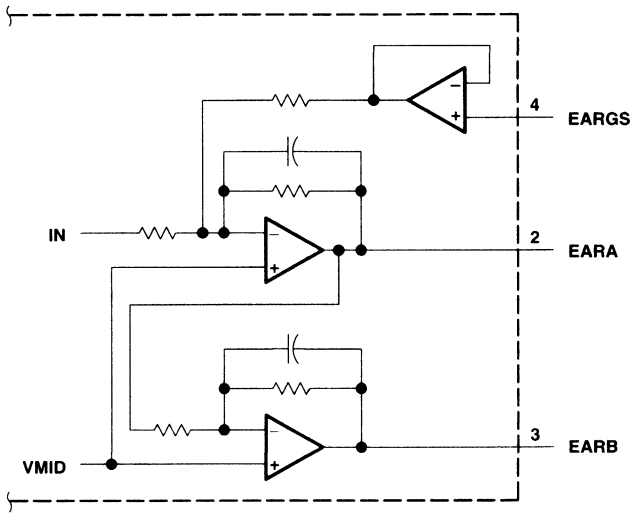
The receive buffer contains the volume control.

earphone amplifier

The earphone audio-output amplifier has a balanced output, as shown in Figure 6, to allow maximum flexibility in output configuration. The output amplifier is designed to directly drive a piezo earphone in the differential configuration without any additional external components. The output can also be used to drive a single-ended load with the output signal voltage centered around $V_{CC}/2$.

The receive-channel output level can be adjusted between specified limits by connecting an external resistor network to EARGS.

PRINCIPLES OF OPERATION



NOTE A: Terminal numbers shown are for the DW and N packages.

Figure 6. Earphone Audio-Output Amplifier Configuration and Internal Gain-Setting Network

receive data format

In the companded mode, eight bits of data are received. The sign bit is the first bit received (see Table 2).

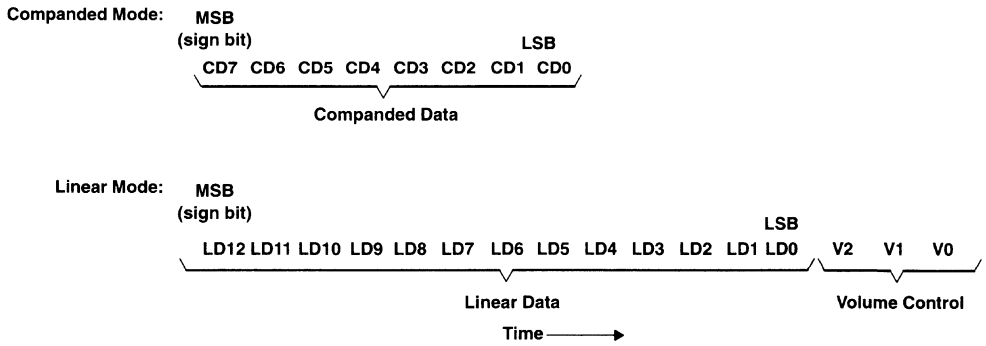
In the linear mode, 16 bits of data are received. The first 13 bits are the D/A code, and the remaining three bits form the volume control word (see Table 2). The volume control function is actually an attenuation control in which the first bit received is the most significant. The maximum volume occurs when all three volume control bits are zero. Eight levels of attenuation are selectable in 3-dB steps, giving a maximum attenuation of 21 dB when all bits are 1s. The volume control bits are not latched into the VBAP and must be present in each received data word.

PRINCIPLES OF OPERATION

Table 2. Receive-Data Bit Definitions

BIT NO.	COMPANDED MODE	LINEAR MODE
0	CD7	LD12
1	CD6	LD11
2	CD5	LD10
3	CD4	LD9
4	CD3	LD8
5	CD2	LD7
6	CD1	LD6
7	CD0	LD5
8	–	LD4
9	–	LD3
A	–	LD2
B	–	LD1
C	–	LD0
D	–	V2
E	–	V1
F	–	V0

Volume control and other control bits always follow the PCM data in time:



where:

CD7–CD0 = Data word when in companded mode
LD12–LD0= Data word when in linear mode
V2, V1, V0 = Volume (attenuation control) 000 = maximum volume, 3 dBm0
111 = minimum volume, –18 dBm0

APPLICATION INFORMATION

output gain set design considerations (see Figure 7)

EARA and EARB are low-impedance complementary outputs. The voltages at the nodes are:
V_{O+} at EARA
V_{O-} at EARB
$V_{OD} = V_{O+} - V_{O-}$ (total differential response)

R1 and R2 are a gain-setting resistor network with the center tap connected to EARGS.

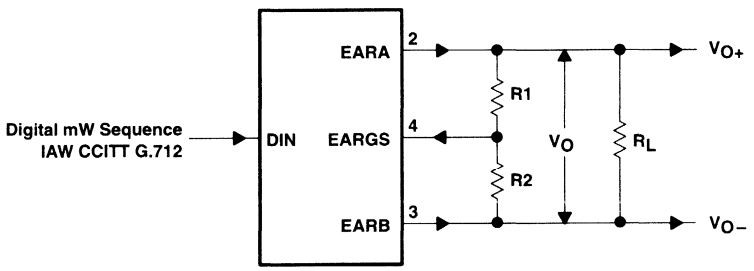
A value greater than 10 kΩ and less than 100 kΩ for R1 + R2 is recommended because of the following:

The parallel combination R1 + R2 and R_L sets the total loading. The total capacitance at EARGS and the parallel combination of R1 and R2 define a time constant that has to be minimized to avoid inaccuracies.

V_A represents the maximum available digital mW output response (V_A = 1.001 Vrms).

$$V_{OD} = A \times V_A$$

$$\text{where } A = \frac{1 + (R1/R2)}{4 + (R1/R2)}$$



NOTE A: Terminal numbers shown are for the DW and N packages.

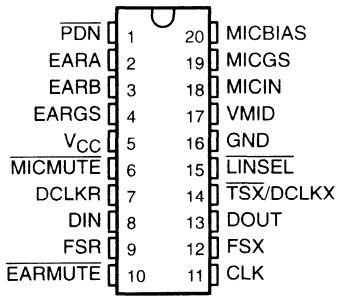
Figure 7. Gain-Setting Configuration

higher clock frequencies and sample rates

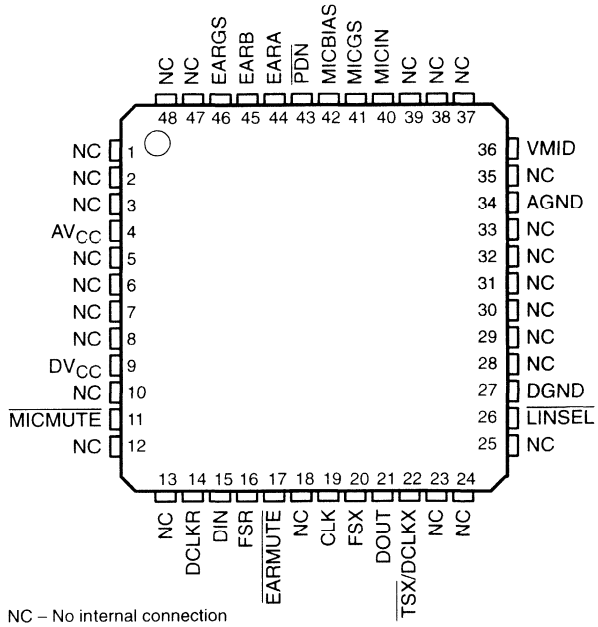
The VBAP is designed to work with sample rates up to 16 kHz where the frequency of the frame sync determines the sampling frequency. However, there is a fundamental requirement to maintain the ratio of the master clock frequency, f_{CLK}, to the frame sync frequency, f_{FSR}/f_{FSX}. This ratio for the VBAP is 2.048 MHz/8 kHz, or 256 master clocks per frame sync. For example, to operate the VBAP at a sampling rate of f_{FSR} and f_{FSX} equal to 16 kHz, f_{CLK} must be 256 times 16 kHz, or 4.096 MHz. If the VBAP is operated above an 8-kHz sample rate, however, it is expected that the performance becomes somewhat degraded. Exact parametric specifications for rates up to 16-kHz sample rate are not specified at this time.

- Single 3-V Operation
- Low Power Consumption:
  - Operating Mode . . . 20 mW Typ
  - Standby Mode . . . 5 mW Typ
  - Power-Down Mode . . . 2 mW Typ
- Combined A/D, D/A, and Filters
- Extended Variable-Frequency Operation
  - Sample Rates up to 16 kHz
  - Pass-Band up to 7.2 kHz
- Electret Microphone Bias Reference Voltage Available
- Drive a Piezo Speaker Directly
- Compatible With All Digital Signal Processors (DSPs)
- Selectable Between 8-Bit Companded and 13-Bit (Dynamic Range) Linear Conversion:
  - TLV320AC40 . . . μ-Law and Linear Modes
  - TLV320AC41 . . . A-Law and Linear Modes
- Programmable Volume Control in Linear Mode
- 300 Hz 3.6 kHz Passband with Specified Master Clock
- Designed for Standard 1.152-MHz Master Clock in DECT Standard for Hand-Held Battery-Powered Telephones

DW OR N PACKAGE
(TOP VIEW)



PT PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCT PREVIEW

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

VBAP is a trademark of Texas Instruments Incorporated.

description

The TLV320AC40 and TLV320AC41 voice-band audio processor (VBAP) integrated circuits are designed to perform the transmit encoding (A/D conversion) and receive decoding (D/A conversion) together with transmit and receive filtering for voice-band communications systems. Cellular telephone systems are targeted in particular; however, these integrated circuits can function in other systems including digital audio, telecommunications, and data acquisition.

These devices are pin-selectable for either of two modes, companded and linear, providing data in two formats. In the companded mode, data is transmitted and received in 8-bit words. In the linear mode, 13 bits of data, and either three bits of gain-setting control data, or three zero bits of padding to create a16-bit word, are sent and received.

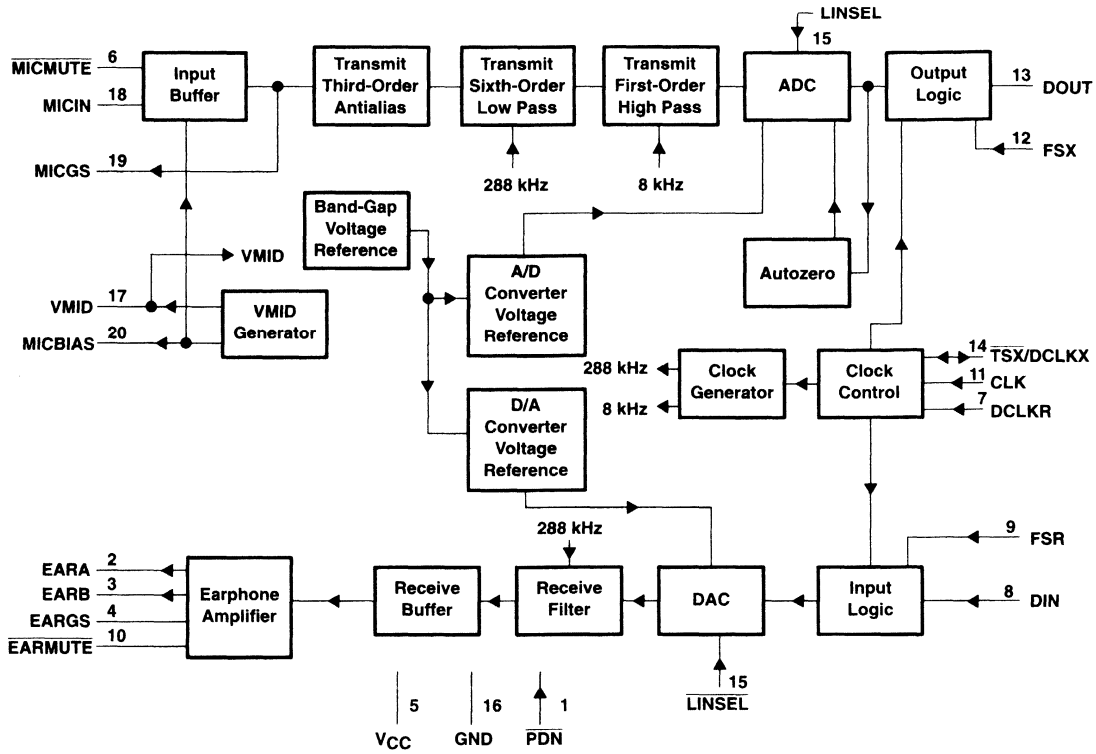
The transmit section is designed to interface directly with an electret microphone element. The microphone input signal (MICIN) is buffered and amplified with provision for setting the amplifier gain to accommodate a range of signal input levels. The amplified signal is passed through antialiasing and band-pass filters. The filtered signal is then applied to the input of a compressing analog-to-digital converter (COADC) when companded mode is selected. Otherwise, the analog-to-digital converter performs a linear conversion. The resulting data is then clocked out of DOUT as a serial data stream.

The receive section takes a frame of serial data on DIN and converts it to analog through an expanding digital-to-analog converter (EXDAC) when the companded mode is selected; otherwise, a linear conversion is performed. The analog signal then passes through switched capacitor filters, which provide out-of-band rejection, (sin x)/x correction functions, and smoothing. The filtered signal is sent to the earphone amplifier. The earphone amplifier has a differential output with adjustable gain and is designed to minimize static power dissipation.

A single on-chip high-precision band-gap circuit generates all voltage references, eliminating the need for external reference voltages. An internal reference voltage equal to $V_{CC}/2$, VMID, is used to develop the midlevel virtual ground for all the amplifier circuits and the microphone bias circuit. Another reference voltage, MICBIAS, can supply bias current for the microphone.

The TLV320AC4xC devices are characterized for operation from 0°C to 70°C. The TLV320AC4xI devices are characterized for operation from –40°C to 85°C.

functional block diagram



NOTE A: Terminal numbers shown are for the DW and N packages.

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Terminal Functions

TERMINAL NAME	TERMINAL NO. DW, N	TERMINAL NO. PT	I/O	DESCRIPTION
AGND	—	34		Ground return for all internal analog circuits
AV_{CC}	—	4		3-V supply voltage for all internal analog circuits
CLK	11	19	I	Clock input. In the fixed-data-rate mode, CLK is the master clock input as well as the transmit and receive data clock input . In the variable-data-rate mode, CLK is the master clock input only (digital).
DCLKR	7	14	I	Selection of fixed- or variable-data-rate operation. When DCLKR is connected to V_{CC}, the device operates in the fixed-data-rate mode. When DCLKR is not connected to V_{CC}, the device operates in the variable-data-rate mode and DCLKR becomes the receive data clock (digital).
DGND	—	27		Ground return for all internal digital circuits
DIN	8	15	I	Receive data input. Input data is clocked in on consecutive negative transitions of the receive data clock, which is CLK for a fixed data rate and DCLKR for a variable data rate (digital).
DOUT	13	21	O	Transmit data output. Transmit data is clocked out on consecutive positive transitions of the transmit data clock, which is CLK for a fixed data rate and DCLKX for a variable data rate (digital).
DV_{CC}	—	9		3-V supply voltage for all internal digital circuits
EARA	2	44	O	Earphone output. EARA forms a differential drive when used with the EARB signal (analog).
EARB	3	45	O	Earphone output. EARB forms a differential drive when used with the EARA signal (analog).
EARGS	4	46	I	Earphone gain set input of feedback signal for the earphone output. The ratio of an external potential divider network connected across EARA and EARB adjusts the power amplifier gain. Maximum gain occurs when EARGS is connected to EARB. Minimum gain occurs when EARGS is connected to EARA. Earphone frequency response correction is performed using an RC approach (analog).
$\overline{\text{EARMUTE}}$	10	17	I	Earphone output mute control signal. When $\overline{\text{EARMUTE}}$ is low, the output amplifier is disabled and no audio is sent to the earphone (digital).
FSR	9	16	I	Frame-synchronization clock input for the receive channel. In the variable-data-rate mode, this signal must remain high for the duration of the time slot. The receive channel enters the standby condition when FSR is TTL-low for five frames or longer. The device enters a production test-mode condition when either FSR or FSX is held high for five frames or longer (digital).
FSX	12	20	I	Frame synchronization clock input for the transmit channel. FSX operates independently of FSR, but also in an analogous manner to FSR. The transmit channel enters the standby condition when FSX is low for five frames or longer. The device enters a production test-mode condition when either FSX or FSR is held high for five frames or longer (digital).
GND	16	—		Ground return for all internal circuits
$\overline{\text{LINSEL}}$	15	26	I	Linear selection input. When low, $\overline{\text{LINSEL}}$ selects linear coding/decoding. When high, $\overline{\text{LINSEL}}$ selects companded coding/decoding. Companding code on the 'AC40 is μ-law, and companding code on the 'AC41 is A-law (digital).
MICBIAS	20	42	O	Microphone bias. MICBIAS voltage for the electret microphone is equal to VMID.
MICGS	19	41	O	Output of the internal microphone amplifier. MICGS is used as the feedback to set the microphone amplifier gain. If sidetone is required, it is accomplished by connecting a series network between MICGS and EARGS (analog).
MICIN	18	40	I	Microphone input. Electret microphone input to the internal microphone amplifier (analog)
$\overline{\text{MICMUTE}}$	6	11	I	Microphone input mute control signal. When $\overline{\text{MICMUTE}}$ is active (low), zero code is transmitted (dig.).
$\overline{\text{PDN}}$	1	43	I	Power-down input. When $\overline{\text{PDN}}$ is low, the device powers down to reduce power consumption (digital).
$\overline{\text{TSX}}$/DCLKX	14	22	I/O	Transmit time slot strobe (active-low output) or data clock (input) for the transmit channel. In the fixed-data-rate mode, $\overline{\text{TSX}}$/DCLKX is an open-drain output that pulls to ground and is used as an enable signal for a 3-state buffer. In the variable-data-rate mode, DCLKX becomes the transmit data clock input (digital).
V_{CC}	5	—		3-V supply voltage for all internal circuits
VMID	17	36	O	$V_{CC}/2$ bias voltage reference. A pair of external, low-leakage, high-frequency capacitors (1 μF and 470 pF) should be connected between VMID and ground for filtering.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.3 V to 5.5 V
Output voltage range at DOUT, V_O . . . . . −0.3 V to 5.5 V
Input voltage range at DIN, V_I . . . . . −0.3 V to 5.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: C suffix . . . . . 0°C to 70°C
I suffix . . . . . −40°C to 85°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage value is with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW
PT	1075 mW	7.1 mW/°C	756 mW	649 mW

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
Supply voltage, V_{CC} (see Note 3)		2.7	3.3	V
High-level input voltage, V_{IH}		2.2		V
Low-level input voltage, V_{IL}			0.8	V
Load resistance between EARA and EARB, R_L (see Note 4)		600		Ω
Load capacitance between EARA and EARB, C_L (see Note 4)			50	nF
Operating free-air temperature, T_A	TLV320AC40C, TLV320AC41C	0	70	°C
	TLV320AC40I, TLV320AC41I	−40	85	

NOTES: 2. To avoid possible damage to these CMOS devices and resulting reliability problems, the power-up sequence detailed in the system reliability features paragraph should be followed.
3. Voltages at analog inputs, outputs, and V_{CC} are with respect to GND.
4. R_L and C_L should not be applied simultaneously.

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electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted)

supply current, f_{DCLKR} or f_{DCLKX} = 1.152 MHz, outputs not loaded, V_{CC} = 3 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
I_{CC}	Supply current from V_{CC}	Operating	$\overline{PDN}$ is high with CLK signal present		7.5	mA
		Power down	$\overline{PDN}$ is low for 500 µs		0.75	
		Standby – both	$\overline{PDN}$ is high with FSX and FSR held low		2	
		Standby – one	$\overline{PDN}$ is high with either FSX or FSR pulsing with the other held low		4.5	

digital interface

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	DOUT	I_{OH} = –3.2 mA, V_{CC} = 3 V	2.4	2.8		V
V_{OL}	Low-level output voltage		I_{OL} = 3.2 mA, V_{CC} = 3 V		0.2	0.4	V
I_{IH}	High-level input current, any digital input		V_I = 2.2 V to V_{CC}			10	µA
I_{IL}	Low-level input current, any digital input		V_I = 0 to 0.8 V			10	µA
C_i	Input capacitance				5		pF
C_o	Output capacitance				5		pF

† All typical values are at V_{CC} = 3 V, T_A = 25°C.

microphone interface

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IO}	Input offset voltage at MICIN		V_I = 0 to 3 V			±5	mV
I_{IB}	Input bias current at MICIN					±200	nA
B_1	Unity-gain bandwidth, open loop at MICIN‡				1.5		MHz
C_i	Input capacitance at MICIN				5		pF
A_V	Large-signal voltage amplification at MICGS				10000		V/V
I_{O}max	Maximum output current	VMID		3			µA
		MICBIAS (source only)		1			mA

† All typical values are at V_{CC} = 3 V, T_A = 25°C.
‡ The frequency of the first pole is 100 Hz.

speaker interface

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{O(PP)}$	AC output voltage				3§	Vpp
V_{OO}	Output offset voltage at EARA, EARB (single-ended)	Relative to GND			80	mVpk
$I_{I(lkg)}$	Input leakage current at EARGS	V_I = 0.5 V to (V_{CC} – 0.5) V			±200	nA
I_{O}max	Maximum output current	R_L = 600 Ω			±2.5	mA
r_o	Output resistance at EARA, EARB			1		Ω
	Gain change	$\overline{EARMUTE}$ low, max level when muted	–60			dB

† All typical values are at V_{CC} = 3 V, T_A = 25°C.
§ 2.5 V_{pp} when V_{CC} is 2.7 V.

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transmit gain and dynamic range, companded mode (μ-law or A-law) or linear mode selected, V_{CC} = 3 V, T_A = 25°C (unless otherwise noted) (see Notes 5 and 6)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit reference-signal level (0 dB) (see Note 7)	Companded mode selected, μ-law ('AC40)		0.614	Vrms
	Companded mode selected, A-law ('AC41)		0.616	
	Linear mode selected ('AC40 and 'AC41)		0.626	
Overload-signal level (MICIN at unity gain)	Companded mode selected, μ-law ('AC40)		2.5	Vpp
	Companded mode selected, A-law ('AC41)		2.5	
	Linear mode selected ('AC40 and 'AC41)		2.5	
Absolute gain error	0-dB input signal		±1	dB
Gain error with input level relative to gain at –10 dBm0	MICIN to DOUT at 3 dBm0 to –40 dBm0		±0.5	dB
	MICIN to DOUT at –41 dBm0 to –50 dBm0		±1.5	dB
	MICIN to DOUT at –51 dBm0 to –55 dBm0		±2	dB
Gain variation	V_{CC} ±10%, T_A = 0°C to 70°C		±0.5	dB

NOTES: 5. Unless otherwise noted, the analog input is 0 dB, 1020-Hz sine wave, where 0 dB is defined as the zero-reference point of the channel under test.
6. The input amplifier is set for inverting unity gain.
7. The reference-signal level, which is input to the transmit channel, is defined as a value 3 dB below the full-scale value of 2 V.

transmit filter transfer, companded mode (μ-law or A-law) or linear mode selected, over recommended ranges of supply voltage and free-air temperature, CLK = 1.152 MHz, FSX = 8 kHz (see Note 6)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to input signal gain at 1.02 kHz	Input amplifier set for unity gain, noninverting maximum gain output signal at MICIN is 0 dB	f_{MICIN} = 50 Hz	–10	0	dB
		f_{MICIN} = 200 Hz	–2.8	0	
		f_{MICIN} = 300 Hz to 3 kHz		±0.25	
		f_{MICIN} = 3.3 kHz	–0.55	0.2	
		f_{MICIN} = 3.4 kHz	–1	–0.1	
		f_{MICIN} = 4 kHz		–14	
		f_{MICIN} ≥4.6 kHz		–32	

NOTE 6. The input amplifier is set for inverting unity gain.

transmit idle channel noise and distortion, companded mode with μ-law or A-law selected, over recommended ranges of supply voltage and operating free-air temperature (see Note 8)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise, psophometrically weighted	MICIN connected to MICGS through a 10-kΩ resistor		–72	dB0p
Transmit noise, C-message weighted	MICIN connected to MICGS through a 10-kΩ resistor		10	dBrnC0
Transmit signal-to-distortion ratio with sine-wave input	MICIN to DOUT at 0 dBm0 to –24 dBm0	36		dB
	MICIN to DOUT at –25 dBm0 to –30 dBm0	34		
	MICIN to DOUT at –31 dBm0 to –38 dBm0	30		
	MICIN to DOUT at –39 dBm0 to –40 dBm0	24		
	MICIN to DOUT at –41 dBm0 to –45 dBm0	20		
Intermodulation distortion, 2-tone CCITT method, composite power level –13 dBm0	CCITT G.712 (7.1), R2	49		dB
	CCITT G.712 (7.2), R3	51		

NOTE 8: Transmit noise, linear mode: 200 μVrms is equivalent to –74 dB (referenced to device 0-dB level).

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transmit idle channel noise and distortion, linear mode selected, over recommended ranges of supply voltage and operating free-air temperature (see Notes 6 and 8)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise	MICIN connected to MICGS through a 10-kΩ resistor		200	μVrms
Transmit signal-to-distortion ratio with sine-wave input	MICIN to DOUT at 0 dBm0 to –10 dBm0	46		dB
	MICIN to DOUT at –11 dBm0 to –12 dBm0	44		
	MICIN to DOUT at –13 dBm0 to –18 dBm0	40		
	MICIN to DOUT at –19 dBm0 to –24 dBm0	35		
	MICIN to DOUT at –25 dBm0 to –40 dBm0	20		
	MICIN to DOUT at –41 dBm0 to –45 dBm0	18		

NOTES: 6. The input amplifier is set for inverting unity gain.
8. Transmit noise, linear mode: 200 μVrms is equivalent to –74 dB (referenced to device 0-dB level).

receive gain and dynamic range, companded mode (μ-law or A-law) or linear mode selected, V_{CC} = 3 V, T_A = 25°C (unless otherwise noted) (see Notes 9 and 10)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive reference-signal level (0 dB) (see Note 11)	Companded mode selected, μ-law ('AC40)		0.736	Vrms
	Companded mode selected, A-law ('AC41)		0.739	
	Linear mode selected ('AC40 and 'AC41)		0.751	
Overload-signal level	Companded mode selected, μ-law ('AC40)		3	Vpp
	Companded mode selected, A-law ('AC41)		3	
	Linear mode selected ('AC40 and 'AC41)		3	
Absolute gain error	0-dB input signal		±1	dB
Gain error with output level relative to gain at –10 dBm0	DIN to EARA and EARB at 3 dBm0 to –38 dBm0		±0.5	dB
	DIN to EARA and EARB at –39 dBm0 to –50 dBm0		±1.5	
	DIN to EARA and EARB at –51 dBm0 to –55 dBm0		±2	
Gain variation	V_{CC} ±10%, T_A = 0°C to 70°C		±0.5	dB

NOTES: 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.
10. Unless otherwise noted, the digital input is a word stream generated by passing a 0-dB sine wave at 1020 Hz through an ideal encoder, where 0 dB is defined as the zero reference.
11. This reference-signal level is measured at the speaker output of the receive channel with the gain of the output speaker amplifier set to unity.

receive filter transfer, companded mode (μ-law or A-law) or linear mode selected, over recommended ranges of supply voltage and operating free-air temperature, FSR = 8 kHz (see Note 9)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	DIN = 0 dBm0	f_{DIN} = < 200 Hz		0.25	dB
		f_{DIN} = 200 Hz	–0.5	0.25	
		f_{DIN} = 300 Hz to 3 kHz		±0.25	
		f_{DIN} = 3.3 kHz	–0.55	0.2	
		f_{DIN} = 3.4 kHz	–1	–0.1	
		f_{DIN} = 4 kHz		–14	
		f_{DIN} = > 4.6 kHz		–30	

NOTE 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.

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receive idle channel noise and distortion, companded mode with μ-law or A-law selected, over recommended ranges of supply voltage and operating free-air temperature (see Note 9)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive noise, psophometrically weighted	DIN = 11010101 (A-law)		–72	dB0p
Receive noise, C-message weighted	DIN = 11111111 (μ-law)		8	dBrnc0
Receive signal-to-distortion ratio with sine-wave input	DIN to EARA and EARB at 0 dBm0 to –18 dBm0	36		dB
	DIN to EARA and EARB at –19 dBm0 to –24 dBm0	34		
	DIN to EARA and EARB at –25 dBm0 to –30 dBm0	30		
	DIN to EARA and EARB at –31 dBm0 to –38 dBm0	23		
	DIN to EARA and EARB at –39 dBm0 to –45 dBm0	17		

NOTE 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.

receive idle channel noise and distortion, linear mode selected, over recommended ranges of supply voltage and operating free-air temperature (see Notes 9 and 12)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive noise	DIN = 00000000		200	μVrms
Receive signal-to-distortion ratio with sine-wave input	DIN to EARA and EARB at 0 dBm0 to –12 dBm0	46		dB
	DIN to EARA and EARB at –13 dBm0 to –18 dBm0	38		
	DIN to EARA and EARB at –19 dBm0 to –24 dBm0	32		
	DIN to EARA and EARB at –25 dBm0 to –40 dBm0	18		
	DIN to EARA and EARB at –41 dBm0 to –45 dBm0	15		
Intermodulation, 2-tone CCITT distortion method, composite power level –13 dBm0	CCITT G.712 (7.1), R2	50		dB
	CCITT G.712 (7.2), R3	54		

NOTES: 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.
12. Receive noise, linear mode: 200 μVrms is equivalent to –71 dB (referenced to device 0-dB level).

power supply rejection and crosstalk attenuation over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Supply voltage rejection, transmit channel	Idle channel, supply signal = 100 mVrms, f = 0 to 30 kHz (measured at DOUT)		–30		dB
Supply voltage rejection, receive channel	Idle channel, supply signal = 100 mVrms, EARGS connected to EARB, f = 0 to 30 kHz (measured differentially between EARA and EARB)		–30		dB
Crosstalk attenuation, transmit-to-receive (differential)	MICIN = 0 dB, f = 1.02 kHz, unity transmit gain, EARGS connected to EARB, measured differentially between EARA and EARB	50			dB
Crosstalk attenuation, receive-to-transmit	DIN = 0 dBm0, f = 1.02 kHz, unity transmit gain, measured at DOUT	50			dB

† All typical values are at V_{CC} = 3 V, T_A = 25°C.

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timing requirements

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figure 1 through Figure 4)

		MIN	NOM†	MAX	UNIT
t_t	Transition time, CLK and DCLKX/DCLKR			10	ns
	Duty cycle, CLK	45%	50%	55%	
	Duty cycle, DCLKX/DCLKR	45%	50%	55%	

† All typical values are at V_{CC} = 3 V, T_A = 25°C.

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 2)

		MIN	MAX	UNIT
$t_{su(FSX)}$	Setup time, FSX high before CLK↓	20	468	ns
$t_{h(FSX)}$	Hold time, FSX high after CLK↓	20	468	ns

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 1)

		MIN	MAX	UNIT
$t_{su(FSR)}$	Setup time, FSR high before CLK↓	20	468	ns
$t_{h(FSR)}$	Hold time, FSR high after CLK↓	20	468	ns
$t_{su(DIN)}$	Setup time, DIN high or low before CLK↓	20		ns
$t_{h(DIN)}$	Hold time, DIN high or low after CLK↓	20		ns

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see Figure 4)

		MIN	MAX	UNIT
$t_{su(FSX)}$	Setup time, FSX high before DCLKX↓	40	$t_{c(DCLKX)}-40$	ns
$t_{h(FSX)}$	Hold time, FSX high after DCLKX↓	35	$t_{c(DCLKX)}-35$	ns

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see Figure 3)

		MIN	MAX	UNIT
$t_{su(FSR)}$	Setup time, FSR high before DCLKR↓	40		ns
$t_{h(FSR)}$	Hold time, FSR high after DCLKR↓	35	$t_{c(DCLKR)}-35$	ns
$t_{su(DIN)}$	Setup time, DIN high or low before DCLKR↓	30		ns
$t_{h(DIN)}$	Hold time, DIN high or low after DCLKR↓	30		ns

switching characteristics

propagation delay times over recommended ranges of operating conditions, fixed-data-rate mode, C_L = 0 to 10 pF (see Figure 2)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	From CLK bit 1 high to DOUT bit 1 valid			35	ns
t_{pd2}	From CLK high to DOUT valid, bits 2 to n			35	ns
t_{pd3}	From CLK bit n low to DOUT bit n Hi-Z		30		ns
t_{pd4}	From CLK bit 1 high to $\overline{TSX}$ active (low)	R_{pullup} = 1.24 kΩ		40	ns
t_{pd5}	From CLK bit n low to $\overline{TSX}$ inactive (high)	R_{pullup} = 1.24 kΩ	30		ns

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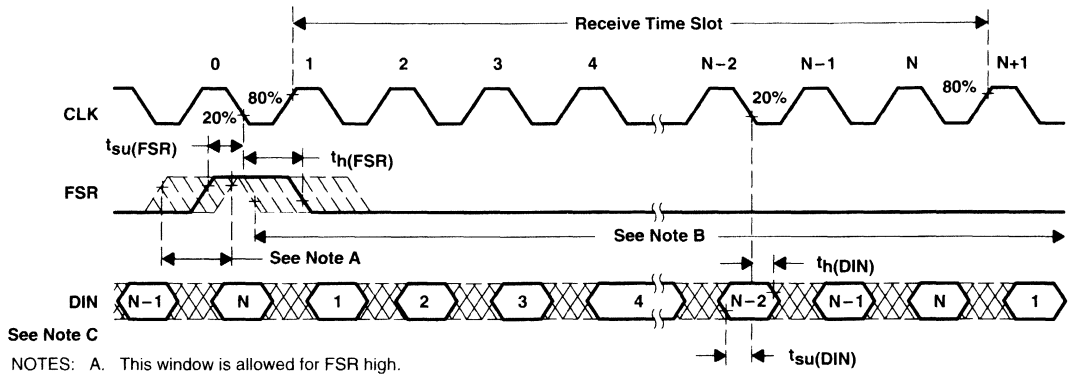
propagation delay times over recommended ranges of operating conditions, variable-data-rate mode (see Figure 4)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd6}	FSX high to DOUT bit 1 valid	C_L = 0 to 10 pF		30	ns
t_{pd7}	DCLKX high to DOUT valid, bits 2 to n	C_L = 0 to 10 pF		40	ns
t_{pd8}	FSX low to DOUT bit n Hi-Z		20		ns

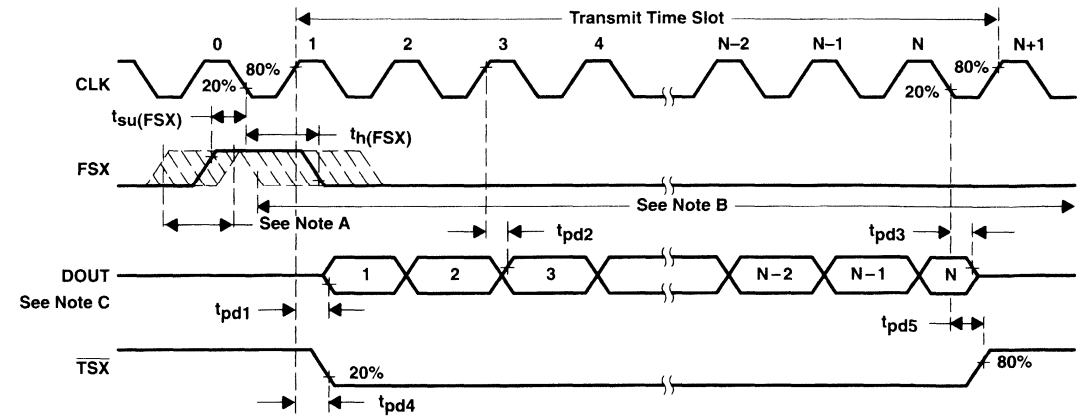
PARAMETER MEASUREMENT INFORMATION

All timing parameters are referenced to V_{IH} and V_{IL}. Bit 1 = MSB (most significant bit) and is clocked in first on DIN or clocked out first on DOUT. Bit n = LSB (least significant bit) and is clocked in last on DIN or is clocked out last on DOUT. N = 8 for the companded mode, and N = 16 for the linear mode.



NOTES: A. This window is allowed for FSR high.
B. This window is allowed for FSR low.
C. Transitions are measured at 50%.

Figure 1. Fixed-Data Rate Mode, Receive Side Timing Diagram

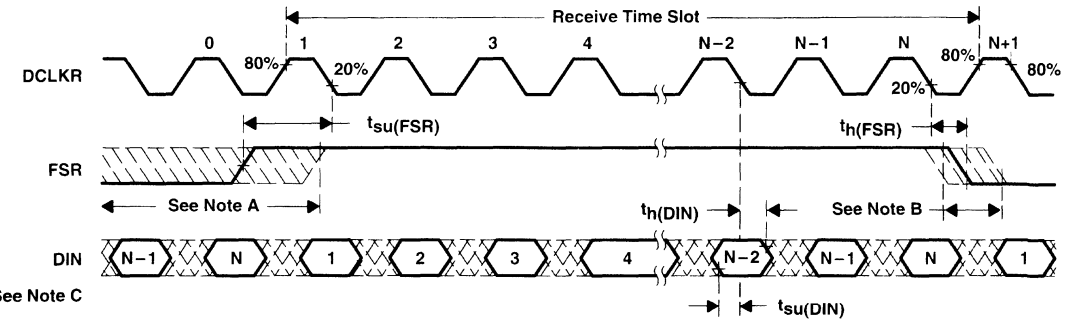


NOTES: A. This window is allowed for FSX high.
B. This window is allowed for FSX low ($t_{h(FSX)}$ max determined by data collision considerations).
C. Transitions are measured at 50%.

Figure 2. Fixed-Data Rate Mode, Transmit Side Timing Diagram

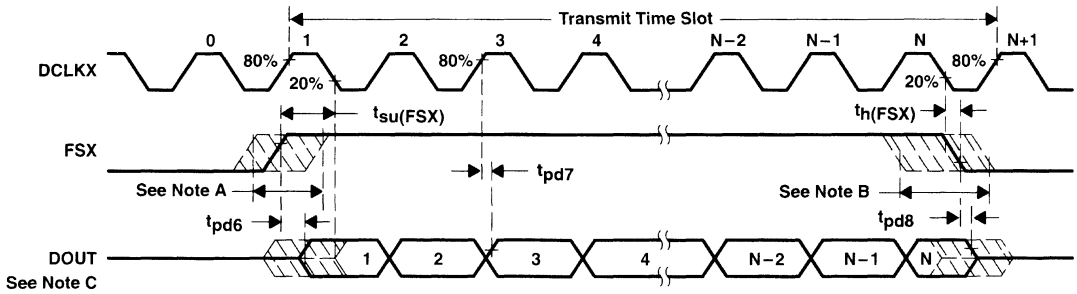
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTES: A. This window is allowed for FSR high ($t_{su(FSR)}$ max determined by data collision considerations).
B. This window is allowed for FSR low.
C. Transitions are measured at 50%.

Figure 3. Variable-Data Rate Mode, Receive Side Timing Diagram



NOTES: A. This window is allowed for FSX high.
B. This window is allowed for FSX low without data repetition.
C. Transitions are measured at 50%.

Figure 4. Variable-Data Rate Mode, Transmit Side Timing Diagram

PRODUCT PREVIEW

PRINCIPLES OF OPERATION

general

system reliability features

The device should be powered up and initialized as follows:

1. Apply GND.
2. Apply V_{CC}.
3. Connect all clocks.
4. Apply TTL high to $\overline{PDN}$.
5. Apply synchronizing pulses to FSX and/or FSR.

Even though the VBAP is heavily protected against latch-up, it is still possible to cause it to latch up under certain improper power conditions. To help ensure that latch-up does not occur, a reverse-biased Schottky diode (with a forward voltage drop of less than or equal to 0.4 V — 1N5711 or equivalent) should be connected between V_{CC} (power supply) and GND.

On the transmit channel, digital outputs DOUT and $\overline{TSX}$ are held in the high-impedance state for approximately four frames (500 µs) after power up or application of V_{CC}. After this delay, DOUT, $\overline{TSX}$, and signaling are functional and occur in the correct time slot. The analog circuits on the transmit side require approximately 60 ms to reach their equilibrium value due to the autozero circuit settling time. To further enhance system integrity, DOUT and $\overline{TSX}$ are placed in the high-impedance state after an interruption of CLK.

power-down and standby operations

To minimize power consumption, a power-down mode and three standby modes are provided.

For power down, an external low signal is applied to $\overline{PDN}$. In the absence of a signal, $\overline{PDN}$ is internally pulled up to a high logic level and the device remains active. In the power-down mode, the average power consumption is reduced to 2 mW.

Three standby modes give the user the option of placing the entire device on standby, placing only the transmit channel on standby, or placing only the receive channel on standby. To place the entire device on standby, both FSX and FSR are held low. For transmit-only operation (receive channel on standby), FSX is pulsing and FSR is held low. For receive-only operation (transmit section on standby), FSR is pulsing and FSX is held low. When the entire device is in standby mode, power consumption is reduced to 5 mW. See Table 1 for power-down and standby procedures.

PRINCIPLES OF OPERATION

Table 1. Power-Down and Standby Procedures

DEVICE STATUS	PROCEDURE	TYPICAL POWER CONSUMPTION	DIGITAL OUTPUT STATUS
Power on	$\overline{PDN}$ = high, FSX = pulses, FSR = pulses	20 mW	Digital outputs active but not loaded
Power down	$\overline{PDN}$ = low, FSX, FSR = X†	2 mW	$\overline{TSX}$ and DOUT in the high-impedance state
Entire device on standby mode	FSX = low, FSR = low, $\overline{PDN}$ = high	5 mW	$\overline{TSX}$ and DOUT in the high-impedance state
Only transmit channel in standby mode	FSX = low, FSR = pulses, $\overline{PDN}$ = high	10 mW	$\overline{TSX}$ and DOUT in the high-impedance state within five frames
Only receive channel in standby mode	FSR = low, FSX = pulses, $\overline{PDN}$ = high	10 mW	Digital outputs active but not loaded

† X = don't care

fixed-data-rate timing

Fixed-data-rate timing is selected by connecting DCLKR to V_{CC} and uses the master clock (CLK), frame synchronization clocks (FSX and FSR), and the $\overline{TSX}$ output. FSX and FSR are inputs that set the sampling frequency. Data is transmitted on DOUT on the positive transitions of CLK following the rising edge of FSX. Data is received on DIN on the falling edges of CLK following FSR. A D/A conversion is performed on the received digital word, and the resulting analog sample is held on an internal sample-and-hold capacitor until transferred to the receive filter. The data word is eight bits long in the companded mode and 16 bits long in the linear mode.

variable-data-rate timing

Variable-data-rate timing is selected by connecting DCLKR to the receive data clock. In this mode, the master clock (CLK) controls the switched-capacitor filters, while data transfer into DIN and out of DOUT is controlled by DCLKR and DCLKX respectively. This allows the data to be transferred in and out of the device at any rate up to the frequency of the master clock. DCLKR and DCLKX must be synchronous with CLK.

While the FSX input is high, data is transmitted from DOUT on consecutive positive transitions of DCLKX. Similarly, while the FSR input is high, the data word is received at DIN on consecutive negative transitions of DCLKR. The transmitted data word at DOUT is repeated in all remaining time slots in the frame as long as DCLKX is pulsed and FSX is held high. This feature, which allows the data word to be transmitted more than once per frame, is available only with variable-data-rate timing.

asynchronous operations

To avoid crosstalk problems associated with special interrupt circuits, the design includes separate converters, filters, and voltage references on the transmit and receive sides to allow completely independent operation of the two channels. In either timing mode, the master clock, data clock, and time-slot strobe must be synchronized at the beginning of each frame.

precision voltage references

A precision band-gap reference voltage is generated internally and is used to supply all the references required for operation of both the transmit and receive channels. The gain in each channel is trimmed during the manufacturing process. This ensures very accurate, stable gain performance over variations in supply voltage and device temperature.

PRINCIPLES OF OPERATION

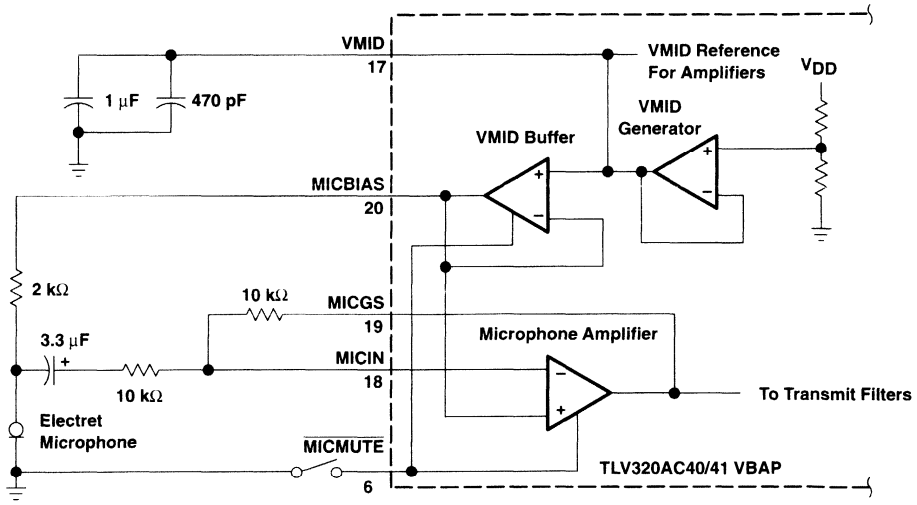
conversion laws

The TLV320AC40 provides μ-law companding operation that approximates the CCITT G.711 recommendation. The TLV320AC41 provides A-law companding operation that approximates the CCITT G.711 recommendation. The linear mode of operation uses a 13-bit two's-complement format and is the same for both the TLV320AC40 and the TLV320AC41.

transmit operation

microphone input

The microphone input amplifier is designed specifically to interface to electret-type microphone elements, as shown in Figure 5. The VMID buffer circuit provides a voltage (MICBIAS) equal to 1/2 V_{CC} as a reference for the microphone amplifier and a bias voltage to the electret microphone. The microphone amplifier output (MICGS) is used in conjunction with a feedback network and applied to the amplifier inverting input (MICIN) to set the amplifier gain. In the companded mode, when the MICIN signal level decreases to a level near the noise floor, the VBAP mutes the signal and outputs zero bits while continuing to monitor the signal level. When the input level once again exceeds the noise threshold, the mute is released and normal operation resumes. Input hysteresis is provided to ensure noiseless transitions in to and out of the muted condition. VMID appears at a terminal to provide a place to filter the VMID voltage.



NOTE A: Terminal numbers shown are for the DW and N packages.

Figure 5. Typical Microphone Interface

microphone mute function

The $\overline{\text{MICMUTE}}$ input causes the digital circuitry to transmit all zero code on DOUT.

transmit filter

A low-pass antialiasing section is included on the device and achieves a 35-dB attenuation at the sampling frequency. No external components are required to provide the necessary antialiasing function for the switched-capacitor section of the transmit filter.

PRODUCT PREVIEW

PRINCIPLES OF OPERATION

encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample-and-hold capacitor. The encoder performs an A/D conversion on a switched-capacitor array. Digital data representing the sample is transmitted on the first 8 or 16 data clock cycles of the next frame.

The autozero circuit corrects for dc offset on the input signal to the encoder using the sign-bit averaging technique. The sign bit from the encoder output is long-term averaged and subtracted from the input to the encoder.

data word structure

The data word is eight bits long in the companded mode and all eight bits represent one audio data sample. The sign bit is the first bit transmitted.

The data word is 16 bits long in the linear mode. The first 13 bits comprise the audio data sample, and the last three bits form the volume control word in the receive direction (DIN) and are zero pad bits in the transmit direction (DOUT). The sign bit is transmitted first.

receive operation

decoding

In the companded mode, the serial data word is received at DIN on the first eight clock cycles in fixed-data rate and on the last eight clock cycles in variable-data rate. In the linear mode, the serial data word is received at DIN on the first 13 clock cycles. D/A conversion is performed, and the corresponding analog sample is held on an internal sample-and-hold capacitor. This sample is transferred to the receive filter.

receive filter

The receive section of the filter provides pass-band flatness and stop-band rejection that approximates both the AT&T D3/D4 specification and CCITT recommendation G.712 when operated at the recommended frequencies. The filter contains the required compensation for the (sin x)/x response of such decoders.

receive buffer

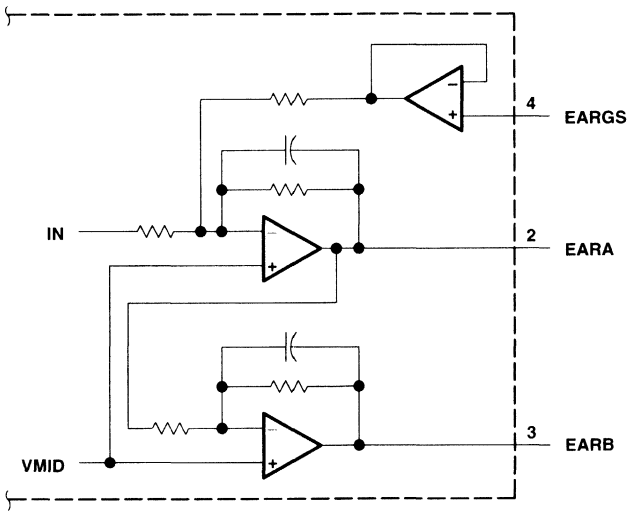
The receive buffer contains the volume control.

earphone amplifier

The earphone audio-output amplifier has a balanced output, as shown in Figure 6, to allow maximum flexibility in output configuration. The output amplifier is designed to directly drive a piezo earphone in the differential configuration without any additional external components. The output can also be used to drive a single-ended load with the output signal voltage centered around $V_{CC}/2$.

The receive-channel output level can be adjusted between specified limits by connecting an external resistor network to EARGS.

PRINCIPLES OF OPERATION



NOTE A: Terminal numbers shown are for the DW and N packages.

Figure 6. Earphone Audio-Output Amplifier Configuration and Internal Gain-Setting Network

receive data format

In the companded mode, eight bits of data are received. The sign bit is the first bit received (see Table 2).

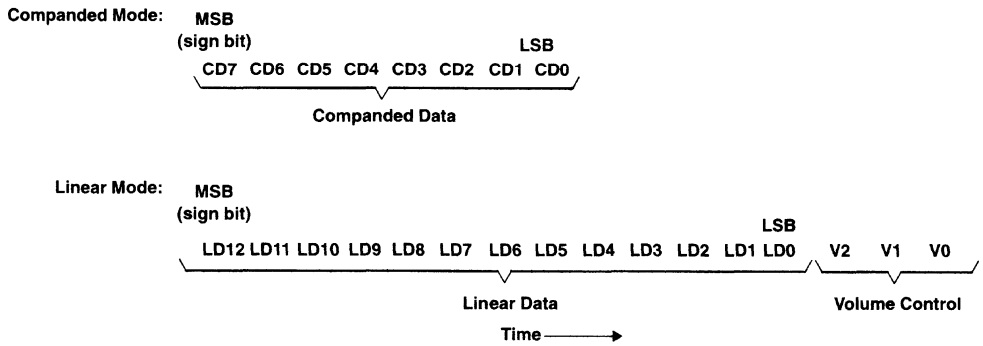
In the linear mode, 16 bits of data are received. The first 13 bits are the D/A code, and the remaining three bits form the volume control word (see Table 2). The volume control function is actually an attenuation control in which the first bit received is the most significant. The maximum volume occurs when all three volume control bits are zero. Eight levels of attenuation are selectable in 3-dB steps, giving a maximum attenuation of 21 dB when all bits are 1s. The volume control bits are not latched into the VBAP and must be present in each received data word.

PRINCIPLES OF OPERATION

Table 2. Receive-Data Bit Definitions

BIT NO.	COMPANDED MODE	LINEAR MODE
0	CD7	LD12
1	CD6	LD11
2	CD5	LD10
3	CD4	LD9
4	CD3	LD8
5	CD2	LD7
6	CD1	LD6
7	CD0	LD5
8	–	LD4
9	–	LD3
A	–	LD2
B	–	LD1
C	–	LD0
D	–	V2
E	–	V1
F	–	V0

Volume control and other control bits always follow the PCM data in time:



where:

CD7–CD0 = Data word when in companded mode
LD12–LD0= Data word when in linear mode
V2, V1, V0 = Volume (attenuation control) 000 = maximum volume, 3 dBm0
111 = minimum volume, –18 dBm0

PRODUCT PREVIEW

APPLICATION INFORMATION

output gain set design considerations (see Figure 7)

EARA and EARB are low-impedance complementary outputs. The voltages at the nodes are:
V_{O+} at EARA
V_{O-} at EARB
$V_{OD} = V_{O+} - V_{O-}$ (total differential response)

R1 and R2 are a gain-setting resistor network with the center tap connected to EARGS.

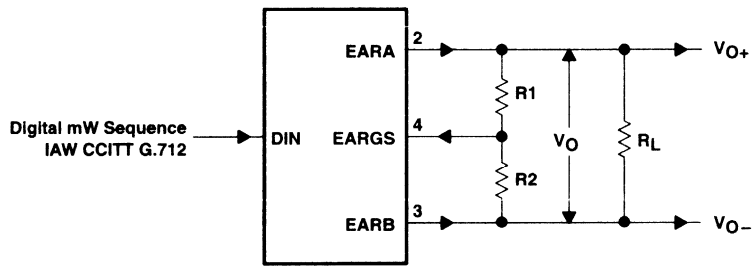
A value greater than 10 kΩ and less than 100 kΩ for R1 + R2 is recommended because of the following:

The parallel combination R1 + R2 and R_L sets the total loading. The total capacitance at EARGS and the parallel combination of R1 and R2 define a time constant that has to be minimized to avoid inaccuracies.

V_A represents the maximum available digital mW output response (V_A = 1.001 Vrms).

$$V_{OD} = A \times V_A$$

$$\text{where } A = \frac{1 + (R1/R2)}{4 + (R1/R2)}$$



NOTE A: Terminal numbers shown are for the DW and N packages.

Figure 7. Gain-Setting Configuration

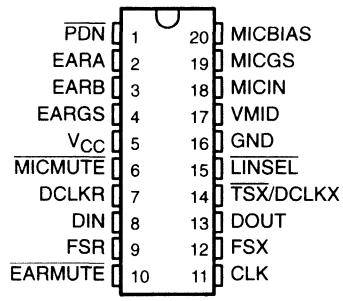
higher clock frequencies and sample rates

The VBAP is designed to work with sample rates up to 16 kHz where the frequency of the frame sync determines the sampling frequency. However, there is a fundamental requirement to maintain the ratio of the master clock frequency, f_{CLK}, to the frame sync frequency, f_{FSR}/f_{FSX}. This ratio for the VBAP is 1.152 MHz/8 kHz, or 144 master clocks per frame sync. For example, to operate the VBAP at a sampling rate of f_{FSR} and f_{FSX} equal to 16 kHz, f_{CLK} must be 144 times 16 kHz, or 2.304 MHz. If the VBAP is operated above an 8-kHz sample rate, however, it is expected that the performance becomes somewhat degraded. Exact parametric specifications for rates up to 16-kHz sample rate are not specified at this time.

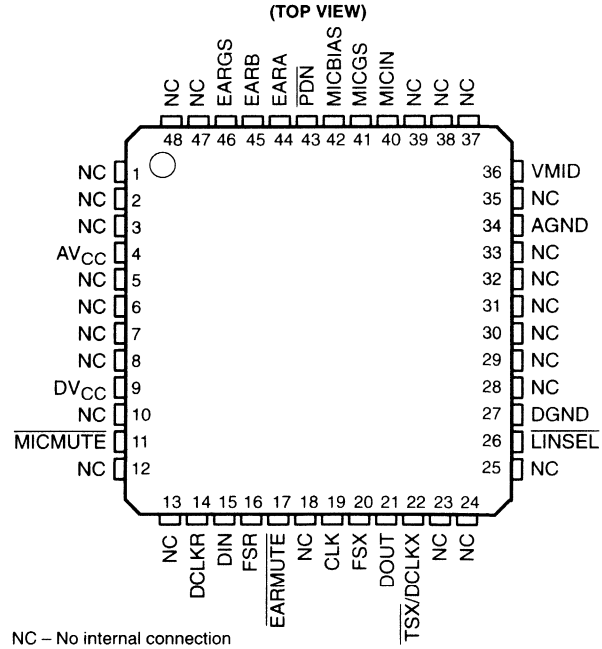
PRODUCT PREVIEW

- Single 3-V Operation
- Low Power Consumption:
  - Operating Mode . . . 20 mW Typ
  - Standby Mode . . . 5 mW Typ
  - Power-Down Mode . . . 2 mW Typ
- Combined A/D, D/A, and Filters
- Extended Variable-Frequency Operation
  - Sample Rates up to 16 kHz
  - Pass-Band up to 7.2 kHz
- Electret Microphone Bias Reference Voltage Available
- Drive a Piezo Speaker Directly
- Compatible With All Digital Signal Processors (DSPs)
- Selectable Between 8-Bit Companded and 13-Bit (Dynamic Range) Linear Conversion:
  - TLV320AC56 . . . μ-Law and Linear Modes
  - TLV320AC57 . . . A-Law and Linear Modes
- Programmable Volume Control in Linear Mode
- 300 Hz – 3.6 kHz Passband with Specified Master Clock
- Designed for Standard 2.048-MHz Master Clock for U.S. Analog, U.S. Digital, and CT2, DECT, GSM, and PCS Standards for Hand-Held Battery-Powered Telephones

DW OR N PACKAGE
(TOP VIEW)



PT PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCT PREVIEW

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

VBAP is a trademark of Texas Instruments Incorporated.

description

The TLV320AC56 and TLV320AC57 voice-band audio processor (VBAP) integrated circuits are designed to perform the transmit encoding (A/D conversion) and receive decoding (D/A conversion) together with transmit and receive filtering for voice-band communications systems. Cellular telephone systems are targeted in particular; however, these integrated circuits can function in other systems including digital audio, telecommunications, and data acquisition.

These devices are pin-selectable for either of two modes, companded and linear, providing data in two formats. In the companded mode, data is transmitted and received in 8-bit words. In the linear mode, 13 bits of data and either three bits of gain-setting control data, or three zero bits of padding to create a16-bit word, are sent and received.

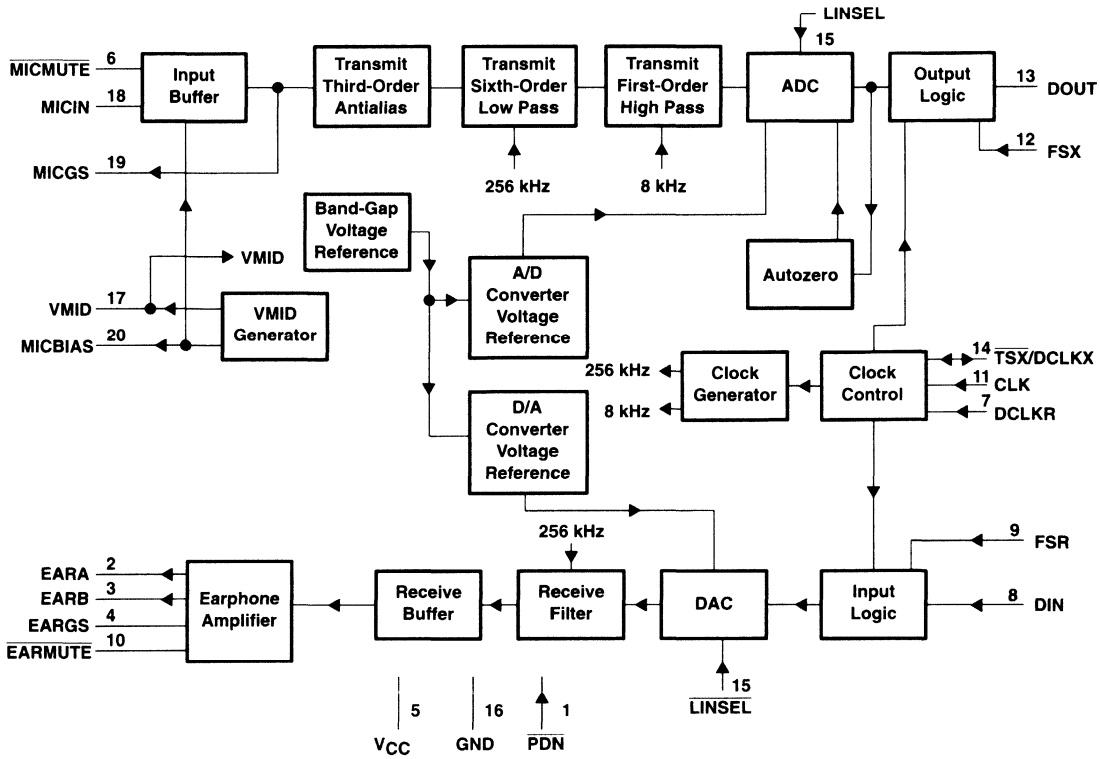
The transmit section is designed to interface directly with an electret microphone element. The microphone input signal (MICIN) is buffered and amplified with provision for setting the amplifier gain to accommodate a range of signal input levels. The amplified signal is passed through antialiasing and band-pass filters. The filtered signal is then applied to the input of a compressing analog-to-digital converter (COADC) when companded mode is selected. Otherwise, the analog-to-digital converter performs a linear conversion. The resulting data is then clocked out of DOUT as a serial data stream.

The receive section takes a frame of serial data on DIN and converts it to analog through an expanding digital-to-analog converter (EXDAC) when the companded mode is selected; otherwise, a linear conversion is performed. The analog signal then passes through switched capacitor filters, which provide out-of-band rejection, (sin x)/x correction functions, and smoothing. The filtered signal is sent to the earphone amplifier. The earphone amplifier has a differential output with adjustable gain and is designed to minimize static power dissipation.

A single on-chip high-precision band-gap circuit generates all voltage references, eliminating the need for external reference voltages. An internal reference voltage equal to $V_{CC}/2$, VMID, is used to develop the midlevel virtual ground for all the amplifier circuits and the microphone bias circuit. Another reference voltage, MICBIAS, can supply bias current for the microphone.

The TLV320AC5xC devices are characterized for operation from 0°C to 70°C. The TLV320AC5xI devices are characterized for operation from –40°C to 85°C.

functional block diagram



NOTE A: Terminal numbers shown are for the DW and N packages.

PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	TERMINAL NO. DW, N	TERMINAL NO. PT	I/O	DESCRIPTION
AGND	—	34		Ground return for all internal analog circuits
AV_{CC}	—	4		3-V supply voltage for all internal analog circuits
CLK	11	19	I	Clock input. In the fixed-data-rate mode, CLK is the master clock input as well as the transmit and receive data clock input . In the variable-data-rate mode, CLK is the master clock input only (digital).
DCLKR	7	14	I	Selection of fixed- or variable-data-rate operation. When DCLKR is connected to V_{CC}, the device operates in the fixed-data-rate mode. When DCLKR is not connected to V_{CC}, the device operates in the variable-data-rate mode and DCLKR becomes the receive data clock (digital).
DGND	—	27		Ground return for all internal digital circuits
DIN	8	15	I	Receive data input. Input data is clocked in on consecutive negative transitions of the receive data clock, which is CLK for a fixed data rate and DCLKR for a variable data rate (digital).
DOUT	13	21	O	Transmit data output. Transmit data is clocked out on consecutive positive transitions of the transmit data clock, which is CLK for a fixed data rate and DCLKX for a variable data rate (digital).
DV_{CC}	—	9		3-V supply voltage for all internal digital circuits
EARA	2	44	O	Earphone output. EARA forms a differential drive when used with the EARB signal (analog).
EARB	3	45	O	Earphone output. EARB forms a differential drive when used with the EARA signal (analog).
EARGS	4	46	I	Earphone gain set input of feedback signal for the earphone output. The ratio of an external potential divider network connected across EARA and EARB adjusts the power amplifier gain. Maximum gain occurs when EARGS is connected to EARB. Minimum gain occurs when EARGS is connected to EARA. Earphone frequency response correction is performed using an RC approach (analog).
$\overline{\text{EARMUTE}}$	10	17	I	Earphone output mute control signal. When $\overline{\text{EARMUTE}}$ is low, the output amplifier is disabled and no audio is sent to the earphone (digital).
FSR	9	16	I	Frame-synchronization clock input for the receive channel. In the variable-data-rate mode, this signal must remain high for the duration of the time slot. The receive channel enters the standby condition when FSR is TTL-low for five frames or longer. The device enters a production test-mode condition when either FSR or FSX is held high for five frames or longer (digital).
FSX	12	20	I	Frame synchronization clock input for the transmit channel. FSX operates independently of FSR, but also in an analogous manner to FSR. The transmit channel enters the standby condition when FSX is low for five frames or longer. The device enters a production test-mode condition when either FSX or FSR is held high for five frames or longer (digital).
GND	16	—		Ground return for all internal circuits
$\overline{\text{LINSEL}}$	15	26	I	Linear selection input. When low, $\overline{\text{LINSEL}}$ selects linear coding/decoding. When high, $\overline{\text{LINSEL}}$ selects companded coding/decoding. Companding code on the 'AC56 is μ-law, and companding code on the 'AC57 is A-law (digital).
MICBIAS	20	42	O	Microphone bias. MICBIAS voltage for the electret microphone is equal to VMID.
MICGS	19	41	O	Output of the internal microphone amplifier. MICGS is used as the feedback to set the microphone amplifier gain. If sidetone is required, it is accomplished by connecting a series network between MICGS and EARGS (analog).
MICIN	18	40	I	Microphone input. Electret microphone input to the internal microphone amplifier (analog)
$\overline{\text{MICMUTE}}$	6	11	I	Microphone input mute control signal. When $\overline{\text{MICMUTE}}$ is active (low), zero code is transmitted (dig.).
$\overline{\text{PDN}}$	1	43	I	Power-down input. When $\overline{\text{PDN}}$ is low, the device powers down to reduce power consumption (digital).
$\overline{\text{TSX}}$/DCLKX	14	22	I/O	Transmit time slot strobe (active-low output) or data clock (input) for the transmit channel. In the fixed-data-rate mode, $\overline{\text{TSX}}$/DCLKX is an open-drain output that pulls to ground and is used as an enable signal for a 3-state buffer. In the variable-data-rate mode, DCLKX becomes the transmit data clock input (digital).
V_{CC}	5	—		3-V supply voltage for all internal circuits
VMID	17	36	O	$V_{CC}/2$ bias voltage reference. A pair of external, low-leakage, high-frequency capacitors (1 μF and 470 pF) should be connected between VMID and ground for filtering.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.3 V to 5.5 V
Output voltage range at DOUT, V_O . . . . . −0.3 V to 5.5 V
Input voltage range at DIN, V_I . . . . . −0.3 V to 5.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: C suffix . . . . . 0°C to 70°C
I suffix . . . . . −40°C to 85°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage value is with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW
PT	1075 mW	7.1 mW/°C	756 mW	649 mW

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
Supply voltage, V_{CC} (see Note 3)		2.7	3.3	V
High-level input voltage, V_{IH}		2.2		V
Low-level input voltage, V_{IL}			0.8	V
Load resistance between EARA and EARB, R_L (see Note 4)		600		Ω
Load capacitance between EARA and EARB, C_L (see Note 4)			50	nF
Operating free-air temperature, T_A	TLV320AC56C, TLV320AC57C	0	70	°C
	TLV320AC56I, TLV320AC57I	−40	85	

NOTES: 2. To avoid possible damage to these CMOS devices and resulting reliability problems, the power-up sequence detailed in the system reliability features paragraph should be followed.
3. Voltages at analog inputs, outputs, and V_{CC} are with respect to GND.
4. R_L and C_L should not be applied simultaneously.

PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted)

supply current, f_{DCLKR} or f_{DCLKX} = 2.048 MHz, outputs not loaded, V_{CC} = 3 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
I_{CC}	Supply current from V_{CC}	Operating	$\overline{PDN}$ is high with CLK signal present		7.5	mA
		Power down	$\overline{PDN}$ is low for 500 µs		0.75	
		Standby – both	$\overline{PDN}$ is high with FSX and FSR held low		2	
		Standby – one	$\overline{PDN}$ is high with either FSX or FSR pulsing with the other held low		4.5	

digital interface

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	DOUT	I_{OH} = –3.2 mA, V_{CC} = 3 V	2.4	2.8		V
V_{OL}	Low-level output voltage		I_{OL} = 3.2 mA, V_{CC} = 3 V		0.2	0.4	V
I_{IH}	High-level input current, any digital input		V_I = 2.2 V to V_{CC}			10	µA
I_{IL}	Low-level input current, any digital input		V_I = 0 to 0.8 V			10	µA
C_i	Input capacitance				5		pF
C_o	Output capacitance				5		pF

† All typical values are at V_{CC} = 3 V, T_A = 25°C.

microphone interface

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IO}	Input offset voltage at MICIN		V_I = 0 to 3 V			±5	mV
I_{IB}	Input bias current at MICIN					±200	nA
B_1	Unity-gain bandwidth, open loop at MICIN‡				1.5		MHz
C_i	Input capacitance at MICIN				5		pF
A_V	Large-signal voltage amplification at MICGS				10000		V/V
I_{O}max	Maximum output current	VMID		3			µA
		MICBIAS (source only)		1			mA

† All typical values are at V_{CC} = 3 V, T_A = 25°C.
‡ The frequency of the first pole is 100 Hz.

speaker interface

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{O(PP)}$	AC output voltage				3§	Vpp
V_{OO}	Output offset voltage at EARA, EARB (single-ended)	Relative to GND			80	mVpk
$I_{I(lkg)}$	Input leakage current at EARGS	V_I = 0.5 V to (V_{CC} – 0.5) V			±200	nA
I_{O}max	Maximum output current	R_L = 600 Ω			±2.5	mA
r_o	Output resistance at EARA, EARB			1		Ω
	Gain change	$\overline{EARMUTE}$ low, max level when muted	–60			dB

† All typical values are at V_{CC} = 3 V, T_A = 25°C.
§ 2.5 V_{pp} when V_{CC} is 2.7 V.

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transmit gain and dynamic range, companded mode (μ-law or A-law) or linear mode selected, V_{CC} = 3 V, T_A = 25°C (unless otherwise noted) (see Notes 5 and 6)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit reference-signal level (0 dB) (see Note 7)	Companded mode selected, μ-law ('AC56)		0.614	Vrms
	Companded mode selected, A-law ('AC57)		0.616	
	Linear mode selected ('AC56 and 'AC57)		0.626	
Overload-signal level (MICIN at unity gain)	Companded mode selected, μ-law ('AC56)		2.5	Vpp
	Companded mode selected, A-law ('AC57)		2.5	
	Linear mode selected ('AC56 and 'AC57)		2.5	
Absolute gain error	0-dB input signal		±1	dB
Gain error with input level relative to gain at −10 dBm0	MICIN to DOUT at 3 dBm0 to −40 dBm0		±0.5	dB
	MICIN to DOUT at −41 dBm0 to −50 dBm0		±1.5	dB
	MICIN to DOUT at −51 dBm0 to −55 dBm0		±2	dB
Gain variation	V_{CC} ±10%, T_A = 0°C to 70°C		±0.5	dB

NOTES: 5. Unless otherwise noted, the analog input is 0 dB, 1020-Hz sine wave, where 0 dB is defined as the zero-reference point of the channel under test.
6. The input amplifier is set for inverting unity gain.
7. The reference-signal level, which is input to the transmit channel, is defined as a value 3 dB below the full-scale value of 2 V.

transmit filter transfer, companded mode (μ-law or A-law) or linear mode selected, over recommended ranges of supply voltage and free-air temperature, CLK = 2.048 MHz, FSX = 8 kHz (see Note 6)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to input signal gain at 1.02 kHz	Input amplifier set for unity gain, noninverting maximum gain output signal at MICIN is 0 dB	f_{MICIN} = 50 Hz	−10	0	dB
		f_{MICIN} = 200 Hz	−2.8	0	
		f_{MICIN} = 300 Hz to 3 kHz		±0.25	
		f_{MICIN} = 3.3 kHz	−0.55	0.2	
		f_{MICIN} = 3.4 kHz	−1	−0.1	
		f_{MICIN} = 4 kHz		−14	
		f_{MICIN} ≥4.6 kHz		−32	

NOTE 6. The input amplifier is set for inverting unity gain.

transmit idle channel noise and distortion, companded mode with μ-law or A-law selected, over recommended ranges of supply voltage and operating free-air temperature (see Note 8)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise, psophometrically weighted	MICIN connected to MICGS through a 10-kΩ resistor		−72	dB0p
Transmit noise, C-message weighted	MICIN connected to MICGS through a 10-kΩ resistor		10	dBrnC0
Transmit signal-to-distortion ratio with sine-wave input	MICIN to DOUT at 0 dBm0 to −24 dBm0	36		dB
	MICIN to DOUT at −25 dBm0 to −30 dBm0	34		
	MICIN to DOUT at −31 dBm0 to −38 dBm0	30		
	MICIN to DOUT at −39 dBm0 to −40 dBm0	24		
	MICIN to DOUT at −41 dBm0 to −45 dBm0	20		
Intermodulation distortion, 2-tone CCITT method, composite power level −13 dBm0	CCITT G.712 (7.1), R2	49		dB
	CCITT G.712 (7.2), R3	51		

NOTE 8: Transmit noise, linear mode: 200 μVrms is equivalent to −74 dB (referenced to device 0-dB level).

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transmit idle channel noise and distortion, linear mode selected, over recommended ranges of supply voltage and operating free-air temperature (see Notes 6 and 8)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise	MICIN connected to MICGS through a 10-kΩ resistor		200	μVrms
Transmit signal-to-distortion ratio with sine-wave input	MICIN to DOUT at 0 dBm0 to –10 dBm0	46		dB
	MICIN to DOUT at –11 dBm0 to –12 dBm0	44		
	MICIN to DOUT at –13 dBm0 to –18 dBm0	40		
	MICIN to DOUT at –19 dBm0 to –24 dBm0	35		
	MICIN to DOUT at –25 dBm0 to –40 dBm0	20		
	MICIN to DOUT at –41 dBm0 to –45 dBm0	18		

NOTES: 6. The input amplifier is set for inverting unity gain.
8. Transmit noise, linear mode: 200 μVrms is equivalent to –74 dB (referenced to device 0-dB level).

receive gain and dynamic range, companded mode (μ-law or A-law) or linear mode selected, V_{CC} = 3 V, T_A = 25°C (unless otherwise noted) (see Notes 9 and 10)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive reference-signal level (0 dB) (see Note 11)	Companded mode selected, μ-law ('AC56)		0.736	Vrms
	Companded mode selected, A-law ('AC57)		0.739	
	Linear mode selected ('AC56 and 'AC57)		0.751	
Overload-signal level	Companded mode selected, μ-law ('AC56)		3	Vpp
	Companded mode selected, A-law ('AC57)		3	
	Linear mode selected ('AC56 and 'AC57)		3	
Absolute gain error	0-dB input signal		±1	dB
Gain error with output level relative to gain at –10 dBm0	DIN to EARA and EARB at 3 dBm0 to –38 dBm0		±0.5	dB
	DIN to EARA and EARB at –39 dBm0 to –50 dBm0		±1.5	
	DIN to EARA and EARB at –51 dBm0 to –55 dBm0		±2	
Gain variation	V_{CC} ±10%, T_A = 0°C to 70°C		±0.5	dB

NOTES: 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.
10. Unless otherwise noted, the digital input is a word stream generated by passing a 0-dB sine wave at 1020 Hz through an ideal encoder, where 0 dB is defined as the zero reference.
11. This reference-signal level is measured at the speaker output of the receive channel with the gain of the output speaker amplifier set to unity.

receive filter transfer, companded mode (μ-law or A-law) or linear mode selected, over recommended ranges of supply voltage and operating free-air temperature, FSR = 8 kHz (see Note 9)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	DIN = 0 dBm0	f_{DIN} = < 200 Hz		0.25	dB
		f_{DIN} = 200 Hz	–0.5	0.25	
		f_{DIN} = 300 Hz to 3 kHz		±0.25	
		f_{DIN} = 3.3 kHz	–0.55	0.2	
		f_{DIN} = 3.4 kHz	–1	–0.1	
		f_{DIN} = 4 kHz		–14	
		f_{DIN} = > 4.6 kHz		–30	

NOTE 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.

PRODUCT PREVIEW

receive idle channel noise and distortion, companded mode with μ-law or A-law selected, over recommended ranges of supply voltage and operating free-air temperature (see Note 9)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive noise, psophometrically weighted	DIN = 11010101 (A-law)		−72	dB0p
Receive noise, C-message weighted	DIN = 11111111 (μ-law)		8	dBrnc0
Receive signal-to-distortion ratio with sine-wave input	DIN to EARA and EARB at 0 dBm0 to −18 dBm0	36		dB
	DIN to EARA and EARB at −19 dBm0 to −24 dBm0	34		
	DIN to EARA and EARB at −25 dBm0 to −30 dBm0	30		
	DIN to EARA and EARB at −31 dBm0 to −38 dBm0	23		
	DIN to EARA and EARB at −39 dBm0 to −45 dBm0	17		

NOTE 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.

receive idle channel noise and distortion, linear mode selected, over recommended ranges of supply voltage and operating free-air temperature (see Notes 9 and 12)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive noise	DIN = 00000000		200	μVrms
Receive signal-to-distortion ratio with sine-wave input	DIN to EARA and EARB at 0 dBm0 to −12 dBm0	46		dB
	DIN to EARA and EARB at −13 dBm0 to −18 dBm0	38		
	DIN to EARA and EARB at −19 dBm0 to −24 dBm0	32		
	DIN to EARA and EARB at −25 dBm0 to −40 dBm0	18		
	DIN to EARA and EARB at −41 dBm0 to −45 dBm0	15		
Intermodulation, 2-tone CCITT distortion method, composite power level −13 dBm0	CCITT G.712 (7.1), R2	50		dB
	CCITT G.712 (7.2), R3	54		

NOTES: 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.
12. Receive noise, linear mode: 200 μVrms is equivalent to −71 dB (referenced to device 0-dB level).

power supply rejection and crosstalk attenuation over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Supply voltage rejection, transmit channel	Idle channel, supply signal = 100 mVrms, f = 0 to 30 kHz (measured at DOUT)		−30		dB
Supply voltage rejection, receive channel	Idle channel, supply signal = 100 mVrms, EARGS connected to EARB, f = 0 to 30 kHz (measured differentially between EARA and EARB)		−30		dB
Crosstalk attenuation, transmit-to-receive (differential)	MICIN = 0 dB, f = 1.02 kHz, unity transmit gain, EARGS connected to EARB, measured differentially between EARA and EARB	50			dB
Crosstalk attenuation, receive-to-transmit	DIN = 0 dBm0, f = 1.02 kHz, unity transmit gain, measured at DOUT	50			dB

† All typical values are at V_{CC} = 3 V, T_A = 25°C.

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timing requirements

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figure 1 through Figure 4)

		MIN	NOM†	MAX	UNIT
t_t	Transition time, CLK and DCLKX/DCLKR			10	ns
	Duty cycle, CLK	45%	50%	55%	
	Duty cycle, DCLKX/DCLKR	45%	50%	55%	

† All typical values are at V_{CC} = 3 V, T_A = 25°C.

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 2)

		MIN	MAX	UNIT
$t_{su(FSX)}$	Setup time, FSX high before CLK↓	20	468	ns
$t_{h(FSX)}$	Hold time, FSX high after CLK↓	20	468	ns

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 1)

		MIN	MAX	UNIT
$t_{su(FSR)}$	Setup time, FSR high before CLK↓	20	468	ns
$t_{h(FSR)}$	Hold time, FSR high after CLK↓	20	468	ns
$t_{su(DIN)}$	Setup time, DIN high or low before CLK↓	20		ns
$t_{h(DIN)}$	Hold time, DIN high or low after CLK↓	20		ns

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see Figure 4)

		MIN	MAX	UNIT
$t_{su(FSX)}$	Setup time, FSX high before DCLKX↓	40	$t_{c(DCLKX)}-40$	ns
$t_{h(FSX)}$	Hold time, FSX high after DCLKX↓	35	$t_{c(DCLKX)}-35$	ns

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see Figure 3)

		MIN	MAX	UNIT
$t_{su(FSR)}$	Setup time, FSR high before DCLKR↓	40		ns
$t_{h(FSR)}$	Hold time, FSR high after DCLKR↓	35	$t_{c(DCLKR)}-35$	ns
$t_{su(DIN)}$	Setup time, DIN high or low before DCLKR↓	30		ns
$t_{h(DIN)}$	Hold time, DIN high or low after DCLKR↓	30		ns

switching characteristics

propagation delay times over recommended ranges of operating conditions, fixed-data-rate mode, C_L = 0 to 10 pF (see Figure 2)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	From CLK bit 1 high to DOUT bit 1 valid			35	ns
t_{pd2}	From CLK high to DOUT valid, bits 2 to n			35	ns
t_{pd3}	From CLK bit n low to DOUT bit n Hi-Z		30		ns
t_{pd4}	From CLK bit 1 high to $\overline{TSX}$ active (low)	R_{pullup} = 1.24 kΩ		40	ns
t_{pd5}	From CLK bit n low to $\overline{TSX}$ inactive (high)	R_{pullup} = 1.24 kΩ	30		ns

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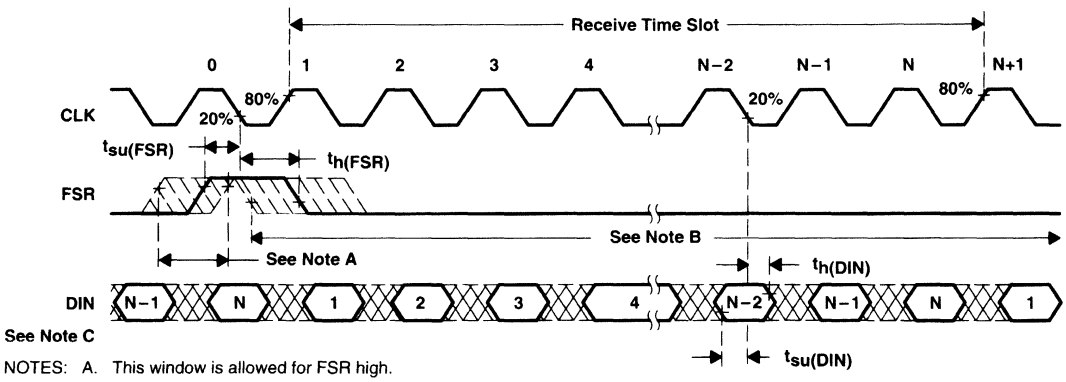
propagation delay times over recommended ranges of operating conditions, variable-data-rate mode (see Figure 4)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{pd6}	FSX high to DOUT bit 1 valid	C_L = 0 to 10 pF		30	ns
t_{pd7}	DCLKX high to DOUT valid, bits 2 to n	C_L = 0 to 10 pF		40	ns
t_{pd8}	FSX low to DOUT bit n Hi-Z		20		ns

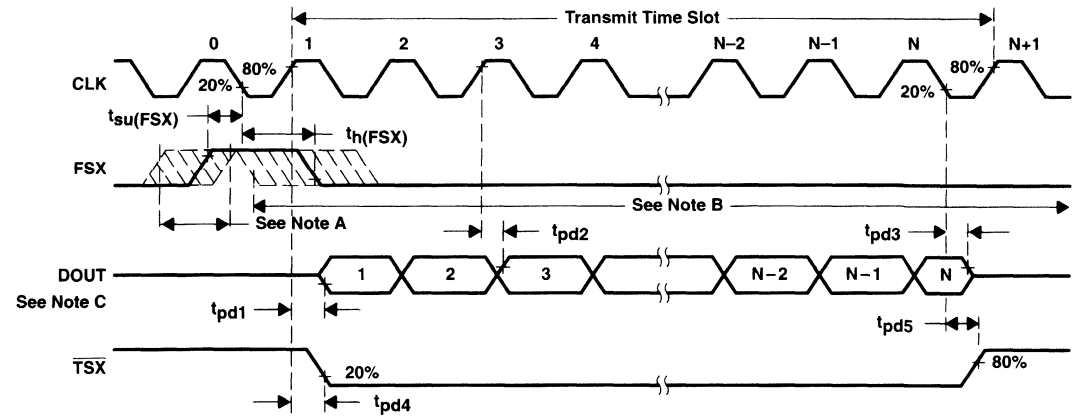
PARAMETER MEASUREMENT INFORMATION

All timing parameters are referenced to V_{IH} and V_{IL}. Bit 1 = MSB (most significant bit) and is clocked in first on DIN or clocked out first on DOUT. Bit n = LSB (least significant bit) and is clocked in last on DIN or is clocked out last on DOUT. N = 8 for the companded mode, and N = 16 for the linear mode.



NOTES: A. This window is allowed for FSR high.
B. This window is allowed for FSR low.
C. Transitions are measured at 50%.

Figure 1. Fixed-Data Rate Mode, Receive Side Timing Diagram



NOTES: A. This window is allowed for FSX high.
B. This window is allowed for FSX low ($t_{h(FSX)}$ max determined by data collision considerations).
C. Transitions are measured at 50%.

Figure 2. Fixed-Data Rate Mode, Transmit Side Timing Diagram

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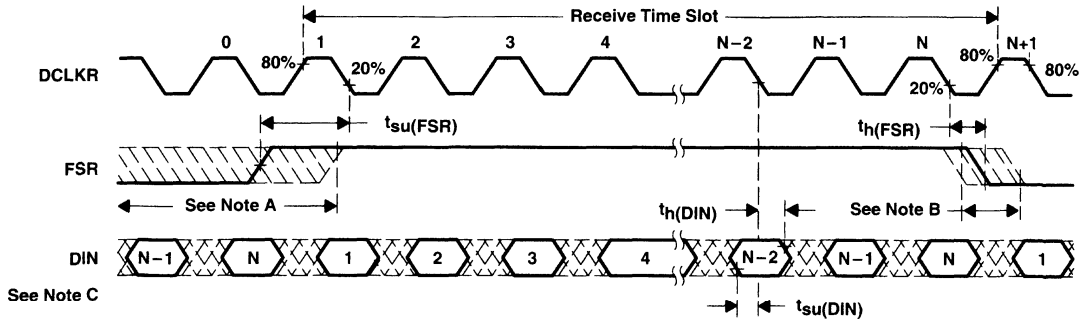
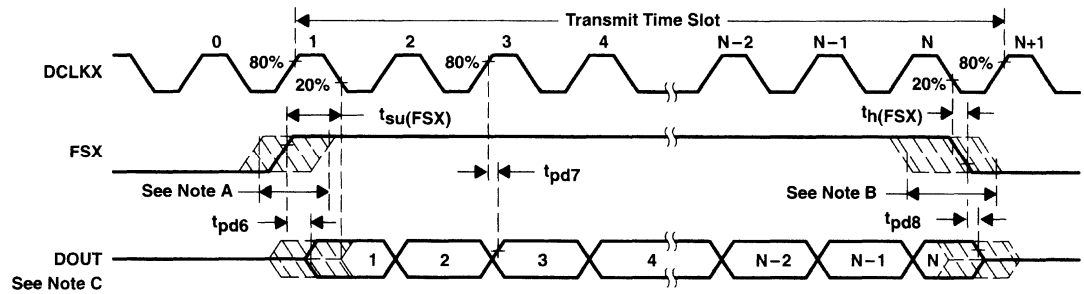
PARAMETER MEASUREMENT INFORMATION



NOTES: A. This window is allowed for FSR high ($t_{su(FSR)}$ max determined by data collision considerations).
B. This window is allowed for FSR low.
C. Transitions are measured at 50%.

Figure 3. Variable-Data Rate Mode, Receive Side Timing Diagram



NOTES: A. This window is allowed for FSX high.
B. This window is allowed for FSX low without data repetition.
C. Transitions are measured at 50%.

Figure 4. Variable-Data Rate Mode, Transmit Side Timing Diagram

PRODUCT PREVIEW

PRINCIPLES OF OPERATION

general

system reliability features

The device should be powered up and initialized as follows:

1. Apply GND.
2. Apply V_{CC}.
3. Connect all clocks.
4. Apply TTL high to $\overline{PDN}$.
5. Apply synchronizing pulses to FSX and/or FSR.

Even though the VBAP is heavily protected against latch-up, it is still possible to cause it to latch up under certain improper power conditions. To help ensure that latch-up does not occur, a reverse-biased Schottky diode (with a forward voltage drop of less than or equal to 0.4 V — 1N5711 or equivalent) should be connected between V_{CC} (power supply) and GND.

On the transmit channel, digital outputs DOUT and $\overline{TSX}$ are held in the high-impedance state for approximately four frames (500 µs) after power up or application of V_{CC}. After this delay, DOUT, $\overline{TSX}$, and signaling are functional and occur in the correct time slot. The analog circuits on the transmit side require approximately 60 ms to reach their equilibrium value due to the autozero circuit settling time. To further enhance system integrity, DOUT and $\overline{TSX}$ are placed in the high-impedance state after an interruption of CLK.

power-down and standby operations

To minimize power consumption, a power-down mode and three standby modes are provided.

For power down, an external low signal is applied to $\overline{PDN}$. In the absence of a signal, $\overline{PDN}$ is internally pulled up to a high logic level and the device remains active. In the power-down mode, the average power consumption is reduced to 2 mW.

Three standby modes give the user the option of placing the entire device on standby, placing only the transmit channel on standby, or placing only the receive channel on standby. To place the entire device on standby, both FSX and FSR are held low. For transmit-only operation (receive channel on standby), FSX is pulsing and FSR is held low. For receive-only operation (transmit section on standby), FSR is pulsing and FSX is held low. When the entire device is in standby mode, power consumption is reduced to 5 mW. See Table 1 for power-down and standby procedures.

PRINCIPLES OF OPERATION

Table 1. Power-Down and Standby Procedures

DEVICE STATUS	PROCEDURE	TYPICAL POWER CONSUMPTION	DIGITAL OUTPUT STATUS
Power on	$\overline{PDN}$ = high, FSX = pulses, FSR = pulses	20 mW	Digital outputs active but not loaded
Power down	$\overline{PDN}$ = low, FSX, FSR = X†	2 mW	$\overline{TSX}$ and DOUT in the high-impedance state
Entire device on standby mode	FSX = low, FSR = low, $\overline{PDN}$ = high	5 mW	$\overline{TSX}$ and DOUT in the high-impedance state
Only transmit channel in standby mode	FSX = low, FSR = pulses, $\overline{PDN}$ = high	10 mW	$\overline{TSX}$ and DOUT in the high-impedance state within five frames
Only receive channel in standby mode	FSR = low, FSX = pulses, $\overline{PDN}$ = high	10 mW	Digital outputs active but not loaded

† X = don't care

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fixed-data-rate timing

Fixed-data-rate timing is selected by connecting DCLKR to V_{CC} and uses the master clock (CLK), frame synchronization clocks (FSX and FSR), and the $\overline{TSX}$ output. FSX and FSR are inputs that set the sampling frequency. Data is transmitted on DOUT on the positive transitions of CLK following the rising edge of FSX. Data is received on DIN on the falling edges of CLK following FSR. A D/A conversion is performed on the received digital word, and the resulting analog sample is held on an internal sample-and-hold capacitor until transferred to the receive filter. The data word is eight bits long in the companded mode and 16 bits long in the linear mode.

variable-data-rate timing

Variable-data-rate timing is selected by connecting DCLKR to the receive data clock. In this mode, the master clock (CLK) controls the switched-capacitor filters, while data transfer into DIN and out of DOUT is controlled by DCLKR and DCLKX respectively. This allows the data to be transferred in and out of the device at any rate up to the frequency of the master clock. DCLKR and DCLKX must be synchronous with CLK.

While the FSX input is high, data is transmitted from DOUT on consecutive positive transitions of DCLKX. Similarly, while the FSR input is high, the data word is received at DIN on consecutive negative transitions of DCLKR. The transmitted data word at DOUT is repeated in all remaining time slots in the frame as long as DCLKX is pulsed and FSX is held high. This feature, which allows the data word to be transmitted more than once per frame, is available only with variable-data-rate timing.

asynchronous operations

To avoid crosstalk problems associated with special interrupt circuits, the design includes separate converters, filters, and voltage references on the transmit and receive sides to allow completely independent operation of the two channels. In either timing mode, the master clock, data clock, and time-slot strobe must be synchronized at the beginning of each frame.

precision voltage references

A precision band-gap reference voltage is generated internally and is used to supply all the references required for operation of both the transmit and receive channels. The gain in each channel is trimmed during the manufacturing process. This ensures very accurate, stable gain performance over variations in supply voltage and device temperature.

PRINCIPLES OF OPERATION

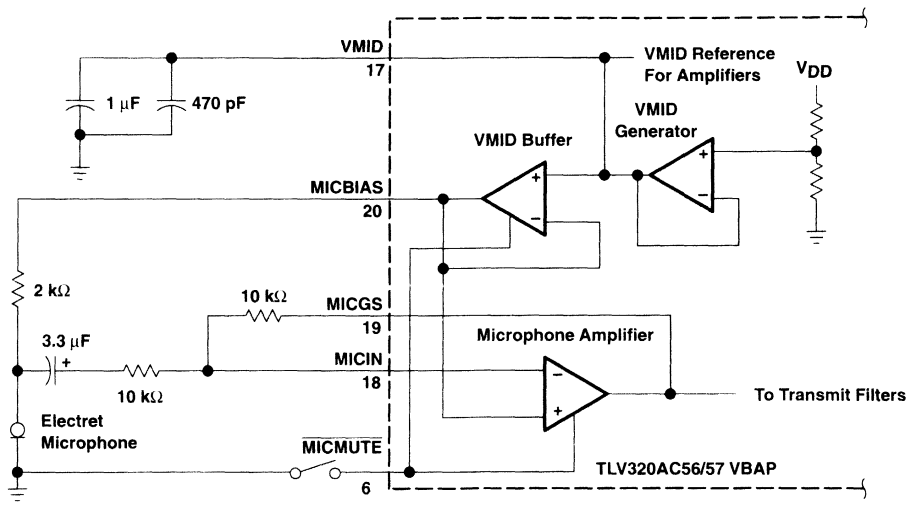
conversion laws

The TLV320AC56 provides μ-law companding operation that approximates the CCITT G.711 recommendation. The TLV320AC57 provides A-law companding operation that approximates the CCITT G.711 recommendation. The linear mode of operation uses a 13-bit two's-complement format and is the same for both the TLV320AC56 and the TLV320AC57.

transmit operation

microphone input

The microphone input amplifier is designed specifically to interface to electret-type microphone elements, as shown in Figure 5. The VMID buffer circuit provides a voltage (MICBIAS) equal to 1/2 V_{CC} as a reference for the microphone amplifier and a bias voltage to the electret microphone. The microphone amplifier output (MICGS) is used in conjunction with a feedback network and applied to the amplifier inverting input (MICIN) to set the amplifier gain. VMID appears at a terminal to provide a place to filter the VMID voltage.



NOTE A: Terminal numbers shown are for the DW and N packages.

Figure 5. Typical Microphone Interface

microphone mute function

The $\overline{\text{MICMUTE}}$ input causes the digital circuitry to transmit all zero code on DOUT.

transmit filter

A low-pass antialiasing section is included on the device and achieves a 35-dB attenuation at the sampling frequency. No external components are required to provide the necessary antialiasing function for the switched-capacitor section of the transmit filter.

PRODUCT PREVIEW

PRINCIPLES OF OPERATION

encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample-and-hold capacitor. The encoder performs an A/D conversion on a switched-capacitor array. Digital data representing the sample is transmitted on the first 8 or 16 data clock cycles of the next frame.

The autozero circuit corrects for dc offset on the input signal to the encoder using the sign-bit averaging technique. The sign bit from the encoder output is long-term averaged and subtracted from the input to the encoder.

data word structure

The data word is eight bits long in the companded mode and all eight bits represent one audio data sample. The sign bit is the first bit transmitted.

The data word is 16 bits long in the linear mode. The first 13 bits comprise the audio data sample, and the last three bits form the volume control word in the receive direction (DIN) and are zero pad bits in the transmit direction (DOUT). The sign bit is transmitted first.

receive operation

decoding

In the companded mode, the serial data word is received at DIN on the first eight clock cycles in fixed-data rate and on the last eight clock cycles in variable-data rate. In the linear mode, the serial data word is received at DIN on the first 13 clock cycles. D/A conversion is performed, and the corresponding analog sample is held on an internal sample-and-hold capacitor. This sample is transferred to the receive filter.

receive filter

The receive section of the filter provides pass-band flatness and stop-band rejection that approximates both the AT&T D3/D4 specification and CCITT recommendation G.712 when operated at the recommended frequencies. The filter contains the required compensation for the (sin x)/x response of such decoders.

receive buffer

The receive buffer contains the volume control.

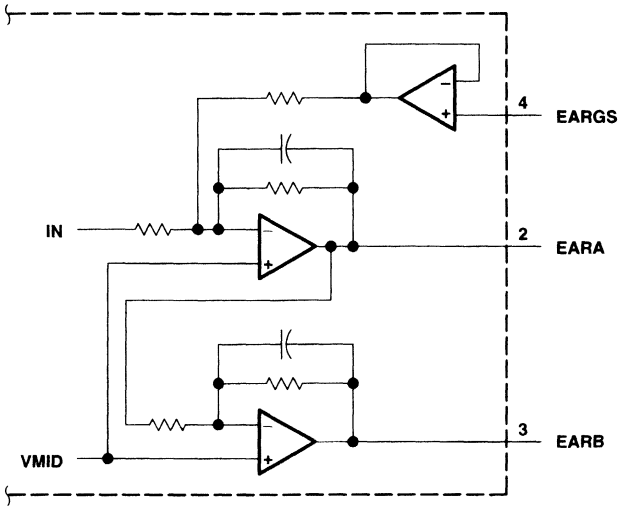
earphone amplifier

The earphone audio-output amplifier has a balanced output, as shown in Figure 6, to allow maximum flexibility in output configuration. The output amplifier is designed to directly drive a piezo earphone in the differential configuration without any additional external components. The output can also be used to drive a single-ended load with the output signal voltage centered around $V_{CC}/2$.

The receive-channel output level can be adjusted between specified limits by connecting an external resistor network to EARGS.

PRODUCT PREVIEW

PRINCIPLES OF OPERATION



NOTE A: Terminal numbers shown are for the DW and N packages.

Figure 6. Earphone Audio-Output Amplifier Configuration and Internal Gain-Setting Network

receive data format

In the companded mode, eight bits of data are received. The sign bit is the first bit received (see Table 2).

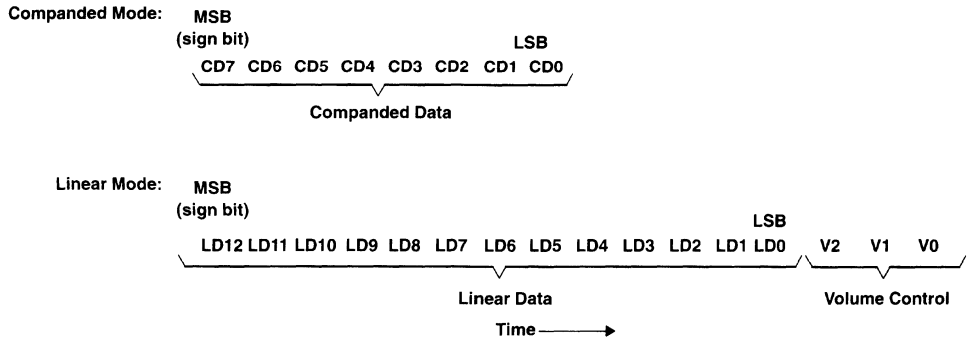
In the linear mode, 16 bits of data are received. The first 13 bits are the D/A code, and the remaining three bits form the volume control word (see Table 2). The volume control function is actually an attenuation control in which the first bit received is the most significant. The maximum volume occurs when all three volume control bits are zero. Eight levels of attenuation are selectable in 3-dB steps, giving a maximum attenuation of 21 dB when all bits are 1s. The volume control bits are not latched into the VBAP and must be present in each received data word.

PRINCIPLES OF OPERATION

Table 2. Receive-Data Bit Definitions

BIT NO.	COMPANDED MODE	LINEAR MODE
0	CD7	LD12
1	CD6	LD11
2	CD5	LD10
3	CD4	LD9
4	CD3	LD8
5	CD2	LD7
6	CD1	LD6
7	CD0	LD5
8	–	LD4
9	–	LD3
A	–	LD2
B	–	LD1
C	–	LD0
D	–	V2
E	–	V1
F	–	V0

Volume control and other control bits always follow the PCM data in time:



where:

CD7–CD0 = Data word when in companded mode
LD12–LD0 = Data word when in linear mode
V2, V1, V0 = Volume (attenuation control) 000 = maximum volume, 3 dBm0
111 = minimum volume, –18 dBm0

PRODUCT PREVIEW

APPLICATION INFORMATION

output gain set design considerations (see Figure 7)

EARA and EARB are low-impedance complementary outputs. The voltages at the nodes are:
V_{O+} at EARA
V_{O-} at EARB
$V_{OD} = V_{O+} - V_{O-}$ (total differential response)

R1 and R2 are a gain-setting resistor network with the center tap connected to EARGS.

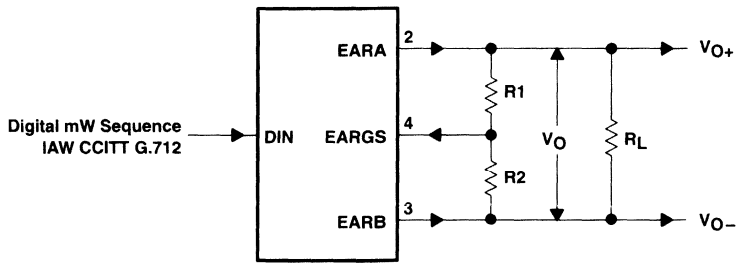
A value greater than 10 kΩ and less than 100 kΩ for R1 + R2 is recommended because of the following:

The parallel combination R1 + R2 and R_L sets the total loading. The total capacitance at EARGS and the parallel combination of R1 and R2 define a time constant that has to be minimized to avoid inaccuracies.

V_A represents the maximum available digital mW output response (V_A = 1.001 Vrms).

$$V_{OD} = A \times V_A$$

$$\text{where } A = \frac{1 + (R1/R2)}{4 + (R1/R2)}$$



NOTE A: Terminal numbers shown are for the DW and N packages.

Figure 7. Gain-Setting Configuration

higher clock frequencies and sample rates

The VBAP is designed to work with sample rates up to 16 kHz where the frequency of the frame sync determines the sampling frequency. However, there is a fundamental requirement to maintain the ratio of the master clock frequency, f_{CLK}, to the frame sync frequency, f_{FSR}/f_{FSX}. This ratio for the VBAP is 2.048 MHz/8 kHz, or 256 master clocks per frame sync. For example, to operate the VBAP at a sampling rate of f_{FSR} and f_{FSX} equal to 16 kHz, f_{CLK} must be 256 times 16 kHz, or 4.096 MHz. If the VBAP is operated above an 8-kHz sample rate, however, it is expected that the performance becomes somewhat degraded. Exact parametric specifications for rates up to 16-kHz sample rate are not specified at this time.

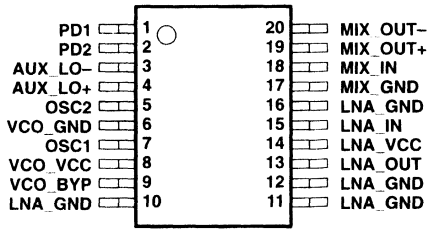
PRODUCT PREVIEW

7 RF for Personal Communications

SLWS021 – JUNE 1996

- **Low-Noise Amplifier (LNA), Radio Frequency (RF) Mixer, and Voltage-Controlled Oscillator (VCO)**
- **High 1-dB Compression Mode**
- **High Linearity Mode**
- **Conversion From RF to Intermediate Frequency (IF) on a Single Chip**
- **Suitable for Portable 900-MHz Cellular and Cordless Telephones**
- **Low Current Consumption**
- **Operates From 3.5 V to 5.5 V**
- **20-Pin Plastic Shrink Small Outline (SSOP) Package**
- **Application Selectable On-board or External Oscillator**

DB PACKAGE
(TOP VIEW)



description

Texas Instruments (TI™) TRF1015 is a single-chip RF down-converter suitable for 900-MHz receiver applications. It combines a low-noise amplifier (LNA), a buffered voltage-controlled oscillator (VCO), and an RF mixer, into a 20-pin SSOP package with very few external components required.

Three independently selectable modes of operation are provided for both the LNA and the mixer: low-current mode, low-noise mode, and high 1-dB compression mode with low-noise and moderate current consumption. The high compression mode is suitable for applications requiring full duplex capability. It is suitable for maintaining receiver sensitivity in the presence of large interfering signals and also has a high bit error rate (BER) mode for digital modulation.

The LNA has a gain of 14 dB and noise figure of 2 dB. Input and output characteristic impedances of the LNA are 50-Ω. The single balanced RF mixer has a gain of 11 dB with single-sideband (SSB) noise figure of 10 dB. The VCO has a operational range from 650 MHz to 1150 MHz and a minimum tuning range of 25 MHz using an external varactor. The VCO gain and tuning range can be adjusted to meet the phase-locked loop (PLL) design requirement with an external shunt and feedback capacitors in series with the resonator. A buffered output of the VCO signal is provided for phase locking capability and can be configured for single-ended or differential operation. The VCO with the RF mixer can convert an RF signal in the range of 800 MHz to 1000 MHz to a first IF of 30 MHz to 100 MHz.

Power consumption is kept to a minimum and can be further reduced by placing only the required modules in operate mode and the remaining modules in standby mode.

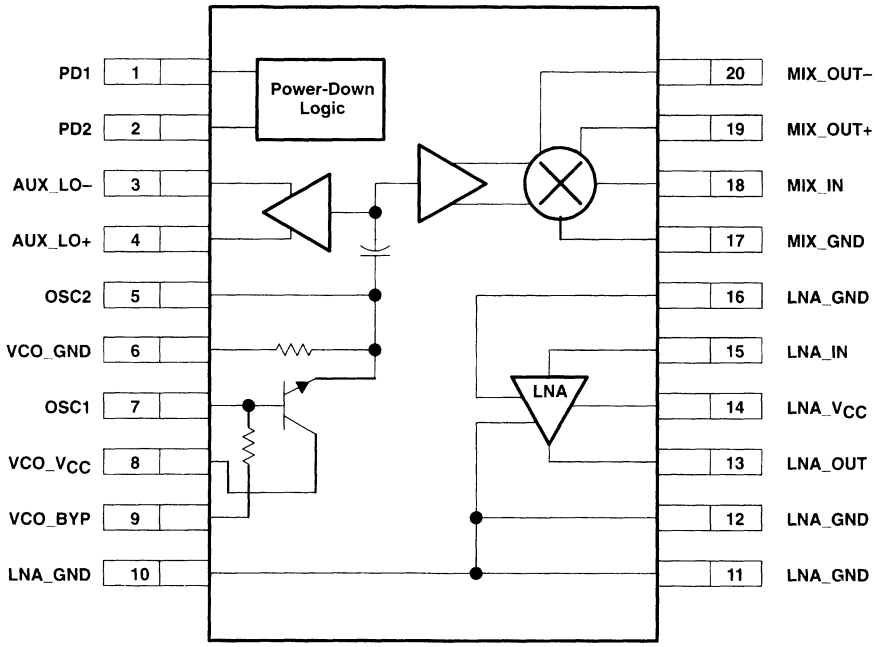
Typical Power Consumption at V_{CC} = 3.75 V

MODULE	STANDBY	OPERATE
LNA (1, 0)	100 µW	26 mW
RF mixer (1, 0)(0,1)	0	30 mW
VCO and buffer amplifiers	0	45 mW
All modules	100 µW	101 mW

The TRF1015 is offered in the 20-pin DB package and is characterized for operation from −40°C to 85°C free-air temperature.

PRODUCT PREVIEW

functional block diagram



PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AUX_LO–	3	O	PLL auxiliary local oscillator (LO) output (inverting)
AUX_LO+	4	O	PLL auxiliary LO output (non-inverting)
LNA_GND	10		LNA ground
LNA_GND	12		LNA ground
LNA_IN	15	I	LNA RF input
LNA_OUT	13	O	LNA RF output
LNA_VCC	14		LNA voltage supply
LNA_GND	11	O	LNA ground
LNA_GND	16	O	LNA ground
MIX_GND	17		Mixer ground
MIX_IN	18	I	Mixer RF input
MIX_OUT–	20	O	Mixer IF output (inverting)
MIX_OUT+	19	O	Mixer IF output (non-inverting)
OSC2	5		External oscillator input
OSC1	7		VCO tank port
PD1	1	I	Powerdown LSB
PD2	2	I	Powerdown MSB
VCO_BYPASS	9		VCO bypass port (external capacitor)
VCO_GND	6		VCO ground
VCO_VCC	8		VCO voltage supply

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} ..... –0.3 V to 6 V
Input voltage range, V_I ..... –0.3 V to V_{CC} + 0.3 V
Power dissipation at or below T_A = 25°C ..... 300 mW
Maximum operating virtual-junction temperature, T_J ..... 150°C
Operating free-air temperature range ..... –40°C to 85°C
Storage temperature range ..... –65°C to 125°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3.5	3.75	5.5	V
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	–0.3		0.8	V
T_A	Operating free-air temperature	–40		85	°C
T_J	Virtual-junction temperature	–30		105	°C

electrical characteristics over recommended operating free-air temperature range and V_{CC} = 3.75 V; measured in recommended application board

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
CASCADE (LNA/SAW‡/MIXER)	IF = 45 MHz				
Power conversion gain		21	22	23	dB
SSB noise figure			3.5	5	dB
Input 1 dB compression point			−26		dBm
Input 3rd order intercept point, 2 $f_2 - f_1$		−14	−12		dBm
Input 2nd order intercept point, 2 $f_{LO} - 2 f_{RF}$	f_{LO} = 914 MHz f_{RF} = 891.5 MHz	6	17		dBm
LO feedthrough to RF	880 MHz to 1070 MHz		−45	−40	dBm
LNA					
RF frequency range		850		970	MHz
Power gain	PD1 = 1, PD2 = 1		13.5		dB
	PD1 = 0, PD2 = 1		14		
Noise figure	PD1 = 1, PD2 = 1		1.8		dB
	PD1 = 0, PD2 = 1		2		
Gain/temperature sensitivity			0.008		dB/°C
Gain/frequency sensitivity			–0.015		dB/MHz
Reverse isolation			−25		dB
Input return loss	Z_I = 50 Ω		−10		dB
Output return loss	Z_O = 50 Ω		−12		dB
Input 1 dB compression	PD1 = 1, PD2 = 1		−15		dBm
	PD1 = 0, PD2 = 1		−10		
Input 3rd-order intercept	PD1 = 1, PD2 = 1		−6		dBm
	PD1 = 0, PD2 = 1		−1		

† Typical values are at T_A = 25°C.
‡ Surface acoustic wave (SAW)

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range and V_{CC} = 3.75 V; measured in recommended application board (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
RF MIXER					
RF frequency range		850		970	MHz
LO frequency range		880		1070	MHz
IF frequency range		30		100	MHz
Power conversion gain			11		dB
SSB noise figure			10		dB
RF input impedance			50		Ω
LO input impedance	External VCO		50		Ω
IF output impedance	Open-collector output		1000		Ω
RF input return loss	Z_I = 50 Ω		–10		dB
LO input return loss	Z_I = 50 Ω		–10		dB
IF output return loss	Z_O = 50 Ω		–10		dB
Input 1 dB compression point			–10		dBm
Input 3rd-order intercept point, 2 $f_2 - f_1$			–1		dBm
Input 2nd-order intercept point, 2 $f_{LO} - 2\ f_{RF}$	f_{LO} = 914 MHz f_{RF} = 891.5 MHz		28		dBm
RF feedthrough to IF	850 MHz to 970 MHz			–20	dB
LO feedthrough to IF	850 MHz to 1070 MHz			–25	dB
LO feedthrough to RF	880 MHz to 1070 MHz			–15	dB
VCO					
Frequency range	Tuning range is 25 MHZ min, 30 MHZ typ, centered around the set VCO frequency.	650		1150	MHz
Auxiliary LO output power	Into 50 Ω load		–11		dBm
Phase noise	Offset = 60 kHz		–114		dBc/Hz
Harmonics			–20		dBc

† Typical values are at T_A = 25°C.

PRODUCT PREVIEW

current consumption over recommended operating free-air temperature range and V_{CC} = 3.75 V; (PD1 = 1, PD2 = 1)

	TYP†	MAX	UNIT
LNA	3	4	mA
RF mixer	6	7	mA
VCO and buffer amplifiers	12	14	mA

current consumption over recommended operating free-air temperature range and V_{CC} = 3.75 V; (PD1 = 0, PD2 = 1)

	TYP†	MAX	UNIT
LNA	7	8	mA
RF mixer	8	9	mA
VCO and buffer amplifiers	12	14	mA

current consumption over recommended operating free-air temperature range and V_{CC} = 3.75 V; (PD1 = 0, PD2 = 0)

	TYP†	MAX	UNIT
LNA	28	100	µA
RF mixer		100	µA
VCO and buffer amplifiers		100	µA

current consumption over recommended operating free-air temperature range and V_{CC} = 3.75 V; (PD1 = 1, PD2 = 0)

	TYP†	MAX	UNIT
LNA	28	100	µA
RF mixer	6	7	µA
VCO and buffer amplifiers	12	14	mA

† Typical values are at T_A = 25°C.

PRODUCT PREVIEW

APPLICATION INFORMATION

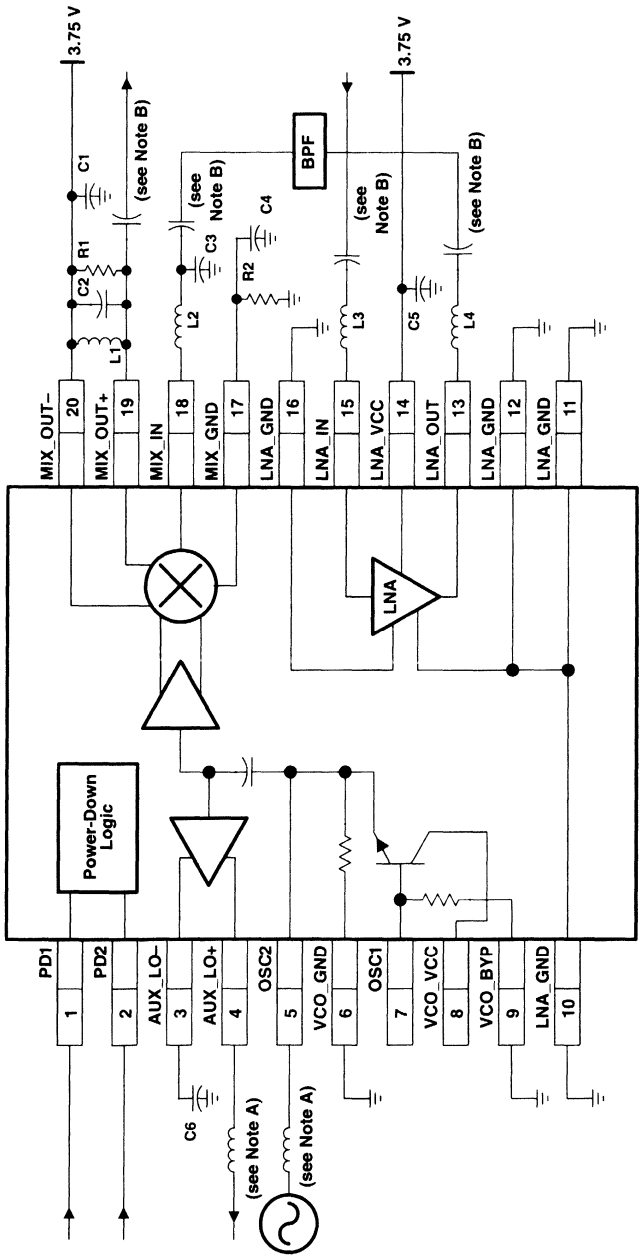


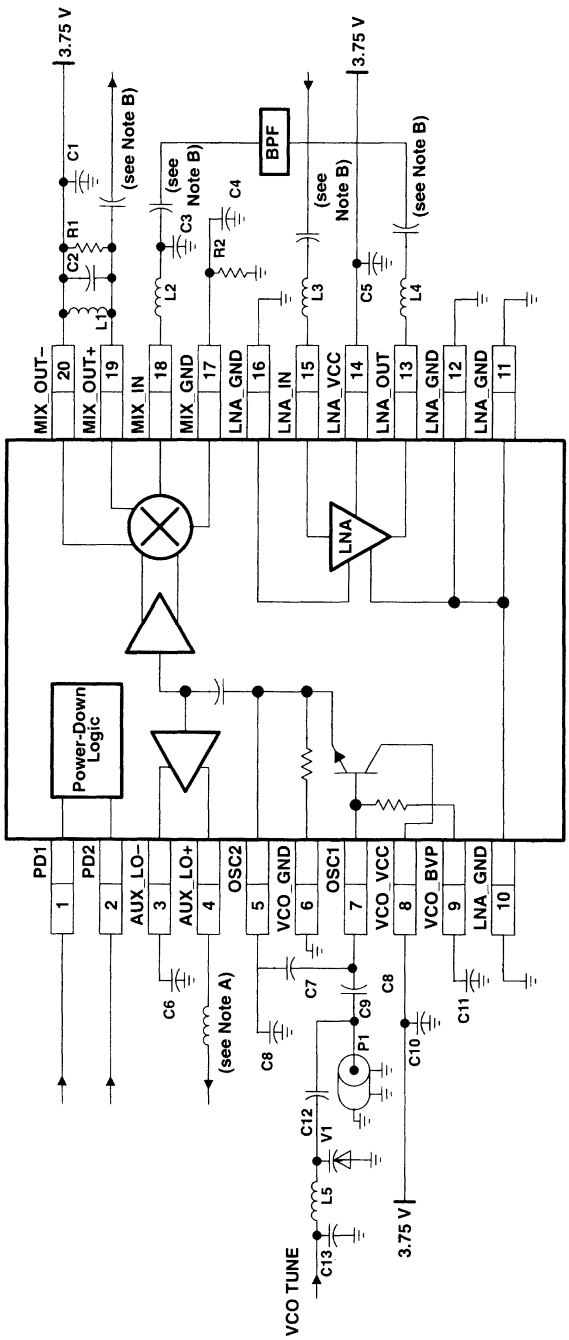
Figure 1. Recommended Application Circuit With External Oscillator

NOTES: A. Optional inductors to improve the LO input and AUX_LO return losses from –6 dB.
B. Optional capacitors to block this ICs dc components from entering the filters

PRODUCT PREVIEW

PRODUCT PREVIEW

APPLICATION INFORMATION



NOTES: A. Optional inductor to improve the LO input and AUX_LO return losses from – 6 dB.
B. Optional capacitors to block thIs ICs dc components from entering the filters

Figure 2. Recommended Application Circuit With Internal Oscillator

recommended component list

RESISTORS:	CAPACITORS:	INDUCTORS:
Kamaya™ 1206	Murata™ 1206	Toko™ LL 1608, LL2012, 32CS
R1 = 1.5 kΩ	C1 = 100 pF	L1 = 220 nH
R2 = 22 Ω	C2 = 56 pF	L2 = 8.2 nH
	C3 = 202 pF	L3 = 8.2 nH
	C4 = 12 pF	L4 = 8.2 nH
	C5 = 100 pF	L5 = 8.2 nH
	C6 = 100 pF	
	C7 = 2 pF	
	C8 = 1 pF	
	C9 = 2 pF	Others:
	C10 = 100 pF	P1 = **Coaxial Resonator** – Trans-Tech™ SR8800LPQ1050BY
	C11 = 100 pF	V1 = **Varactor** – Siemens™ BBY51–03W
	C12 = 2 pF	U1 = **TRF1015**
	C13 = 68 pF	U2 = **Saw Filter** – Murata SAFC881.5MA70N

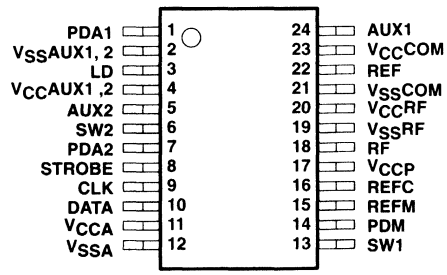
PRODUCT PREVIEW

Kamaya is a trademark of Kamaya Electric Company, Ltd.
Murata is a trademark of Murata Manufacturing Co., Ltd.
Siemens is a trademark of Siemens Corporation.
Toko is a trademark of Toko, Inc.
Trans-Tech is a trademark of Trans-Tech, Inc.

SLWS022 – JUNE 1996

- **Fractional-N/Integer-N High-Frequency (0.7–2.2 GHz) Synthesizer for Radio Frequency (RF) Channel**
- **Dual Integer-N Low-Frequency Synthesizers (70–250 MHz) for Transmit and Receive Intermediate Frequency (IF) Local Oscillators (LO)**
- **Variable Denominator for Fractions 1:1 Through 1:13**
- **Dual-Modulus Prescaler of 1:32, 33**
- **Built-In Analog Switch and Timer to Dynamically Change Filter Time Constants**
- **Up to 20 MHz 3-Wire High-Speed Serial Data Input Interface**
- **Low Current Consumption and Standby Mode**
- **Suitable for Many Portable Cellular Telephone Standards**

PW PACKAGE
(TOP VIEW)



description

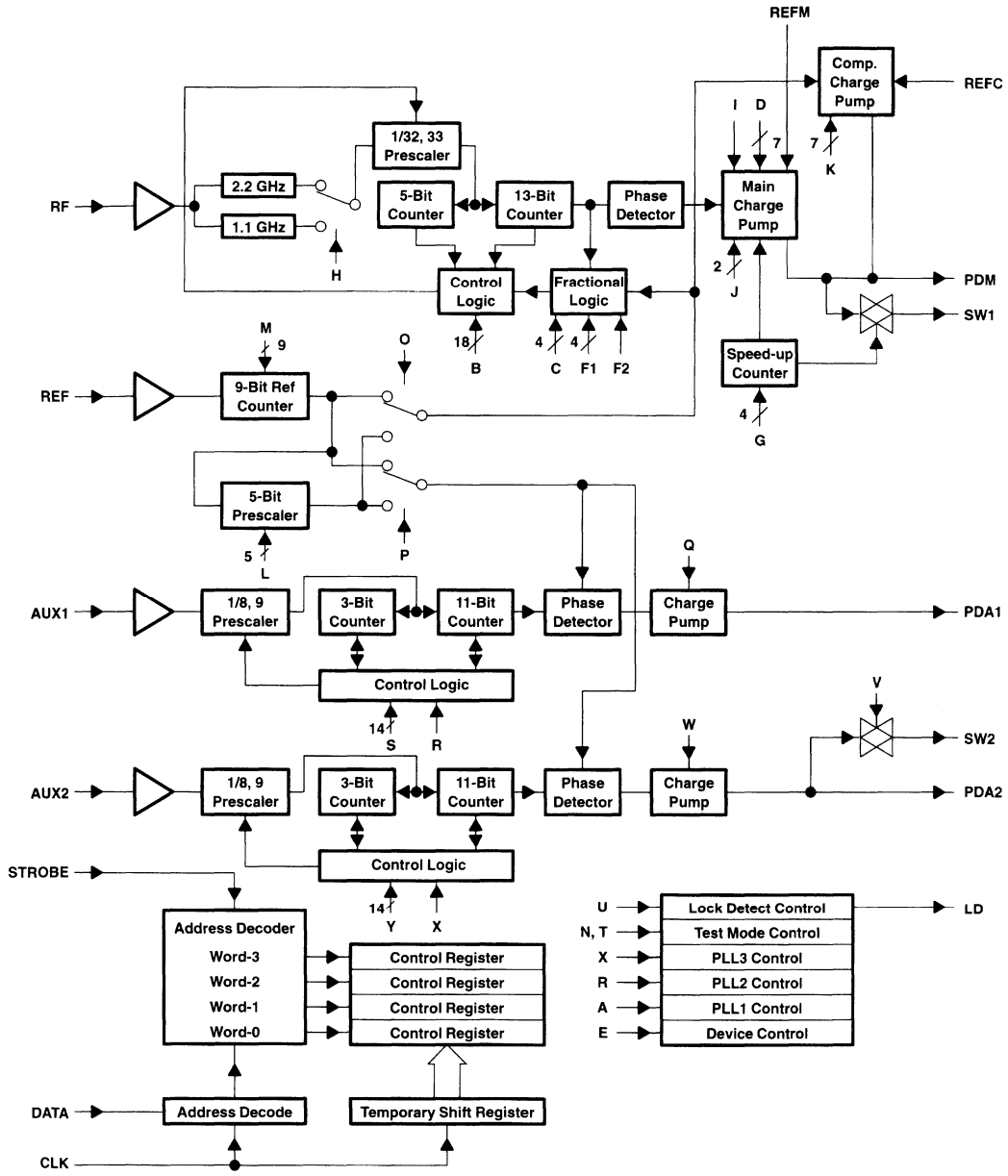
Texas Instruments (TI™) TRF2040 is a triple-channel, fractional-N/integer-N frequency synthesizer component for use in phase-locked loop (PLL) circuits. The high-frequency channel operates in fractional-N or integer-N modes up to 2.2 GHz. The low-frequency channels operate in integer-N mode up to 250 MHz. The extreme flexibility of this device and wide array of operating options furnish the user with reliable solutions to the synthesizer needs of systems as diverse as advanced mobile phone service (AMPS), global system for mobile (GSM), personal digital cellular (PDC), personal communication service (PCS1900). and digital cellular systems (DCS1800). A high-speed three-wire bus serial data structure provides broad control system design compatibility. An 18-bit main counter provides division for input signals in two modes: a range of 700 MHz to 1,100 MHz and 1,100 MHz to 2,200 MHz. The auxiliary counters accept inputs between 70 MHz and 250 MHz. The TRF2040 provides a channel selection local oscillator, a receiver auxiliary local oscillator, and transmitter offset local oscillator control signals. These are charge pump output control currents for three separate loops.

The TRF2040 is offered in a 24-pin plastic thin shrink PW small-outline package. The TRF2040 is characterized for free-air operation from –40°C to 85°C.

PRODUCT PREVIEW

TI is a trademark of Texas Instruments Incorporated.

functional block diagram



PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AUX1	24	I	Auxiliary-1 PLL signal input
AUX2	5	I	Auxiliary-2 PLL signal input
CLK	9	I	Serial interface clock input
DATA	10	I	Serial interface data input
LD	3	O	Lock detector output
PDA1	1	O	Auxiliary-1 PLL phase detector and charge pump output
PDA2	7	O	Auxiliary-2 PLL phase detector and charge pump output
PDM	14	O	Main RF PLL phase detector and charge pump output
REFC	16		External resistor connection to set fractional compensation charge pump output current
REFM	15		External resistor connection to set main charge pump output current
REF	22	I	External reference oscillator input
RF	18	I	Main RF PLL signal input
STROBE	8	I	Serial interface load input
SW1	13	O	Analog switch 1 output
SW2	6	O	Analog switch 2 output
V_{CC}RF	20		Main RF PLL supply voltage
V_{CC}A	11		Analog supply voltage for main RF PLL charge pumps
V_{CC}AUX1,2	4		Auxiliary-1, -2 PLL supply voltage
V_{CC}COM	23		Supply voltage for oscillator amplifier, control registers, and reference clock divider
V_{CC}P	17		Main RF PLL prescaler supply voltage
V_{SS}A	12		Analog ground for main RF charge pumps
V_{SS}AUX1,2	2		Ground connection for auxiliary dividers and phase detectors
V_{SS}COM	21		Ground connection for oscillator amplifier, control registers, and reference clock divider
V_{SS}RF	19		Ground connection for main RF dividers and phase detector

PRODUCT PREVIEW

control register bit assignment

FIRST IN MSB — LAST IN LSB

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	A	B																		C			
1	0	0	D							E	F2	F1				G				H	I	J	
1	0	1	K							L						M							
1	1	0	N			O	P	Q	R	S													
1	1	1	T			U	V	W	X	Y													

A: 1-bit data to control PLL1. When 1, the PLL1 is on. When 0, the PLL1 is off.
B: 18-bit data for PLL1 counter.
C: 4-bit fractional numerator data.
D: 7-bit data to define main charge pump1 output factor.
E: 1-bit data to control all TRF2040 circuits. When 1, all circuits are on. When 0, all circuits are off.
F1: 4-bit fractional denominator data.
F2: 1-bit data to control 13 denominator spreader function. When 1, spreader is on. May be used only in low range input (H = 0).
G: 4-bit timer data to control low-pass filter switch and charge pump output current. When the reference clock of PLL1 counts to 16 times of this value, the mode is changed from fast lockup mode to locked mode.
H: 1-bit data to select input range of PLL1. When 1, the input range is 2 GHz. When 0 the range is 1 GHz.
I: 1-bit data to control charge pump1 output polarity. When I = 0, VCO frequency below reference frequency results in source output current from charge pump.
J: 2-bit data to select the ratio of charge pump output current for PLL1.
Output current ratio of fast lockup mode to locked mode is:

DATA	RATIO
00	9/1
01	9/2
10	9/3
11	9/4

K: 7-bit data to define fractional compensation charge pump1 output factor.
L: 5-bit data for reference post counter.
M: 9-bit data for reference counter.
N: 3-bit data for test mode.
O: 1-bit data to select reference clock for PLL1. When 1, the 3-bit post counter output is selected. When 0, the 11-bit reference counter outputs is selected.
P: 1-bit data to select reference clock for PLL2 and PLL3. When 1, the 3-bit post counter output is selected. When 0, the 11-bit reference counter output is selected.
Q: 1-bit data to control the output charge pump polarity of PLL2. When I = 0, VCO frequency below reference frequency results in source output current from charge pump.
R: 1-bit data to control PLL2. When 1, the PLL2 is on. When 0, the PLL2 is off.
S: 14-bit data for PLL2 counter.
T: 3-bit data for test mode.
U: 1-bit data to select clock for lock detection circuit. When 1, the reference clock for PLL2 and PLL3 is selected. When 0, the reference clock for PLL1 is selected.
V: 1-bit data to control low-pass filter switch of PLL3. When 1, the switch is closed (on) and is in the lockup mode. When 0, the switch is open (off) and is in the FM modulation mode.
W: 1-bit data to control the output charge pump polarity of PLL3.
X: 1-bit data to control PLL3. When 1, the PLL3 is on. When 0, the PLL3 is off.
Y: 14-bit data for PLL3 counter.

main divider operation

The main RF divider in the TRF2040 divides by B for F1-C cycles and divides by B+1 for C cycles resulting in an average divide ratio of B+C/F1. The process is controlled by a modulo F1 accumulator which increments in steps of C. B, C, and F1 are programmed using the serial interface.

B is the integer portion of the main divider ratio and can take on values ranging from 992 to 262143 ($2^{18}-1$). The lower range value is constrained by the type of dual-modulus prescaler implemented in the main divider. Because the prescaler is a 32/33 prescaler, the minimum division ratio is determined by 32*31=992.

The ratio of C to F1 provides the fractional portion of the main divider ratio. C can take on values ranging from 0 to F1–1, where F1 can take on ratios of 1 to 13. Because C can have a value of zero (0), the main divider can operate in integer mode only, as opposed to integer plus fraction mode.

fractional compensation

Fractional-N division is used to achieve channel spacing frequencies that are much less than the phase detector reference frequency. The benefits of fractional-N division are higher loop bandwidth and phase detector reference frequency suppression. Unfortunately, fractional-N sidebands at, and factors of, the channel spacing frequency will be present with non-zero fraction channels ($C \neq 0$).

The TRF2040 design incorporates fractional sideband suppression methods. The scheme uses a compensation charge pump to generate opposite polarity current pulses that are a function of the contents of the fractional accumulator. These compensation pulses help to cancel the effects of the fractional error component of the normal charge pump current. The pulse width of the compensation pulse is modulated by the fractional accumulator in a manner so that the area (time x current) is proportional to the fractional error. The magnitude of the compensation current is programmable (K).

denominator spreading

A secondary method for reducing fractional sidebands is provided in the TRF2040. The user may selectively (F2) activate a denominator spreading function which tends to spread the energy of the distinct fractional sidebands over the system loop bandwidth. The denominator value is changed by –1, 0, +1, or +2 every time the fractional accumulator overflows. The frequency of the spreading is proportional to the numerator value. This function is completely transparent to the user, and channel solutions need not be altered.

speed-up mode operation

Additional charge pumps and an analog switch are provided in order to achieve faster tuning times. The loop gain can be increased and the filter time constant can be reduced by incorporating the speed-up mode charge pumps and the analog switch. The normal/speed-up mode current ratio is programmable (J) as well as the speed-up mode duration (G). A 4-bit counter is referenced to the main loop reference clock; the counter is decremented once for every 16 main divider reference counts. Speed-up mode will terminate when the 4-bit counter reaches its terminal count of zero.

main RF synthesizer charge pump current plan

The charge pumps for the main RF synthesizer are current outputs and are programmable with external scaling resistors (REFM and REFC) and internal programmable DACs. The normal mode and speed-up mode main and compensation charge pump currents are found as follows.

1. Determine the reference voltages as a function of control fields D and K.
   a. Main charge pump reference voltage Vm as seen on terminal 15 (REFM),

$$Vm = \frac{(128 + D)}{256} \times 1.25\ V$$

   i.e., If D = 0, Vm = 0.625 V. If D = 127, Vm = 1.245 V.

   b. Compensation charge pump reference voltage Vc as seen on terminal 16 (REFC),

$$Vc = \frac{(128 + D)}{256} \times 1.25\ V$$

2. Determine normal mode and speed-up mode main charge pump currents as a function of Vm, REFM, and J.
   a. Calculate normal mode main charge pump current Inm,

$$Inm = \frac{Vm}{REFM} \times (J + 1) \times 5,$$ where REFM is in kΩ and Inm is in mA.

   b. Calculate normal mode main charge pump current Inm,

$$Ism = \frac{Vm}{REFM} \times 9 \times 5,$$ where REFM is in kΩ and Ism is in mA.

   i.e., REFM = 24 kΩ, D = 128, J = 0; Inm = 0.259 mA peak; Ism = 2.33 mA peak.

3. Determine normal mode and speed-up mode compensation charge pump currents as a function of Vc, REFC, and J.
   a. Calculate normal mode compensation charge pump current Inc,

$$Inc = \frac{Vc}{REFC} \times (J + 1) \div 60,$$ where REFC is in kΩ and Inc is in μA.

   b. Calculate speed-up mode compensation charge pump current Isc,

$$Isc = \frac{Vc}{REFC} \times 9 \div 60,$$ where REFC is in kΩ and Isc is in μA.

   i.e., REFC = 24 kΩ, K = 128, J = 0; Inc = 0.856 μA peak; Isc = 7.78 μA peak.

The average normal mode and speed-up mode main charge pump current is a function of the phase error by:

$$I_{avg-main} = \frac{Inm + Ism}{2\pi} \times \text{Phase error.}$$

The total average normal mode and speed-up mode charge pump current for the main RF synthesizer is the sum of $I_{avg-main}$ and the compensation currents Inc and Isc by:

$$I_{total} = I_{avg-main} + Inc + Isc.$$

PRODUCT PREVIEW

auxiliary divider operation

The auxiliary synthesizer loops operate in integer-only mode. The 8/9 prescalers used in the auxiliary dividers (S and Y) provide division ranging from 56 to 16384 ($2^{14}-1$). An additional analog switch is provided with the auxiliary-2 charge pump output. This analog switch can be selected (V) on (low-impedance) or off (high-impedance) in order to accommodate two loop filter frequency responses, one for normal locked mode and another for frequency modulation (FM) mode.

auxiliary synthesizer charge pump current plan

The charge pumps for the auxiliary synthesizers are current outputs. The average auxiliary charge pump currents will be a function of the phase error by:

$$I_{avg-aux1,2} = \frac{0.3}{2\pi} \times \text{Phase error, mA.}$$

reference divider operation

The reference divider circuit consists of a main, 9-bit count (M) and a 5-bit post-counter (L). The main RF synthesizer phase detector can be connected to output of the 9-bit counter directly or to the output of the 5-bit post-counter directly using the programmable DPST switch (O). The auxiliary synthesizer phase detectors can be connected in a similar fashion (P).

lock detection

The unlocked state for an active channel is detected when the associated phase comparator output pulse width becomes larger than one clock cycle of the selected reference frequency. A logic high on the LD pin indicates a locked condition. A logic low on the LD pin indicates an unlocked condition.

The lock detect selection bit U in Word 3 selects the reference clock for the lock detection circuitry. If U = 0 and the main RF PLL is activated by A = 1, the locked or unlocked state of the main RF PLL will be indicated on LD. If U = 1 and the auxiliary-1 PLL and/or the auxiliary-2 PLL is activated by R = 1 and/or X = 1, respectively, the locked or unlocked state(s) of auxiliary-1, -2 PLL(s) will be indicated on LD.

powerdown control

Four control bits (A, E, R, X) are provided for power consumption control of the TRF2040. Bit E disables the entire circuitry of the TRF2040 except the serial data interface. Bits A, R, and X disable the Main RF synthesizer, the auxiliary-1 synthesizer and the auxiliary-2 synthesizer, respectively.

test mode operation

Various internal signals can be routed to the LD terminal for test purposes using N and T fields as defined in the following table:

N-BITS	T-BITS†	ROUTING TO LD
000	X00	Lock detect pulse
001	X00	Main prescaler output
000	X01	Main 5-bit sub counter output
001	X01	Main 13-bit main counter output
001	X10	Main phase detector down pulse output
000	X11	Main phase detector up pulse output
001	X11	Main phase detector VCO-side input
011	X00	Reserved
010	X01	Reserved
011	X01	Fractional compensation pulse
011	X10	Auxiliary-1 prescaler output
010	X11	Auxiliary-1 3-bit sub counter output
011	X11	Auxiliary-1 11-bit main counter output
101	X00	Auxiliary-1 phase detector down pulse output
100	X01	Auxiliary-1 phase detector up pulse output
101	X01	Auxiliary-1 phase detector VCO-side input
101	X10	Auxiliary-2 prescaler output
100	X11	Auxiliary-2 3-bit sub counter output
101	X11	Auxiliary-2 11-bit main counter output
111	X00	Auxiliary-2 phase detector down pulse output
110	X01	Auxiliary-2 phase detector up pulse output
111	X01	Auxiliary-2 phase detector VCO-side input
111	X11	Lock detect clock pulse

† Bit 2 of the T-word is defined for an external clock pulse mode. In this mode, the internal counters of all three synthesizers are fed clock pulses from an external clock source through SW1 as opposed to being fed from the internal prescalers as in normal operation.

For normal device operation, zeros should be written to all bits of N and T.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC}RF, V_{CC}AUX1,2, V_{CC}COM . . . . . –0.3 V to 4.8 V
Input voltage range, V_I . . . . . –0.3 V to V_{CC} + 0.3 V
Power dissipation at or below T_A = 25°C . . . . . 300 mW
Maximum virtual-junction temperature, T_J . . . . . 150°C
Operating free-air temperature range T_A . . . . . –55°C to 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}RF	Main RF PLL supply voltage	2.7	3	3.6	V
V_{CC}AUX1,2	Auxiliary-1 and Auxiliary-2 supply voltage	2.7	3	3.6	V
V_{CC}COM	Common circuits supply voltage	2.7	3	3.6	V
V_{CCA}	Analog supply voltage	2.7	3	3.6	
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	–0.3		0.8	V
f_{RF}	RF input frequency in the 2 GHz mode (H = 1)	1100		2200	MHz
f_{RF}	RF input frequency in the 1 GHz mode (H = 0)	700		1100	MHz
f_{AUX1}	AUX1 input frequency	70		250	MHz
f_{AUX2}	AUX2 input frequency	70		250	MHz
f_{REF}	REF input frequency			25	MHz
T_A	Operating free-air temperature	–40	25	85	°C
T_J	Virtual-junction temperature	–30		105	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	LD	$V_{CC}AUX1,2$ = 3 V,	I_{OH} = –1 mA	$V_{CC}AUX1,2-0.4$			V
V_{OL}	Low-level output voltage	LD	$V_{CC}AUX1,2$ = 3 V,	I_{OL} = 1 mA			0.4	V
V_T	Input threshold voltage	STROBE				$V_{CC}COM/2$		V
		CLOCK						
		DATA						
r_O	Output resistance	PDA1	$V_{CC}AUX1,2$ = 3 V,	V_O = 1.5 V			50	Ω
		PDA2	$V_{CC}AUX1,2$ = 3 V,	V_O = 1.5 V				
	Analog switch on resistance	SW1	$V_{CC}RF$ = 3 V,	V_O = 1.5 V			50	Ω
		SW2	$V_{CC}AUX1,2$ = 3 V,	V_O = 1.5 V				
	Main charge pump output current	PDM	Fast lockup mode, D = 127, J = 3	REFM = 24 kΩ,		4.67		mA
			Fast lockup mode, D = 0, J = 3	REFM = 24 kΩ,		2.34		
			Locked mode, D = 127	REFM = 24 kΩ,		0.52		
			Locked mode, D = 0	REFM = 24 kΩ,		0.26		
	Compensation charge pump output current	PDM	Fast lockup mode, K = 127, J = 3	REFC = 24 kΩ,		19.5		µA
			Fast lockup mode, K = 0, J = 3	REFC = 24 kΩ,		9.7		µA
			Locked mode, K = 127	REFC = 24 kΩ,		2.2		µA
			Locked mode, D = 0	REFC = 24 kΩ,		1.1		µA
	Auxiliary charge pump output currents	PDA1,2				300		µA
$I_{CC}RF$	PLL1 supply current		$V_{CC}RF$ = 3 V					
$I_{CC}AUX1,2$	PLL2 and PLL3 supply current		$V_{CC}AUX1,2$ = 3 V					
$I_{CC}COM$	Common circuits supply current		$V_{CC}COM$ = 3 V					
I_{CCA}	Analog supply current		V_{CCA} = 3 V					

PRODUCT PREVIEW

serial interface timing requirements

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Clock frequency			0		10	MHz
t_wH	Pulse duration	CLK high		30			ns
t_wL	Pulse duration	CLK low		30			ns
t_{su}	Setup time	Data before CLK high		30			ns
		STROBE before CLK high		30			ns
t_h	Hold time	Data after CLK high		30			ns
		STROBE after CLK low		30			ns

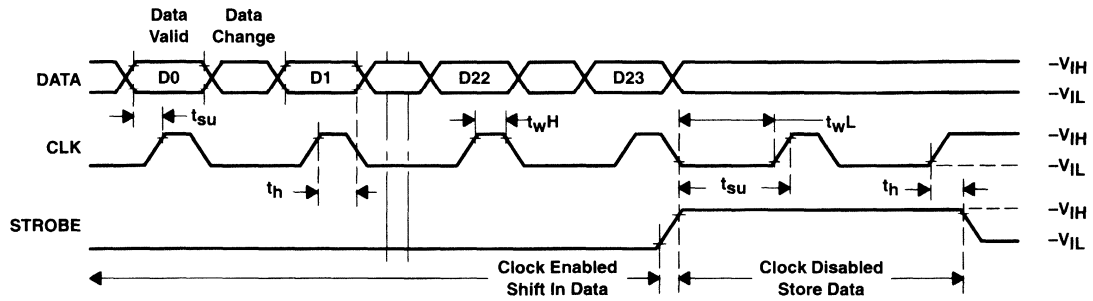
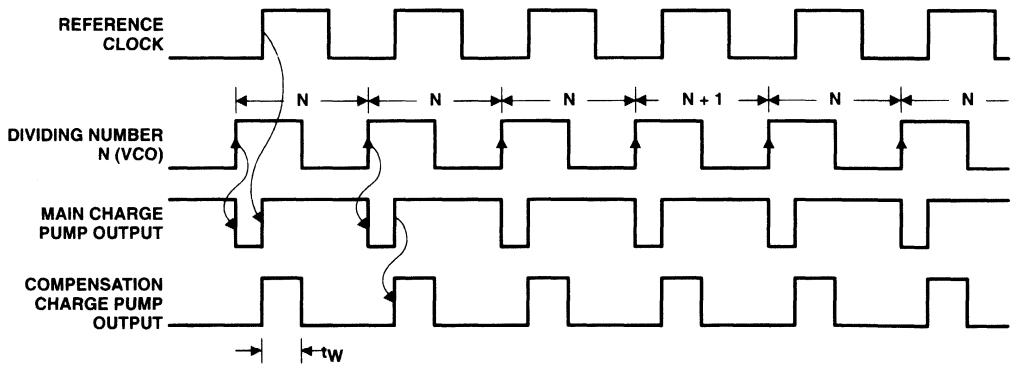


Figure 1. Serial Input Timing Requirements



NOTE: t_W is proportional to the contents of the fractional accumulator.

Figure 2. Charge Pump Output Ripple Compensation

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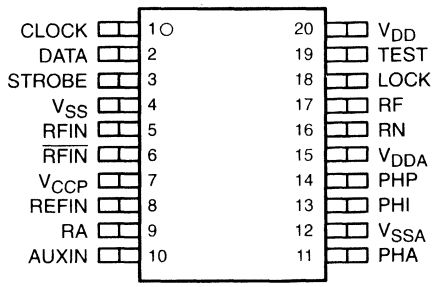
SLWS030 – JUNE 1996

- **2.7 V – 5.1 V Operation**
- **Low-Power Operation: 7 mA at 3.6 V**
- **1.1 GHz Operation**
- **Two Operating Modes:**
  - **Philips SA7025 Emulation Mode Pin-for-Pin and Programming Compatible**
  - **Extended Performance Mode (EPM)**
- **Programmable EPM Fractional Modulus of 1–16**
- **Dual RF – IF Phase-Locked Loops**
- **Fractional-N or Integer-N Operation**
- **Normal, Speed-Up, and Fractional Compensation Charge Pumps**

PW PACKAGE
(TOP VIEW)



description

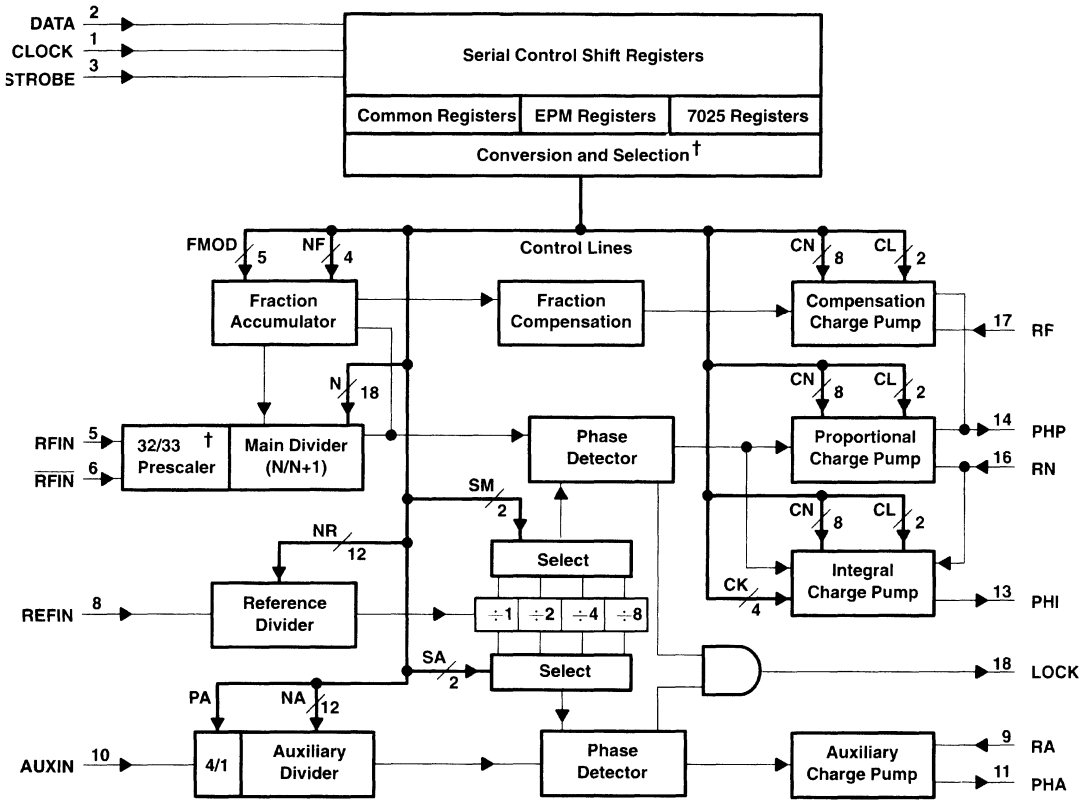
The TRF2050 is a low-voltage, 1.1-GHz, fractional-N/integer-N, dual-channel, low-power, PLL (phase-locked loop) frequency synthesizer component for IS54 cellular applications. Fractional-N division and an integral speed-up charge pump are used to achieve rapid channel switching. Two operating modes are available: 1) SA7025 emulation mode in which the part emulates the Philips SA7025 fractional-N synthesizer for a wide range of main divider division ratios, and 2) EPM (extended performance mode) that provides additional features including fractional accumulator modulos from 1 to 16 (compared to only five or eight for the SA7025) and programmable control of the speed-up mode duration (compared to the SA7025 method of holding the strobe line high).

Along with external loop filters, the TRF2050 provides all functions necessary for VCO control in a dual-PLL frequency synthesizer system. A main channel is provided for RF (radio frequency) channels and an auxillary channel for IF channels. The current-output charge pumps directly drive passive RC filter networks to generate VCO control voltages. Rapid main-channel frequency switching is achieved with a charge pump arrangement that increases the current drive and alters the loop-filter frequency response during the speed-up mode portion of the switching interval.

PRODUCT PREVIEW

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

functional block diagram



† Conversion and selection block provides emulation of SA7025 64/65/72 triple-modulus prescaler operation using the TRF2050 32/33 dual-modulus prescaler.

PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AUXIN	10	I	Auxiliary channel RF input
CLOCK	1	I	Serial interface clock signal
DATA	2	I	Serial interface data signal
LOCK	18	O	Lock detector output
PHA	11	O	Auxiliary charge pump output
PHI	13	O	Integral charge pump output
PHP	14	O	Proportional charge pump output
RFIN	5	I	Prescaler positive RF input
$\overline{\text{RFIN}}$	6	I	Prescaler negative RF input
REFIN	8	I	Reference frequency input signal
RA	9	I	Resistor to V_{SSA} sets auxillary charge pump reference current
RN	16	I	Resistor to V_{SSA} sets proportional and integral charge pump reference current
RF	17	I	Resistor to V_{SSA} sets compensation charge pump reference current
STROBE	3	I	Serial interface strobe signal
TEST	19	I	Test Terminal
V_{CCP}	7		Prescaler positive supply voltage
V_{DD}	20		Digital supply voltage
V_{DDA}	15		Analog supply voltage
V_{SS}	4		Digital ground
V_{SSA}	12		Analog ground

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CCP}, V_{DD}, V_{DDA} (see Note 1) . . . . . −0.6 V to 5.6 V
Input voltage range, logic signals . . . . . −0.6 V to 5.6 V
Operating ambient temperature range, T_A . . . . . −55°C to 85°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to V_{SSA}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CCP}, V_{CC}, V_{DD}, V_{DDA}	2.7	3.6	5.1	V
High-level input voltage, V_{IH}	V_{CC} −0.5			V
Low-level input voltage, V_{IL}			0.5	V
RF input frequency, $f_{(RFIN)}$	0.05		1.6	GHz
Reference input frequency, $f_{(REFIN)}$	0		50	MHz
Auxiliary input frequency, $f_{(AUXIN)}$	0		200	MHz
Differential RF input power, $V_{ID(RFIN)}$ (50-Ω characteristic impedance)	−20			dBm
Reference input voltage, $V_{I(REFIN)}$	0.2			Vpp
Auxiliary input voltage, $V_{I(AUXIN)}$	0.2			Vpp
Operating free-air temperature, T_A	−40	25	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 3.6 V, T_A = 25°C (unless otherwise noted)

supply current

PARAMETER	MIN	MAX	UNIT
Average operational supply current		7	mA

digital interface

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	LOCK	I_{OH} = 3.2 mA	V_{CC} −0.5			V
V_{OL}	Low-level output voltage		I_{OL} = −3.2 mA			0.5	V
I_{IH}	High-level input current	DATA, CLOCK, STROBE			10		µA
I_{IL}	Low-level input current				10		µA

auxiliary pump currents

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{PHA}	RA = 100 kΩ		±0.25		mA

proportional charge pump current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{PHP_N}	Normal mode (locked)	CN = 128, RN = 18 kΩ		±0.5		mA
I_{PHP_S}	Speed-up (channel-switching) mode	CN = 128, CL = 1, RN = 18 kΩ		±2.5		mA

compensation charge pump current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{PHC_N}	Normal mode (locked)	RN = 18 kΩ, RF = 24 kΩ		±1.3		uA
I_{PHC_S}	Speed-up (channel-switching) mode	CL = 1, RN = 18 kΩ, RF = 24 kΩ		±6.3		uA

integral charge pump current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{PHI_N}	Normal mode (locked)			0		mA
I_{PHN_S}	Speed-up (channel-switching) mode	CN = 128, CL = 1, CK = 4, RN = 18 kΩ		±8		mA

main charge pumps current plan

PARAMETER	OPERATION MODE	TEST CONDITION	UNIT
Peak proportional output ($PHP_{PK\text{-}NM}$) = [(18.75 / (RN + 0.75)) × CN/256)]	Normal	(RN in kΩ)	mA
Average proportional output ($PHP_{AVG\text{-}NM}$) = (Phase Error / 2π) × $PHP_{PK\text{-}NM}$	Normal		mA
Peak proportional output ($PHP_{PK\text{-}SM}$)= {[(18.75 / (RN + 0.75)) × (CN/256)] + [(18.75 / (RN + 0.75)) × (CN/256) × 2^{CL+1}]}	Speed-up	(RN in kΩ)	mA
Average proportional output ($PHP_{AVG\text{-}SM}$) = (Phase Error / 2π) × ($PHP_{PK\text{-}SM}$)	Speed-up		mA
Peak integral output ($PHI_{PK\text{-}SM}$) = [(18.75 / (RN + 0.75)) × CK × (CN/256) × 2^{CL+1}]	Speed-up	(RN in kΩ)	mA
Average Integral output ($PHI_{AVG\text{-}SM}$) = (Phase Error / 2π) × $PHI_{PK\text{-}SM}$)	Speed-up		mA
Peak compensation output = 30/RF†		(RF in kΩ)	µA

† The average compensation output current is a pulse-width-modulated function of the contents of the fractional accumulator and the peak compensation output current.

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auxiliary charge-pump current plan

PARAMETER	TEST CONDITION	UNIT
Peak auxiliary output (PHA_{PK}) = 20 × 1.25 / RA	(RA in kΩ)	mA
Average auxiliary output (PHA_{AVG}) = (Phase Error / 2 π) × PHA_{PK}		mA

timing requirements, serial data interface

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$f_{(CLOCK)}$	Clock frequency			10	MHz
$t_{w(CLKHI)}$	Clock high time pulse width, CLOCK high		30		ns
$t_{w(CLKLO)}$	Clock low time pulse width, CLOCK low		30		ns
$t_{su(D)}$	Setup time, data valid before CLOCK↑		30		ns
$t_{h(D)}$	Hold time, data valid after CLOCK↑		30		ns
$t_{su(Strobe)}$	Setup time, STROBE↑ before CLOCK↑		30		ns
$t_{h(Strobe)}$	Hold time, STROBE↓ after CLOCK low		30		ns

PARAMETER MEASUREMENT INFORMATION

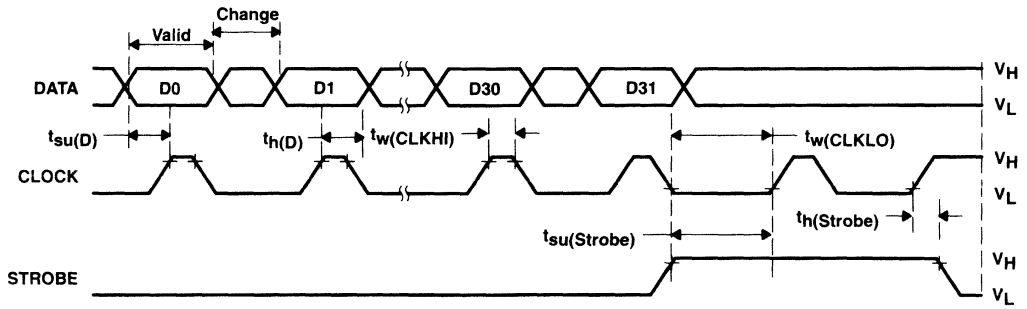


Figure 1. Serial-Data Interface Timing

PRODUCT PREVIEW

PRINCIPLES OF OPERATION

serial control

Instruction word formats for the SA7025 emulation mode are shown in Figure 2; Table 1 lists the corresponding function table.

Instruction word formats for extended performance mode are shown in Figure 3; Table 2 lists the corresponding function table.

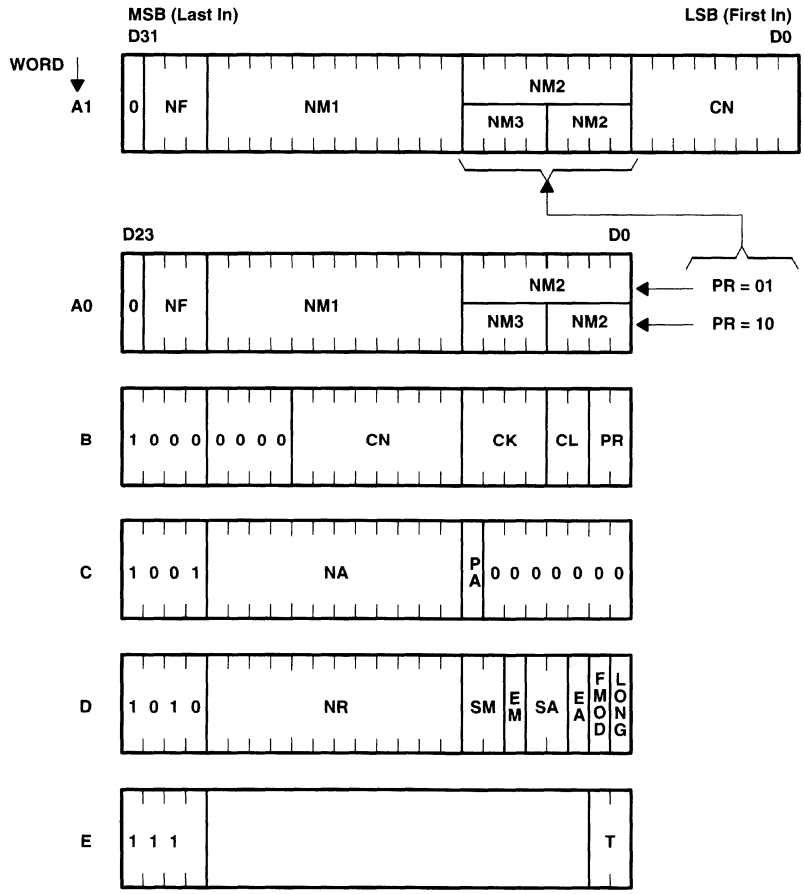


Figure 2. Serial Word Format for SA7025 Emulation Mode

PRODUCT PREVIEW

PRINCIPLES OF OPERATION

Table 1. SA7025 Emulation Serial-Word-Format Function Listing

SYMBOL	BITS	FUNCTION
NM1	12	Number of main divider cycles when prescaler modulus = 64
NM2	8 if PR = 01 4 if PR = 10	Number of main divider cycles when prescaler modulus = 65
NM3	4 if PR = 10	Number of main divider cycles when prescaler modulus = 72
PR	2	Prescaler type: PR = 01; modulus 2 prescaler (64/65) PR = 10; modulus 3 prescaler (64/65/72)
NF	3	Fractional-N increment
FMOD	1	Fractional-N modulus selection: 0 = modulo 5 1 = modulo 8
LONG	1	A word format selection: 0 = 24-bit A0 format 1 = 32-bit A1 format
CN	8	Binary current-setting factor for main charge pumps
CK	4	Binary acceleration factor for integral charge pump current
CL	2	Binary acceleration factor for proportional charge pump current
EA	1	Auxiliary divider enable flag: 0 = disabled 1 = enabled
NA	12	Auxiliary divider ratio
PA	1	Auxiliary prescaler select: 0 = divide by 4 1 = divide by 1
NR	12	Reference divider ratio
SM	2	Reference select for main phase detector
EM	1	Main divider enable flag: 0 = disabled 1 = enabled
SA	2	Reference select for auxiliary phase detector
T	2	Test mode connection of internal signals to the LOCK terminal: 00 = LOCK 01 = Auxiliary divider 10 = Main divider 11 = Reference divider

PRODUCT PREVIEW

PRINCIPLES OF OPERATION

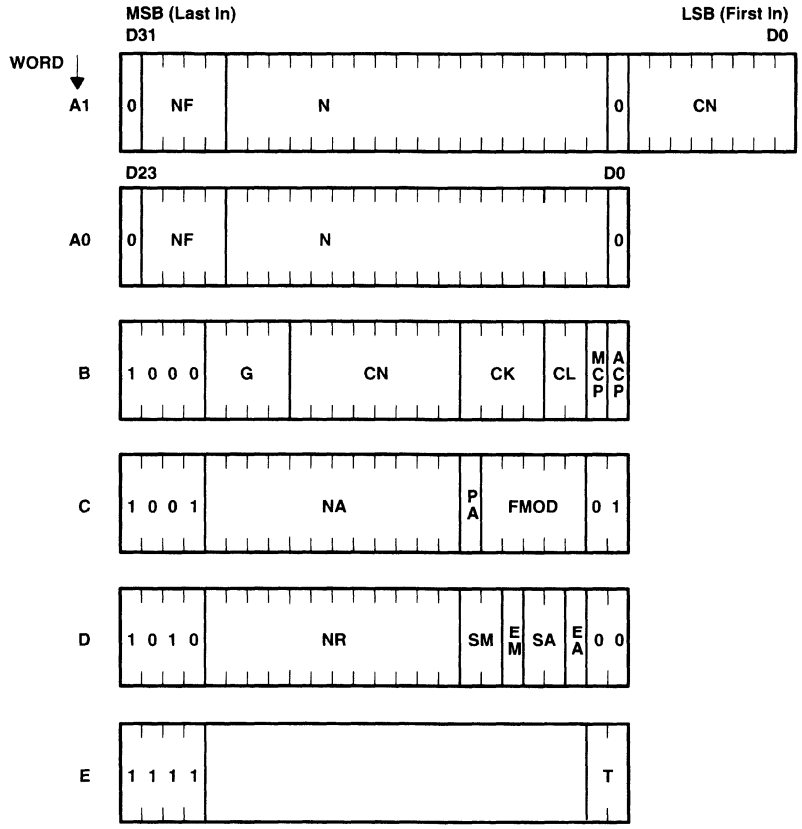


Figure 3. Serial Word Format for Extended Performance Mode

PRODUCT PREVIEW

PRINCIPLES OF OPERATION

Table 2. Extended Performance Mode Function Table

Symbol	Bits	Same as SA7025 Mode	Function
NF	4	No	Fractional-N increment
N	18	No	Overall main divider integer division ratio (NM)
CN	8	Yes	Binary current setting factor for main charge pumps
G	4	No	Speed-up mode duration (number of reference divider cycles)
CK	4	Yes	Binary acceleration factor for integral charge pump current
CL	2	Yes	Binary acceleration factor for proportional charge pump current
EA	1		Auxiliary divider enable flag: 0 = disabled 1 = enabled
MCP	1	No	Main charge pump polarity: 0 = positive 1 = negative
ACP	1	No	Auxilliary charge polarity: 0 = positive 1 = negative
NA	12	Yes	Auxiliary divider ratio
PA	1	Yes	Auxiliary prescaler select: 0 = divide by 4 1 = divide by 1
FMOD	5	No	Fraction accumulator modulus
NR	12	Yes	Reference divider ratio
SM	2	Yes	Reference select for main phase detector
EM	1	Yes	Main divider enable flag: 0 = disabled 1 = enabled
SA	2	Yes	Reference select for auxiliary phase detector
T	2		Test mode connection of internal signals to the LOCK terminal: 00 = LOCK 01 = Auxiliary divider 10 = Main divider 11 = Reference divider

PRODUCT PREVIEW

PRINCIPLES OF OPERATION

main divider

The main divider in the TRF2050 divides by N for FMOD–NF cycles and by N+1 for NF cycles resulting in an average divide ratio of N+NF/FMOD. The process is controlled by a modulo FMOD accumulator, which increments in steps of NF. N, FMOD, and NF are programmable using the serial interface.

The main divider organization is shown in Figure 4. The 32/33 prescaler uses a bipolar design to meet the requirement of 1.6-GHz maximum RF input frequency. All remaining blocks are low-power CMOS designs.

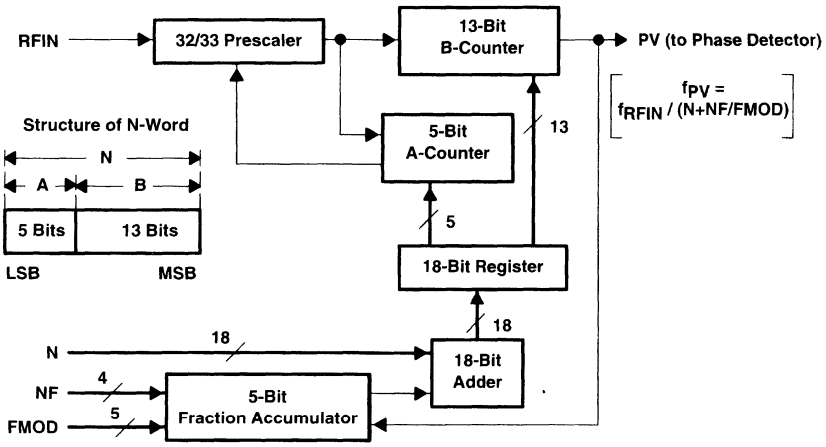


Figure 4. Main Divider Organization

PRODUCT PREVIEW

PRINCIPLES OF OPERATION

fractional compensation

Fractional-N division is used to achieve channel spacing that is much smaller than the phase detector comparison frequency. As an example of this application, Figure 5 shows a configuration for generating the RF local oscillator for a TIA (Telecommunications Industry Association) Standard IS54 cellular telephone application. A phase detector compares the reference divider frequencies (f_{CR}) with the feedback signal (f_{CV}) from the VCO. Channel spacing is 30 kHz for a phase detector comparison frequency of 240 kHz.

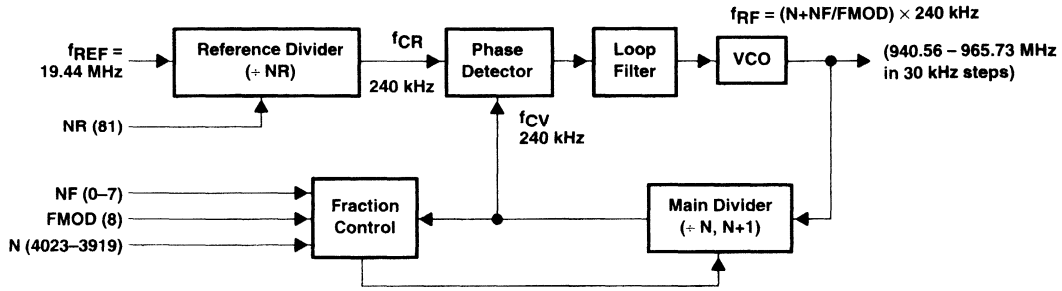


Figure 5. IS54 Fractional-N Synthesizer Example

The fractional divide process causes variations in the period of the main divider output waveform because dividing by N+1 requires one more input cycle than dividing by N. For example, in a 1-GHz application, the main divider output period is 1 ns longer when dividing by N+1 than when dividing by N. This results in a periodic phase error and corresponding sidebands (fractional spurs) in the VCO output spectrum. The TRF2050 design includes a fractional compensation scheme for surpressing the fractional spurs. The scheme uses a compensation charge pump to generate opposite polarity current pulses that cancel the effects of the fractional error component of the normal charge pump current. The fractional accumulator contents are used to modulate the width of the compensation current pulses so that the area (current × time) is proportional to the fractional error. An offset is introduced so that the compensation pulses are always the same polarity. Figure 6 shows the fractional compensation operation of the synthesizer for an output frequency of 953.25 MHz.

PRINCIPLES OF OPERATION

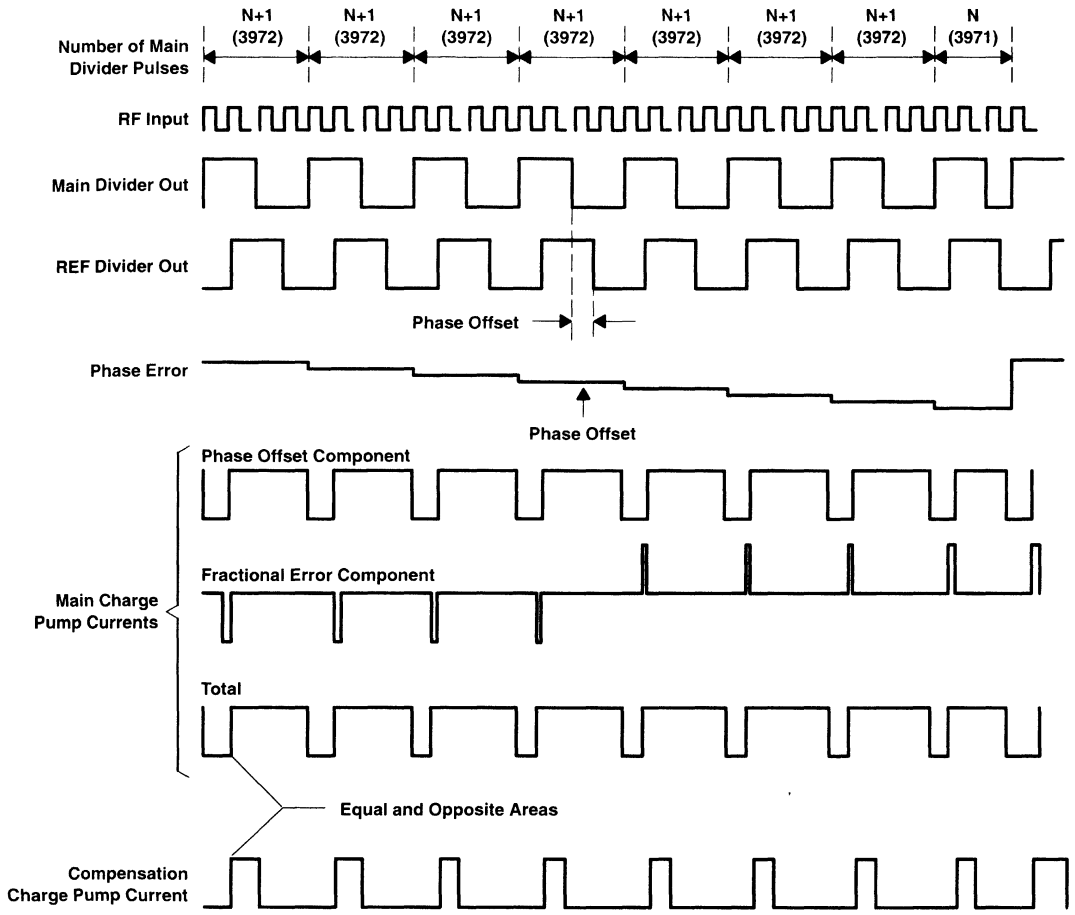


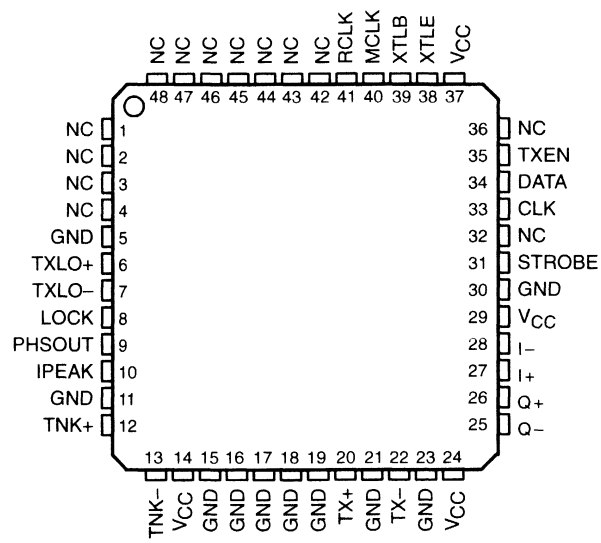
Figure 6. IS54 Fractional-N Synthesizer
Operational at 953.25 MHz with N = 3971, NF = 7 and FMOD = 8

PRODUCT PREVIEW

SLWS019 – JUNE1996

- **Offset Voltage-Controlled Oscillator (VCO) and Single-Sideband Suppressed Carrier (SSBSC) Downconverter Generate TX Carrier From External Receive Local Oscillator (RXLO)**
- **Direct I/Q Modulator For Digital π/4-Differential Quadrature Phase-Shift Key (DQPSK) Gaussian Mean Shift Key (GMSK) Transmission**
- **Frequency Modulation (FM) of VCO or FM Synthesis Using I/Q Modulator for Analog Transmission**
- **Variable Gain Amplifier (VGA) With −31 to 9 dBm Output Power Control**
- **Operates From 3.5 V to 4.2 V**
- **Suitable for Portable Digital Cellular Telephones [(IS-54), Global System for Mobile (GSM)]**
- **Serial Data Interface**
- **48-Pin Quad Flatpack (LQFP)**

PT PACKAGE
(TOP VIEW)



description

Texas Instruments (TI™) TRF3020 is an integrated I/Q and FM modulator circuit suitable for 900 MHz digital and dual-mode applications. It consists of an offset VCO, single-sideband suppressed carrier downconverter, a direct modulator, and a variable gain amplifier in a small surface mount package. Very few external components are required.

The VCO produces the offset frequency needed to translate the (external) RXLO to the correct frequency for transmission. The VCO can operate at 90 MHz to 200 MHz, depending on the values chosen for the external tank circuit and can also be frequency modulated for analog transmission in a dual-mode handset.

PRODUCT PREVIEW

description (continued)

The SSBSC downconverter translates the RXLO signal down to the transmit carrier using the VCO offset frequency. The RXLO signal may be differential or single-ended. Typically, the undesired sideband and carrier are suppressed –45 dBc and the RXLO signal is suppressed –21 dBc without trimming.

The direct conversion quadrature modulator places the modulation signal (π/4-DQPSK, GMSK) directly on to the transmit carrier frequency in digital mode. The modulator can also be used to synthesize the FM for analog transmission (or the VCO can be directly modulated).

The VGA has an output range of –31 dBm to 9 dBm into 100 Ω differential. The gain is guaranteed monotonic and can be stepped in 0.2 dB increments between –3 dBm and 9 dBm and in 2 dB increments from –31 dBm to –3 dBm. The balanced output is also well suited for use with the most recent balanced-input surface acoustic wave (SAW) filters. A single-ended output may also be used if desired.

Power consumption is low and can be further reduced by operating the integrated circuit (IC) in powerdown or standby modes when possible, as shown in Table 1.

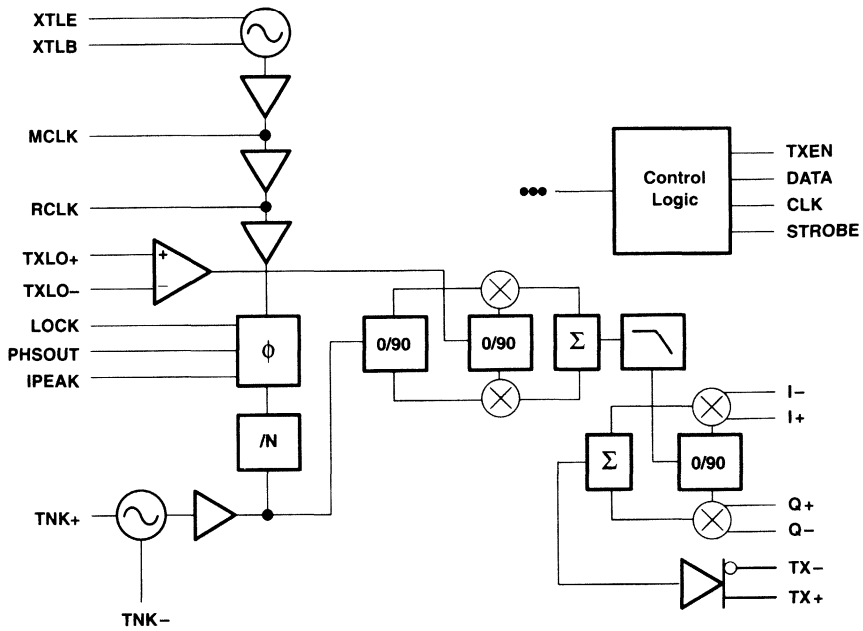
Table 1. Typical Power Consumption at 3.75 V

MODULE	POWERDOWN	STANDBY	TRANSMIT
Crystal oscillator and RCLK buffer amp	100 μW	10 mW	10 mW
Downconverter	100 μW	100 μW	150 mW
Quadrature modulator	100 μW	100 μW	60 mW
Variable gain amp	100 μW	100 μW	300 mW
All modules	400 μW	10 mW	510 mW

The TRF3020 is offered in the 48-pin LQFP package and is characterized for free-air operation from –40°C to 85°C.

PRODUCT PREVIEW

functional block diagram



PRODUCT PREVIEW

Terminal Functions

PIN NAME	PIN NO.	I/O	DESCRIPTION
CLK	33	I	Clock input
DATA	34	I	Serial data input
GND	5, 11, 15, 16, 17, 18, 19, 21, 23, 30,		Ground
I+	27	I	Noninverting in-phase baseband input
I–	28	I	Inverting in-phase baseband input
IPEAK	10	I	Peak charge pump current set
LOCK	8	O	Lock detect digital output signal
MCLK	40	O	Master clock output
NC	1, 2, 3, 4, 32, 36, 42, 43, 44, 45, 46, 47, 48		No connect
PHSOUT	9	O	Phase detector charge pump output
Q+	26	I	Noninverting quadrature baseband input
Q–	25	I	Inverting quadrature baseband input
RCLK	41	O	Reference clock output
STROBE	31	I	Data strobe enable
TNK+	12	I	Offset VCO noninverting tank port
TNK–	13	I	Offset VCO inverting tank port
TX+	20	O	Noninverting transmit output
TX–	22	O	Inverting transmit output
TXEN	35	I	Transmit enable
TXLO+	6	I	Noninverting transmit LO input
TXLO–	7	I	Inverting transmit LO input
XTLB	39	I	Crystal oscillator base
XTLE	38	O	Crystal oscillator emitter
V_{CC}	14, 24, 29, 37		Power supply

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage range, V_{CC} . . . . . −0.3 V to 4.5 V
Power dissipation, T_A = 25°C, 48-pin plastic LQFP . . . . . 450 mW
Maximum operating virtual-junction temperature, T_J . . . . . 150°C
Operating free-air temperature range . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

	PARAMETER	MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3.6	3.75	3.9	V
V_{IH}	High-level input voltage	$0.7V_{CC}$		VCC+0.3	V
V_{IL}	Low-level input voltage	−0.3		$0.3V_{CC}$	V
V_{IC}	Common mode voltage of baseband inputs		$0.5V_{CC}$		V
TXLO	Input power	−13		−10	dBm
TXLO	Input frequency	900		1040	MHz
T_A	Operating free-air temperature	−40		85	°C
T_J	Operating virtual-junction temperature	−40		105	°C

electrical characteristics at V_{CC} = 3.75 V, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	Sleep		3		V
		Receive		6		
		Transmit		130		
V_{OL}	Low-level output voltage, LOCK	$I_{O(LOCK)}$ = 2 mA			0.40	V
		$I_{O(LOCK)}$ = 1 µA			0.05	
V_{OH}	High-level output voltage, LOCK	$I_{O(LOCK)}$ = −2 mA	V_{CC}−0.40			V
		$I_{O(LOCK)}$ = −1 µA	V_{CC}−0.05			

PRODUCT PREVIEW

electrical characteristics at V_{CC} = 3.75 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TXLO input VSWR		ac coupled, 50 Ω single-ended and 100 Ω differential		2:1		
Offset VCO frequency			90		200	MHz
PHSOUT output level			0.5		V_{CC}–0.5	V
PHSOUT peak current		Rset = 4.7 kΩ		6.4		mA
XO frequency			10		45	MHz
XO external drive level			1		2	V_{p-p}
CLK duty cycle				50%		
MCLK duty cycle				50%		
CLK1 duty cycle				50%		
CLK output level		5 kΩ ‖ 7 pF		1		V_{p-p}
MCLK output level		5 kΩ ‖ 7 pF		1		V_{p-p}
CLK1 output level		5 kΩ ‖ 7 pF		1		V_{p-p}
TX+/TX– frequency			820		920	MHz
TX+/TX– impedance		Differential		200		Ω
TX+/TX– VSWR		Z_O = 200 Ω		2:1		
TX+/TX– level		Z_O = 200 Ω, I/Q quadrature		9		dBm
TX+/TX– level flatness		Z_O = 200 Ω,, I/Q quadrature 824-849 MHz		1	2	dB
TX+/TX– 3rd order modulation spurious		I/Q in-phase		–42	–36	dBc
TX+/TX– 5th order modulation spurious		I/Q in-phase		–55	–45	dBc
TX+/TX– 7th order modulation spurious		I/Q in-phase		–65	–53	dBc
TX+/TX– carrier suppression		I/Q quadrature		–45		dBc
TX+/TX– sideband suppression		I/Q quadrature		–45		dBc
TX+/TX– broadband noise		869-894 MHz		–136		dBm/Hz
TX+/TX– phase noise		f = 30 kHZ		–95		dBc/Hz
		f = 60 kHZ		–101		
TX+/TX– other spurious	2–824 MHz			–45		dBc
	824–849 MHz			–47		dBc
	849–869 MHz			–45		dBc
	869–894 MHz			–104		dBm
	894–8490 MHz			–45		dBc
	TXLO and harmonics			–21		dBc
Baseband frequency				2		MHz
Baseband level		Differential	0.6	0.8	1	Vp-p
Baseband impedance		Differential	10			kΩ
Offset loop lock time		f_O = ±200 Hz		80		µs

PRODUCT PREVIEW

serial control interface timing requirements

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Clock frequency			0		10	MHz
$t_{w}H$	Pulse duration	CLK high		30			ns
$t_{w}L$	Pulse duration	CLK low		30			ns
t_{su}	Setup time	DATA before CLK high		30			ns
		STROBE before CLK high		30			ns
t_{h}	Hold time	DATA after CLK high		30			ns
		STROBE after CLK low		30			ns

serial control interface timing characteristics

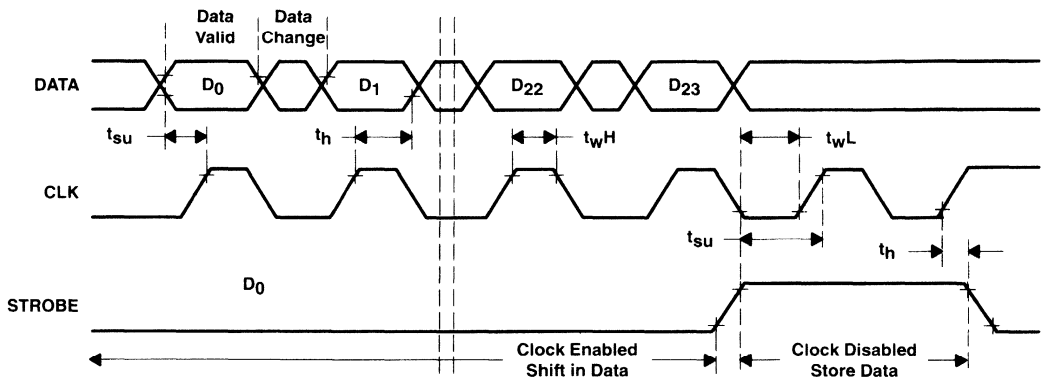


Figure 1. Serial Input Timing Sequence

G word

D23 D0

1	0	1	1	PC							N		MODE	SE	0	SM1	SM2	SPARE
				PC6	PC5	PC4	PC3	PC2	PC1	PC0	N1	N0						

data field description

Table 2 describes the data field assignments found in the 24-bit, serial data G word.

Table 2. G Word Data Field Functions

DATA FIELD	BITS	FUNCTION
PC	7	Power control
N	2	÷N, N=6, 7, 8, 9
MODE	1	AMPS mode
SE	1	Synthesizer on/off
SM1	1	Sleep mode 1
SM2	1	Sleep mode 2

PRODUCT PREVIEW

PC – power control (VGA)

The power control circuit has a control range of 40 dB (0 dB to –40 dB) with a monotonically decreasing slope. Power control decreases in steps of 0.2 dB from 0 dB to –12 dB and in steps of 2 dB from –12 dB to –40 dB. The nominal power output of the VGA is 9 dBm.

N – variable modulus select

The offset VCO modulus division ratio (÷N) is determined by the values of bits N1 and N0 as shown in Table 3.

Table 3. Offset VCO Modulus Select

N1	N0	÷N
0	0	6
0	1	7
1	0	8
1	1	9

MODE – output driver mode select

The mode bits allows a reduction in current for the TX output driver while in AMPS mode. MODE = 1 for non-AMPS, MODE = 0 for AMPS.

SE – synthesizer enable

The SE bit turns on and off the offset loop synthesizer circuits. SE = 1, synthesizer on; SE = 0, synthesizer off.

SM1 – sleep mode 1

The SM1 bit is used to shut down the TXLO buffer. SM1 = 1, buffer on; SM1 = 0, buffer off.

SM2 – sleep mode 2

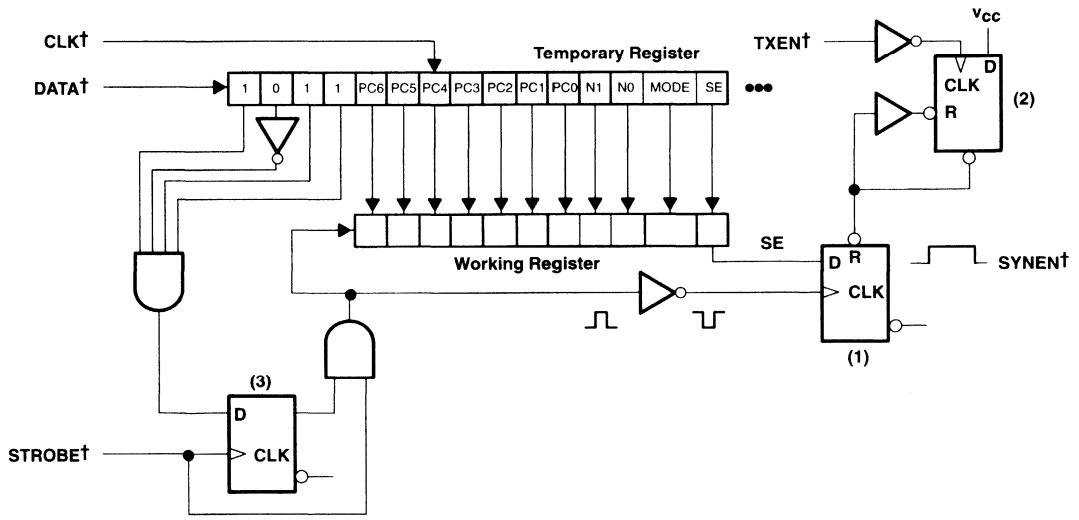
The SM2 bit is used to shut down the RCLK buffer. SM2 = 1, buffer on; SM2 = 0, buffer off.

powerdown control

The powerdown control of TRF3020 internal functions is determined by the states of G word data bits SE, SM1, SM2, and PC and by external control signal TXEN as shown in Table 4.

Table 4. Powerdown Control

FUNCTION	SLEEP	MODE RECEIVE	TRANSMIT	DATA BIT/ CONTROL BIT
Crystal oscillator	On	On	On	
Phase detector			On	SE
Offset divider			On	SE
Offset VCO			On	SE
VCO buffer			On	SE
SSBSC downconverter			On	SE
MCLK buffer	On	On	On	
RCLK buffer		On	On	SM2
TXLO buffer			On	SM1
I/Q modulator			On	SE
VGA			On	TXEN, PC
Control logic	On	On	On	
Lock detect			On	SE



† CLOCK, DATA, STROBE, and TXEN are device terminal connections. SYNEN is an internal signal.

SYNEN and TXEN Enable Control

SYNEN	TXEN
Phase detector	
VCO	VGA
÷N variable modulus select	
SSB downconverter	
I/Q modulator	

Figure 2. Transmit Offset Synthesizer Reset Circuit

transmit offset synthesizer reset circuit

The transmit offset synthesizer reset circuit, as shown in Figure 2, provides power control of the transmit offset synthesizer, TXLO buffer, and the SSB downconverter during transmit frame sequences. The address decoder for the G word ANDed together with the strobe signal is used to transfer the contents of the temporary holding register into the working register. D-flip-flop (3) is used to prevent multiple strobe and address pulses in the event the address decoder output toggles on garbage bits during the time the strobe remains in a high state.

With the falling edge of the strobe signal and SE = 1, the transmit offset synthesizer, TXLO buffer, modulator and SSB downconverter are enabled with SYNEN = 1. After the synthesizer is locked and just before the beginning of a transmit frame, the TXEN = 1 signal turns on the variable gain amplifier.

The rising edge of TXEN has no effect on SYNEN, but the falling edge of TXEN toggles the $\overline{Q}$ output of D flip-flop (2) to a 0 state. This, in turn, resets D flip-flop (1) which causes SYNEN to go to a 0 state thereby disabling the synthesizer, modulator, and variable gain amplifier.

The G word must be reloaded and the above sequence repeated for every subsequent transmit frame event.

PRODUCT PREVIEW

Table 5. Typical Filter Network

COMPONENT DESIGNATOR	VALUE	
	DUAL MODE	AMPS MODE
R1	560 Ω	560 Ω
R2	1 kΩ	5.6 kΩ
C1	2.2 nF	2.7 µF
C2	No load	0.27 µF
C3	33 pF	6.8 nF
R_{SET}	15 kΩ	75 kΩ

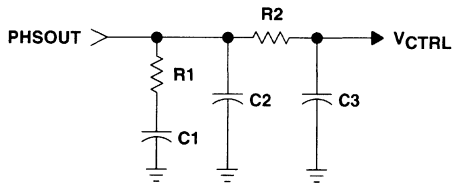
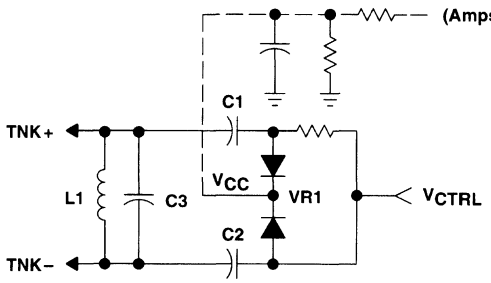


Figure 3. Typical PLL Filter



$$f_{VCO} = 120\ MHz = \frac{1}{2\pi\sqrt{L1\ C'}}$$

$$C' = C3 + \left(\frac{1}{C1} + \frac{1}{C2} + \frac{1}{CVR1}\right)^{-1}$$

C1 = C2 = 33 pF
C3 = 12 pF
L1 = 82 nH

Figure 4. VCO Tank Configuration

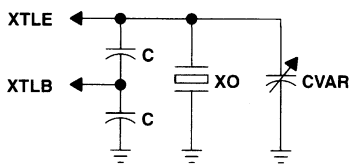


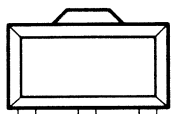
Figure 5. Crystal Oscillator Configuration

PRODUCT PREVIEW

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

- 3.6-V and 4.8-V Operating Voltage for AMPS/NADC and GSM Cellular Telephone Applications Respectively
- Wide UHF Frequency Range: 800 to 2000 MHz, Suitable for PCS Applications
- High Output Power
  - at 4.8 V and 900 MHz, 35 dBm Typical (CW or pulsed)
  - at 3.6 V and 836 MHz, 31 dBm Typical (CW or pulsed)
- High Gain
  - at 4.8 V and 900 MHz, 14 dB Typical Gain at P_O = 35 dBm
  - at 3.6 V and 836 MHz, 19 dB Typical Gain at P_O = 29 dBm
- High Power Efficiency
  - at 35 dBm Output Power, 53% PAE Typical
  - at 29 dBm Output Power, 30% PAE Typical
- Extremely Reliable
- Suitable for GSM and Highly Linear NADC Applications
- SOT-89 Plastic Power Package

PK PACKAGE
(TOP VIEW)



description

The TRF7000 is a gallium arsenide MESFET (metal Schottky field-effect transistor) housed in an SOT-89 (PK) plastic power package. It is designed for high power applications in the 800 MHz to 2000 MHz frequency range and is a low cost solution that is suitable for use in either GSM (Global System for Mobil Communications) or highly linear dual-mode AMPS/NADC (Advanced Mobile Phone Service/North American Digital Cellular) mobile telephone systems. A wide operational frequency range allows the TRF7000 to be used in PCS (personal communications systems) applications.

A 0.5-micron gate length and an interdigitated structure using airbridge interconnects between drain fingers provide high gain, high frequency cut-off, and high power-efficiency (PAE). Gold metalization and silicon nitride passivation assure a reliable device.

PRODUCT PREVIEW

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the gates.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Drain-source voltage, V_{DS} (see Note 1) ..... 15 V
Gate-source voltage, V_{GS} ..... −5 V
Drain current, I_{DS} (V_G = 0 V) ..... 6 A
Total power dissipation, P_T at T_C = 25 °C ..... 4 W
Storage temperature, T_{stg} ..... −65°C to 150°C
Channel temperature, T_{CH} ..... 175°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltages are with respect to GND.

electrical characteristics at V_{DS} as specified and T_A = 25°C

DC characteristics

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
I_D	Saturated drain current	V_{GS} = 0, V_{DS} swept between 0.5 V and 3.5 V, searching for maximum I_{DS}, V_{DS} at I_{DSS} recorded as V_{DSP}		7		A
g_m	Transconductance	$\lvert I_{DSS} - I_{DS1} \rvert / V_{GS}$, V_{DS} swept between 0.5 V and V_{DSP}, searching for maximum I_{DS}, recorded as I_{DS1},V_{GS} = −0.5 V		3300		mS
	Pinch-off voltage (V_p)	V_{DS} = 2 V, V_{GS} swept to bring I_{DS} = 0.5 mA/mm	−3.8	−2.9	−2	V
$V_{(BR)GD}$	Gate-drain breakdown voltage	Drain is grounded, Source is floating, 1 mA/mm drawn at the gate	−30	−14	−8	V
R_θ	Thermal resistance	Channel to case		15		°C/W

NADC RF characteristics

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNITS
P_O	Output power	Class A/AB, I_{DSQ} = 900 mA, f = 836 Mhz,	V_{DS} = 4.8 V, P_I = 10 dBm, Fixed test circuit		29		dBm
G	Power gain				19		dB
	Power-added efficiency, (PAE)				30%		

AMPS RF characteristics

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNITS
P_O	Output power	Class A/AB, I_{DSQ} = 900 mA, f = 836 Mhz,	V_{DS} = 3.6 V, P_I = 17 dBm, Fixed test circuit		31		dBm
G	Power gain				14		dB
	Power-added efficiency, (PAE)				53%		

GSM RF characteristics

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNITS
P_O	Output power	Class AB/B, I_{DSQ} = 900 mA, f = 900 Mhz,	V_{DS} = 4.8 V, P_I = 21 dBm, Fixed test circuit		35		dBm
G	Power gain				14		dB
	Power-added efficiency, (PAE)				53%		

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

POWER DERATING CURVE

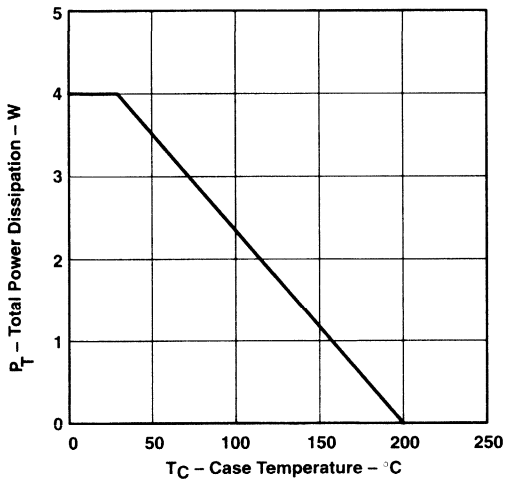


Figure 1

DRAIN CURRENT
vs
DRAIN-SOURCE VOLTAGE

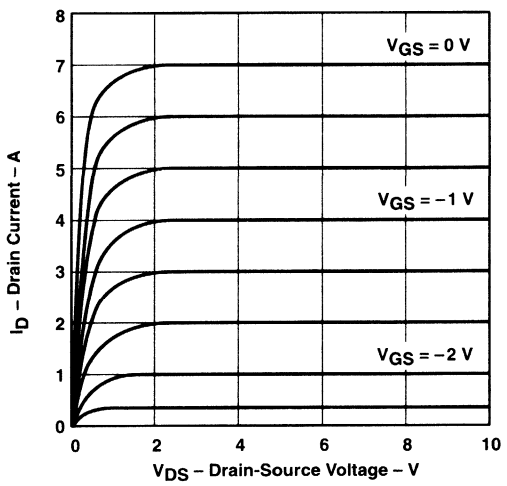


Figure 2

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

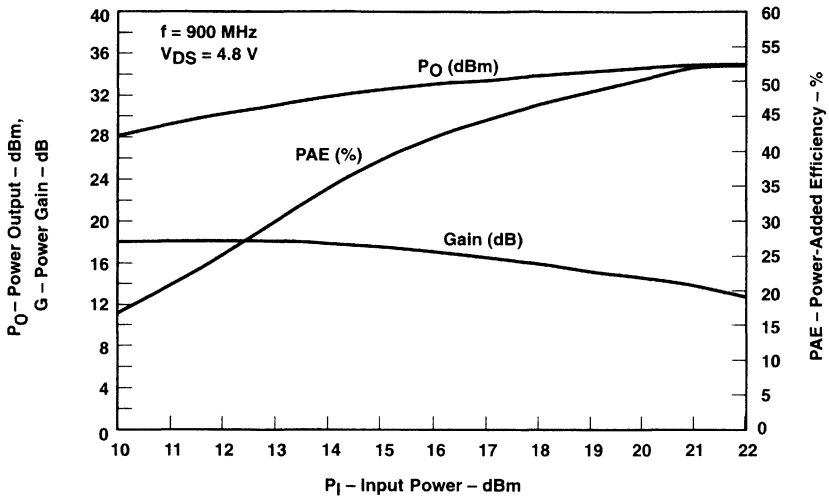


Figure 3. Typical RF Performance for GSM

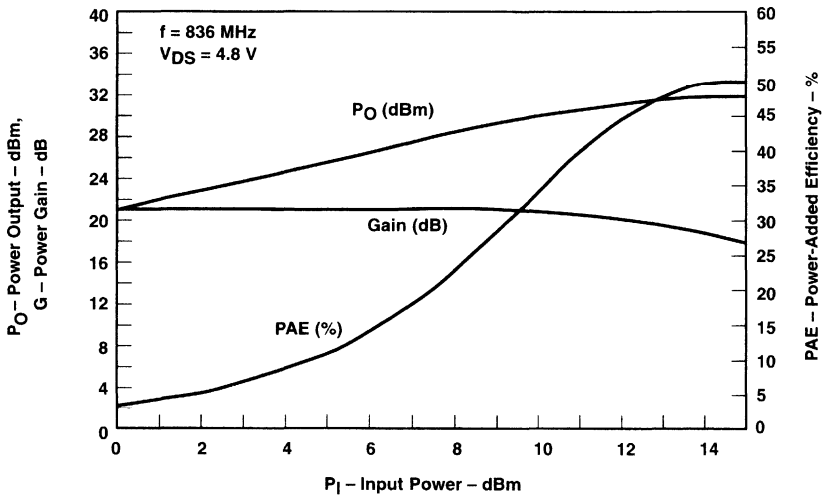


Figure 4. Typical RF Performance for NADC

PRODUCT PREVIEW

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TYPICAL CHARACTERISTICS

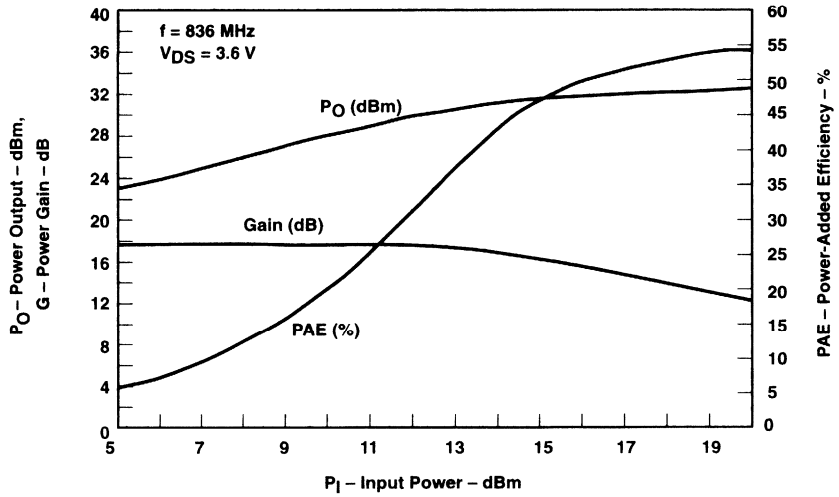
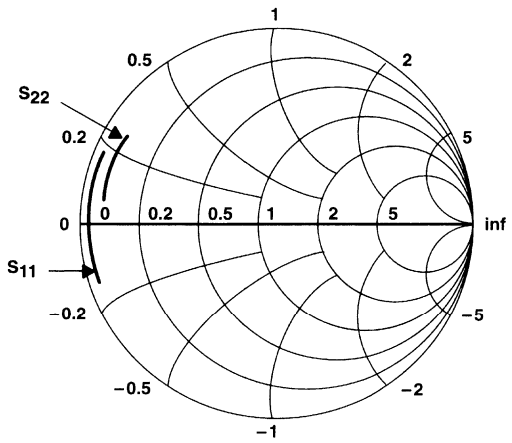


Figure 5. Typical RF Performance for AMPS

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

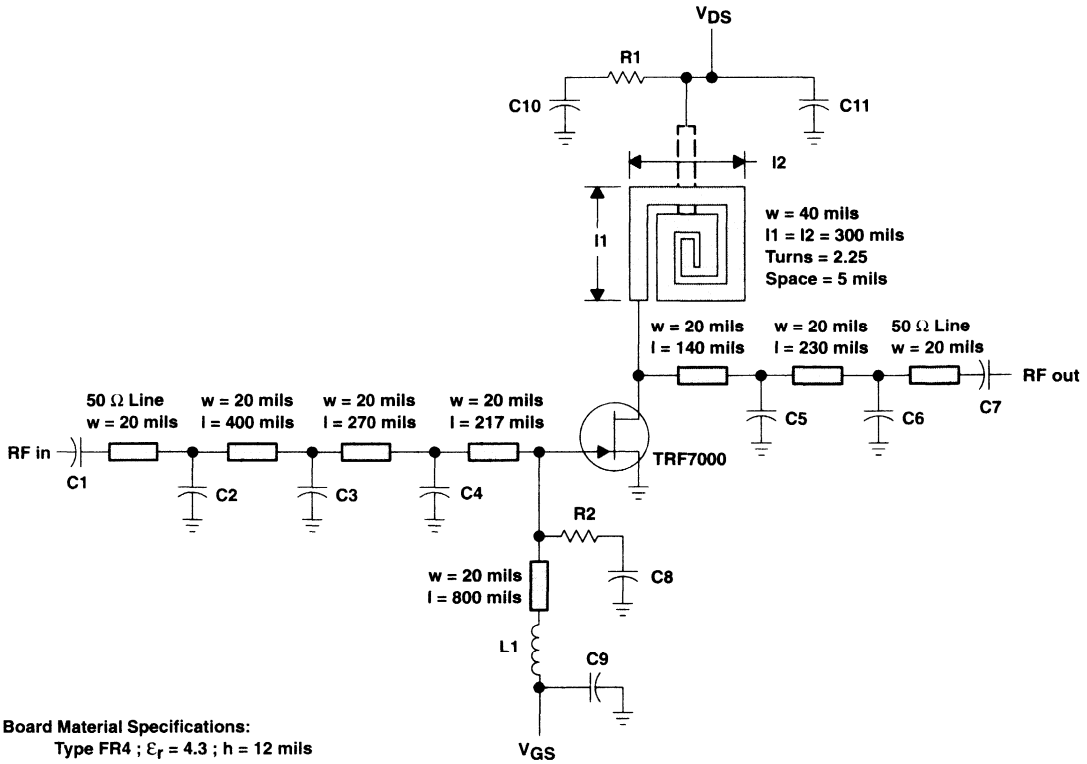


Frequency (MHz)	S[1,1] Mag	S[1,1] Ang (deg)	S[2,1] Mag	S[2,1] Ang (deg)	S[1,2] Mag	S[1,2] Ang (deg)	S[2,2] Mag	S[2,2] Ang (deg)
700	0.971	−164.9	2.660	89	0.011	2	0.896	170.9
800	0.971	−169.6	2.334	85.5	0.011	−1.1	0.897	169.4
900	0.971	−173.5	2.077	82.3	0.011	−3.8	0.898	167.9
1000	0.971	−177	1.869	79.4	0.011	−6.3	0.898	166.4
1100	0.971	179.9	1.696	76.7	0.011	−8.6	0.899	164.9
1200	0.971	177.1	1.552	74.1	0.011	−10.7	0.900	163.5
1300	0.971	174.4	1.428	71.6	0.011	−12.8	0.900	162
1400	0.971	172	1.321	69.2	0.011	−14.7	0.901	160.6
1500	0.971	169.6	1.228	66.9	0.011	−16.6	0.902	159.2
1600	0.971	167.4	1.146	64.6	0.011	−18.5	0.902	157.8
1700	0.971	165.3	1.074	62.4	0.011	−20.3	0.903	156.4
1800	0.971	163.3	1.009	60.2	0.011	−22	0.903	155
1900	0.972	161.3	0.950	58.1	0.010	−23.7	0.904	153.6
2000	0.972	159.4	0.897	56	0.010	−25.4	0.905	152.2

Figure 6. Typical Small Signal Scattering Parameters

PRODUCT PREVIEW

APPLICATION INFORMATION



Board Material Specifications:
Type FR4 ; ε_r = 4.3 ; h = 12 mils

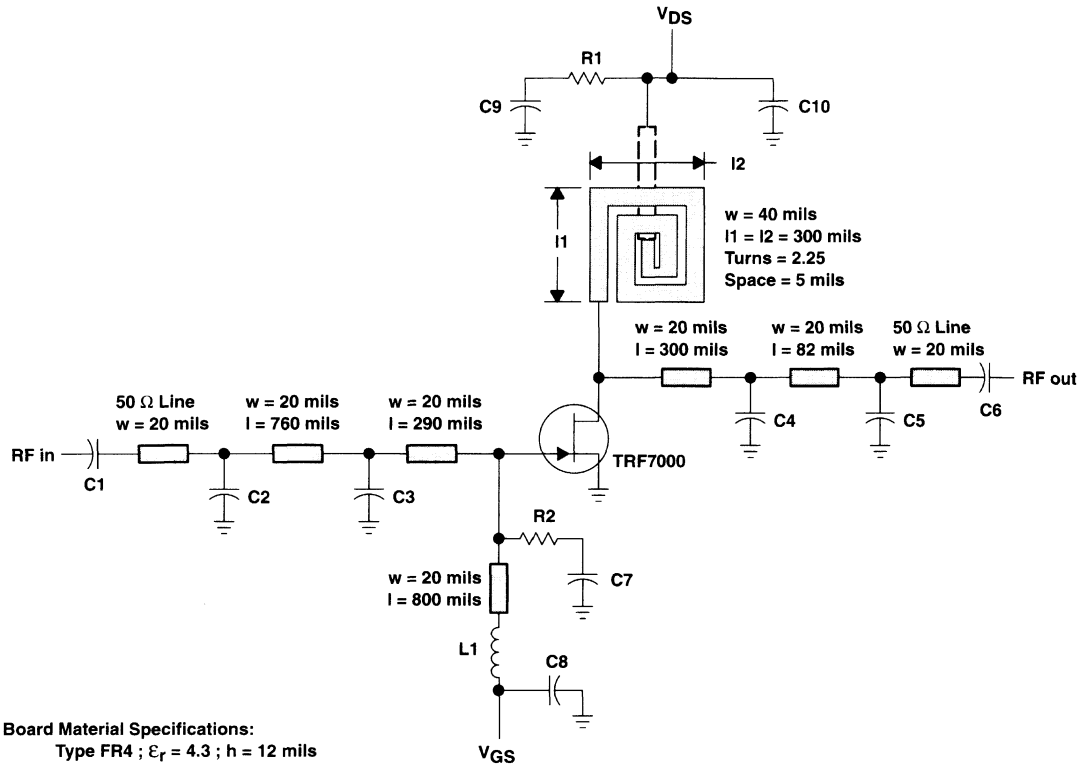
COMPONENT DESIGNATION	TYPICAL VALUE (GSM)	FUNCTION
C1	1000 pF	DC blocking capacitor for RF input
C2	1.6 pF	Matching capacitor
C3	5.6 pF	Matching capacitor
C4	24 pF	Matching capacitor
C5	7.5 pF	Matching capacitor
C6	2.7 pF	Matching capacitor
C7	1000 pF	DC blocking capacitor for RF output
C8	100 pF	Stability network capacitor
C9	100 pF	Power supply decoupling capacitor
C10	1000 pF	Stability network capacitor
C11	20 pF	Power supply decoupling capacitor
L1	12 nH	RF choke
R1	3 Ω	Stability network resistor (optional)
R2	100 Ω	Stability network resistor

Figure 7. Application/Demonstration Board Schematic for GSM

PRODUCT PREVIEW

PRODUCT PREVIEW

APPLICATION INFORMATION

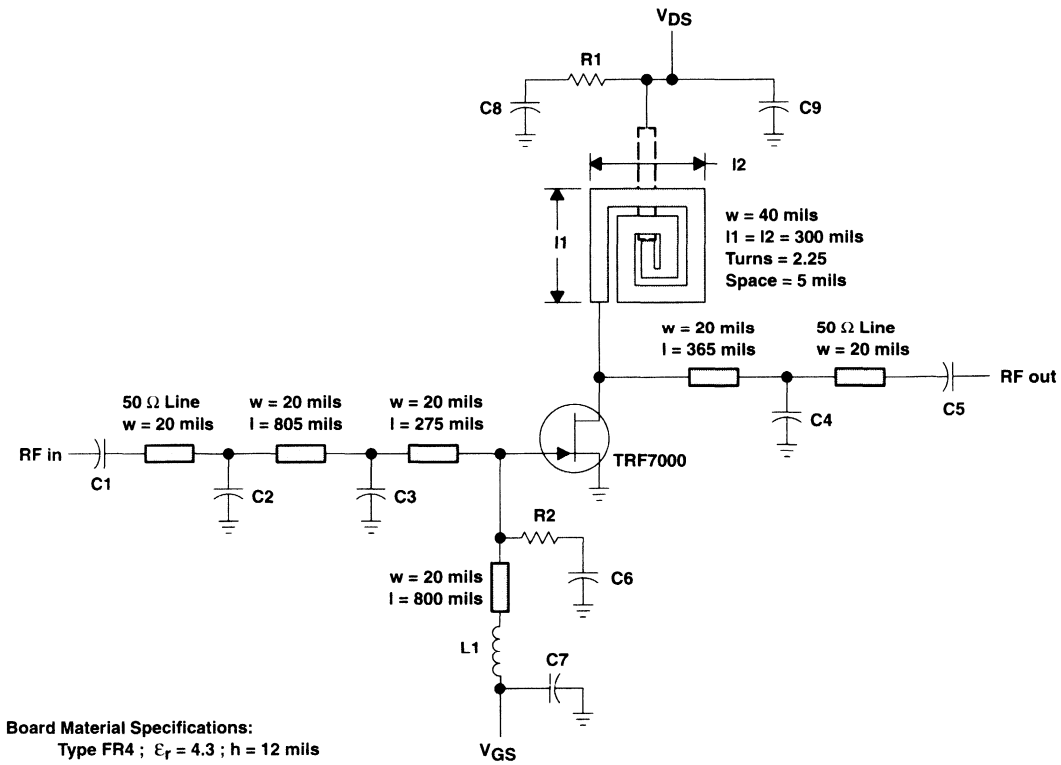


Board Material Specifications:
Type FR4 ; ε_r = 4.3 ; h = 12 mils

COMPONENT DESIGNATION	TYPICAL VALUE (NADC)	FUNCTION
C1	1000 pF	DC blocking capacitor for RF input
C2	4.7 pF	Matching capacitor
C3	30 pF	Matching capacitor
C4	7.5 pF	Matching capacitor
C5	2.5 pF	Matching capacitor
C6	1000 pF	DC blocking capacitor for RF output
C7	100 pF	Stability network capacitor
C8	100 pF	Power supply decoupling capacitor
C9	1000 pF	Stability network capacitor
C10	20 pF	Power supply decoupling capacitor
L1	12 nH	RF choke
R1	3 Ω	Stability network resistor (optional)
R2	100 Ω	Stability network resistor

Figure 8. Application/Demonstration Board Schematic for NADC

APPLICATION INFORMATION



Board Material Specifications:
Type FR4 ; ε_r = 4.3 ; h = 12 mils

COMPONENT DESIGNATION	TYPICAL VALUE (AMPS)	FUNCTION
C1	1000 pF	DC blocking capacitor for RF input
C2	3.3 pF	Matching capacitor
C3	30 pF	Matching capacitor
C4	7.5 pF	Matching capacitor
C5	1000 pF	DC blocking capacitor for RF output
C6	100 pF	Stability network capacitor
C7	100 pF	Power supply decoupling capacitor
C8	1000 pF	Stability network capacitor
C9	20 pF	Power supply decoupling capacitor
L1	12 nH	RF choke
R1	3 Ω	Stability network resistor (optional)
R2	100 Ω	Stability network resistor

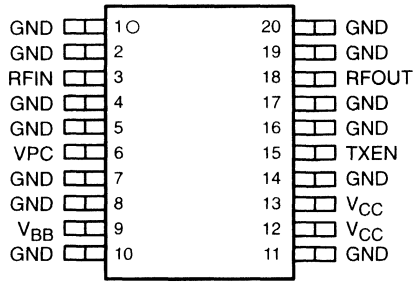
Figure 9. Application/Demonstration Board Schematic for AMPS

PRODUCT PREVIEW

SLWS031 – JULY 1996

- **Operates from 3.6-V and 4.8-V Supplies for AMPS/NADC and GSM Applications Respectively**
- **Unconditionally Stable**
- **Wide UHF Frequency Range — 800 MHz to 1000 MHz**
- **21 dBm and 22 dBm Power Outputs in AMPS/NADC and GSM Applications Respectively**
- **Linear Ramp Control**
- **Transmit Enable/Disable Control**
- **Advanced BiCMOS Processing Technology for Low-Power Consumption, High Efficiency, and Highly Linear Operation**
- **Minimum of External Components Required for Operation**
- **Surface-Mount Thermally-Enhanced Package for Extremely Small Circuit Footprint**

PWP PACKAGE
(TOP VIEW)



description

The TRF8010 is an RF transmit driver amplifier designed for 900-MHz digital, analog, and dual-mode communication applications. It consists of a 2-stage driver amplifier and a linear ramp controller for burst control in TDMA (time division multiple access) applications. Very few external components are required for operation.

The TRF8010 amplifies the RF signal from the preceding modulator and upconverter stages in an RF section of a transmitter to a level sufficient to drive a final RF power output device. The output impedance of RFOUT is approximately 50 Ω. But, since this terminal is connected to an open-collector output device, minimal external matching is required.

The device is enabled when the TXEN input is held high. A power-control signal applied to the VPC input can be used to ramp the RF output power up or down to meet ramp and spurious emission specifications in TDMA systems. The power control signal causes a linear change in output power as the voltage applied to VPC varies between 0 V and 3 V. With the RF input power applied to RFIN at 0 dBm and TXEN high, adjusting VPC from 0 V to 3 V linearly increases the output power from a maximum of –10 dBm at VPC = 0 V to the output power appropriate for the application (21 dBm for AMPS/NADC [Advanced Mobile Phone Service/North American Digital Cellular] operation or 22 dBm for GSM [Global Systems for Mobile Communications] operation). Forward isolation with the RF input power applied to RFIN at 0 dBm, VPC = 0 V, and TXEN low is a minimum of 47 dB.

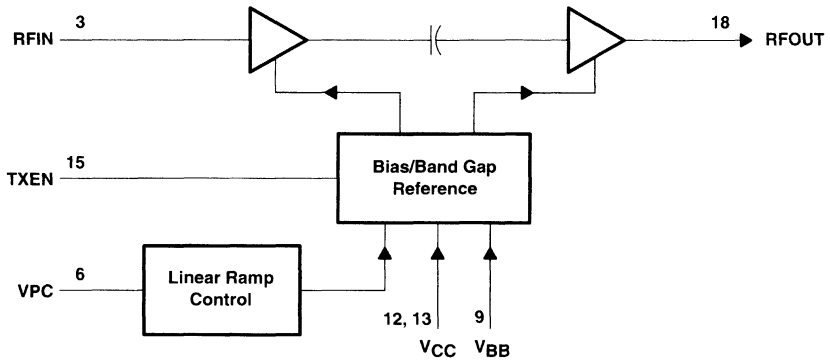
PRODUCT PREVIEW

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

description (continued)

The TRF8010 is available in a small, surface-mount, thermally-enhanced TSSOP 20-pin (PWP) package, and is characterized for operation from –25°C to 85°C. The PWP package has a solderable thermal pad that can be used to improve the package thermal performance by bonding the pad to an external thermal plane. The pad also acts as a low-inductance electrical path to ground, and for the TRF8010, should be electrically connected to the PCB ground plane as a continuation of the regular package pins that are designated GND.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND	1, 2, 4, 5, 7, 8, 10, 11, 14, 16, 17, 19, 20		Analog ground for all internal analog circuits. All signals are referenced to this terminal.
RFIN	3	I	RF input. This terminal accepts signals between 800 MHz and 1000 MHz.
RFOUT	18	O	RF output. This is an open-collector output and requires a decoupled connection to V_{CC} for operation.
TXEN	15	I	Transmit enable input (digital). A logic high applied to TXEN enables the device output.
V_{BB}	9		Control section supply voltage
V_{CC}	12, 13		First stage bias
VPC	6	I	Output-power control input (analog). A signal between 0 V and 3 V applied to VPC adjusts output power between –10 dBm and the maximum output power appropriate for the application.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.6 V to 5.6 V
Input voltage range at TXEN, VPC . . . . . –0.6 V to 5.6 V
Input power at RFIN . . . . . 10 dBm
Continuous total power dissipation at T_A = 25°C . . . . . 1 W
Operating junction temperature, T_J . . . . . 150°C
Operating free-air temperature range, T_A . . . . . –25°C to 85°C
Storage temperature range, T_{stg} . . . . . –30°C to 100°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see Note 2)	3		5	V
High-level input voltage at TXEN, V_{IH}	V_{CC} –0.8			V
Low-level input voltage, TXEN, V_{IL}			0.8	V
Operating free-air temperature, T_A	–25		85	°C

NOTE 2: Voltage values are with respect to GND.

electrical characteristics over full range of operating conditions

supply current, V_{CC} = 3.6 V and V_{CC} = 4.8 V

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{CC} Supply current from V_{CC}	Operating at maximum power out	TXEN high, VPC = 3 V		170		mA
	Operating at minimum power out	TXEN high, VPC = 0 V		25		mA
	Power down	TXEN low, VPC = 0 V			0.05	mA

† Typical values are at T_A = 25°C.

AMPS/NADC operation, V_{CC} = 3.6 V, TXEN high, VPC = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Operating frequency range			824		849	MHz
Output power		P_I = 0 dBm		21		dBm
Gain (small signal)		P_I = –20 dBm		26		dB
Power added efficiency (PAE)		P_I = 0 dBm		24%		
Input return loss (internally matched)				7		dB
Output return loss (externally matched, small signal)				10		dB
Noise power in 30 kHz channel		45 MHz offset at 21 dBm P_O		–92		dBm
Harmonics ($2f_0$, $3f_0$)		P_O = 21 dBm		–30		dBc
Adjacent channel leakage power	Padj (30 kHz)	P_I = –2 dBm, BW = 24.3 kHz		–30		dBc
	Padj (60 kHz)			–55		
	Padj (90 kHz)			–65		
P_O Output power	TXEN high	P_I = 0 dBm, VPC = 0 V			–10	dBm
	TXEN low				–47	

† Typical values are at T_A = 25°C.

PRODUCT PREVIEW

GSM operation, V_{CC} = 4.8 V, TXEN high, VPC = 3 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Extended GSM operating frequency range			870		925	MHz
P_O	Output power		P_I = 0 dBm, pulsed with a pulse width of 577 µs, and 1:8 duty cycle		22		dBm
	Gain (small signal)		P_I = –20 dBm, pulsed with a pulse width of 577 µs, and 1:8 duty cycle		27		dB
	Power added efficiency (PAE)		P_I = 0 dBm, pulsed with a pulse width of 577 µs, and 1:8 duty cycle		25%		
	Input return loss (internally matched)				7		dB
	Output return loss (externally matched, small signal)				10		dB
	Δ Phase shift		Δ P_O = 1dB for P_O 21 to 22 dBm		2.5		deg
	Harmonics ($2f_0$, $3f_0$)		P_O = 22 dBm		–30		dBc
	Noise power in 30 kHz bandwidth	20 MHz above f_0	P_O = 22 dBm		–89		dBm
		10 MHz above f_0			–77		dBm
	Output power	TXEN high	P_I = 0 dBm, VPC = 0 V			–10	dBm
		TXEN low				–47	

stability, AMPS/NADC and GSM operation

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Stability	Output VSWR† < 6:1 all phases, V_{CC} < 7.5 V, P_I = 0 dBm, P_O ≤ 22 dBm	No parasitic oscillations (all spurious < –70 dBc)			

† VSWR = voltage standing wave ratio.

switching characteristics

AMPS/NADC and GSM operation, V_{CC} = 3.6 V or 4.8 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{on}	Switching time, RF output OFF to ON	TXEN = high, VPC step 0 V to 3 V		2	µs
t_{off}	Switching time, RF output ON to OFF	TXEN = high, VPC step 3 V to 0 V		2	µs

PRODUCT PREVIEW

APPLICATION INFORMATION

A typical application example for AMPS/NADC cellular telephone systems is shown in Figure 1.

In all cases, a capacitor must be connected from the positive supply to ground as close to the IC pins as possible for power supply bypassing. A dc-blocking capacitor is also required on the output RF terminal.

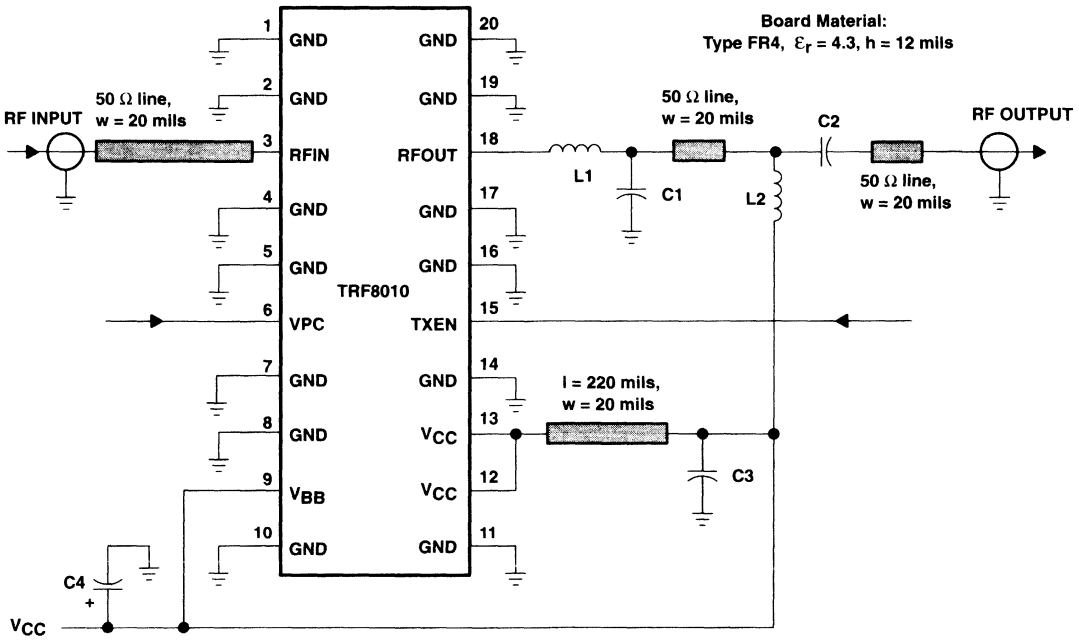


Figure 1. Typical AMPS/NADC Cellular Telephone Application

external component selection

COMPONENT DESIGNATION	TYPICAL VALUE (AMPS/NADC)	FUNCTION
C1	3.3 pF	Output impedance matching capacitor
C2	100 pF	DC-blocking capacitor for RF output
C3	100 pF	Matching capacitor
C4	1000 pF	Power supply decoupling capacitor
L1	5.7 nH	Output impedance-matching inductor
L2	100 nH	DC bias/RF choke

PRODUCT PREVIEW

APPLICATION INFORMATION

typical RF performance curves

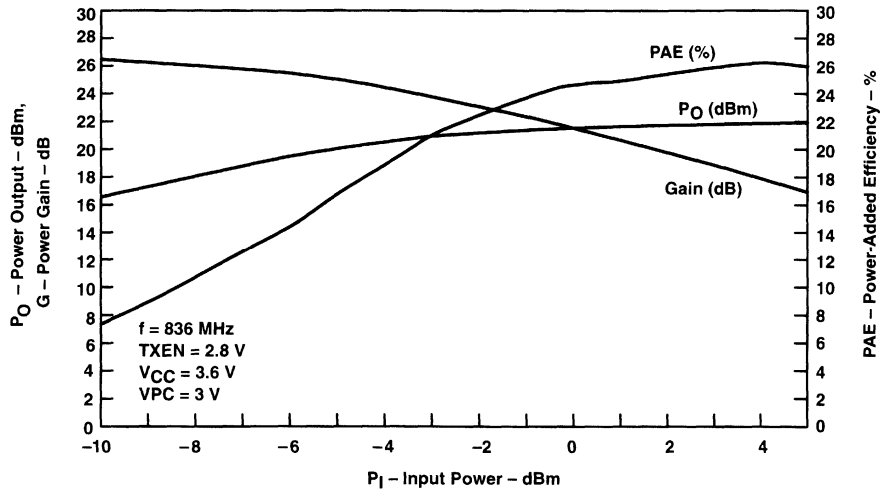


Figure 2. Typical P_O/Gain/PAE vs P_I Curves for AMPS

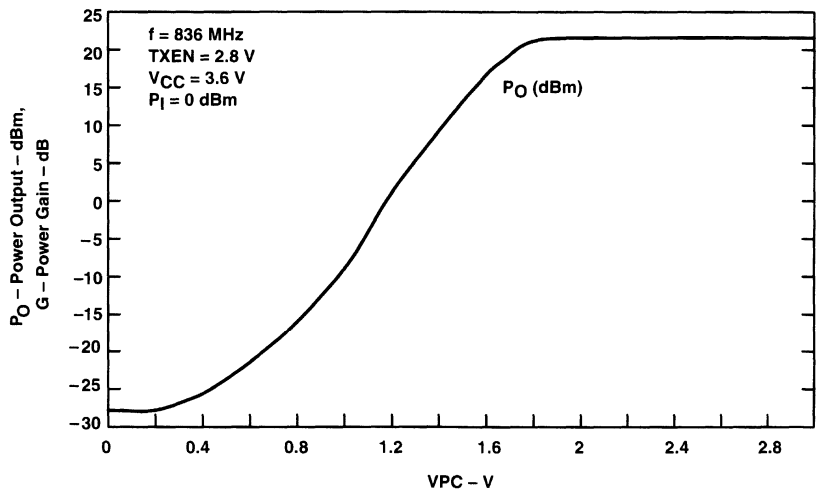


Figure 3. Typical P_O/Gain vs VPC Curve for AMPS

PRODUCT PREVIEW

APPLICATION INFORMATION

A typical application example for GSM cellular telephone systems is shown in Figure 4.

In all cases, a capacitor must be connected from the positive supply to ground as close to the IC pins as possible for power supply bypassing. A dc-blocking capacitor is also required on the output RF terminal.

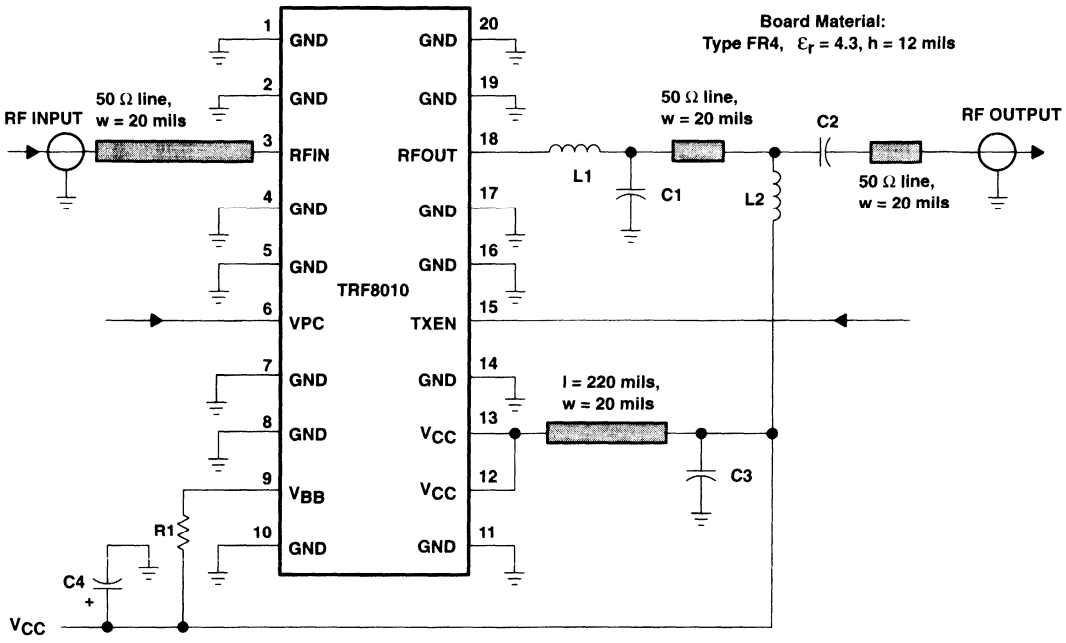


Figure 4. Typical GSM Cellular Telephone Application

external component selection

COMPONENT DESIGNATION	TYPICAL VALUE (GSM)	FUNCTION
C1	3.3 pF	Output impedance matching capacitor
C2	100 pF	DC-blocking capacitor for RF output
C3	100 pF	Matching capacitor
C4	1000 pF	Power supply decoupling capacitor
L1	6.8 nH	Output impedance-matching inductor
L2	100 nH	DC bias/RF choke
R1	180 Ω	Bias supply resistor

PRODUCT PREVIEW

APPLICATION INFORMATION

typical RF performance curves

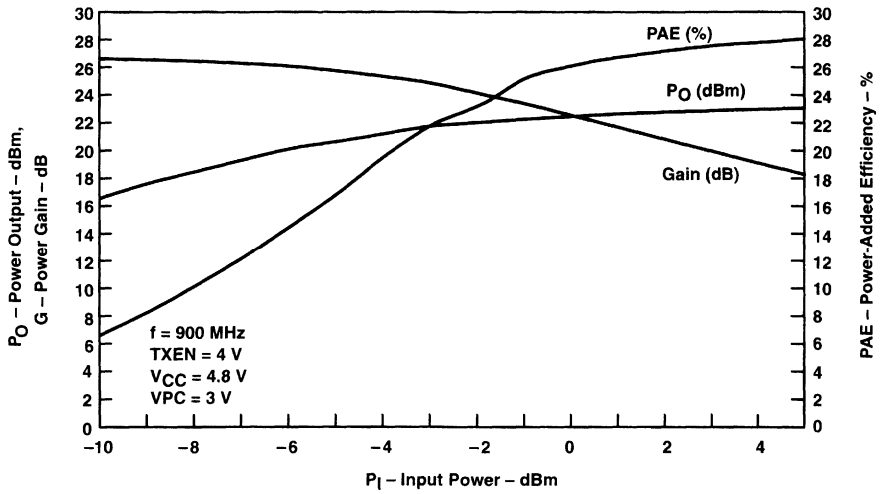


Figure 5. Typical P_O/Gain/PAE vs P_I Curves for GSM

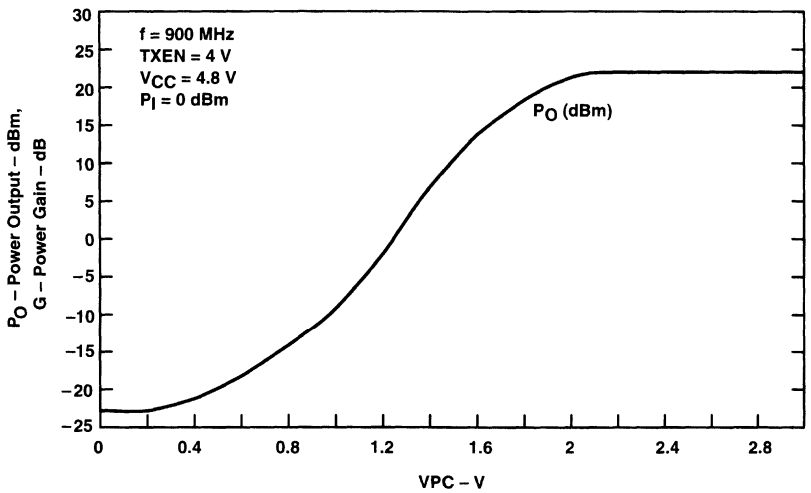
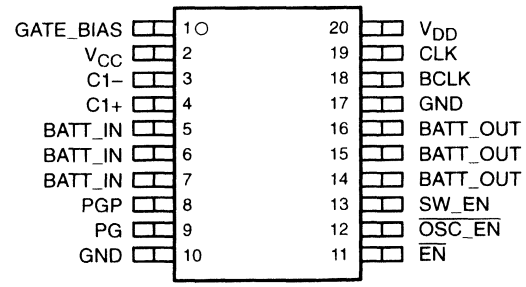


Figure 6. Typical P_O/Gain vs VPC Curve for GSM

PRODUCT PREVIEW

- **Charge Pump Provides Negative Gate Bias for Depletion-Mode GaAs Power Amplifiers**
- **Buffered Clock Output to Drive Additional External Charge Pump**
- **135-mΩ High-Side Switch Controls Supply Voltage to the GaAs Power Amplifier**
- **Power-Good Circuitry Prevents High-Side Switch Turn-on Until Negative Gate Bias is Present**
- **Charge Pump Can Be Driven From the Internal Oscillator or An External Clock**
- **10-μA Maximum Standby Current**
- **Low-Profile (1.2-mm Max Height), 20-Pin TSSOP Package**

PW PACKAGE
(TOP VIEW)



description

The TPS9103 is a highly integrated power supply for depletion-mode GaAs power amplifiers (PA) in cellular handsets and other wireless communications equipment. Functional integration and low-profile packaging combine to minimize circuit-board area and component height requirements. The device includes: a p-channel MOSFET configured as a high-side switch to control the application of power to the PA; a driver for the high-side switch with a logic-compatible input; a charge pump to provide negative gate-bias voltage; and logic to prevent turn-on of the high-side switch until gate bias is present. The high-side switch has a typical on-state resistance of 135 mΩ.

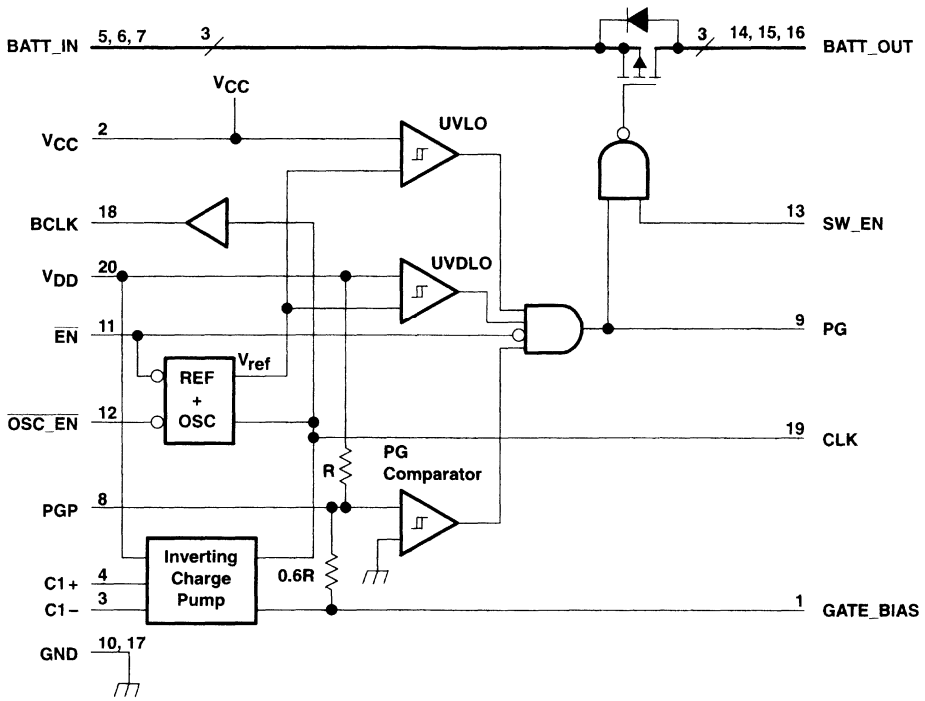
The TPS9103 is available in a 20-pin thin shrink small-outline package (TSSOP) or in chip form. Contact factory for die sales. The device operates over a junction temperature range of –25°C to 125°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE	CHIP FORM (Y)
	TSSOP (PW)	
–25°C to 85°C	TPS9103PWLE	TPS9103Y

The PW package is only available left-end taped and reeled (indicated by the LE suffix on the device type).

functional block diagram



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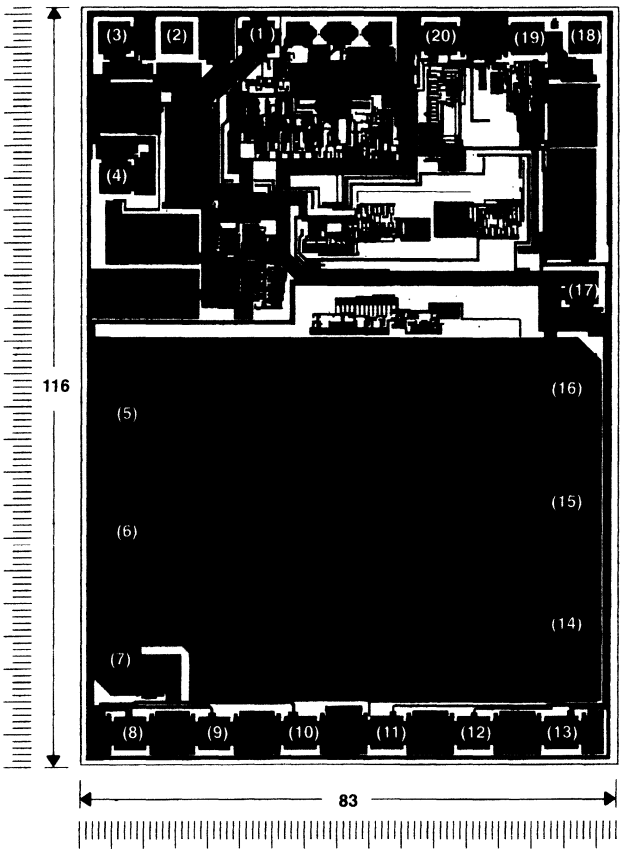
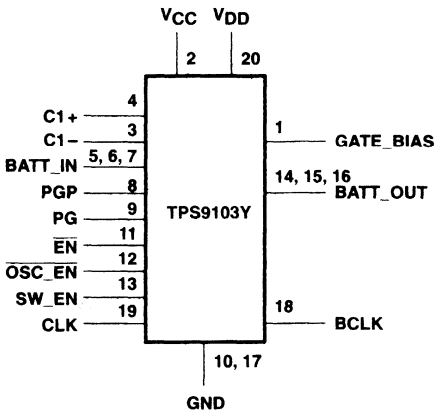
TPS9103Y chip information

This chip, when properly assembled, displays characteristics similar to the TPS9103. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform. Contact factory for die sales.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
GATE_BIAS	1	Negative gate-bias output voltage
V_{CC}	2	Logic supply voltage
C1–	3	External capacitor connection (inverting charge pump)
C1+	4	External capacitor connection (inverting charge pump)
BATT_IN	5	High-side switch input voltage
BATT_IN	6	High-side switch input voltage
BATT_IN	7	High-side switch input voltage
PGP	8	Program input for power-good threshold
PG	9	Power-good output
GND	10	Ground
$\overline{EN}$	11	Chip-enable input
$\overline{OSC\_EN}$	12	Oscillator-enable input
SW_EN	13	High-side switch enable input
BATT_OUT	14	High-side switch output voltage
BATT_OUT	15	High-side switch output voltage
BATT_OUT	16	High-side switch output voltage
GND	17	Ground
BCLK	18	Buffered clock output
CLK	19	Clock (bidirectional)
V_{DD}	20	Charge-pump supply voltage

detailed description

high-side switch and driver (BATT_IN, BATT_OUT, SW_EN)

The high-side switch is a p-channel MOSFET with a maximum on-state resistance of 180 mΩ ($V_{I(BATT\_IN)}$ = 6 V and V_{CC} = 3.3 V). The driver pulls the gate of the high-side switch to GATE_BIAS instead of ground to reduce the MOSFET on-state resistance. Gate breakdown considerations limit the voltage between BATT_IN and GATE_BIAS to 15 V. Extremely fast switching times are not required in this application, and the high-side switch/driver is designed to provide 2 μs maximum switching times with minimum power consumption. The GaAs depletion-mode MOSFETs in the PA are protected from damage at power-up by internal logic that inhibits the driver until negative gate bias is available. The control input SW_EN is compatible with 3-V and 5-V CMOS logic; a logic-high input turns the high-side switch on.

oscillator ($\overline{\text{OSC\_EN}}$, CLK)

The internal oscillator drives the charge pump at 50 kHz with a nominal duty cycle of 50% when both the $\overline{\text{EN}}$ and $\overline{\text{OSC\_EN}}$ inputs are logic lows. CLK outputs the internal oscillator signal (no buffer). A logic-high input to $\overline{\text{OSC\_EN}}$ disables the internal oscillator and allows the charge pump to operate from an external clock connected to CLK. When an external clock with negative overshoot is applied, a Schottky diode must be added to limit the amplitude of the overshoot.

charge pump (GATE_BIAS, C1+, C1–)

The inverting charge pump generates the negative gate-bias voltage output at GATE_BIAS.

chip enable ($\overline{\text{EN}}$)

A logic high on $\overline{\text{EN}}$ shuts down the internal functions of the TPS9103 and turns the bias system off, reducing the supply current to less than 10 μA. A low input on $\overline{\text{EN}}$ causes normal operation to resume.

power good (PG, PGP)

PG output is logic high when GATE_BIAS is in regulation. PG output is logic low when GATE_BIAS is not in regulation. The high-side switch is disabled and PG is forced to logic low whenever the magnitude of GATE_BIAS is less than 0.6 × V_{DD}. A modified threshold for the power-good function can be achieved by programming PGP with an external resistor.

undervoltage lockout for V_{CC} and V_{DD} (UVLO and UVDLO)

Undervoltage lockout prevents operation at supply voltages too low for proper operation. When UVLO or UVDLO is active, all power-switch drives are forced to the off state and bias is removed from unneeded functions. Hysteresis is provided to minimize cycling on and off because of source impedance loading when the supply voltage is close to the threshold.

buffered clock output (BCLK)

The buffered clock output is a driver for an external charge pump. When the optional external charge pump is not needed, BCLK should be left unconnected. For more details, see the application section.

supply input for inverting charge pump (V_{DD})

V_{DD} is the supply voltage for the inverting charge pump. In normal operation, V_{DD} is connected to V_{CC}. If the negative gate-bias needs to be larger than V_{CC} (i.e., more negative), then a higher voltage supply needs to be connected to V_{DD}. This can be supplied from an external charge pump driven from BCLK.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PW	645 mW	6.5 mW/°C	353 mW	255 mW

Maximum values are calculated using a derating factor based on $R_{\theta JA}$ = 154°C/W for the package. These devices are mounted on an FR4 board with no special thermal considerations.

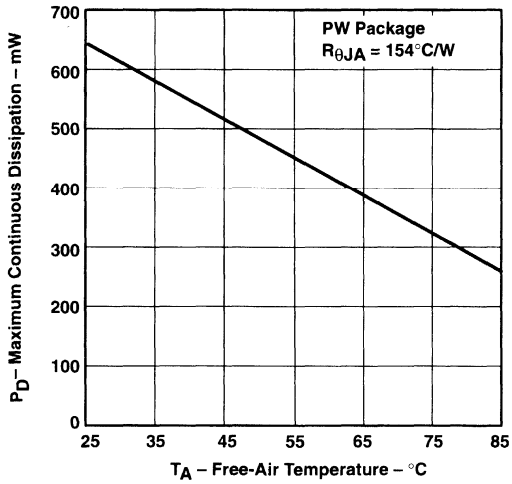


Figure 1. Dissipation vs Free-Air Temperature

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

High-side switch input voltage range, BATT_IN (see Note 1) ..... −0.3 V to 15 V
Supply voltage range, V_{CC}, V_{DD} ..... −0.3 V to 7 V
Differential voltage, |BATT_IN|–|GATE_BIAS| ..... 15 V
Input voltage range, SW_EN, $\overline{EN}$, CLK, $\overline{OSC\_EN}$, PG ..... −0.3 V to V_{CC} + 0.3 V
GATE_BIAS ..... −5.5 V
Output current, PG ..... 5 mA
Output current, BCLK ..... 50 mA
Output current, GATE_BIAS ..... 10 mA
Output current, BATT_OUT ..... 2 A
Peak output current, BATT_OUT ..... 4 A
Maximum external clock frequency, CLK ..... 100 kHz
Continuous total power dissipation ..... See Dissipation Rating Table
Junction temperature range, T_J ..... −25°C to 150°C
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to device GND.
2. Differential voltage calculated: |$V_I$max| + |GATE_BIAS|

recommended operating conditions

		MIN	NOM	MAX	UNIT
Input voltage, BATT_IN		3		9	V
Supply voltage, V_{CC}, V_{DD}		2.7		5.5	V
Output voltage, GATE_BIAS, V_O		–2		–5	V
Continuous output current, GATE_BIAS		0		10	mA
Continuous output current, BATT_OUT		0		2	A
Charge-pump capacitor value at C1+/C1–			0.33		µF
External clock frequency, CLK		25		75	kHz
High-level input voltage, V_{IH}	SW_EN, $\overline{EN}$, $\overline{OSC\_EN}$, CLK	2			V
Low-level input voltage, V_{IL}				0.8	V
Input current, I_I		–1		1	µA
Operating junction temperature, T_J		–25		125	°C

electrical characteristics over recommended operating junction temperature range, BATT_IN = 6 V, V_{CC} = V_{DD} = 3.3 V, $I_{O(BATT\_OUT)}$ = 0.5 A, $I_{O(GATE\_BIAS)}$ = 2 mA, $\overline{EN}$ = $\overline{OSC\_EN}$ = 0 V, SW_EN = V_{CC}, C1 = 0.33 µF (unless otherwise noted)

charge pump

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage		–3	–3.10	–3.3	V
Output resistance			95		Ω

high-side switch

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Dran-to-source on-state resistance	T_A = 25°C				135	180	mΩ
	T_A = –25°C to 85°C					210	
	T_A = 25°C,	$V_{I(BATT\_IN)}$ = 3 V			160	220	
	T_A = –25°C to 85°C,	BATT_IN = 3 V				260	
Leakage current	T_A = 25°C,	$V_{I(BATT\_IN)}$ = 9 V,	SW_EN = 0 V			1	µA
	T_A = 85°C,	$V_{I(BATT\_IN)}$ = 9 V,	SW_EN = 0 V			10	
Delay to high-level output	SW_EN from 0 to V_{CC}				0.2	2	µs
Delay to low-level output	SW_EN from V_{CC} to 0				0.9	2	µs

oscillator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency	V_{CC} = 2.7 V to 5.5 V	35	50	60	kHz
Duty cycle	V_{CC} = 2.7 V to 5.5 V	40%	50%	60%	

buffered clock output (BCLK)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output resistance				10	Ω
High-level output voltage	I(BCLK) = 30 mA	V_{CC} –0.3			V
Low-level output voltage	I(BCLK) = 30 mA			0.3	V

power good (PG)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Threshold voltage	V_{DD} = 2.7 V to 5.5 V		0.60 × V_{DD}		V
On-state voltage	$I_{O(PG)}$ = 500 µA, V_{CC} = 2.7 V to 5.5 V			0.3	V
Off-state voltage	$I_{O(PG)}$ = −500µA, V_{CC} = 2.7 V to 5.5 V	V_{CC} −0.3			V
Hysteresis			130		mV

power good (PGP)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input impedance		85			kΩ

undervoltage lockout (UVLO + UVDLO)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start threshold voltage	V_{CC} increasing	2.4		2.7	V
Hysteresis			130		mV

supply current (I_{CC} and I_{DD})

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Standby mode	$\overline{EN}$ = V_{CC}		1	10	µA
Undervoltage lockout	V_{CC} = V_{DD} < 2.3 V		35	50	µA
Operating mode	No load		300	500	µA

PARAMETER MEASUREMENT INFORMATION

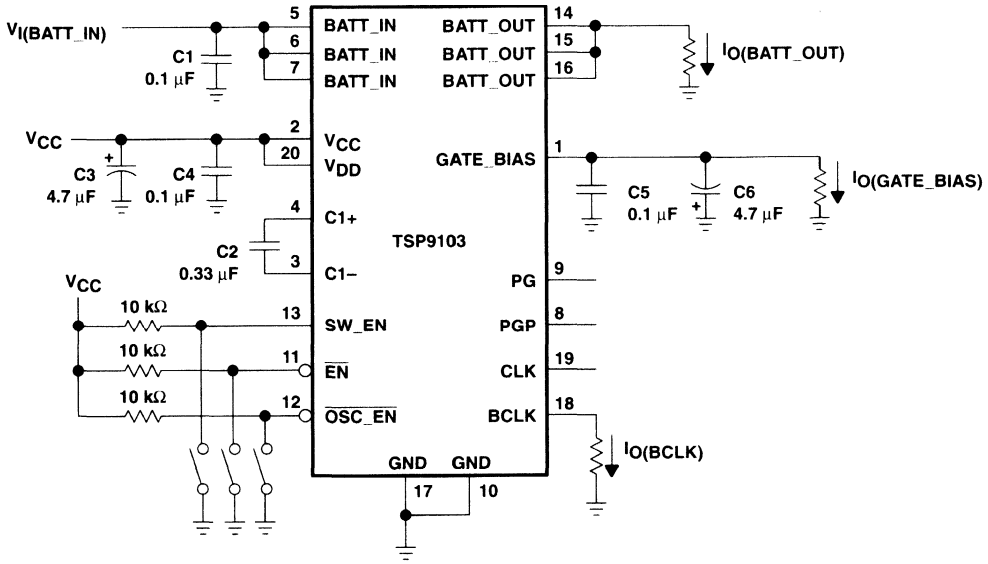


Figure 2. Test Circuit

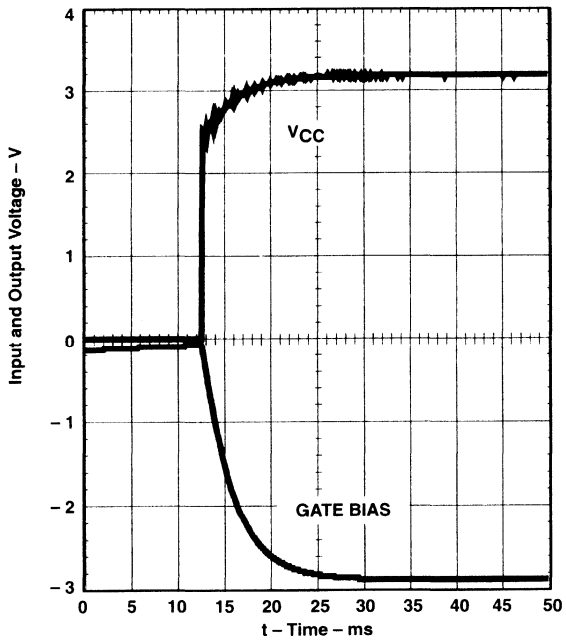


Figure 3. GATE_BIAS Output Voltage Rise Time

PARAMETER MEASUREMENT INFORMATION

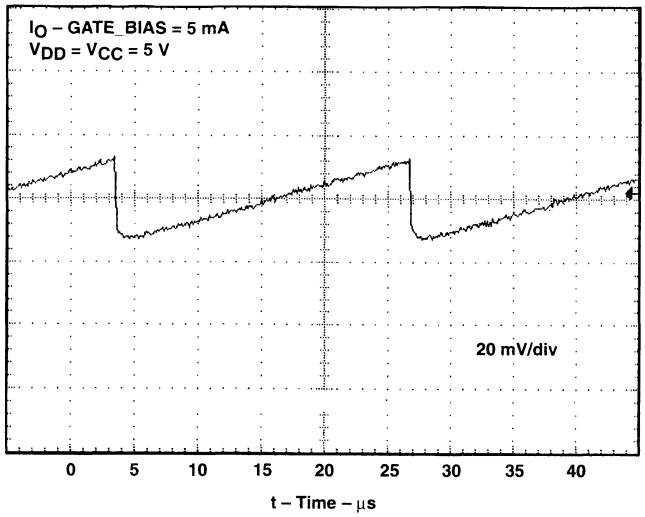


Figure 4. Ripple on GATE_BIAS

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

			FIGURE
$r_{DS(on)}$	Static drain-source on-state resistance	vs Gate-source voltage, dc	5
		vs Temperature	6
F_{osc}	Oscillator frequency	vs Supply voltage	7
		vs Temperature	8
V_O	Output voltage	vs Output current	9
		vs CLK frequency	10
V_{IT}	Threshold voltage	vs Temperature	11
	Supply current (I_{CC} + I_{DD})	vs Supply voltage	12
		vs Temperature	13

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs GATE-SOURCE VOLTAGE, dc ($V_{O(GATE\_BIAS)} - V_{I(BATT\_IN)}$)

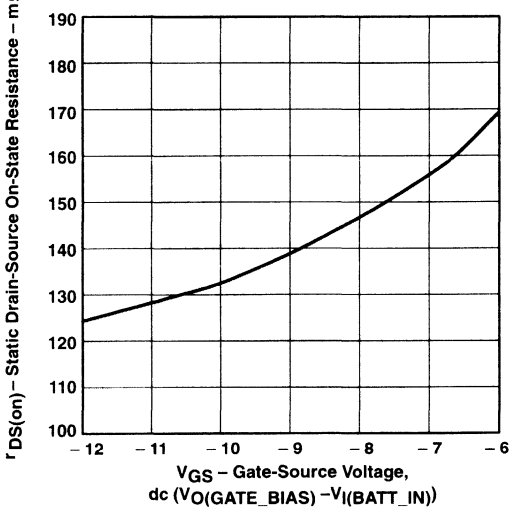


Figure 5

HIGH-SIDE SWITCH STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs TEMPERATURE

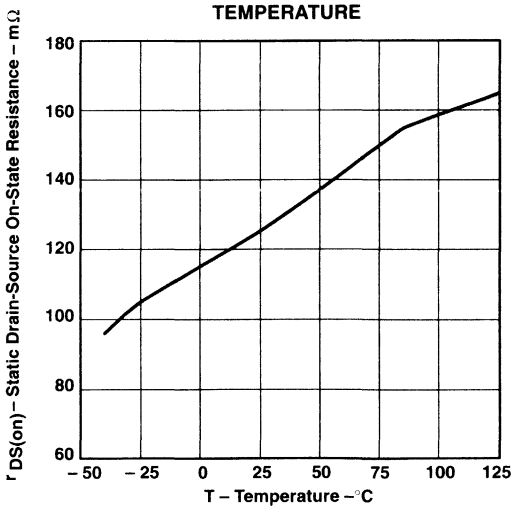


Figure 6

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY
vs
SUPPLY VOLTAGE

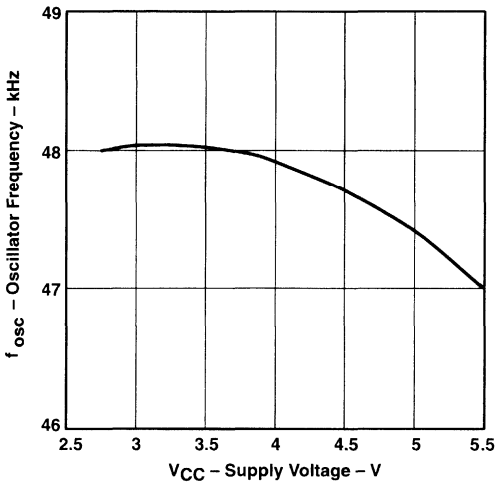


Figure 7

OSCILLATOR FREQUENCY
vs
TEMPERATURE

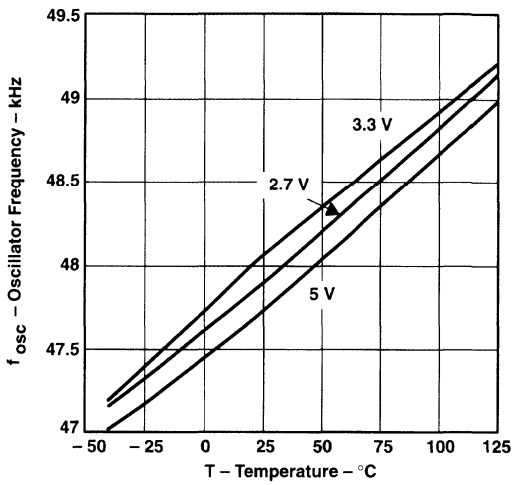


Figure 8

GATE BIAS
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

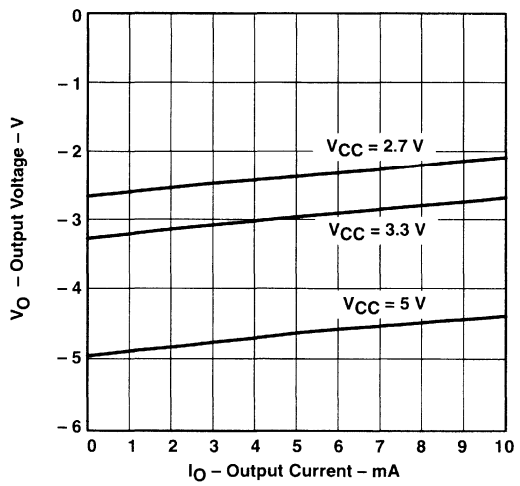


Figure 9

GATE BIAS
OUTPUT VOLTAGE
vs
CLK FREQUENCY

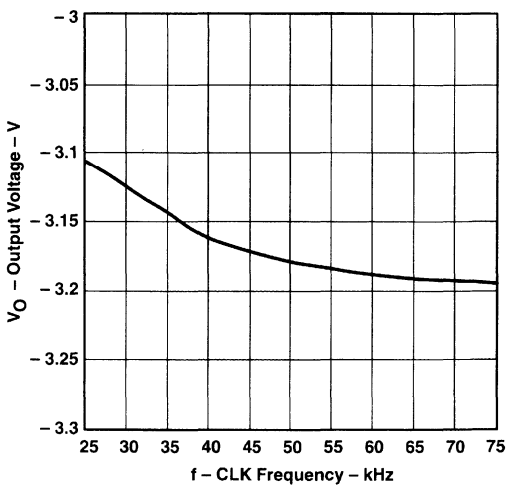


Figure 10

TYPICAL CHARACTERISTICS

UNDERVOLTAGE LOCKOUT (V_{CC}, V_{DD})
THRESHOLD VOLTAGE
vs
TEMPERATURE

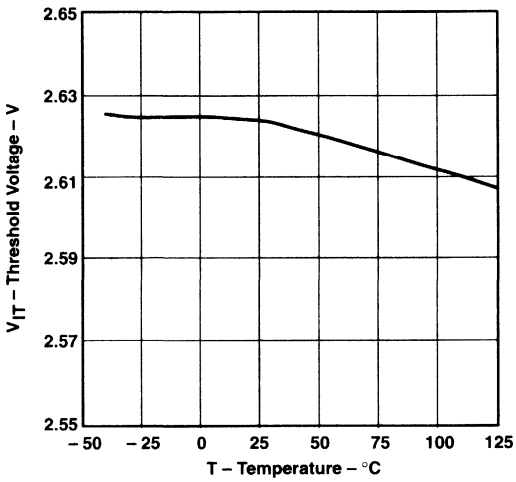


Figure 11

SUPPLY CURRENT (I_{CC} + I_{DD})
vs
SUPPLY VOLTAGE

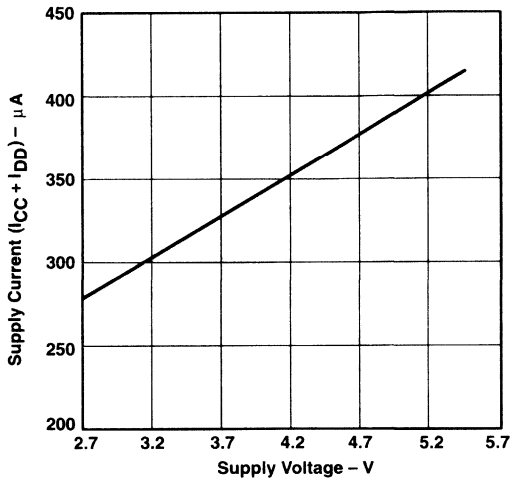


Figure 12

SUPPLY CURRENT (I_{CC} + I_{DD})
vs
TEMPERATURE

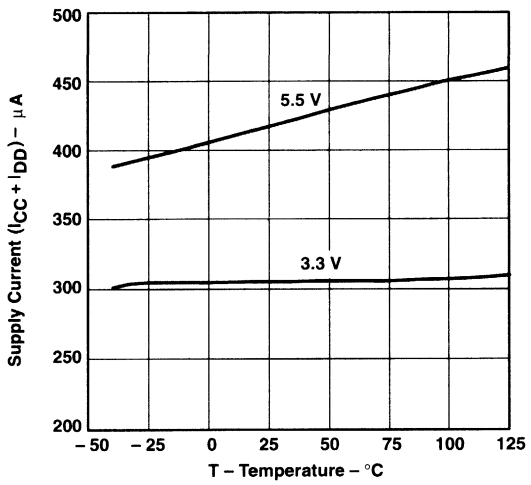


Figure 13

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch packages requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power-dissipation capability of the PWB design
- Improving the thermal coupling of the component to the PWB
- Introducing airflow in to the system

Using the given $R_{\theta JA}$ for this IC, the maximum power dissipation can be calculated with the equation:

$$P_D max = \frac{T_J max - T_A}{R_{\theta JA}}$$

For the TPS9103, the power dissipation is in the PMOSFET. To calculate the power, use: $I^2 \times R$ where I is the current through the device and R is the internal resistance as shown in the electrical characteristics table.

For a V_I of 6 V, the resistance at 85°C is 0.210 Ω. At a current of 2 A, the peak power dissipation is:

$$P_D = 2^2 \times 0.210 = 0.84 \text{ W}$$

Assuming a duty cycle of 1/8 or 0.125, the average power is:

$$0.84 \text{ W} \times 0.125 = 0.105 \text{ W}$$

The change in temperature is:

$$\Delta T = 0.105 \text{ W} \times 154°C/W = 16.2°C$$

and the junction temperature is:

$$T_J = 85°C + 16.2°C = 101.2°C$$

APPLICATION INFORMATION

introduction

Traditionally the RF power amplifier (PA) is powered directly from the battery, with a switching arrangement for powering down when not in use. GaAs FET PAs require a negative bias voltage that must be present before the supply is connected, or there is risk of destroying the FET. Logic must be provided to ensure the presence of the negative bias voltage.

A secondary charge pump is necessary for systems in which the supply voltage is insufficiently high – the negative bias produced from the charge pump is inadequate. In mobile telephony a second charge pump (regulated or unregulated) may also be needed, e.g. for varicap diodes/VCOs and some preamplifiers. The need for larger dynamic range or control-voltage range can become critical in certain applications.

the TPS9103 approach

The TPS9103 integrates a P-channel MOSFET high-side switch together with a selectable oscillator and charge pump for the GaAs FET power-amplifier gate bias, which is monitored.

Complete precautions are taken to ensure that the PA supply is not enabled unless the gate bias is present while V_{CC} and V_{DD} are also good. This protects the PA from inadvertent damage–without a major system size/cost increase.

The bias regulation monitor is flexible, accommodating both fixed and programmable approaches. The fixed resistors, provided internally, set the trip voltage to $-0.6 \times V_{DD}$. If V_{DD} is 5 V, then the trip voltage is –3 V. Should another value be preferred, it can be set by applying voltage divider to PGP. See the section "dimensioning the external voltage divider" for more details.

The charge pump clock is also flexible. The on-chip oscillator runs at a nominal 50 kHz, or alternatively an external oscillator can be connected to CLK. When an external clock is used, $\overline{\text{OSC\_EN}}$ should be taken high to disable the oscillator. When $\overline{\text{OSC\_EN}}$ is low and the on-chip oscillator is used, CLK provides an unbuffered clock output.

The circuit provides for a secondary charge pump driver. The buffered BCLK output can be used (with four external components) to provide a higher supply, both for those system functions that require it and for those GaAs PAs that need a more negative bias than is made possible by inverting the existing supply. This is facilitated by use of single-cell Li-ion batteries.

Figure 14 shows the TPS9103 in a typical application.

APPLICATION INFORMATION

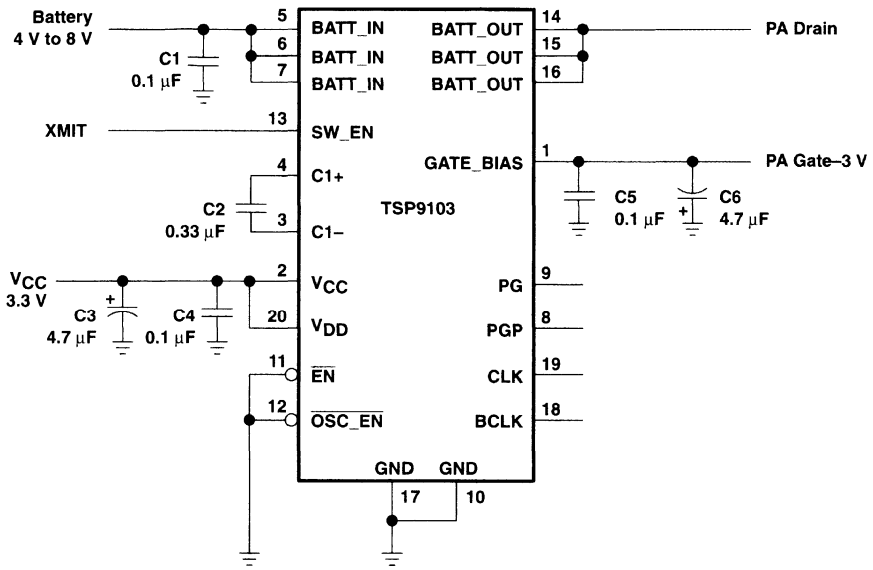


Figure 14. Typical Application

APPLICATION INFORMATION

capacitors of the internal inverting charge pump (see Figure 15)

This charge pump inverts the voltage at V_{DD} and provides a negative output voltage at GATE_BIAS.

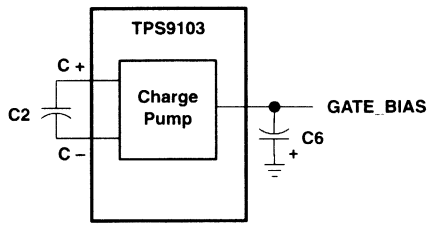


Figure 15. Internal Inverting Charge Pump

The output capacitor C6 limits the voltage ripple at GATE_BIAS:

$$V_{Ripple} = \frac{I_{O(GATE\_BIAS)}}{C6 \times f}$$

With a capacitor C6 of 4.7 μF and an output current of 10 mA, the voltage ripple at GATE_BIAS is 42 mV.

The capacitor C2 can be calculated using an equivalent resistance method:

$$R_{equivalent} = \frac{1}{C2 \times f}$$

Using 0.33 μF for C2, the equivalent resistance is:

$$R_{equivalent} = \frac{1}{0.33\ \mu F \times 50\ kHz} = 60.6\ \Omega$$

Add the internal resistance of the switches (35 Ω) to get a total resistance seen by the current:

$$R_{TOTAL} = 60 + 35 = 95\ \Omega$$

With a total resistance of 95 Ω and 10 mA flowing through it, a voltage drop of 0.95 V occurs. With 5 V on V_{DD}, the output is –4.05 V with a 42 mV ripple.

The capacitors should have a low equivalent series resistance (ESR) to maintain low ripple and low noise. Careful layout is required. In most instances it is advisable to add a small decoupling capacitor C5 close to the GATE_BIAS. An additional 0.1-μF capacitor at other locations may be necessary if the power amplifier is located away from the TPS9103.

APPLICATION INFORMATION

dimensioning of the external charge pump

For systems in which the bias voltage requirement is not met by inverting the power rail, the BCLK output can be used (with four passive components) to generate a higher V_{DD}. The higher voltage is then inverted as before to produce the bias voltage. This voltage is also available for other parts of the main circuitry (see Figure 16).

With the TPS9103, an external charge pump could be used to increase the voltage at V_{DD}, thereby deriving a higher negative voltage at GATE_BIAS than would otherwise be available.

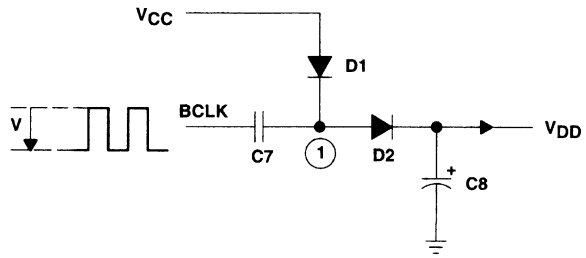


Figure 16. External Charge Pump

When BCLK is low, node 1 charges up to $V_{CC} - V_{diode}$. When BCLK goes high, node 1 is $2\ V_{CC} - V_{diode}$. The capacitor C8 charges up to $2\ V_{CC} - 2\ V_{diode}$. This voltage can then be connected to V_{DD}.

The magnitude of V_{ripple} of V_{DD} is determined by the value of C8. Capacitor value must be large enough that the discharge during one period is not as great as the maximum voltage variation allowable. The discharge of C8 depends on the load current.

$$C8 = \frac{I_{O(GATE\_BIAS)}}{V_{ripple} \times f}$$

With a supply voltage of V_{CC} = 3.3 V, a maximum voltage variation (V_{ripple}) of 2% = 66 mV and a load of I_{CC} = 10 mA, the value of C8 is 3 µF. A 4.7 µF meets this requirement.

The capacitance of C7 can be calculated using an equivalent resistance method:

$$R_{equivalent} = \frac{1}{C7 \times f}$$

Using 0.22 µF for C7, the equivalent resistance is:

$$R_{equivalent} = \frac{1}{0.22\ \mu F \times 50\ kHz} = 90\,\Omega$$

Add the equivalent resistance to the internal resistance of the switch (10 Ω):

$$R_{TOTAL} = 90 + 10 = 100\ \Omega$$

With a total resistance of 100 Ω and with 10 mA flowing through it, a voltage drop of 1 V occurs. Thus with 3.3 V on V_{CC} the output is 4.2 V with a 42-mV ripple.

Care must be taken that the maximum voltages are not exceeded when using BCLK as a charge pump (see Figure 17).

APPLICATION INFORMATION

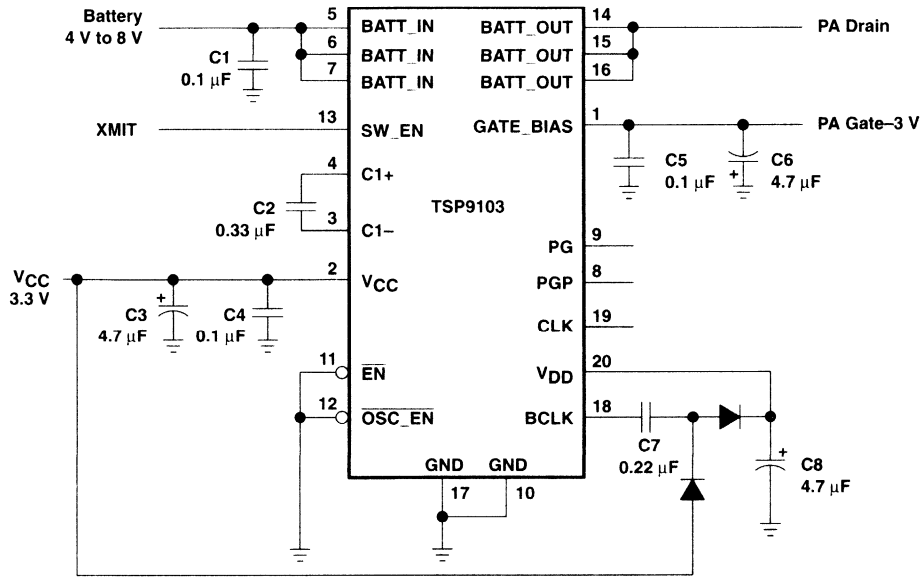


Figure 17. TPS9103 Configured With External Charge Pump

dimensioning the external voltage divider

Drain voltage should only be applied to the power amplifier when the complete negative voltage from the GATE_BIAS output is provided to the gate of the GaAs power amplifier. For that reason there is an internal voltage divider R/0.6R and a PG comparator in the TPS9103 (see Figure 15). When the voltage at the inverting input of the comparator reaches zero, the output goes high and the high-side MOSFET switches on, provided a SW_EN high signal is applied. For example, when the supply voltage at V_{DD} is 5 V, the high-side switch is switched on when the voltage at GATE_BIAS reaches –3 V.

This trip point can be changed to another value by using an external voltage divider connected between V_{DD}, GATE_BIAS, and PGP. The resistor values should be low enough to minimize the error that is present when the internal resistor values (typ R = 100 kΩ ± 30%) are taken into consideration. Therefore, the external resistor values, R1 and R2, are chosen within the 10-kΩ range.

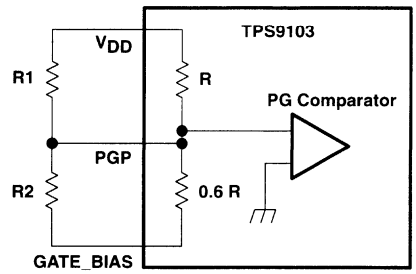


Figure 18. External Voltage Divider for Setting the Trip Point

R1 = 10 kΩ. The value of R2 can then be calculated using:

$$R2 = \frac{-0.6 \times R \times R1 \times V_{trip}}{0.6 \times V_{DD} \times [R1 + R] + V_{trip} \times R1}$$

where V_{DD} = supply voltage, and V_{trip} = chosen value to trip PG comparator.

The values of the internal resistor can vary about 30%, and can move the trip point. In a worst-case condition, with a resistor variation of 30%, the shifting of the trip point can be calculated to:

$$\Delta V_{trip\_point} = V_{DD} \times \left(\frac{R1 + 1.3 \times R}{R1} \times \frac{0.6 \times R2}{R2 + 0.78 \times R} - \frac{R1 + R}{R1} \times \frac{0.6 \times R2}{R2 + 0.6 \times R} \right)$$

8 Baseband Interface Circuits

TCM4300
ADVANCED RF CELLULAR TELEPHONE INTERFACE CIRCUIT (ARCTIC™)

SLWS010E – DECEMBER 1994 – REVISED JUNE 1996

- **Compliance With TIA IS-54B Dual-Mode Cellular Standard**
- **Baseband Transmit Digital-to-Analog (D/A) Conversion and Receive Analog-to-Digital (A/D) Conversion in Analog Transmit Mode Using Dual 10-Bit Sigma-Delta Converters**
- **Square Root Raised Cosine (SQRC) Filtering in the Digital Mode Using Dual 10-Bit Sigma-Delta Converters**
- **π/4-Differential Quadrature Phase-Shift Key (DQPSK) Modulation Encoder in Digital Transmit Mode**
- **Power Control Supervision for Radio Frequency (RF) Power Amplifier, Automatic Frequency Control (AFC), Automatic Gain Control (AGC), and Synthesizer**
- **Received Signal Strength Indicator (RSSI) and Battery-Level A/D Conversion Circuitry**
- **Internal Clock Generation**
- **Wide-Band Data Clock Recovery and Manchester Decoding**
- **General-Purpose Digital Signal Processor (DSP) and Microcontroller Interface**
- **3.3-V and 5-V Operation**
- **Low Power Consumption**

description

Texas Instruments (TI™) TCM4300 IS-54B advanced RF cellular telephone interface circuit (ARCTIC) provides a baseband interface between digital signal processor (DSP), microcontroller, and RF modulator/demodulator in a dual-mode IS-54B cellular telephone.

In the analog mode, the TCM4300 provides all required baseband filtering as well as transmit D/A conversion and receive A/D conversion using dual 10-bit sigma-delta converters. In addition, a WBD (wide-band data) –10 kb/s Manchester frequency shift key (FSK) demodulator is provided to allow reduced DSP processing load during subscriber standby mode.

In the digital mode, the TCM4300 accepts I and Q baseband data and performs A/D and D/A conversion and square root raised cosine filtering using dual 10-bit sigma-delta converters. The TCM4300 also has a π/4-DQPSK modulation encoder for dibit-to-symbol conversion in the digital transmit mode.

The microcontroller interface is compatible with a wide range of microcontrollers. A microcontroller can be used to communicate with the user interface (keyboard, display, etc.) and to program up to three frequency synthesizers by using the on-chip synthesizer interface circuit.

The TCM4300 provides advanced power control to minimize the power consumption of many dual-mode telephone functional blocks such as the speech codec, FM receiver, I and Q demodulator, transmitter signal processor, and RF power amplifier. In addition, the TCM4300 is designed to reduce system power consumption through low-voltage operation and standby mode (see Table 1).

The TCM4300 is offered in the 100-pin PZ package and is characterized for free-air operation from –40°C to 85°C.

PRODUCT PREVIEW

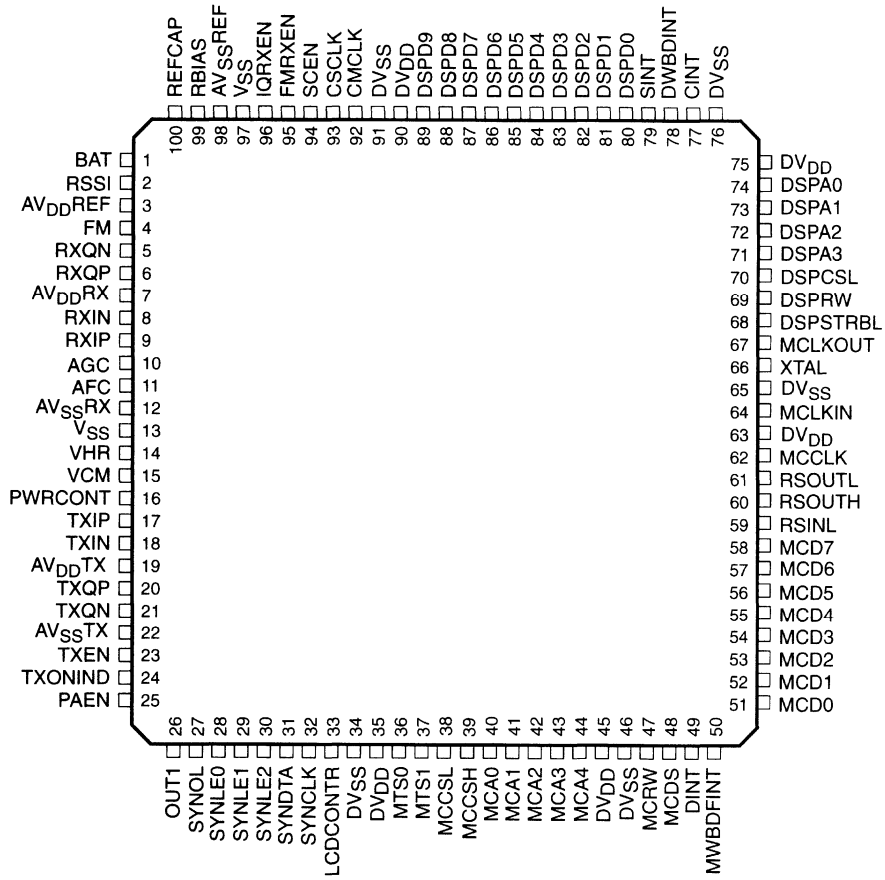
NOTE: The data provided in this Product Preview is for the prototype version of the TCM4300.

description (continued)

Table 1. Typical Power Consumption

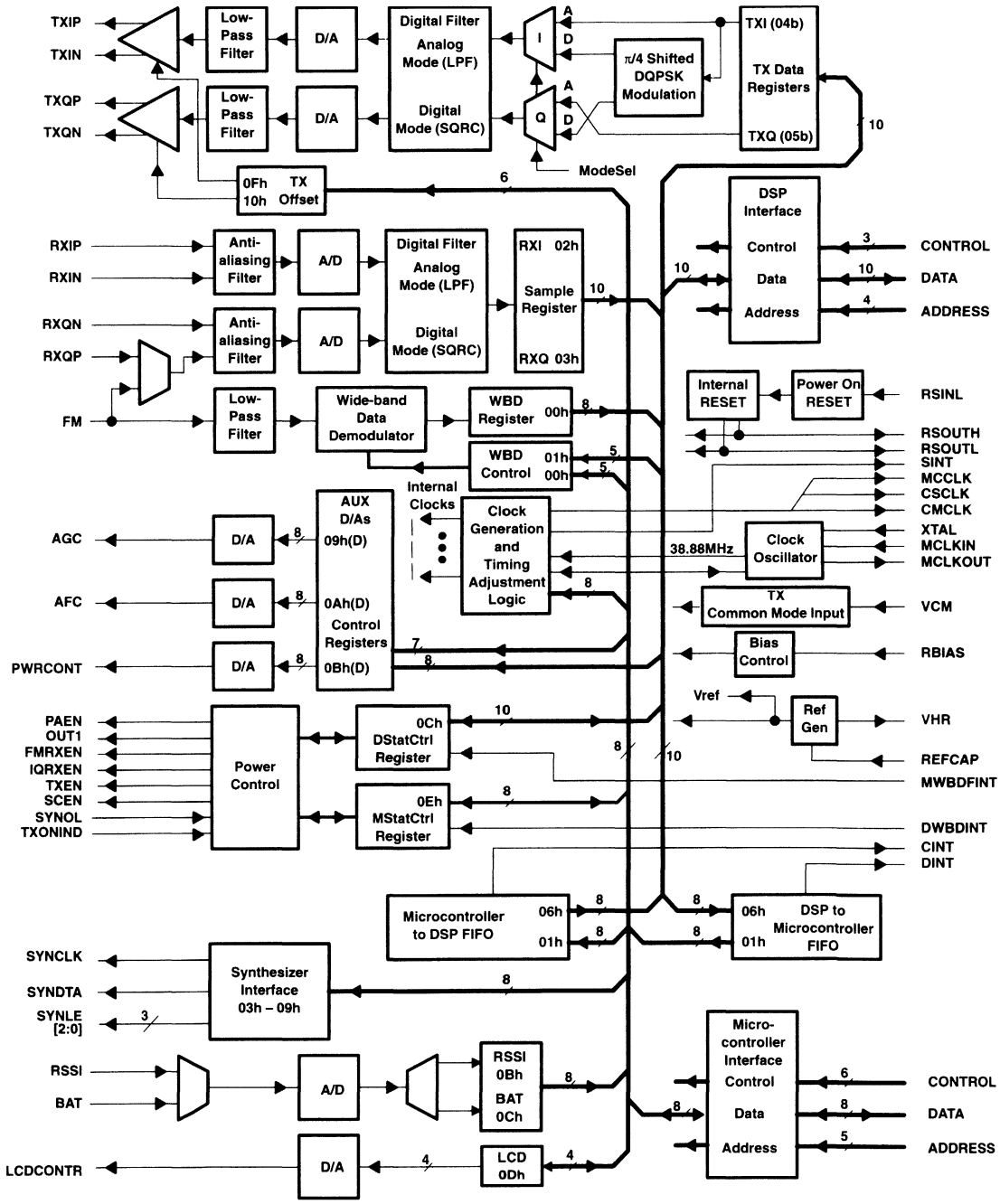
OPERATING MODE		3 V	5.5 V
Analog transmitting and receiving		75 mW	275 mW
Digital receiving		60 mW	250 mW
Digital transmitting		85 mW	300 mW
Idle mode	MCLKOUT enabled	45 mW	190 mW
	MCLKOUT disabled	17 mW	96 mW
Digital mode, 1/3 transmitting + 1/3 receiving +1/3 standby		60 mW	220 mW

PZ PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

functional block diagram



PRODUCT PREVIEW

Terminal Functions

RF interface analog signals

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
RECEIVE CHANNEL			
FM	4	I	Input from FM discriminator analog mode voice and wide-band data
RXIN	8	I	In-phase differential negative baseband received signal
RXIP	9	I	In-phase differential positive baseband received signal
RXQN	5	I	Quadrature differential negative baseband received signal
RXQP	6	I	Quadrature differential positive baseband received signal
TRANSMIT CHANNEL			
TXIN	18	O	In-phase differential negative baseband transmit signal
TXIP	17	O	In-phase differential positive baseband transmit signal
TXQN	21	O	Quadrature differential negative baseband transmit signal
TXQP	20	O	Quadrature differential positive baseband transmit signal
MONITORS			
BAT	1	I	Battery strength monitor
RSSI	2	I	Received signal strength indicator. Used for signal strength measurements
CONTROLS			
AGC	10	O	Automatic gain control digital-to-analog converter (DAC) output
AFC	11	O	Automatic frequency control DAC output
LCDCONTR	33	O	Liquid-crystal display (LCD) contrast control DAC output
PWRCONT	16	O	Power amplifier (PA) power control DAC output
BIAS SETTING			
RBIAS	99	I	Input for bias current-setting resistor. A 100 kΩ, 1% tolerance resistor to AV_{SS} is recommended.
REFCAP	100	I	Input for reference decoupling capacitor. 3.3 μF in parallel with 470 pF is recommended.

RF interface digital signals

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
POWER AMPLIFIER, SYNTHESIZER, AND TRANSMIT CONTROLS			
PAEN	25	O	Power enable for the transmit power amplifier, active high
OUT1	26	O	User-defined general purpose data or control signal
SYNCLK	32	O	Synthesizer serial-data clock
SYNDTA	31	O	Synthesizer serial-data bit
SYNLE0	28	O	Synthesizer 0, 1, and 2 latch enables. An active high indicates the latch is enabled.
SYNLE1	29	O	
SYNLE2	30	O	
SYNOL	27	I	Synthesizer out-of-lock indicator. Active high indicates out of lock.
TXEN	23	O	Power enable signal. Enables transmit signal processing, active high
TXONIND	24	I	Transmit on indicator. Signal indicating power is applied to the power amplifier.

PRODUCT PREVIEW

Terminal Functions (Continued)

miscellaneous digital signals

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
RSINL	59	I	Reset input, active low
RSOUTH	60	O	Power on reset output, active high. At powerup, RSOUTH goes high for 10 ms.
RSOUTL	61	O	Power on reset output, active low. At powerup, RSOUTL goes low for 10 ms causing an internal reset of the TCM4300.
CLOCKS			
CMCLK	92	O	Codec master clock. 2.048-MHz clock is provided as master clock and bit clock for speech codec.
CSCLK	93	O	Codec sample clock. 8-kHz frame synchronization pulse for speech codec. Connected to DSP for speech sample interrupts.
MCCLK	62	O	Microcontroller clock. Adjustable frequency with 1.215 MHz at powerup.
MCLKIN	64	I	Master clock input. Frequency 38.88 MHz ±100 ppm. A crystal can be connected between MCLKIN and XTAL to provide an oscillator circuit. Alternately, XTAL can be left open and an external TTL/CMOS-level clock signal can be connected to MCLKIN.
MCLKOUT	67	O	Buffered version of MCLKIN
XTAL	66	I	Use with MCLKIN to form an oscillator circuit.
POWER ENABLES			
FMRXEN	95	O	Power enable for receiver FM path, active high
IQRXEN	96	O	Power enable for receiver I/Q path, active high
SCEN	94	O	Power enable for speech codec, active high

DSP interface

TERMINAL NAME	TERMINAL NO.	I/O/Z	DESCRIPTION
CINT	77	O	Controller data interrupt. Microcontroller data interrupt (active low) sent to DSP. Caused by the microcontroller writing into the Send-C Int register location
DSPA0	74	I	DSP 4-bit parallel address bus. DSPA3 is the MSB, and DSPA0 is the LSB.
DSPA1	73		
DSPA2	72		
DSPA3	71		
DSPCSL	70	I	DSP interface chip select signal, active low
DSPD0	80	I/O/Z	DSP 10-bit parallel data bus. DSPD9 is the MSB, and DSPD0 is the LSB.
DSPD1	81		
DSPD2	82		
DSPD3	83		
DSPD4	84		
DSPD5	85		
DSPD6	86		
DSPD7	87		
DSPD8	88		
DSPD9	89		
DSPRW	69	I	DSP read/write signal. DSPRW is active high for read cycles and active low for write cycles.
DSPSTRBL	68	I	DSP strobe signal, active low
DWBDINT	78	O	DSP wide-band data interrupt. Wide-band data-ready interrupt (active low) caused by WBD demodulation circuits.
SINT	79	O	Sample interrupt (active low). Operates at 40 kHz in the analog mode and 48.6 kHz in the digital mode.

Terminal Functions (Continued)

microcontroller interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
DINT	49	O	Microcontroller interrupt request signal. DSP data-ready interrupt sent to controller. Caused by DSP writing to SEND DINT register location. DINT can be active high or low according to the levels of the microcontroller type select (MTS) (1:0) signals.
MCA0	40	I	Microcontroller 5-bit parallel address bus. MCA4 is the MSB, and MCA0 is the LSB.
MCA1	41		
MCA2	42		
MCA3	43		
MCA4	44		
MCCSH	39	I	Microcontroller interface chip-select signal, active high. Chip select occurs if MCCSH is high and MCCSL is low.
MCCSL	38	I	Microcontroller interface chip-select signal, active low. Chip select occurs if MCCSH is high and MCCSL is low.
MCD0	51	I/O/Z	Microcontroller 8-bit parallel data bus. MCD7 is the MSB, and MCD0 is the LSB.
MCD1	52		
MCD2	53		
MCD3	54		
MCD4	55		
MCD5	56		
MCD6	57		
MCD7	58		
MCDS	48	I	Microcontroller data strobe. Operational characteristics are selected by MTS (1:0).
MCRW	47	I	Microcontroller read/write. Operational characteristics are selected by MTS (1:0).
MTS0	36	I	Microcontroller type select configuration control inputs. The interface is controlled by MTS (1:0) as follows: 00 – Intel™ microcontroller interface characteristics 10 – Mitsubishi™ microcontroller and Motorola microcontroller 16-bit bus interface characteristics 01 – Motorola™ microcontroller 8-bit bus characteristics 11 – Reserved
MTS1	37	I	
MWBDFINT	50	O	Microcontroller interrupt request signal. Wide-band data-ready interrupt caused by WBD demodulator in analog mode or frame interrupt sent by the DSP in digital mode. MWDBFINT can be active high or low, according to the levels of the MTS (1:0) signals.

PRODUCT PREVIEW

Intel is a trademark of Intel Systems, Inc.
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Motorola is a trademark of Motorola Inc.

Terminal Functions (Continued)

supply and reference voltages

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$AV_{DD}RX$	7	—	Analog supply voltage for RX receive path
$AV_{DD}REF$	3	—	Analog supply voltage for RX FM receive path
$AV_{DD}TX$	19	—	Analog supply voltage for TX transmit path
$AV_{SS}REF$	98	—	Analog ground for REFCAP
$AV_{SS}RX$	12	—	Analog ground for RX receive path
$AV_{SS}TX$	22	—	Analog ground for TX transmit path
DV_{DD}	35, 45, 63, 75, 90	—	Digital power supply. All supply pins must be connected.
DV_{SS}	34, 46, 65, 76, 91	—	Digital ground. All supply pins must be connected.
VCM	15	I	Voltage common mode. VCM is used to establish dc operating point for TX outputs and can be tied to VHR.
VHR	14	O	Half-rail reference voltage (VHR), approximately $0.5 \times AV_{DD}$. VHR is used to establish dc operating point for RX inputs.
V_{SS}	13, 97	—	Substrate ground

detailed description

data transfer

The interface to both the system digital signal processor and microcontroller is in the form of 2s complement.

receive section

The mode of operation is determined by the state of the MODE, FMVOX, IQRXEN, and FMRXEN bits of the DStatCtrl register, as shown in Table 2. The specifications for the receive section are included in Table 3.

Table 2. TCM4300 Receive Channel Control Signals

CONTROL SIGNAL	ANALOG MODE	DIGITAL MODE
MODE	0	1
FMVOX	1	0
IQRXEN	0	1
FMRXEN	1	0

In the digital mode (MODE=1), the receive section accepts RXIP, RXIN, RXQP, and RXQN analog inputs. These inputs are passed to continuous-time antialiasing filters (AAF), baseband filtering, and A/D conversion blocks, and then to sample registers where 10-bit registers can be read. The sample rate is 48.6 ksps.

In the analog mode (MODE = 0), the FMVOX bit of the DStatCtrl register enables or disables the Q side of the receiver channel, and the FMRXEN bit controls the external functions. In the digital mode, IQRXEN enables both the I and Q receive channels and external functions as well.

To save power, the receive I and Q channels are enabled separately. This operation occurs because in the analog mode, only the Q channel is used. When the FMVOX bit is set to 1, it controls the input multiplexer, connects the FM input to the receiver RXQP signal, and connects the RXQN signal to VHR. When the MODE control bit and the IQRXEN control bit are set to 1, both sides of the receive channel are enabled for use in the digital mode.

PRODUCT PREVIEW

receive section (continued)

The input signals RXIP, RXIN and RXQP, RXQN are differential pair signals. Differential signals are used to minimize the pickup of interference, ground, and supply noise, while maintaining a larger signal level. In single-ended applications, the unused RXIN and RXQN terminals must be connected to VHR or to an externally supplied bias voltage, and the input signal level must be adjusted in the RF circuitry to provide a higher level signal so that the digital output codes are properly calibrated (0.5 V peak-to-peak corresponds to full-scale digital output). In the analog mode, the RXQN input is internally referenced to VHR. Alternatively, the unused inputs can be connected to VHR and the used inputs can be capacitively coupled. Note that when the RX and FM inputs are capacitively coupled, the input pins to the TCM4300 are self-biased to VHR; no external bias is needed at the input pins.

The single-ended output of an external FM discriminator is connected to the FM pin for analog mode voice and WBD reception. The signal at this pin is conveyed to the Q side of the receiver via the multiplexer, and the other Q input is connected internally to the VHR reference voltage. The I input of the RX circuitry is disabled in the analog mode. The FM signal passes through the antialiasing filter, as specified in Table 4, before passing through the A/D converter. The signal at the FM pin is also routed directly to the WBD demodulator through a low-pass filter (LPF) with the –3 dB point at 270 kHz.

The VHR can provide a bias voltage for the received inputs when capacitively coupled from the RF section. To meet noise requirements, the VHR output should have an external decoupling capacitor connected to ground. The VHR output buffer is enabled by the OR of TXEN, FMVOX, and IQRXEN. The VHR output is high impedance otherwise.

In the digital mode, both the I and Q receive sides are enabled. Table 5 lists the receive channel frequency response.

When the I and Q sample conversion is complete and the data is placed in the RXI and RXQ sample registers, the SINT interrupt line is asserted to indicate the presence of that data. This occurs at 48.6-kHz rate in the digital mode and at 40-kHz rate in the analog mode. In the analog mode, only the RXQ conversion path is used, and the RXI path is powered down.

Table 3. RXIP, RXIN, RXQP, and RXQN Inputs (AV_{DD} = 3 V, 4.5 V, 5 V)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Common-mode input voltage range			0.3		AV_{DD}–0.3	V
Input voltage for full-scale digital output	Differential			0.5		Vp-p
	Single-ended			0.5		
Nominal operating level	Differential			0.125		Vp-p. Provides 12 dB headroom for AGC fading conditions.
	Single-ended			0.125		
Input CMRR (RXI, RXQ)			45			dB
Sampling frequency, SINT				48.6/40		Digital/Analog kHz
Receive error vector magnitude (EVM)				6%	7%	
I/Q sample timing skew		Input signal 0 – 15 kHz		50		ns
A/D resolution				10		Bits
Signal to noise-plus distortion		Input at full scale – 1 dB	50	56		dB
Integral nonlinearity		0 dB to –60 dB input		1		LSB
Gain error (I or Q channel)					±10%	
Gain mismatch between I and Q					±0.3	dB
Differential dc offset voltage					±30	mV
FM input sensitivity				2.5		Vp-p for full scale (±14 kHz deviation)
FM input dc offset (wrt VHR)					±90	mV
FM input idle channel noise					–45	dB below full scale input
FM gain error					±7%	
Power supply rejection		f = 0 kHz to 15 kHz		40		dB

PRODUCT PREVIEW

receive section (continued)

Table 4. RX Channel Frequency Response (FM Input in Analog Mode)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Frequency response	2.5 V peak-to-peak,	0 kHz to 6 kHz (see Note 1)			±0.5	dB
	2.5 V peak-to-peak,	20 kHz to 30 kHz (see Note 2)	−18			
	2.5 V peak-to-peak,	34 kHz to 46 kHz (see Note 3)	−48			
Peak-to-peak group delay distortion	2.5 V peak-to-peak,	0 kHz to 6 kHz			2	µs
Absolute channel delay	2.5 V peak-to-peak,	0 kHz to 6 kHz		400		µs

NOTES: 1. Ripple magnitude
2. Stopband
3. Stopband and multiples of stopband

Table 5. RX Channel Frequency Response (RXI, RXQ Input in Digital Mode)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Frequency response	0.125 V peak-to-peak,	0 kHz to 8 kHz (see Note 4)		±0.5	±0.75	dB
	0.125 V peak-to-peak,	8 kHz to 15 kHz (see Note 4)			±1	
	0.125 V peak-to-peak,	16.2 kHz to 18 kHz (see Note 5)	−26			
	0.125 V peak-to-peak,	18 kHz to 45 kHz (see Note 5)	−30			
	0.125 V peak-to-peak,	45 kHz to 75 kHz (see Note 5)	−46			
	0.125 V peak-to-peak,	> 75 kHz	−60			
Peak-to-peak group delay distortion	0.125 V peak-to-peak,	0 kHz to 15 kHz			2	µs
Absolute channel delay, RXI, Q IN to digital OUT	0.125 V peak-to-peak,	0 kHz to 15 kHz		325		µs

NOTES: 4. Deviation from ideal 0.35 SQRC response
5. Stopband

transmit section

The transmit section operates in two distinct modes, digital or analog. The mode of operation is determined by the MODE bit of the DStatCtrl register. In the digital mode, data is input to the transmit section by writing to the TXI register. The resulting output is a $\pi/4$ DQPSK-modulated time division multiplexed (TDM) burst. In the analog mode, the data is in the form of direct I and Q samples which are written to both the TXI and TXQ registers, then D/A converted, filtered, and output through TXIP, TXIN, TXQP, and TXQN. The I and Q outputs are zero-IF FM signals; that is, no baseband connection is necessary for FM transmission.

In the digital mode (MODE=1), the data is written to the TXI register using the SINT interrupt to synchronize the data transfer. The TCM4300 performs parallel-to-serial conversion of the bits in the TXI register and encodes the resulting bit stream as $\pi/4$ DQPSK data samples. These samples are then filtered by a digital square root raised cosine (SQRC) shaping filter with a roll-off rate of $\alpha = 0.35$ and converted to sampled analog form by two 9-bit digital-to-analog converters (DACs). The output of the DAC is then filtered by a continuous-time resistance-capacitance (RC) filter.

The TCM4300 generates a power amplifier (PA) control signal, PAEN, to enable the power supply for the PA. The start and stop times of the TDM burst are controlled by writing to a single bit, TXGO, in the DSP DStatCtrl register.

In the analog mode (MODE = 0), the DSP writes 8-bit I and Q samples into the TXI and TXQ data registers at a 40-ksps rate. These writes are timed by the SINT interrupt signal. The samples are fed to a low-pass filter before D/A conversion. In the transmit analog mode, the PAEN signal is always set to 1.

The transmitter section provides differential I and Q outputs for both analog and digital modes. The differential dc offset for the TXI and TXQ outputs can be independently adjusted using the TX offset registers.

PRODUCT PREVIEW

transmit section (continued)

Table 6. Transmit I and Q Channel Outputs

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Peak output voltage full scale, centered at VCM	Differential		2.24		Vp
	Single-ended		1.12		
Nominal output-level (constellation radius) centered at VCM	Differential		1.5		V
	Single-ended		0.75		
Low-level drift			±200		PPM/°C
Transmit error vector magnitude (EVM)			3%	4%	
Resolution			8		bits
S/(N+D) ratio at differential outputs		40	48		dB
Gain error (I or Q channel)			±10%	±15%	
Gain mismatch between I and Q				±0.3	dB
Gain sampling mismatch between I and Q			20		ns
Zero code error differential				±90	mV
Zero code error, each output, with respect to VCM				±90	mV
Zero code error, I to Q, with respect to other channel (differential or single-ended)				±10	mV
Load impedance, between P and N pins		10			kΩ
Load capacitance				50	pF
VCM input voltage range		1.3		$AV_{DD}-1.3$	V
Transmit offset DACs I and Q resolution			6		bits
Transmit offset DACs I and Q average step size		3	3.4	3.9	mV
Transmit offset DACs I and Q full-scale positive output			105.4		mV
Transmit offset DACs I and Q full-scale negative output			−108.8		mV
Transmit offset DACs differential nonlinearity				±1.1	LSB
Transmit offset DACs integral nonlinearity				±1.1	LSB

Modulation Error: In the digital mode, during the transmit burst, the complex output of the transmitter circuits consists of an ideal output $s = I_{ideal} + jQ_{ideal}$ + error $e = e_i + je_q$. In Table 6, the modulation error (EVM) is defined as the peak value of the magnitude of e relative to the ideal output:

$$\text{Modulation error percentage} = 100\,\frac{|e|}{|s|}\,\%$$

PRODUCT PREVIEW

transmit section (continued)

Table 7 and Table 8 show the frequency response of the transmit section for digital and analog mode, respectively.

Table 7. Transmit Channel Frequency Response (Digital Mode)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency response	0 kHz to 8 kHz (see Note 4)			±0.3	dB
	8 kHz to 15 kHz (see Note 4)			±0.5	
	20 kHz to 45 kHz (see Note 5)	−29			
	45 kHz to 75 kHz (see Note 5)	−55			
	> 75 kHz (see Note 5)	−60			
	Any 30 kHz band centered at > 90 kHz (see Note 5)	−60			
Peak-to-peak group delay distortion	0 kHz to 15 kHz			3	µs
Absolute channel delay	0 kHz to 15 kHz		320		µs

NOTES: 4. Deviation from ideal 0.35 SQRC response
5. Stopband

Table 8. Transmit Channel Frequency Response (Analog Mode)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency response	0 kHz to 8 kHz (see Note 1)			±0.5	dB
	8 kHz to 15 kHz (see Note 1)			±0.5	
	20 kHz to 45 kHz (see Note 5)	−31			
	45 kHz to 75 kHz (see Note 5)	−70			
	> 75 kHz (see Note 5)	−70			
	Any 30 kHz band centered at > 90 kHz (see Note 5)	−70			
Peak-to-peak group delay distortion	0 kHz to 15 kHz			3	µs
Absolute channel delay	0 kHz to 15 kHz		540		µs

NOTES: 1. Ripple magnitude
5. Stopband

PRODUCT PREVIEW

transmit burst operation (digital mode)

In the digital mode, the TCM4300 performs all encoding, signal processing, and power ramping for the burst. Start and stop timing of the variable length bursts are set by means of the TXGO bit in the DStatCtrl register. The SINT interrupt output interrupts the DSP at 48.6 kHz which is T/2 interval (T = 1 symbol period = 1/24.3 kHz). The burst is initiated by the DSP writing 1 to 5 dibits to the TXI register, a small positive delay offset value d to the base station (BST) register, and a 1 to the TXGO bit in the DStatCtrl register.

The TXGO bit is sampled on the falling edge of SINT. The TX outputs are held at zero differential voltage (each output pin is held at the voltage supplied to the VCM input pin) for 9.5 SINT periods (195.5 μs) plus BST offset delay after SINT has detected TXGO high; then the TX outputs begin to ramp to the initial π/4 DQPSK constellation value. The shape of the ramp is the transient resulting from the internal SQRC filtering. At the same time that the TX outputs are beginning to ramp, the PAEN digital output goes high. This output can be used to enable the power amplifier of a cellular radio transmitter. The TCM4300 TX outputs reach the first π/4 DQPSK constellation value (maximum effect point, MEP) 6 SINT periods (3 symbol periods) after the start of the ramp.

The bit stream to be encoded as π/4 DQPSK symbols is generated by right shifts on each SINT of the TXI register with bit 0 (LSB) used first.

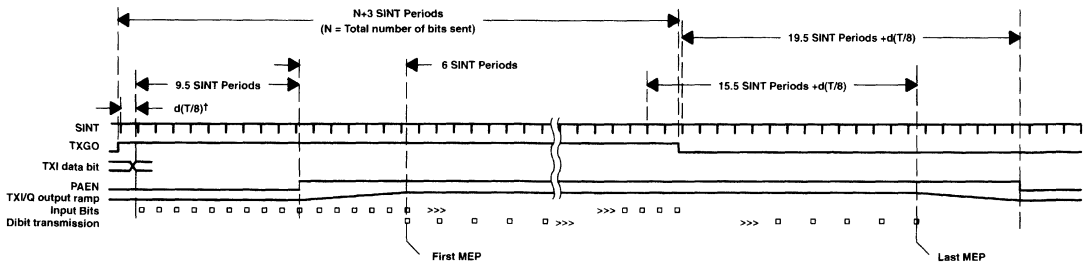
Previously written data continues to propagate through the TCM4300 internal filters until the last π/4 DQPSK constellation value (last MEP) occurs at the TX outputs 15.5 SINT periods (318.9 μs) plus BST offset delay after the last symbol occurs (2 SINT periods before TXGO goes low); then the TX outputs decay to zero differential voltage (each output at the voltage supplied to the VCM input pin). The shape of the decay is the transient resulting from the internal SQRC filtering. The TX outputs are held at zero differential voltage 6 SINT periods (3 symbol periods) after the start of the decay. At this time the PAEN digital output is set low (see Figure 1 and Figure 2).

Non-zero values of the BST offset register increase the delays of both the TX waveforms and PAEN relative to the edges of TXGO after it is internally sampled by SINT. The delays are increased in increments of 1/4 SINT (1/8 symbol period).

For delays of 1 SINT or greater, the fractional part of the delay can be achieved using the BST offset register with the remaining integer SINT delay implemented externally by delaying the writing to TXGO and TXI.

The relative timing of PAEN and the TX waveforms is not affected by the BST offset register.

The IS-54 standard describes shortened bursts and normal bursts. The two types differ in duration and number of transmitted bursts, burst length being determined by the TXGO bit.



† Total delay = d (SINT/4 or T/8) where d = integer value (0,1,2,3) written to the BST offset register.

Figure 1. Power Ramp-Up/Ramp-Down Timing Diagram

transmit burst operation (digital mode) (continued)

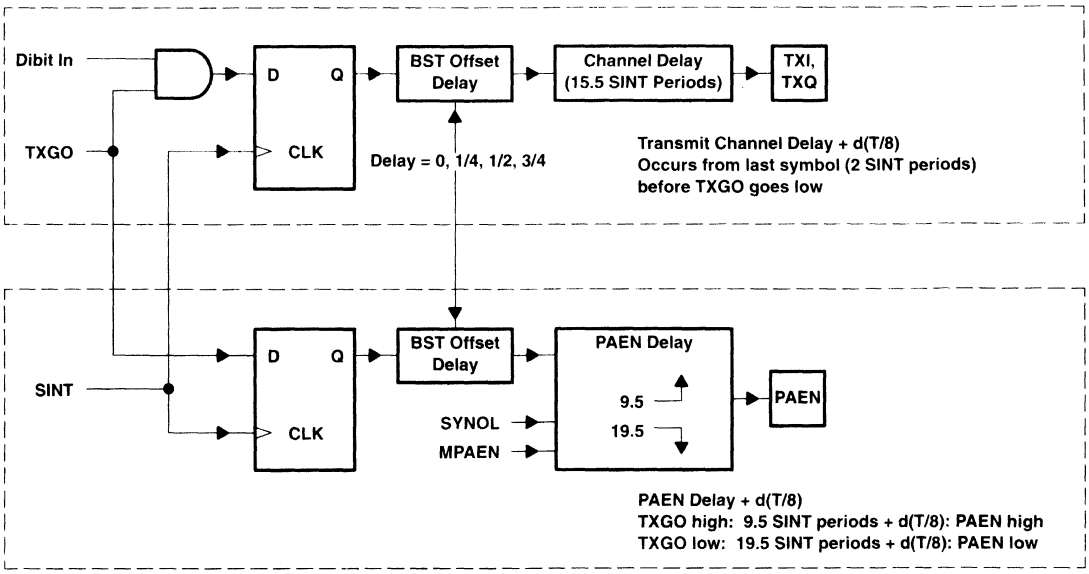


Figure 2. TX Power Ramp-Up/Ramp-Down Functional Diagram

transmit I and Q output level

In the digital mode, the output level at TXI and TXQ is controlled by the TCM4300. During the burst, but not including ramp-up or ramp-down periods, the average output level $(I^2 + Q^2)^{1/2}$ should approximate the specified value. There is no variable level control for TXI and TXQ within the TCM4300 other than the fixed ramping. In the analog mode, the output of the TCM4300 depends only on the sample values written to the TXI and TXQ registers.

There are small differences in the average output power levels between the digital and the analog modes. These differences require compensation at the system level by a small attenuation in the sample values of the analog output.

When a change in transmit power is necessary, the microcontroller can change the value sent to the PWRCONT DAC, the output of which can be connected to a voltage-controlled attenuator in the transmit path of the RF section.

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wide-band data demodulator

The wide-band data demodulator (WBDD) module demodulates the FM signal and outputs a Manchester-decoded data stream. The WBDD is used for receiving the analog control channels of forward control channel (FOCC) and forward voice channel (FVC). The bit error rate (BER) performance requirements are listed in Table 9.

Table 9. Typical Bit Error Rate Performance (WBD_BW = 000)

PARAMETER	TEST CONDITIONS MEAN CNR (dB)	MIN	MAX	UNIT
Bit error rate	−5		0.4	
	0		0.279	
	5		0.143	
	10		0.056	
	15		0.0192	
	20		0.00623	
	25		0.00199	

The WBDD is controlled by the bits in the control register WBDCtrl (see Table 10).

Table 10. Bits in Control Register WBDCtrl

NAME	BIT CODE	FUNCTION
WBD_LCKD	—	Indicates whether edge detector is locked (1) or unlocked (0)
WBD_ON	—	Turns the WBDD module on/off (1/0)
WBD_BW		Sets the appropriate PLL bandwidth
	000	20 Hz
	001	39 Hz
	010	78 Hz
	011	156 Hz
	100	313 Hz
	101	625 Hz
	110	1250 Hz

WBD_LCKD: This bit can be used to reduce the effects of signal dropouts due to fading. In the Manchester-coded signal, there are two types of data edges. One type occurs at the midpoint of each data bit, and the other occurs randomly, depending on the transmitted data sequence. Inside the WBDD, an edge detector rapidly synchronizes itself to the midpoint edges when the WBD_LCKD bit is set to 0. However, if a signal dropout occurs, the edge detector may momentarily lock to the wrong edge because it cannot distinguish the midpoint edges from the data edges. A small number of additional bits may be lost in this instance.

When the WBD_LCKD bit is set to 1, the edge detector uses the WBDD internal PLL output to distinguish the correct edge. Once acquisition of data has occurred, if this bit is set to 1, the loss of bits due to signal dropouts is restricted to the fade duration only.

When the WBDD PLL is not synchronized, as at powerup, the WBD_LCKD bit must be cleared to 0 to allow edge synchronization to the data.

WBD_BW: The variable bandwidth is required for fast acquisition in the beginning using a wide bandwidth for the PLL, and a narrower bandwidth is used afterwards to reduce the likelihood of noise-causing loss of synchronization.

The WBDCtrl register is accessible by both the DSP and the microcontroller.

wide-band data interrupts

The WBDD operates whenever WBD_ON is high, and it does not require the receive channels to be enabled. While WBD_ON is high, every 800 µs, 8 bits are placed in the WBD register, which is accessible by both the DSP and the microcontroller ports. This value should be written at the same time as WBD_ON is initially set high.

At the same time, the interrupts DWBDINT and MWBDFINT are asserted. The interrupt rate is 800 µs (8 bits/10 kHz). These interrupts are individually cleared when the WBD register is read by the corresponding processor. They can also be cleared by their respective processor by writing a 1 to the corresponding clear WBD bit.

There is one WBD control register. It can be written to by either processor port.

wide-band data demodulator: general information

The WBDD recovers the transmitter clock from the data stream, which is Manchester encoded, and decodes the data bits. Consideration at the system level is required to ensure data integrity.

The WBD stream carries with it a 10-kHz clock. The Manchester-coded data format contains a transition at the middle of every bit-clock period, which aids in clock recovery. The polarity of the transition is data-dependent. In a typical Manchester-coded WBD stream, a positive voltage for the first half of the data sequence bit time followed by a negative voltage for the second half of the data sequence bit time represents the value 0 in the data sequence. Likewise, a negative voltage followed by a transition to a positive voltage represents the value 1 in the data sequence. This is illustrated in Figure 3. The WBD stream can also be seen as the exclusive-OR of the clock and data sequence. The data sequence is in nonreturn to zero (NRZ) format.

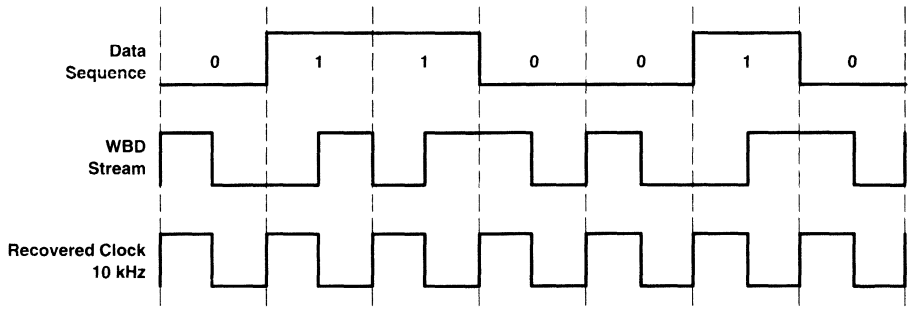

Figure 3. WBD Manchester-Coded Data Stream

auxiliary digital-to-analog converters (DACs), LCD contrast converter

Auxiliary DACs generate AFC, AGC and power control signals for the RF system. These three D/A converters are updated when the corresponding data is received from the DSP. In fewer than 5 µs after the corresponding registers are written to, the output has settled to within 1/2 LSB of its new value (see Table 11).

The LCDCONTR output is used by the microcontroller to adjust the contrast of the liquid-crystal display (LCD). This converter is a separate 4-bit DAC.

auxiliary digital-to-analog converters (DACs), LCD contrast converter (continued)

Table 11. Auxiliary D/A Converters

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output range	AV_{DD} > 3 V†, AUXFS [1:0] = 00	0.2		2.5	V
	AV_{DD} > 4.5 V†, AUXFS [1:0] = 10	0.2		4	
	AV_{DD} > 5 V†, AUXFS [1:0] = 11	0.2		4.5	
Resolution AGC, AFC, PWRCONT DACs			8		bits
Resolution LCDCONTR DAC			4		bits
Gain + offset error (full scale) AGC, AFC, PWRCONT DAC				±5%	
Gain + offset error (full scale) LCDCONTR DAC				±8%	
Differential nonlinearity			±1.3	±2	LSB
Integral nonlinearity			±1.3	±2	LSB
Load resistance		10			kΩ
Load capacitance				50	pF

† Range settings depends only on AUXFS [1:0]. The supply voltage is not detected.

The auxiliary DACs can be powered down. The AGC and AFC DACs have dedicated bits in the MIntCtrl register to enable the DACs. The PWRCONT DAC is enabled by the TXEN bit in the DStatCtrl register. The LCDCONTR DAC is enabled when the LCDEN bit of the LCD D/A register is set to 0, the four data bits being left justified. The AFC, AGC, and PWRCONT DACs are disabled after powerup or after a reset of the TCM4300. After powerup or reset, the default AUXFS[1:0] is 00. When the DACs are powered down, their output pins go to a high-impedance state and can tolerate any voltage present on the pin that falls within the supply range.

The slope and the corresponding output values for the auxiliary DACs are listed in Table 12 and Table 13.

Table 12. Auxiliary D/A Converters Slope (AGC, AFC, PWRCONT)

AUXFS[1:0] SETTING	SLOPE	NOMINAL LSB VALUE (V)	NOMINAL OUTPUT VOLTAGE FOR DIGITAL CODE = 128 (MIDRANGE) (V)	NOMINAL OUTPUT VOLTAGE FOR DIGITAL CODE = 256‡ (MAX VALUE) (V)
00	2.5/256	0.0098	1.25	2.5
01	Do not use	Do not use	Do not use	Do not use
10	4/256	0.0156	2	4
11	4.5/256	0.0176	2.25	4.5

‡ The maximum input code is 255. The value shown for 256 is extrapolated.

Table 13. Auxiliary D/A Converters Slope (LCDCONTR)

AUXFS[1:0] SETTING	SLOPE	NOMINAL LSB VALUE (V)	NOMINAL OUTPUT VOLTAGE FOR DIGITAL CODE = 8 (MIDRANGE) (V)	NOMINAL OUTPUT VOLTAGE FOR DIGITAL CODE = 16§ (MAX VALUE) (V)
00	2.5/16	0.1563	1.25	2.5
01	Do not use	Do not use	Do not use	Do not use
10	4/16	0.2500	2	4
11	4.5/16	0.2813	2.25	4.5

§ The maximum input code is 15. The value shown for 16 is extrapolated.

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RSSI, battery monitor

The received signal strength indicator (RSSI) and battery (BAT) strength monitor share a common register. The input source is determined by writing any value to the mapped register location for that analog-to-digital converter (see Table 14), and the result of the conversion is stored in both register locations. The conversion process is initiated when the register is written to. The CVRDY bit in the MStatCtrl register is set to 1 to show completion of the conversion process. Reading from either of the register locations causes the CVRDY bit to change to 0. The received signal strength indicator allows the mobile unit to choose the proper control channels and to report signal levels to the base stations.

When CVRDY in the MStatCtrl register goes to 1, this indicates that the latest RSSI or battery voltage A/D conversion has been completed and can be read from the RSSI or BAT register location. CVRDY goes to 0 when the microcontroller reads either of these locations.

Table 14. RSSI/Battery A/D Converter

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input range	AV_{DD} = 3 V, 4.5 V, 5 V	0.2		2	V
Resolution			8		bits
Conversion time	AV_{DD} = 3 V, 4.5 V, 5 V		20		µs
Gain + offset error (full scale)			±4%	±5%	
Differential nonlinearity				±1.5	LSB
Integral nonlinearity				±1.5	LSB
Input resistance		1	2		MΩ

In order to save power, the entire RSSI/battery converter circuit is powered down when no A/D conversions are requested for 40 µs. The microcontroller writes to RSSI or BAT registers, causing power to be applied to the converter circuit. Power is applied to the converter circuit until the data value has been latched into the corresponding register, at which time power to the converter is removed. Data remains in the result registers after the converter is powered down.

timing and clock generation

The digital timing generation system uses a 38.88-MHz master clock, as shown in Figure 6. The upper half of the figure shows the clock generation for clocks that must be phase adjusted in order to synchronize the mobile unit with the received symbol stream in the digital mode. In the analog mode, these clocks operate without phase adjustments. The lower half of Figure 6 shows the clocks that are directly derived from the master clock.

clock generation

There are three options for generating the master clock. A fundamental crystal or a third-overtone crystal with a frequency of 8 MHz can be connected between the MCLKIN and the XTAL terminals or an external clock source can be connected directly to the MCLKIN terminal. The MCLKOUT is a buffered master clock output at the same frequency as MCLKIN. MCLKOUT can be used as the source clock for other devices in the system. Setting the MCLKEN bit in the MStatCtrl register enables or disables this output. The MCLKOUT enable is synchronous to eliminate abnormal cycles of the clock output.

All output clocks are derived from the master clock (MCLKIN). The sample clocks for the digital and analog modes, the 8-kHz speech codec sample clock, and the clocks for the A/D and D/A functions are also derived from the master clock.

speech codec clock generation

The TCM4300 generates two clock outputs for use with speech codecs: the 2.048-MHz CMCLK and the 8-kHz CSCLK. These clocks are generated so that each CSCLK period contains exactly 256 cycles of CMCLK. Since 2.048 MHz is not an integer division of the 38.88-MHz MCLKIN, one out of every 64 CMCLK cycles is 18 MCLKIN periods long, and the remaining 63 out of 64 are 19 MCLKIN periods long. The average frequency of MCLKIN is therefore

$$\text{MCLKIN} \times \frac{\left(\frac{63}{19} + \frac{1}{18}\right)}{64} = 2.048092 \text{ MHz}$$

CSCLK is exactly CMCLK divided by 256. See Figure 4.

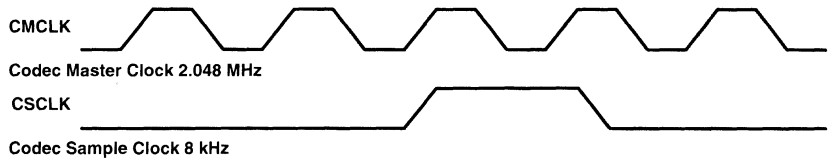

Figure 4. Codec Master and Sample Clock Timing

To save power, the codec clocks are only generated by TCM4300 when the SCEN bit of the DStatCtrl register is set high. When SCEN is low, both outputs, CSCLK and CMCLK, are held low. SCEN is also available as an output.

microcontroller clock

A variable modulus divider provides a selection of frequencies for use as a microcontroller clock. The master clock is divided by an integer from 32 to 2, giving a wide range of frequencies available to the microcontroller (1.215 MHz to 19.88 MHz). The modulus can be changed by writing to the microcontroller clock register. The output duty cycle is within the requirements of most microcontrollers, that is, from 40% to 60%. At power-on reset, the clock divider defaults to 1.215 MHz.

sample interrupt SINT

The SINT interrupt signal is the primary timing signal for the TCM4300 interface. The primary function of the SINT is to indicate the ready condition to receive or transmit data. It also conveys timing marks to allow for the synchronization of system DSP functions. In the digital mode, SINT is used in conjunction with the received sync word to track cellular system timing. The SINT can be disabled by writing a 1 to the SDIS bit of the DIntCtrl register. When enabled, the SINT operates continuously at 48.6 kHz in the digital mode and at 40 kHz in the analog mode. The SINT signal does not require an interrupt acknowledge. The SINT is active low for 5.5 MCLK cycles (141.5 ns) in the analog mode and 6.5 MCLK cycles (167.2 ns) in the digital mode.

phase-adjustment strategy

In the digital mode IS-54 system, receiver sample timing must be phase adjusted to synchronize the A/D conversions to optimum sampling points of the received symbols, and to synchronize the mobile unit timing to the base station timing. This is done by temporarily increasing or decreasing the periods of the clocks to be adjusted. To avoid undesirable transients, each cycle of the clock being adjusted is altered by only one period of MCLKIN. A total adjustment equivalent to multiple MCLKIN periods is accomplished by altering multiple cycles of the clock being adjusted. The number of cycles altered is controlled by internal counters.

In the TCM4300 there are two clocks which must be adjusted: CMCLK and an internal 9.72-MHz clock from which SINT is derived. Each of these clocks has an associated counter that counts the number of cycles that have been lengthened or shortened by one MCLKIN period each and thus detects when the total adjustment is complete. These counters are shown in Figure 6 as Adjust Counter A and Adjust Counter B.

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phase-adjustment strategy (continued)

The magnitude of the 2s complement value written to the timing adjustment register determines the number of cycles of the clocks to be lengthened or shortened by one MCLKIN period each to achieve the total desired timing adjustment in units of MCLKIN periods. If a negative number is written, the clock periods are lengthened for the duration of the timing adjustment, resulting in a timing delay. If a positive number is written, the clock periods are shortened for the duration of the timing adjustment, resulting in a timing advance.

The divider used to generate CMCLK normally divides MCLKIN by either 19 or 18. When the CMCLK period is being lengthened during a timing adjustment, MCLKIN is divided by either 20 or 19. When the CMCLK period is being shortened, MCLKIN is divided by either 18 or 17 (see the section on speech codec clock generation). The divider used to generate a 9.72-MHz clock divides by 4 during normal operation, by 5 when its period is being lengthened during timing adjustments, and by 3 when its period is being shortened during timing adjustments.

Because CMCLK and the 9.72-MHz internal clock have different periods, and the timing adjustments are limited to one period of MCLKIN per period of the clock, these clocks take different times to complete the entire timing adjustment. Because the total adjustment is the same number of MCLKIN periods for both clocks, the relative phases of the two clocks are the same after the adjustment as they were before.

Both adjust counters reach zero when the adjustment is complete, so there is no need to write to the timing adjustment register until another timing adjustment is required. For each write to the timing adjustment register, a single timing adjustment of the direction and magnitude requested is performed.

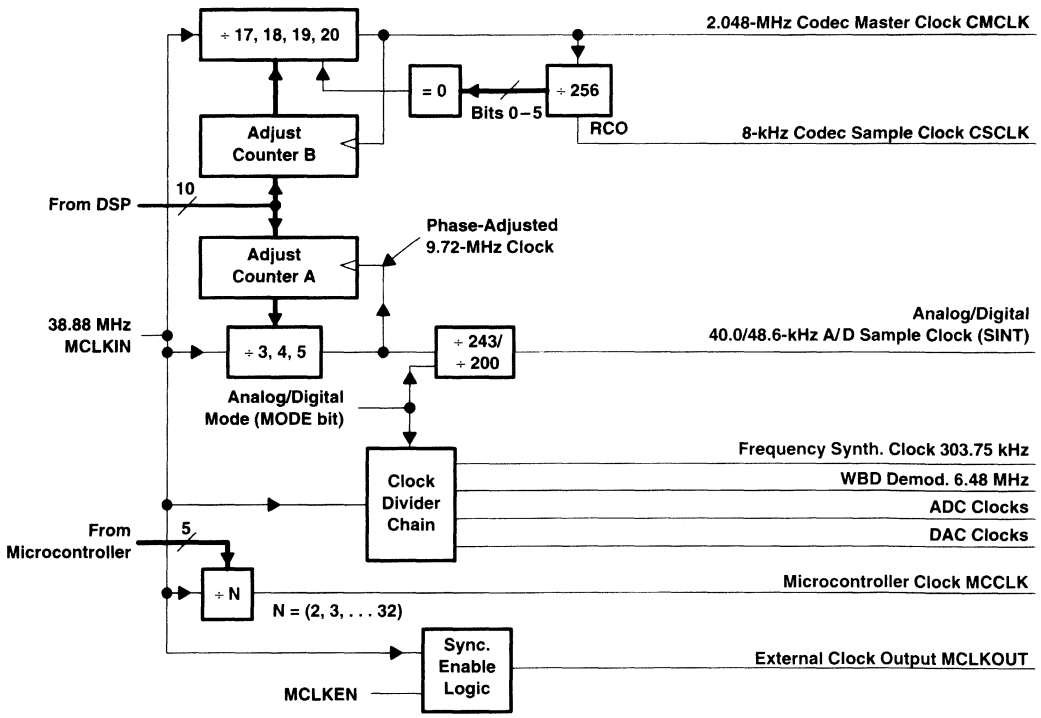

Figure 5. Timing and Clock Generation for 38.88-MHz Clock

The output of each adjustment counter is fed to a variable modulus divider. For counter A, there are three possible moduli, 3, 4, and 5. For counter B there are four possible moduli, 17, 18, 19, and 20.

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frequency synthesizer interface

The synthesizer interface provides a means of programming three synthesizers. The synthesizer-side outputs are a data line, a clock line, and three latch enable lines that separately strobe data into each synthesizer. The control inputs are registers mapped into the microcontroller address space. The status of the interface can be monitored to determine when the programming operation has been completed.

The synthesizer interface is designed to be general purpose. Most of the currently available synthesizers can be accommodated by programming the interface according to the required synthesizer data and logic level formats.

The output of the synthesizer interface consists of five signals. SYNCLK is the common data clock for all attached synthesizer chips. The clock rate is MCLK/128 (≈304 kHz). The clock pulse has a 50% duty factor. The serial data output SYNDTA is common to all synthesizers. Three strobe signals, SYNLE[2:0], are provided. There is one for each synthesizer chip. The attributes of this interface are controlled by means of the synthesizer control registers, SynCtrl[2,1,0]. These attributes determine:

- The polarity of the clock (rising or falling edge)
- Whether data is shifted left or right
- The number of bits sent to the synthesizer
- The timing and polarity of the latch enable bits
- The selection of which synthesizer to program

Programming of the synthesizers is accomplished by writing to four microcontroller-mapped data registers. These registers are chained to form a 32-bit data shift register that can be operated in either shift left or shift right mode. This register set can accommodate various formats of synthesizer control data. When fewer than 32 bits of data are to be transmitted, the significant data bits must be justified such that the first bit to be transferred is either the LSB or the MSB of the register set, as defined by the control register for LSB or MSB first operation. All 32 bits of the data register are transmitted each time. See Table 17 for register location. See Figure 6 for a representative block diagram of the frequency synthesizer interface.

frequency synthesizer interface (continued)

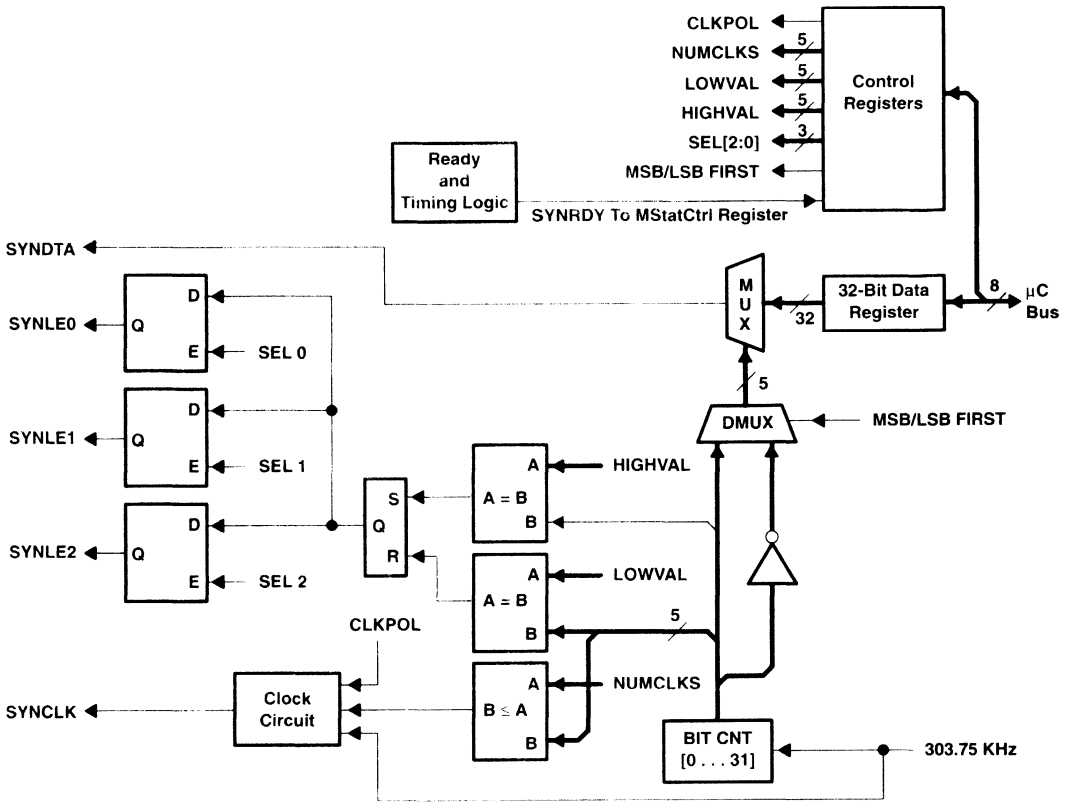

Figure 6. Synthesizer Interface Circuit Block Diagram

The SynData0 register contains the least significant bits of the 32-bit data register. SynData3 contains the most significant bits. The bits in the SynCtrl0, SynCtrl1, and SynCtrl2 registers are allocated as shown in Figure 8.

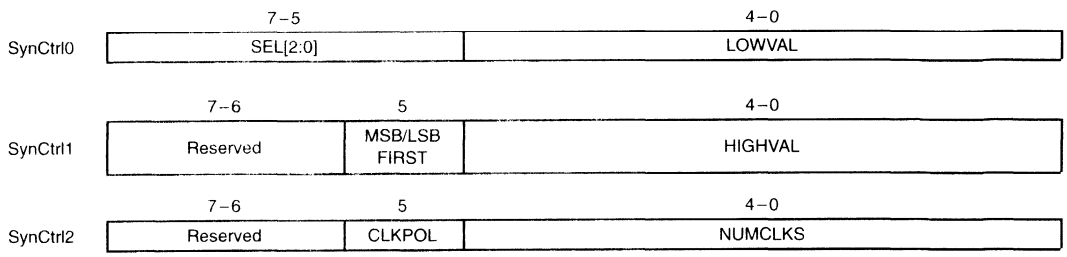

Figure 7. Contents of SynData Registers

Table 15 identifies the meaning of each of the bit fields in SynCtrl[2:0].

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frequency synthesizer interface (continued)

In the status register MStatCtrl, two bits, SYNOL and SYNRDY, are dedicated to the synthesizers. The first is an out-of-lock indicator that comes from the SYNOL input terminal. If the SYNOL input terminal is connected to the OR of the out-of-lock signals from the external synthesizers, the lock condition of the synthesizers can be monitored by reading the MStatCtrl register. A high on SYNOL also prevents the PAEN output from being asserted and forces the TXI and TXQ outputs to zero. The SYNRDY bit, active high, indicates when the synthesizer interface is idle and ready for programming. When SYNRDY is low, the synthesizer interface is busy.

Controlling the synthesizer interface is straightforward. The microcontroller checks to see if the SYNRDY bit is low. When it is low, the synthesizer interface is not ready. When SYNRDY goes high, the microcontroller programs the desired information into the four registers. When the microcontroller write to the SynCtrl2 register is complete, the synthesizer interface sets the SYNRDY bit low and begins to send data, clock, and latch enable according to the format established in the registers. SYNRDY returns high when the entire operation is complete.

Table 15. Synthesizer Control Fields

NAME	DESCRIPTION
CLKPOL	1 Bit. When CLKPOL = 1, the SYNCLK signal is a positive-going, 50% duty cycle pulse. CLKPOL = 0 reverses the polarity of SYNCLK.
NUMCLKS	This 5-bit field defines the total number of clock pulses that are to be produced on the SYNCLK terminal. The value written into this field is the desired number of output clock pulses, with one exception: When 32 clock pulses are desired, all zeroes are written into NUMCLKS.
HIGHVAL	This 5-bit field defines when the strobe signal for the selected synthesizer is driven high. This number is the bit number at which the signal changes state. Bits being transferred on SYNDTA are sequentially designated 0, 1, . . . 31, independent of any MSB/LSB selection.
LOWVAL	The value written into this 5-bit field affects the strobe signal for the selected synthesizer. This number is the bit number at which the strobe signal is driven low. The first bit transferred out of the serial interface is defined to occur at bit-time 0, independent of any MSB/LSB selection.
MSB/LSB FIRST	Writing a 0 to this bit causes the LSB (SynData0[0]) to be the first bit sent to the SYNDTA terminal of the serial synthesizer interface. Writing a 1 to this bit programs the block for MSB first operation (SynData3[7]).
SEL[2:0]	3 Bits. Select which synthesizer strobe line is active. A 1 in any of these bits activates the corresponding latch enable.

Up to 31 data bits plus a latch enable (SYNLE0,1,2) can be programmed in one programming cycle. If greater than or equal to 32 bits of data must be programmed, TI recommends using two or more programming cycles with data in each cycle and a latch enable in the final programming cycle. Two or more programming cycles are recommended because all programming cycles must contain at least one SYNCLK pulse, whereas the latch enable can be suppressed in any programming cycle.

frequency synthesizer interface (continued)

Figure 9 shows an example of the synthesizer output signals. In this case, an 18-bit pattern, 0x10664, was chosen to write into synthesizer 1 with a positive-going latch enable pulse at the eighteenth bit. In order to do so, the microcontroller writes the values 00h into SynData0, 00h into SynData1, 99h into SynData2, 41h into SynData3, 52h into SynCtrl0, 31h into SynCtrl1, and 32h into SynCtrl2.

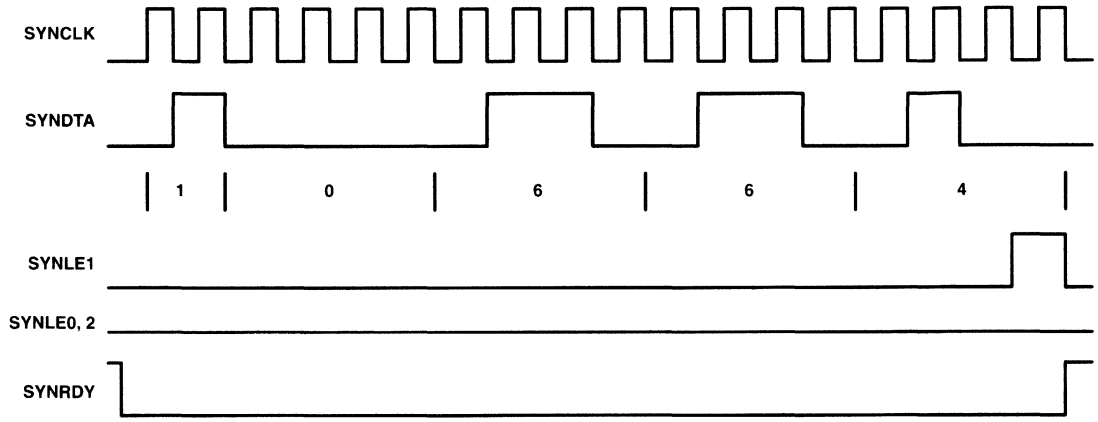

Figure 8. Example Synthesizer Output

power control port

For systems requiring minimum system current consumption, power can be provided to each functional part of the TCM4300 only when that function is required for proper system operation. To accomplish this, the TCM4300 provides six external power control signals accessible through the DStatCtrl and MStatCtrl registers. These signals can be used to minimize the on time of the functional units. These power control signals are SCEN, FMRXEN, IQRXEN, TXEN, PAEN, and OUT1 (see Table 16). The polarity of each of these signals is high enable, low disable.

Table 16. External Power Control Signals

NAME	SUGGESTED EXTERNAL APPLICATION	RESET VALUE
SCEN	Speech codec (microphone/speaker interface circuit) enable	0
FMRXEN	FM demodulator enable	0
IQRXEN	I and Q receive enable. Enables QPSK demodulator and AGC amplifier	0
TXEN	Transmit enable. Enables power to the transmitter signal processing circuits: QPSK modulator, voltage-controlled amplifier, driver amplifier, PA negative bias. This signal can be used to enable these subsystems only during the TX burst in digital mode.	0
OUT1	User defined	0
PAEN	Power amplifier enable. Enables power to PA.	0

In addition to allowing control of power to external functional modules, these power control bits combined with other control bits are used to control internal TCM4300 functions. This control system is shown in Figure 12.

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power control port (continued)

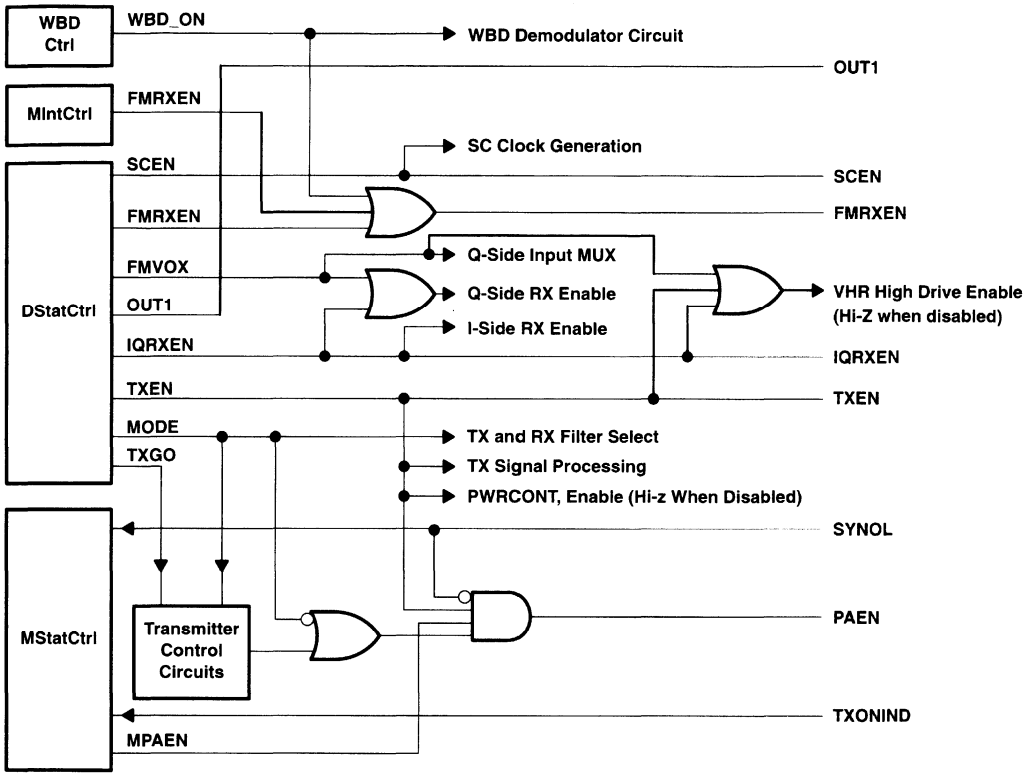

Figure 9. Internal and External Power Control Logic

To allow for further system power savings, the TCM4300 receive I and Q channels are enabled separately because only the Q side is used in analog mode. The FMVOX bit controls the Q-side input multiplexer. When FMVOX is high, the QP side of the receiver is connected to the FM input terminal, the QN input is connected to the VHR reference voltage, and the Q side of the receiver is powered up. The MODE bit controls the Q-side filter characteristics for digital or analog mode. The IQRXEN bit enables both the I and Q receiver sides. The bit IQRXEN can be set high while still in analog mode (FMVOX high or MODE low) to allow sufficient power-up settling time for the external receiver I and Q circuits.

Setting the MODE bit low connects RXQP to the FM input and RXQN to VHR.

In the digital mode (MODE bit set high), setting IQRXEN high turns on both sides of the receiver. The TXEN enables the internal TX functions. When the TXEN bit is set low, the PWRCONT output goes to a high-impedance state and the PAEN output is set low. The TXEN signal can be used to power down most of the external transmit circuits between transmit bursts.

In the analog mode, (MODE bit set low), PAEN is high whenever TXEN is active and SYNOL is low. The SYNOL input can be used as an indication to the TCM4300 that the external synthesizers are out of lock. The PAEN signal is gated by SYNOL to prevent off-channel transmissions.

The TXEN, IQRXEN, FMVOX, and MODE signals are generated by sampling the corresponding bits of the DStatCtrl register with the internal SINT. The effect of a write to the DStatCtrl register on these signals does not appear until the next SINT after the write.

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microcontroller-DSP communications

The microcontroller and the DSP communicate by means of two separate 32-byte first-in first-out (FIFO) buffers. Figure 13 illustrates this scheme. The microcontroller writes to FIFO A, but data read from the same address comes from FIFO B. On the DSP side, the situation is reversed.

To send data to the DSP, the microcontroller writes data to FIFO A. To indicate to the DSP that FIFO A is ready to be read, the microcontroller writes a 1 to the Send-C bit of the microcontroller interrupt control register MIntCtrl. When this happens, the DSP interrupt line CINT goes active, signaling to the DSP that data is waiting. At the same time, the value that can be read from the Clear-C bit in the DIntCtrl register goes from 0 to 1, indicating that the interrupt is pending. When the DSP writes a 1 to the Clear-C bit, the CINT line returns to the inactive state and the value that can be read from Clear-C is 0. The microcontroller cannot deassert the CINT line.

The microcontroller-DSP communications interface is symmetric. Data sent from the DSP to the microcontroller is handled as described above, with the roles of A and B FIFOs and C and D bits and interrupts reversed. If the number of reads exceeds the number of writes from the other side, the values read are undefined.

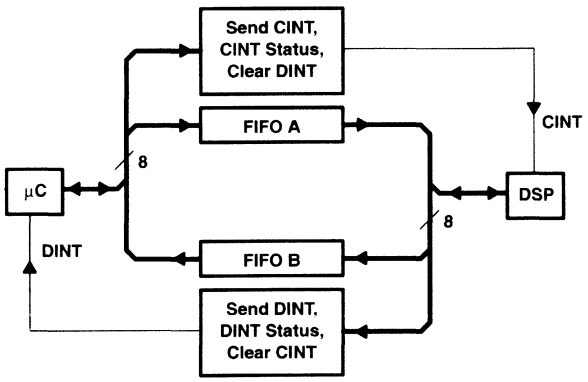

Figure 10. Microcontroller-DSP Data Buffers

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microcontroller register map

The microcontroller can access 17 locations within the TCM4300. The register locations are 8 bits wide, as shown in Table 17 and Table 18.

Table 17. Microcontroller Register Map

ADDR	NAME	D7	D6	D5	D4	D3	D2	D1	D0
00h	WBDCtrl	WBD_LCKD	WBD_ON	WBD_BW			Reserved		
00h	WBD	MSB							LSB
01h	FIFO	MSB		FIFO A(B) Microcontroller to DSP (DSP to Microcontroller)					LSB
02h	MIntCtrl	Clear WBD	Clear-F	Clear-D	Send-C	AGCEN	AFCEN	FMRXEN	Reserved
03h	SynData0	MSB							LSB
04h	SynData1	MSB							LSB
05h	SynData2	MSB							LSB
06h	SynData3	MSB							LSB
07h	SynCtrl0	SEL[2:0]			LOWVAL				
08h	SynCtrl1	Reserved		MSB/LSB FIRST	HIGHVAL				
09h	SynCtrl2	Reserved		CLKPOL	NUMCLKS				
0Ah	MCClock	Reserved		MSB					LSB
0Bh	RSSI A/D	MSB							LSB
0Ch	BAT A/D	MSB							LSB
0Dh	LCD D/A	MSB			LSD	Reserved			LCDEN
0Eh	MStatCtrl	SYNOL	TXONIND	SYNRDY	MCLKEN	CVRDY	AuxFS1	AuxFS0	MPAEN
0Fh	TXI Offset	Reserved		Sign	MSB				LSB
10h	TXQ Offset	Reserved		Sign	MSB				LSB

Table 18. Microcontroller Register Definitions

ADDR	NAME	CATEGORY	R/W
00h	WBDCtrl	Wide-band data	W
00h	WBD		R
01h	FIFO	FIFO A(B) microcontroller to DSP (DSP to microcontroller)	W/(R)
02h	MIntCtrl	Interrupt/control status	R/W
03h	SynData0	Synthesizer interface	W
04h	SynData1		W
05h	SynData2		W
06h	SynData3		W
07h	SynCtrl0		W
08h	SynCtrl1		W
09h	SynCtrl2		W
0Ah	MCClock	Microcontroller clock speed	W
0Bh	RSSI A/D	RSSI level	R
0Ch	BAT A/D	Battery level monitor	R
0Dh	LCD D/A	LCD contrast control	W
0Eh	MStatCtrl	Miscellaneous status/control	R/W
0Fh	TXI Offset	Transmit dc offset compensation	W
10h	TXQ Offset		W

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wide-band data/control register

This register is used for two functions, depending on whether it is being read from or written to. When read from, the register provides the latest 8 bits of received and demodulated data to the microcontroller. When it is written to, the bits are placed into the WBDCtrl register (see Table 17) as shown here:

	7	6	5–3	2–0
WBDCtrl	WBD_LCKD	WBD_ON	WBD_BW[2:0]	Reserved
	W	W	W	

When the WBDCtrl register is read, bit 7 (MSB) is the last received data bit.

The definition of the WBDCtrl register, according to the DSP register map, is shown in Table 19.

Table 19. WBDCtrl Register

BIT	R/W	NAME	FUNCTION	RESET VALUE
9	R/W	WBD_LCKD	Wide-band data lock data. Determines whether edge detector is locked (1) or unlocked (0).	0
8	R/W	WBD_ON	Wide-band data on. Turns the WBDD module on/off (1/0).	0
7–5	R/W	WBD_BW[2:0]	Wide-band data bandwidth. Sets the appropriate PLL bandwidth. 000 : 20 Hz 001 : 39 Hz 010 : 78 Hz 011 : 156 Hz 100 : 313 Hz 101 : 625 Hz 110 : 1250 Hz	110
4–0	—	—	Reserved	—

microcontroller status and control registers

MCClock: This location is used by the microcontroller to change the speed of its own clock. The division modulus is equal to a binary coded value written into this register. Only bits [5:0] are significant. After reset, MCClock is equal to MCLKIN/32. Division modulus 2-32 are valid (0,1 are prohibited). The clock speed change occurs after the write is complete.

MIntCtrl Bits [7:4]: These bit names in this field indicate the resulting action when the bit is set to 1. When these bits are being read, a 1 indicates that the corresponding interrupt is pending. A 0 indicates that the interrupt is clear. Writing a 0 into any bit location has no effect.

MIntCtrl Bits [3:1]: These bits enable power to the AGC and AFC DACs and their corresponding outputs. FMRXEN can be used to assert (set to 1) the FMRXEN external function. The reset value is 0 (off).

	7	6	5	4	3	2	1	0
MIntCtrl	Clear WBD	Clear-F	Clear-D	Send-C	AGCEN	AFCEN	FMRXEN	Reserved
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

MStatCtrl: This register contains various signals needed for system monitoring and control (see Table 20).

	7	6	5	4	3	2	1	0
MStatCtrl	SYNOL	TXONIND	SYNRDY	MCLKEN	CVRDY	AuxFS1	AuxFS0	MPAEN
	R	R	R	R/W	R	R/W	R/W	R/W

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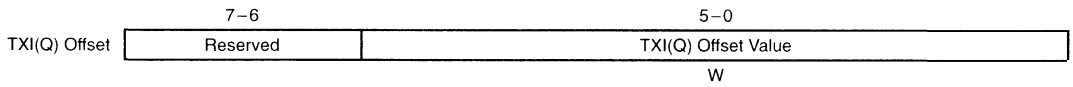
microcontroller status and control registers (continued)

Table 20. MStatCtrl Register Bits

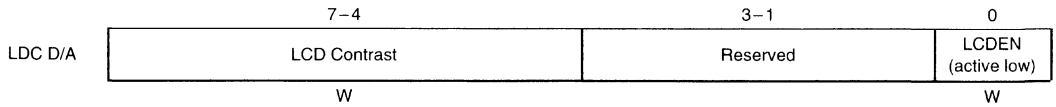
BIT	R/W	NAME	FUNCTION	RESET VALUE
7	R	SYNOL	Synthesizer out of lock. Equal to level applied to SYNOL input pin. Can be used as an input for an externally generated status signal to prevent transmission when external synthesizers are out of lock. In digital mode, when SYNOL is high, PAEN will not be asserted and no signal can be transmitted from TXIP, TXIN, TXQP, and TXQN.	Ext. pin
6	R	TXONIND	Transmitter on indicator. Equal to level applied to TXONIND input pin. Can be used to indicate power is applied to power amplifier.	Ext. pin
5	R	SYNRDY	Synthesizer interface ready to be programmed by the microcontroller. When a 1, the microcontroller can program the frequency synthesizer interface. A 0 indicates the interface circuit is busy.	1
4	R/W	MCLKEN	MCLKOUT enable. When set to 1 by the microcontroller, the 38.88-MHz master clock is sent out via MCLKOUT. Writing 0 to this bit disables MCLKOUT signal.	1
3	R	CVRDY	Conversion ready. A 1 indicates that the latest RSSI or battery voltage A/D conversion is complete and can be read from the RSSI or battery register location. Goes to 0 when microcontroller reads from either of these locations.	1
2	R/W	AuxFS[1]	Auxiliary DACs full-scale select. The auxiliary DACs are AGC, AFC, PWRCONT and also LCD CONTR DAC. The microcontroller selects the full-scale output ranges with these bits. See Table 12 and Table 13 for bit-to-output range mapping.	0
1		AuxFS[0]		0
0	R/W	MPAEN	Microcontroller PA enable. A 0 indicates the external PA enable line PAEN is prevented from going active. See Figure 12.	0

TXI Offset and TXQ Offset: These registers allow the differential offset voltages TXIP – TXIN and TXQP – TXQN to be adjusted to compensate for internal and/or external offsets. The magnitude of adjustment is D × step size, where D is a 6-bit, 2s complement integer written into bits 5–0 of these registers (see Table 6).



LCD contrast

The LCD contrast register allows for 16 levels of control of terminal LCD contrast. The register is input to the LCD contrast D/A allowing control of the level of intensity of the LCD display.



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DSP register map

The register map accessible to the DSP port is shown in Table 21 and Table 22. There are 14 system addressable locations. Note that the write address of FIFO B is the same as the read address of FIFO A. Figure 14 details the connection of TCM4300 to an example DSP.

Table 21. DSP Register Map

ADDR	NAME	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00h	WBD	MSB							LSB	Reserved	
01h	WBDCtrl	WBD_LCKD	WBD_ON	WBD_BW			Reserved				
02h	RXI	Sign	MSB								LSB
03h	RXQ	Sign	MSB								LSB
04h	TXI	Sign	MSB								LSB
05h	TXQ	Sign	MSB								LSB
06h	FIFO	MSB	FIFO A(B) microcontroller to DSP (DSP to microcontroller)						LSB	Reserved	
07h	DIntCtrl	Clear WBD	SDIS	Clear-C	Send-D	Send-F	Reserved				
08h	Timing Adj	MSB									LSB
09h	AGC DAC	MSB							LSB	Reserved	
0Ah	AFC DAC	MSB							LSB	Reserved	
0Bh	PWR DAC	MSB							LSB	Reserved	
0Ch	DStatCtrl	TXGO	MODE	SCEN	FMVOX	FMRXEN	IQRXEN	TXEN	OUT1	RXOF	ALB
0Dh	BST Offset	Reserved								MSB	LSB

Table 22. DSP Register Definitions

ADDR	NAME	CATEGORY	R/W
00h	WBD	Wide-band data	R
01h	WBDCtrl	Wide-band data control	R/W
02h	RXI	RX channel A/D results	R
03h	RXQ		
04h	TXI	Analog mode: TXI D/A data	W
		Digital mode: π/4 DQPSK modulator input data	
05h	TXQ	Analog mode: TXQ D/A data	W
		Digital mode: Not used	
06h	FIFO	FIFO A(B) microcontroller to DSP (DSP to microcontroller)	R/(W)
07h	DIntCtrl	Interrupt control/status	R/W
08h	Timing Adj	Symbol timing adjust	W
09h	AGC DAC	AGC	W
0Ah	AFC DAC	AFC	W
0Bh	PWR DAC	Power control	W
0Ch	DStatCtrl	Miscellaneous status/control	R/W
0Dh	BST Offset	TDM burst offset	W

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wide-band data registers

Bit 9 of the wide-band data register is the most recently received bit.

	9–2	1–0
WBD	WB Data	Reserved
	R	

	9	8	7–5	4–0
WBDCtrl	WBD_LCKD	WBD_ON	WBD_BW	Reserved
			R/W	

base station offset register

BST offset values are 00, 01, 10, and 11, which correspond to an offset value d of 0, 1, 2, and 3, respectively.

	9–2	1–0
BST	Reserved	Offset[1:0]
Offset		W

The delay in the TCM4300 TX channels is increased by the amount

$$d \times \frac{T_{SINT}}{4}$$

DSP status and control registers

DIntCtrl, Clear and Send BIts: The bit names in the DIntCtrl register indicate the action to be taken when a 1 is written to the respective bit. When these bits are being read, a 1 indicates that the corresponding interrupt is pending. A 0 indicates that the interrupt is not pending. Writing a 0 to any bit has no effect. Writing a 1 to the clear bits clears the corresponding interrupt, and the interrupt terminal returns to its inactive level. Writing a 1 to the send bits causes the corresponding interrupt to go active.

DIntCtrl, SDIS: When a 1 is written to the SDIS bit, the SINT interrupt going to the DSP is disabled. The disabling and re-enabling function is buffered to prevent the SINT signal from having shortened periods of output active. The SDIS bit is active (1) upon reset.

	9	8	7	6	5	4–0
DIntCtrl	Clear WBD	SDIS	Clear-C	Send-D	Send-F	Reserved
			R/W			

	9	8	7	6	5	4	3	2	1	0
DStatCtrl	TXGO	MODE	SCEN	FMVOX	FMRXEN	IQRXEN	TXEN	OUT1	RXOF	ALB
					R/W					

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DSP status and control registers (continued)

The DStatCtrl register contains various signals needed for system monitoring and control. These are described in Table 23.

Table 23. DStatCtrl Register Bits

BIT	R/W	NAME	FUNCTION	RESET VALUE
9	R/W	TXGO	Transmitter go. Used in digital mode to initiate (1) and terminate (0) a transmit burst.	0
8	R/W	MODE	Digital (1) – Analog (0) mode select. Affects the clock dividers and the transmitter modes of operation and the Q side filter.	0
7	R/W	SCEN	Speech codec enable. (microphone/speaker interface chip.) The SCEN output pin is connected to this bit. Also enables (1) or disables (0) the internal speech codec clock generation circuits. (2.048 MHz – 8 kHz outputs)	0
6	R/W	FMVOX	FM voice enable. FMVOX = 1 enables the Q side of the internal receiver circuits and connects the receivers Q channel input to FM input pin (see Figure 12).	0
5	R/W	FMRXEN	FM receiver enable. The FMRXEN output pin is connected to this bit (see Figure 12).	0
4	R/W	IQRXEN	I and Q receiver enable. The IQRXEN output pin is connected to this bit. Enables (1), disables (0) power to the I and Q sides of the internal receiver circuits (see Figure 12).	0
3	R/W	TXEN	Transmitter enable. The TXEN output pin is connected to this bit. Enables (1), disables (0) power to the internal transmitter circuits (see Figure 12).	0
2	W	OUT1	Output 1. User-defined general purpose data or control signal.	0
1	R/W	RXOF	Receive channel offset. RXOF=1 disconnects the RXIP, RXIN, RXQP, and RXQN pins from receive channel, and shorts internal RXIP to RXIN and RXQP to RXQN. It provides the capability of measuring the dc offset of the receive channel.	0
0	R/W	ALB	Analog loop-back. ALB=1 disconnects the RXIP, RXIN, RXQP, and RXQN pins from the internal receive channels and connects the corresponding internal signals to attenuated copies of the TXIP, TXIN, TXQP, and TXQN signals. The attenuated factor is 8.	0

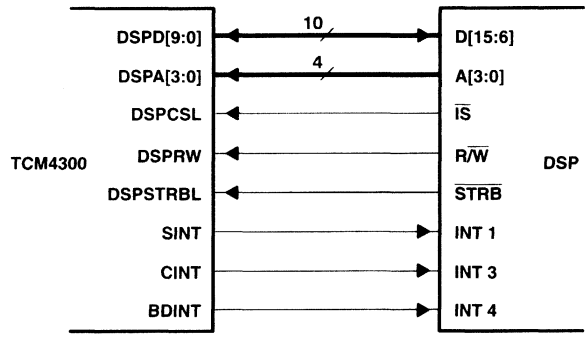

Figure 11. DSP Interface

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reset

internal reset

A low on RSINL causes the TCM4300 internal registers to assume their reset values. The power-on reset circuit also causes internal reset. However, the logic level at RSINL has no effect on reset outputs RSOUTH and RSOUTL.

power-on reset

The power-on reset (POR) is digitally implemented and provides a timed POR signal at RSOUTL and RSOUTH. The POR pulse duration is equal to 388,800 cycles of MCLKIN (10 ms). There are two outputs to provide a high reset and a low reset in order to accommodate the reset polarity requirements of any external device. The TCM4300 internal registers are reset when the POR outputs are activated. See Figure 12.

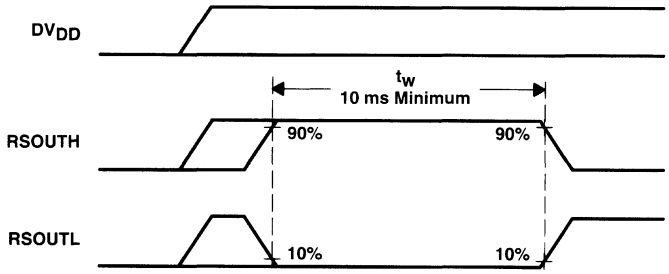

Figure 12. Power-On Reset Timing

internal reset state

After power-on reset, the TCM4300 register bits are initialized to the values shown in Table 25. The synthesizer control pins SYNCLK, SYNLE[0:2], and SYNDTA are high after reset, and the synthesizer interface circuit is in the stable idle state with no SYNCLK outputs.

Table 24. Power-On Reset Register Initialization

REGISTER NAME	BIT 9	8	7	6	5	4	3	2	1	0
DIntCtrl	0	1	0	0	0	r	r	r	r	r
DStatCtrl	0	0	0	0	0	0	0	0	0	0
MIntCtrl			0	0	0	0	0	0	0	r
MStatCtrl			ext	ext	1	1	0	0	0	0
MCClock					0	0	0	0	0	0

r: reserved
ext: bit value from external pin

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microcontroller interface

The microcontroller interface of the TCM4300 is a general purpose bus interface which ensures compatibility with a wide range of microcontrollers, including the Mitsubshi M37700 series and most Intel and Motorola series. The interface consists of a pair of microcontroller type select (MTS[1:0]) inputs, address and data buses, as well as several input and output control signals that are designed to operate in a manner compatible with the microcontroller selected by the user.

Table 25. Microcontroller Interface Confirguration

MTS1	MTS0	MODE	POLARITY	
			DATA STROBE (DS) ACTIVE	INTERRUPT/OUTPUT ACTIVE
0	0	Intel	Low (separate read and write)	High
1	0	Motorola 16-bit and Mitsubishi	Low	Low
0	1	Motorola 8-bit	High	Low
1	1	Reserved	N/A	N/A

The microcontroller interface of the TCM4300 is designed to allow direct connection to many microcontrollers. Except for the interrupt pins, it is designed to connect to microcontrollers in the same manner as a memory device.

The internal chip select is asserted when MCCSH = 1 and MCCSL = 0.

Intel microcontroller mode of operation

When the microcontroller type select (MTS[1:0]) inputs are both held low, the TCM4300 microcontroller interface is configured into Intel mode (see Table 25). In this mode, the interface uses separate read and write control strobes and active-high interrupt signals. The processor $\overline{RD}$ and $\overline{WR}$ strobe signals should be connected to the TCM4300 MCDS signal and MCRW signal, respectively. The multiplexed address and data buses of the microcontroller must be demultiplexed by external hardware. Table 27 lists the microcontroller interface connections for Intel mode.

Table 26. Microcontroller Interface Connections for Intel Mode

TCM4300 PIN	MICROCONTROLLER PIN
MTS[1:0]	Tie to logic levels: low and low, respectively
MCCSH	Not on microcontroller; can be used for address decoding
MCCSL	Not on microcontroller; can be used for address decoding
MCD[7:0]	AD[7:0] data bus on microcontroller
MCA[4:0]	Demultiplexed address bits not on microcontroller
MCRW	$\overline{WR}$ (Active-low write data strobe)
MCDS	$\overline{RD}$ (Active-low read data strobe) MCDS configured to active-low operation by MTS[1:0]. The microcontroller bus must be demultiplexed by external hardware.
MWBDFINT	One of INT[3:0] as appropriate
DINT	One of INT[3:0] as appropriate

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Mitsubishi microcontroller mode of operation

When the microcontroller type select (MTS[1:0]) inputs are held high and low, respectively, the TCM4300 microcontroller interface is configured into Mitsubishi mode. In this mode, the interface has a single read/write control (R/$\overline{W}$) signal, an active-low data strobe (MCDS) signal, and active-low interrupt request signals. The processor $\overline{E}$ and R/($\overline{W}$) signals should be connected to the TCM4300 MCDS signal and the MCRW signal, respectively. Table 28 lists the microcontroller interface connections for Mitsubishi mode.

Table 27. Microcontroller Interface Connections for Mitsubishi Mode

TCM4300 PIN	MICROCONTROLLER PIN
MTS[1:0]	Tie to logic levels: high and low, respectively
MCCSH	Not on microcontroller; can be used for address decoding
MCCSL	Not on microcontroller; can be used for address decoding
MCD[7:0]	D[7:0] data bus on microcontroller
MCA[4:0]	A[4:0]
MCRW	R/$\overline{W}$
MCDS	$\overline{E}$ (Active-low read data strobe) MCDS configured to active-low operation by MTS[1:0].
MWBDFINT	One of INT[3:0] as appropriate
DINT	One of INT[3:0] as appropriate

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Motorola microcontroller mode of operation

When the microcontroller type select MTS0 = high and MTS1 = low, the TCM4300 microcontroller interface is configured for 8-bit family (6800 family derivatives, e.g., 68HC11D3 and 68HC11G5) bus characteristics, and when the microcontroller type select MTS0 = low and MTS1 = high, the microcontroller interface is configured for 16-bit family (680 × 0 family derivatives, e.g., 68008 and 68302) characteristics. The Motorola mode makes use of a single read/write control (R/$\overline{W}$) signal and active-low interrupt request signals. The processor E (8 bit) or $\overline{DS}$ (16 bit) and (R/$\overline{W}$) control signals should be connected to the TCM4300 MCDS signal and the MCRW signal, respectively. Table 29 illustrates the connections between the TCM4300 and an 8-bit Motorola processor. Table 30 illustrates the connections between the TCM4300 and a 16-bit Motorola processor.

Table 28. Microcontroller Interface Connections for Motorola Mode (8 bit)

TCM4300 PIN	MICROCONTROLLER PIN
MTS[1:0]	Tie to logic levels: low and high, respectively
MCCSH	Not on microcontroller; can be used for address decoding
MCCSL	Not on microcontroller; can be used for address decoding
MCD[7:0]	PC[7:0] data bus on microcontroller
MCA[4:0]	Demultiplexed address output. PF[4:0] on microcontroller for nonmultiplexed machines (e.g., 68CH11G5) and not on micro for multiplexed bus machines (e.g., 68HC11D3).
MCRW	R/$\overline{W}$
MCDS	E (Active-high data strobe) MCDS configured to active-high operation by MTS[1:0].
MWBDFINT	$\overline{IRQ}$ and/or $\overline{NMI}$ as appropriate
DINT	$\overline{IRQ}$ and/or $\overline{NMI}$ as appropriate

Table 29. Microcontroller Interface Connections for Motorola Mode (16 bit)

TCM4300 PIN	MICROCONTROLLER PIN
MTS[1:0]	Tie to logic levels: high and low, respectively
MCCSH	Not on microcontroller; can be used for address decoding
MCCSL	Not on microcontroller (68000, 68008) $\overline{CS1}$, $\overline{CS2}$, or $\overline{CS3}$ (68302)
MCD[7:0]	D[7:0] data bus on microcontroller
MCA[4:0]	A[4:0] (68008) A[5:1] (68000, 68302)
MCRW	R/$\overline{W}$
MCDS	$\overline{DS}$ (active-low data strobe) (68008) $\overline{LDS}$ (active-low data strobe) (68000, 68302) MCDS configured to active-low operation by MTS[1:0]
MWBDFINT	$\overline{IACK7}$, $\overline{IACK6}$, or $\overline{IACK1}$ (68302) Not on microcontroller (68000, 68008)
DINT	One of INT[3:0] as appropriate

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range: DV_{DD} (see Notes 6 and 7): Condition 1 ..... V_{SS} −0.3 to +6 V
Condition 2 ..... V_{SS} −0.3 to AV_{DD} +0.3 V
AV_{DD} (see Notes 7 and 8): Condition 1 ..... V_{SS} −0.3 to +6 V
Condition 2 ..... V_{SS} −0.3 to DV_{DD} +0.3 V
Input voltage range, V_I: Digital signals ..... V_{SS} −0.3 to DV_{DD} +0.3 V
Analog signals ..... V_{SS} −0.3 to AV_{DD} +0.3 V
Output voltage range, V_O: Digital signals ..... V_{SS} to DV_{DD}
Analog signals ..... V_{SS} to AV_{DD}
Continuous total power dissipation ..... See Dissipation Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 6. Voltage values are with respect DV_{SS}.
7. Maximum voltage is the minimum of the two conditions.
8. Voltage values are with respect to AV_{SS}.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR (T_{JA}) ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
PZ	2222 mW	45°C/W	889 mW

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recommended operating conditions

			MIN	MAX	UNIT
DV_{DD}	Supply voltage		3	5.5	V
V_{IH}	High-level input voltage	Digital	0.7 DV_{DD}	DV_{DD}+0.3	V
V_{IL}	Low-level input voltage	Digital	0	0.3 DV_{DD}	V
V_{OH}	High-level output voltage	Digital	0.7 DV_{DD}	DV_{DD}	V
V_{OL}	Low-level output voltage	Digital	0	0.5	V
I_{OH}	High-level output current at 3 V	Digital	2		mA
I_{OL}	Low-level output current at 3 V	Digital	2		mA
I_{OH}	High-level output current at 5 V	Digital	2		mA
I_{OL}	Low-level output current at 5 V	Digital	2		mA
T_A	Operating free-air temperature		−40	85	°C

electrical characteristics power consumption over full range of operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Analog transmitting and receiving		DV_{DD} = 3 V,	AV_{DD} = 3 V		75		mW
		DV_{DD} = 5.5 V,	AV_{DD} = 5.5 V		275		
Digital receiving		DV_{DD} = 3 V,	AV_{DD} = 3 V		60		mW
		DV_{DD} = 5.5 V,	AV_{DD} = 5.5 V		250		
Digital transmitting		DV_{DD} = 3 V,	AV_{DD} = 3 V		85		mW
		DV_{DD} = 5.5 V,	AV_{DD} = 5.5 V		300		
Idle mode	MCLKOUT enabled	DV_{DD} = 3 V,	AV_{DD} = 3 V		45		mW
	MCLKOUT disabled	DV_{DD} = 3 V,	AV_{DD} = 3 V		17		
	MCLKOUT enabled	DV_{DD} = 5.5 V,	AV_{DD} = 5.5 V		190		
	MCLKOUT disabled	DV_{DD} = 5.5 V,	AV_{DD} = 5.5 V		96		
Digital mode, 1/3 transmitting +1/3 receiving + 1/3 standby		DV_{DD} = 3 V,	AV_{DD} = 3 V		60		mW
		DV_{DD} = 5.5 V,	AV_{DD} = 5.5 V		220		

† All typical values are at T_A = 25°C

reference characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$V_{OH(VHR)}$	High-level output voltage		0.5 AV_{DD}–0.2		0.5 AV_{DD}+0.2	V
r_O	Output resistance	FMVOX or IQRXEN or TXEN = high		80	100	Ω
		FMVOX or IQRXEN or TXEN = low	15	40		kΩ

‡ All typical values are at DV_{DD} = 5 V, AV_{DD} = 5 V, and T_A = 25°C

terminal impedance

FUNCTION	TERMINAL NAME	MIN	TYP§	MAX	UNIT
Receive channel input impedance (single-ended)	RXIP/N and RXQP/N	40	70		kΩ
Transmit channel output impedance (single-ended)	TXIP/N and TXQP/N	40	50	100	Ω
FM input impedance	WBD	25	200		kΩ
MCLKOUT impedance	MCLKOUT @ 3.3 V		240		Ω
	MCLKOUT @ 5 V		180		

§ All typical values are at DV_{DD} = 5 V, AV_{DD} = 5 V, and T_A = 25°C, unless otherwise specified.

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MCLKOUT timing requirements

		MIN	NOM	MAX	UNIT
t_{wH}	Pulse duration high	9	10	12	ns
t_{wL}	Pulse duration low	9	10	12	ns
t_r	Rise time	2	3	4	ns
t_f	Fall time	2	3	4	ns

NOTE: Tested with 15 pF loading on MCLKOUT

PARAMETER MEASUREMENT INFORMATION

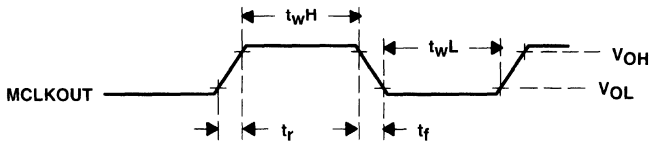

Figure 13. MCLKOUT Timing Diagram

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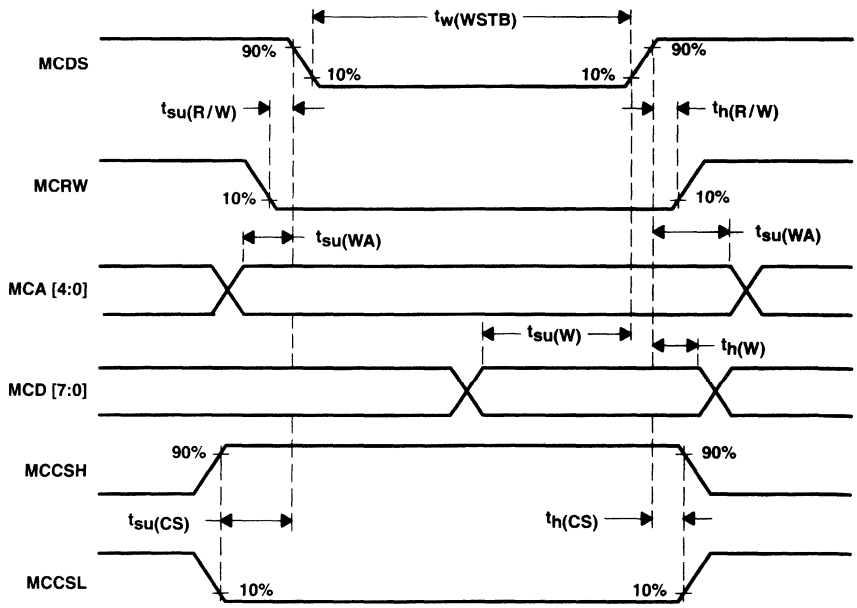
PARAMETER MEASUREMENT INFORMATION

TCM4300 to microcontroller interface timing requirements (Mitsubishi write cycle)

PARAMETER			ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(R/W)}$	Setup time, read/write	Read/write (MCRW) stable before falling edge of strobe (MCDS)	$TRW_{(SU)}$	0		ns
$t_{h(R/W)}$	Hold time, read/write	Read/write (MCRW) stable after rising edge of strobe (MCDS)	$TRW_{(HO)}$	10		ns
$t_{su(WA)}$	Setup time, write address	Address (MCA) stable before falling edge of strobe (MCDS)	$TWA_{(SU)}$	0		ns
$t_{h(WA)}$	Hold time, write address	Address (MCA) stable after rising edge of strobe (MCDS)	$TWA_{(HO)}$	10		ns
$t_{su(W)}$	Setup time, write data	Data stable (MCD) before rising edge of strobe (MCDS)	$TWD_{(SU)}$	14		ns
$t_{h(W)}$	Hold time, write data	Data stable (MCD) after rising edge of strobe (MCDS)	$TWD_{(HO)}$	0		ns
$t_{w(WSTB)}$	Pulse duration, write strobe	Write strobe pulse width	$TWR_{(STB)}$	60		ns
$t_{h(CS)}$	Hold time, chip select	Chip select (MCCSH and MCCSL) stable before rising edge of strobe (MCDS)	$TCS_{(HO)}$	0		ns
$t_{su(CS)}$	Setup time, chip select	Chip select stable (MCCSH and MCCSL) before falling edge of strobe (MCDS)	$TCS_{(SU)}$	0		ns

NOTE: Timings based upon Mitsubishi 37732S4 (16 MHz) and Mitsubishi 3772S4L (8 MHz).



NOTE: Chip selection is defined as both MCCS and MCDS active.

Figure 14. Microcontroller Interface Timing Requirements (Mitsubishi Configuration Write Cycle, MTS[1:0] = 10)

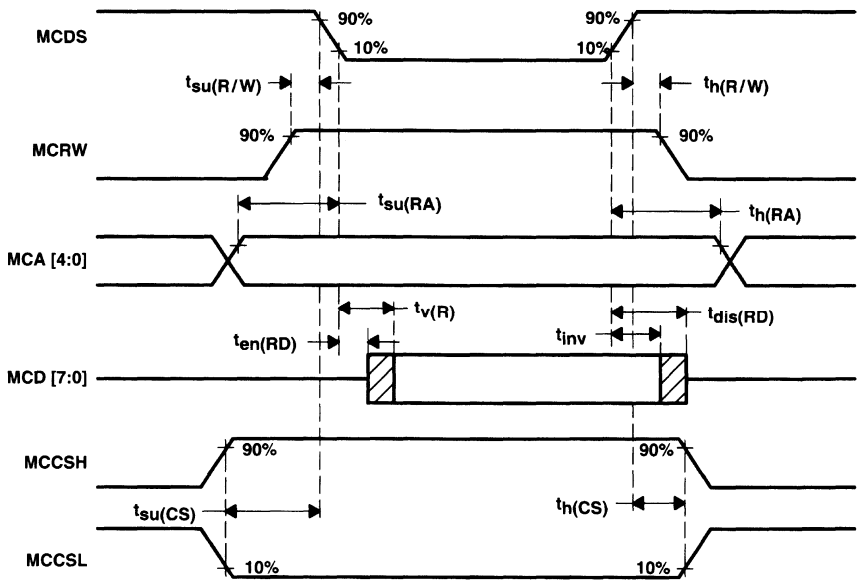
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

TCM4300 to microcontroller interface timing requirements (Mitsubishi read cycle)

PARAMETER			ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(R/W)}$	Setup time, read/write	Read/write (MCRW) stable before falling edge of strobe (MCDS)	$TRW_{(SU)}$	0		ns
$t_{h(R/W)}$	Hold time, read/write	Read/write (MCRW) stable after rising edge of strobe (MCDS)	$TRW_{(HO)}$	10		ns
$t_{su(RA)}$	Setup time, read address	Read address (MCS) stable before falling edge of strobe (MCDS)	$TRA_{(SU)}$	0		ns
$t_{h(RA)}$	Hold time, read address	Read address (MCA) stable after rising edge of strobe (MCDS)	$TRA_{(HO)}$	10		ns
$t_{en(RD)}$	Enable time, read data	Falling edge of strobe (MCDS) to TCM4300 driving data bus (MCD)	$TRD_{(EN)}$	10		ns
$t_{v(R)}$	Read data valid time	Falling edge of strobe (MCDS) to valid data (MCD)	$TRD_{(DV)}$		50	ns
t_{inv}	Data invalid time	Data (MCD) invalid after rising edge of strobe (MCDS)	$TRD_{(INV)}$		10	ns
$t_{dis(RD)}$	Disable time, read data	TCM4300 releases data bus after rising edge of strobe (MCDS)	$TRD_{(DIS)}$		28	ns
$t_{h(CS)}$	Hold time, chip select	Chip select (MCCSH and MCCSL) stable before rising edge of strobe (MCDS)	$TCS_{(HO)}$	0		ns
$t_{su(CS)}$	Setup time, chip select	Chip select stable (MCCSH and MCCSL) before falling edge of strobe (MCDS)	$TCS_{(SU)}$	0		ns

NOTE: Timings are based upon Mitsubishi 37732S4 (16 MHz) and Mitsubishi 3772S4L (8 MHz).



NOTE: Chip selection is defined as both MCCS and MCDS active.

Figure 15. Microcontroller Interface Timing Requirements (Mitsubishi Configuration Read Cycle, MTS[1:0] = 10)

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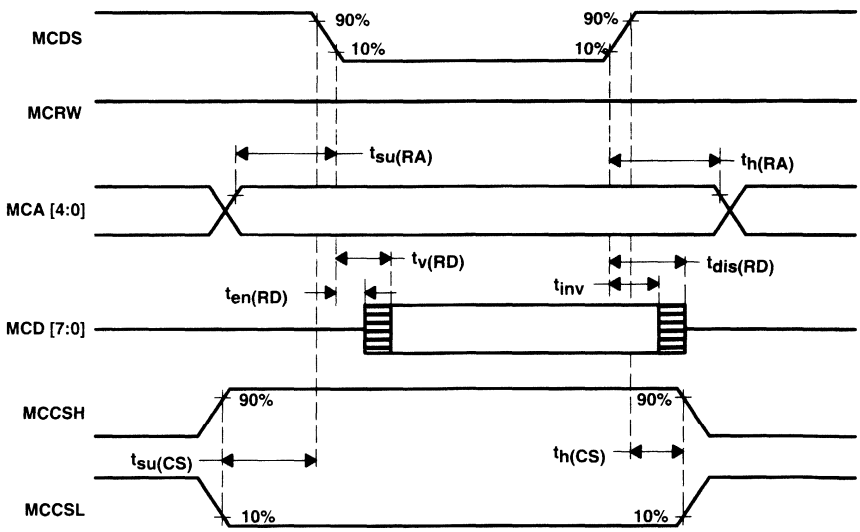
PARAMETER MEASUREMENT INFORMATION

TCM4300 to microcontroller interface timing requirements (Intel read cycle)

PARAMETER			ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(RA)}$	Setup time, read address	Read address (MCA) stable before falling edge of strobe (MCDS)	$TRA_{(SU)}$	0		ns
$t_{h(RA)}$	Hold time, read address	Read address (MCA) stable after rising edge of strobe (MCDS)	$TRA_{(HO)}$	10		ns
$t_{en(RD)}$	Enable time, read data	Falling edge of strobe (MCDS) to TCM4300 driving data bus (MCD)	$TRD_{(EN)}$	10		ns
$t_{v(RD)}$	Valid time, read data	Falling edge of strobe (MCDS) to valid data (MCD)	$TRD_{(DV)}$		50	ns
t_{inv}	Data invalid time	Data (MCD) invalid after rising edge of strobe (MCDS)	$TRD_{(INV)}$		10	ns
$t_{dis(RD)}$	Disable time, read data	TCM4300 releases data bus after rising edge of strobe (MCDS)	$TRD_{(DIS)}$		28	ns
$t_{su(CS)}$	Setup time, chip select	Chip select (MCCSH and MCCSL) stable before falling edge of strobe (MCDS)	$TCS_{(SU)}$	0		ns
$t_{h(CS)}$	Hold time, chip select	Chip select (MCCSH and MCCSL) stable before rising edge of strobe (MCDS)	$TCS_{(HO)}$	0		ns

NOTE: Timings are based upon Intel 80C186 (16 MHz).



NOTE: Chip selection is defined as both MCCS and MCDS active.

Figure 16. Microcontroller Interface Timing Requirements (Intel Configuration Read Cycle, MTS[1:0] = 00)

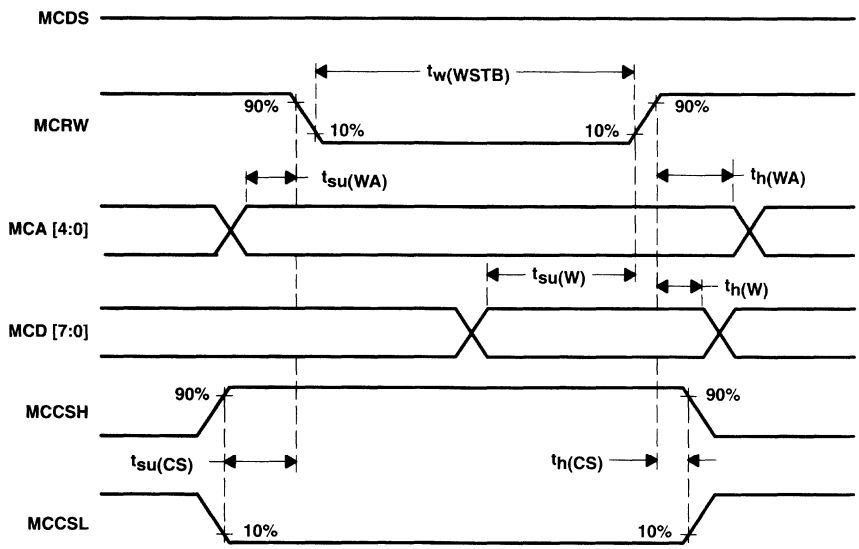
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

TCM4300 to microcontroller interface timing requirements (Intel write cycle)

PARAMETER			ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(WA)}$	Setup time, write address	Address (MCA) stable before falling edge of strobe (MCRW)	$TWA_{(SU)}$	0		ns
$t_{h(WA)}$	Hold time, write address	Address (MCA) stable after rising edge of strobe (MCRW)	$TWA_{(HO)}$	10		ns
$t_{su(W)}$	Setup time, write data	Data stable (MCD) before rising edge of strobe (MCRW)	$TWD_{(SU)}$	14		ns
$t_{h(W)}$	Hold time, write data	Data stable (MCD) after rising edge of strobe (MCRW)	$TWD_{(HO)}$	0		ns
$t_{w(WSTB)}$	Pulse duration, write strobe	Write strobe pulse width	$TWR_{(STB)}$	60		ns
$t_{su(CS)}$	Setup time, chip select	Chip select (MCCSH and MCCSL) stable before falling edge of strobe (MCRW)	$TCS_{(SU)}$	0		ns
$t_{h(CS)}$	Hold time, chip select	Chip select (MCCSH and MCCSL) stable before rising edge of strobe (MCRW)	$TCS_{(HO)}$	0		ns

NOTE: Timings are based upon Intel 8C186 (16 MHz).



NOTE: Chip selection is defined as both MCCS and MCRW active.

Figure 17. Microcontroller Interface Timing Requirements (Intel Configuration Write Cycle, MTS[1:0] = 00)

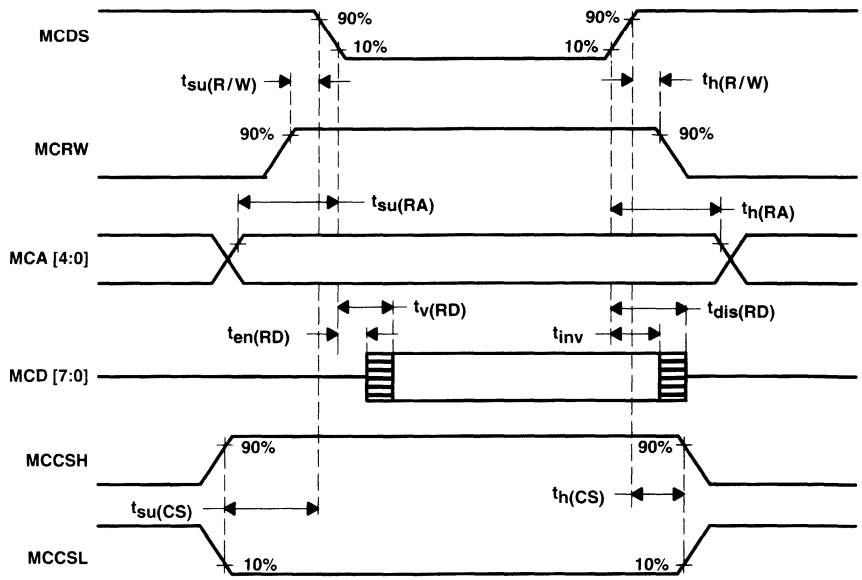
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

TCM4300 to microcontroller interface timing requirements (Motorola 16-bit read cycle)

PARAMETER			ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(R/W)}$	Setup time, read/write	Read/write (MCRW) stable before falling edge of strobe (MCDS)	$TRW_{(SU)}$	0		ns
$t_{h(R/W)}$	Hold time, read/write	Read/write (MCRW) stable after rising edge of strobe (MCDS)	$TRW_{(HO)}$	10		ns
$t_{su(RA)}$	Setup time, read address	Read address (MCA) stable before falling edge of strobe (MCDS)	$TRA_{(SU)}$	0		ns
$t_{h(RA)}$	Hold time, read address	Read address (MCA) stable after rising edge of strobe (MCDS)	$TRA_{(HO)}$	10		ns
$t_{en(RD)}$	Enable time, read data	Falling edge of strobe (MCDS) to TCM4300 driving data bus (MCD)	$TRD_{(EN)}$	10		ns
$t_{v(RD)}$	Valid time, read data	Falling edge of strobe (MCDS) to valid data (MCD)	$TRD_{(DV)}$		50	ns
t_{inv}	Data invalid time	Data (MCD) invalid after rising edge of strobe (MCDS)	$TRD_{(INV)}$		10	ns
$t_{dis(RD)}$	Disable time, read data	TCM4300 releases data bus after rising edge of strobe (MCDS)	$TRD_{(DIS)}$		28	ns
$t_{h(CS)}$	Hold time, chip select	Chip select (MCCSH and MCCSL) stable before falling edge of strobe (MCDS)	$TCS_{(HO)}$	0		ns
$t_{su(CS)}$	Setup time, chip select	Chip select stable (MCCSH and MCCSL) before rising edge of strobe (MCDS)	$TCS_{(SU)}$	0		ns

NOTE: Timings are based upon Motorola 68HC000 (16.67 MHz) and Motorola 68302 (16 MHz).



NOTE: Chip selection is defined as both MCCS and MCDS active.

Figure 18. Microcontroller Interface Timing Requirements (Motorola 16-Bit Read Cycle, MTS[1:0] = 10)

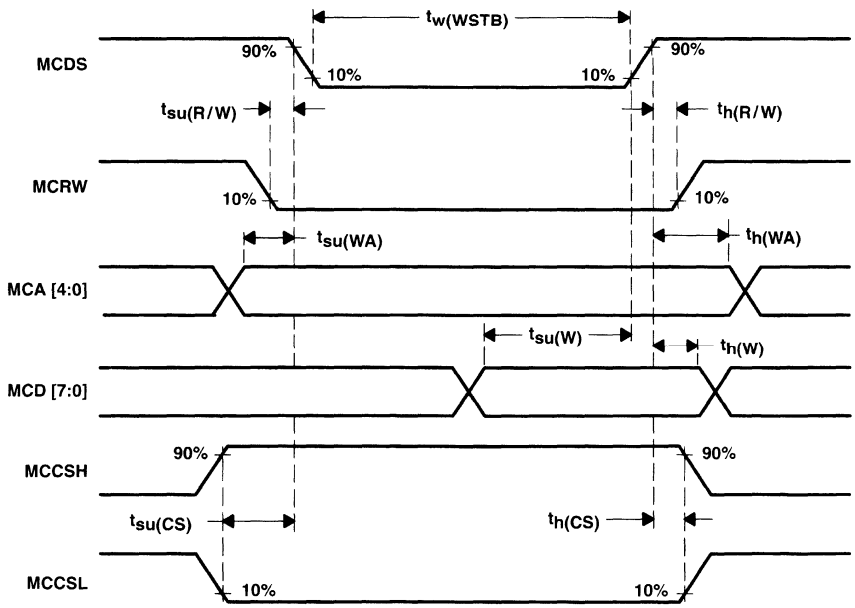
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

TCM4300 to microcontroller interface timing requirements (Motorola 16-bit write cycle)

PARAMETER			ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(R/W)}$	Setup time, read/write	Read/write (MCRW) stable before falling edge of strobe (MCDS)	$TRW_{(SU)}$	0		ns
$t_{h(R/W)}$	Hold time, read/write	Read/write (MCRW) stable after rising edge of strobe (MCDS)	$TRW_{(HO)}$	10		ns
$t_{su(WA)}$	Setup time, write address	Address (MCA) stable before falling edge of strobe (MCDS)	$TWA_{(SU)}$	0		ns
$t_{h(WA)}$	Hold time, write address	Address (MCA) stable after rising edge of strobe (MCDS)	$TWA_{(HO)}$	10		ns
$t_{su(W)}$	Setup time, write data	Data stable (MCD) before rising edge of strobe (MCDS)	$TWD_{(SU)}$	14		ns
$t_{h(W)}$	Hold time, write data	Data stable (MCD) after rising edge of strobe (MCDS)	$TWD_{(HO)}$	0		ns
$t_{w(WSTB)}$	Pulse duration, write strobe	Write strobe pulse width	$TWR_{(STB)}$	60		ns
$t_{h(CS)}$	Hold time, chip select	Chip select (MCCSH and MCCSL) stable before falling edge of strobe (MCDS)	$TCS_{(HO)}$	0		ns
$t_{su(CS)}$	Setup time, chip select	Chip select (MCCSH and MCCSL) stable before rising edge of strobe (MCDS)	$TCS_{(SU)}$	0		ns

NOTE: Timings are based upon Motorola 68HC000 (16.67 MHz) and Motorola 68302 (16 MHz).



NOTE: Chip selection is defined as both MCCS and MCDS active.

Figure 19. Microcontroller Interface Timing Requirements (Motorola 16-Bit Write Cycle, MTS[1:0] = 10)

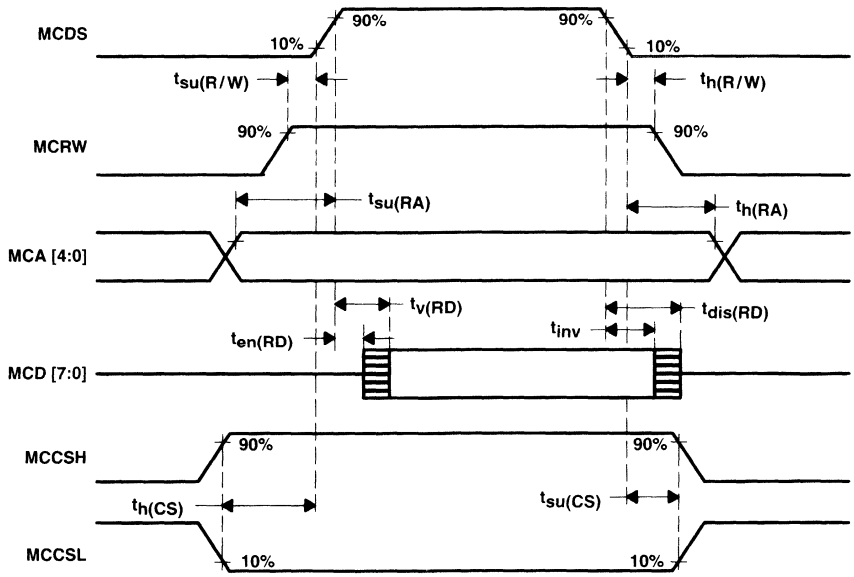
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

TCM4300 to microcontroller interface timing requirements (Motorola 8-bit read cycle)

PARAMETER			ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(R/W)}$	Setup time, read/write	Read/write (MCRW) stable before rising edge of strobe (MCDS)	$TRW_{(SU)}$	0		ns
$t_{h(R/W)}$	Hold time, read/write	Read/write (MCRW) stable after falling edge of strobe (MCDS)	$TRW_{(HO)}$	10		ns
$t_{su(RA)}$	Setup time, read address	Read address (MCA) stable before rising edge of strobe (MCDS)	$TRA_{(SU)}$	0		ns
$t_{h(RA)}$	Hold time, read address	Read address (MCA) stable after falling edge of strobe (MCDS)	$TRA_{(HO)}$	10		ns
$t_{en(RD)}$	Enable time, read data	Rising edge of strobe (MCDS) to TCM4300 driving data bus (MCD)	$TRD_{(EN)}$	10		ns
$t_{v(RD)}$	Valid time, read data	Rising edge of strobe (MCDS) to valid data (MCD)	$TRD_{(DV)}$		50	ns
t_{inv}	Data invalid time	Data (MCD) invalid after falling edge of strobe (MCDS)	$TRD_{(INV)}$		10	ns
$t_{dis(RD)}$	Disable time, read data	TCM4300 releases data bus after falling edge of strobe (MCDS)	$TRD_{(DIS)}$		28	ns
$t_{h(CS)}$	Hold time, chip select	Chip select (MCCSH and MCCSL) stable before falling edge of strobe (MCDS)	$TCS_{(HO)}$	0		ns
$t_{su(CS)}$	Setup time, chip select	Chip select (MCCSH and MCCSL) stable before rising edge of strobe (MCDS)	$TCS_{(SU)}$	0		ns

NOTE: Timings are based upon Motorola 68HC11D3 (3 MHz) and Motorola 68HC11G5 (2.1 MHz).



NOTE: Chip selection is defined as both MCCS and MCDS active.

Figure 20. Microcontroller Interface Timing Requirements (Motorola 8-Bit Read Cycle, MTS[1:0] = 01)

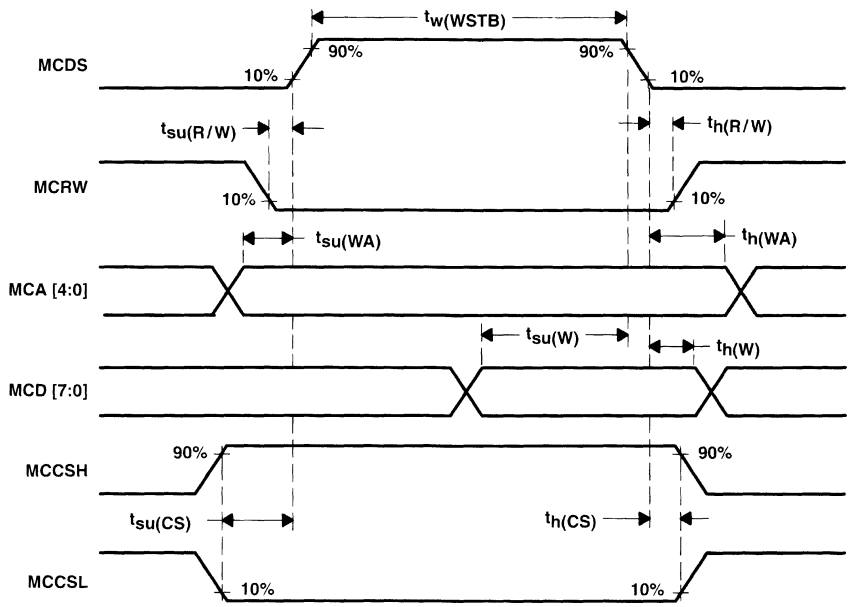
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

TCM4300 to microcontroller interface timing requirements (Motorola 8-bit write cycle)

PARAMETER			ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(R/W)}$	Setup time, read/write	Read/write (MCRW) stable before rising edge of strobe (MCDS)	$TRW_{(SU)}$	0		ns
$t_{h(R/W)}$	Hold time, read/write	Read/write (MCRW) stable after falling edge of strobe (MCDS)	$TRW_{(HO)}$	10		ns
$t_{su(WA)}$	Setup time, write address	Address (MCA) stable before rising edge of strobe (MCDS)	$TWA_{(SU)}$	0		ns
$t_{h(WA)}$	Hold time, write address	Address (MCA) stable after falling edge of strobe (MCDS)	$TWA_{(HO)}$	10		ns
$t_{su(W)}$	Setup time, write data	Data stable (MCD) before falling edge of strobe (MCDS)	$TWD_{(SU)}$	14		ns
$t_{h(W)}$	Hold time, write data	Data stable (MCD) after falling edge of strobe (MCDS)	$TWD_{(HO)}$	0		ns
$t_{w(WSTB)}$	Pulse duration, write strobe	Write strobe pulse width	$TWR_{(STB)}$	60		ns
$t_{h(CS)}$	Hold time, chip select	Chip select (MCCSH and MCCSL) stable before rising edge of strobe (MCDS)	$TCS_{(HO)}$	0		ns
$t_{su(CS)}$	Setup time, chip select	Chip select (MCCSH and MCCSL) stable before falling edge of strobe (MCDS)	$TCS_{(SU)}$	0		ns

NOTE: Timings are based upon Mitsubishi 37732S4 (16 MHz) and Mitsubishi 3772S4L (8 MHz).



NOTE: Chip selection is defined as both MCCS and MCDS active.

Figure 21. Microcontroller Interface Timing Requirements (Motorola 8-Bit Write Cycle, MTS[1:0] = 01)

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

switching characteristics, TCM4300 to DSP Interface (write cycle)

PARAMETER			ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(R/W)}$	Setup time, read/write	Read/write (DSPRW) stable before falling edge of strobe (DSPSTRBL)	$TRW_{(SU)}$	0		ns
$t_{h(R/W)}$	Hold time, read/write	Read/write (DSPR W) stable after rising edge of strobe (DSPSTRBL)	$TRW_{(HO)}$	0		ns
$t_{su(CS)}$	Setup time, chip select	Chip select stable (DSPCSL) before falling edge of strobe (DSPSTRBL)	$TCS_{(SU)}$	0		ns
$t_{h(CS)}$	Hold time, chip select	Chip select (DSPCSL) stable after rising edge of strobe (DSPSTRBL)	$TCS_{(HO)}$	0		ns
$t_{su(WA)}$	Setup time, write address	Address (DSPA) stable before falling edge of strobe (DSPSTRBL)	$TWA_{(SU)}$	0		ns
$t_{h(WA)}$	Hold time, write address	Address (DSPA) stable after rising edge of strobe (DSPSTRBL)	$TWA_{(HO)}$	0		ns
$t_{su(W)}$	Setup time, write data	Data stable (DSPD) before rising edge of strobe (DSPSTRBL)	$TWD_{(SU)}$	3		ns
$t_{h(W)}$	Hold time, write data	Data stable (DSPD) after rising edge of strobe (DSPSTRBL)	$TWD_{(HO)}$	0		ns
$t_{w(WSTB)}$	Pulse duration, write strobe	Write strobe pulse width	$TWR_{(STB)}$	25		ns

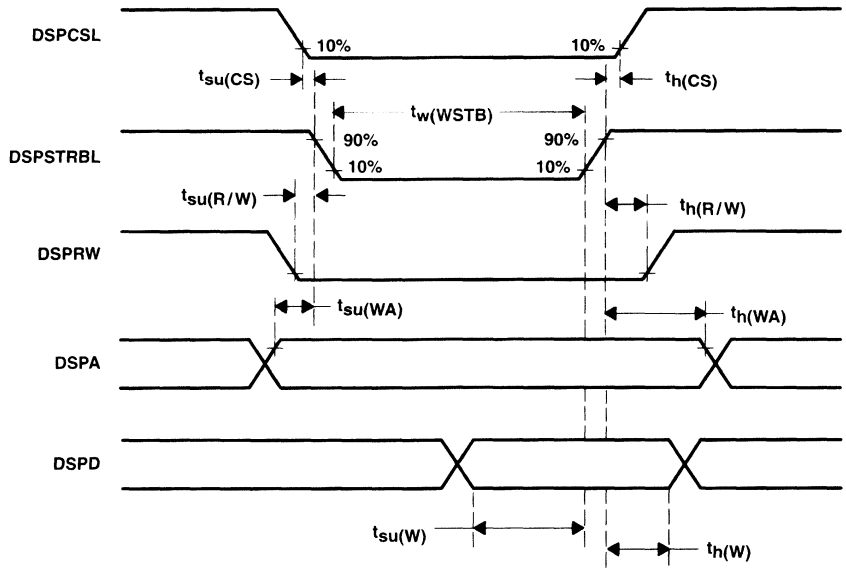


Figure 22. TCM4300 to DSP Interface (Write Cycle)

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

switching characteristics, TCM4300 to DSP Interface (read cycle)

PARAMETER			ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(R/W)}$	Setup time, read/write	Read/write (DSPRW) stable before falling edge of strobe (DSPSTRBL)	$TRW_{(SU)}$	0		ns
$t_{h(R/W)}$	Hold time, read/write	Read/write (DSPRW) stable after rising edge of strobe (DSPSTRBL)	$TRW_{(HO)}$	0		ns
$t_{su(CS)}$	Setup time, chip select	Chip select stable (DSPCSL) before falling edge of strobe (DSPSTRBL)	$TCS_{(SU)}$	0		ns
$t_{h(CS)}$	Hold time, chip select	Chip select (DSPCSL) stable after rising edge of strobe (DSPSTRBL)	$TCS_{(HO)}$	0		ns
$t_{su(RA)}$	Setup time, read address	Read address (DSPA) stable before strobe (DSPSTRBL) goes low	$TWA_{(SU)}$	0		ns
$t_{h(RA)}$	Hold time, read address	Read address (DSPA) stable after strobe (DSPSTRBL) goes high	$TWA_{(HO)}$	0		ns
$t_{en(R)}$	Enable time, read data	Falling edge of strobe (DSPSTRBL) to TCM4300 driving data bus (DSPD)	$TRD_{(EN)}$	0		ns
$t_{d(DV)}$	Delay read data valid time	Falling edge of strobe (DSPSTRBL) to valid data (DSPD)	$TRD_{(DV)}$		50	ns
$t_{h(R)}$	Hold time, read data	Data (DSPD) invalid after rising edge of strobe (DSPSTRBL)	$TRD_{(INV)}$	5		ns
$t_{dis(R)}$	Disable time, read data	TCM4300 releases data bus after rising edge of strobe (DSPSTRBL)	$TRD_{(DIS)}$		12	ns

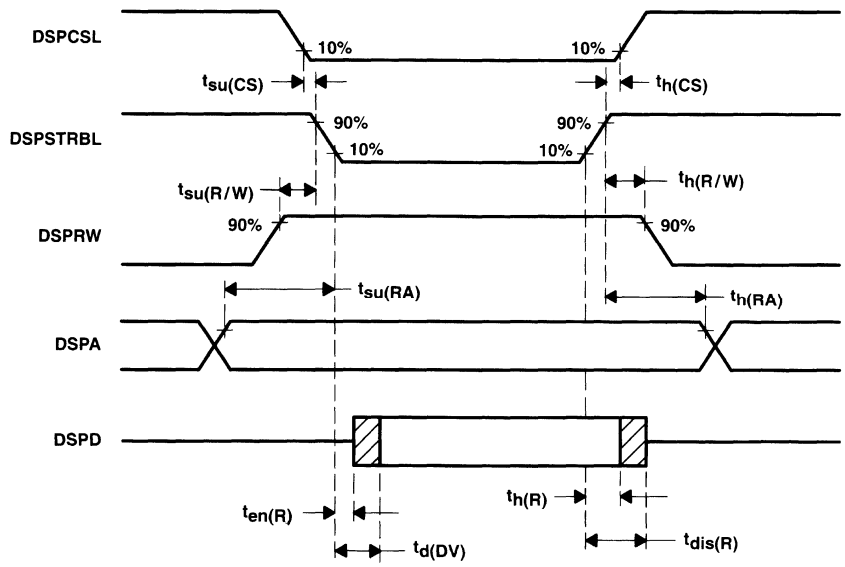


Figure 23. TCM4300 to DSP Interface (Read Cycle)

PRODUCT PREVIEW

TCM4301
ADVANCED RF CELLULAR TELEPHONE INTERFACE CIRCUIT (ARCTIC™136)

SLWS042 – JUNE 1996

- **Compliance With TIA IS-136 Dual-Mode Cellular Standard**
- **Baseband Transmit Digital-to-Analog (D/A) Conversion and Receive Analog-to-Digital (A/D) Conversion in Analog Mode Using Dual 10-Bit Sigma-Delta Converters**
- **Square Root Raised Cosine (SQRC) Filtering in the Digital Mode Using Dual 10-Bit Sigma-Delta Converters**
- **$\pi/4$-Differential Quadrature Phase-Shift Key (DQPSK) Modulation Encoder in Digital Transmit Mode**
- **Power Control Supervision for Radio Frequency (RF) Power Amplifier, Automatic Frequency Control (AFC), Automatic Gain Control (AGC), and Synthesizer**
- **Received Signal Strength Indicator (RSSI) and Battery-Level A/D Conversion Circuitry**
- **Internal Clock Generation**
- **Wide-Band Data Clock Recovery and Manchester Decoding**
- **General-Purpose Digital Signal Processing (DSP) and Microcontroller Interface**
- **3.3-V and 5-V Operation**
- **Low Power Consumption**
- **Backward Compatible With TCM4300 ARCTIC**

description

Texas Instruments (TI™) TCM4301 IS-136 advanced RF cellular telephone interface circuit (ARCTIC™136) provides a baseband interface between digital signal processor (DSP), microcontroller, and RF modulator/demodulator in a dual-mode IS-136 cellular telephone.

In the analog mode, the TCM4301 provides all required baseband filtering as well as transmit D/A conversion and receive A/D conversion using dual 10-bit sigma-delta converters. In addition, a WBD (wide-band data) –10 kb/s Manchester frequency shift key (FSK) demodulator is provided to allow reduced DSP processing load during subscriber standby mode.

In the digital mode, the TCM4301 accepts I and Q baseband data and performs A/D and D/A conversion and square root raised cosine filtering using dual 10-bit sigma-delta converters. The TCM4301 also has a $\pi/4$-DQPSK modulation encoder for dibit-to-symbol conversion in the digital transmit mode.

The microcontroller interface is compatible with a wide range of microcontrollers. A microcontroller can be used to communicate with the user interface (keyboard, display, etc.) and to program up to three frequency synthesizers by using the on-chip synthesizer interface circuit.

The TCM4301 provides advanced power control to minimize power consumption of many dual-mode telephone functional blocks such as the speech codec, FM receiver, I and Q demodulator, transmitter signal processor, and RF power amplifier. In addition, the TCM4301 is designed to reduce system power consumption through low-voltage operation and standby mode (see Table 1).

The TCM4301 is offered in the 100-pin PZ package and is characterized for free-air operation from –40°C to 85°C.

PRODUCT PREVIEW

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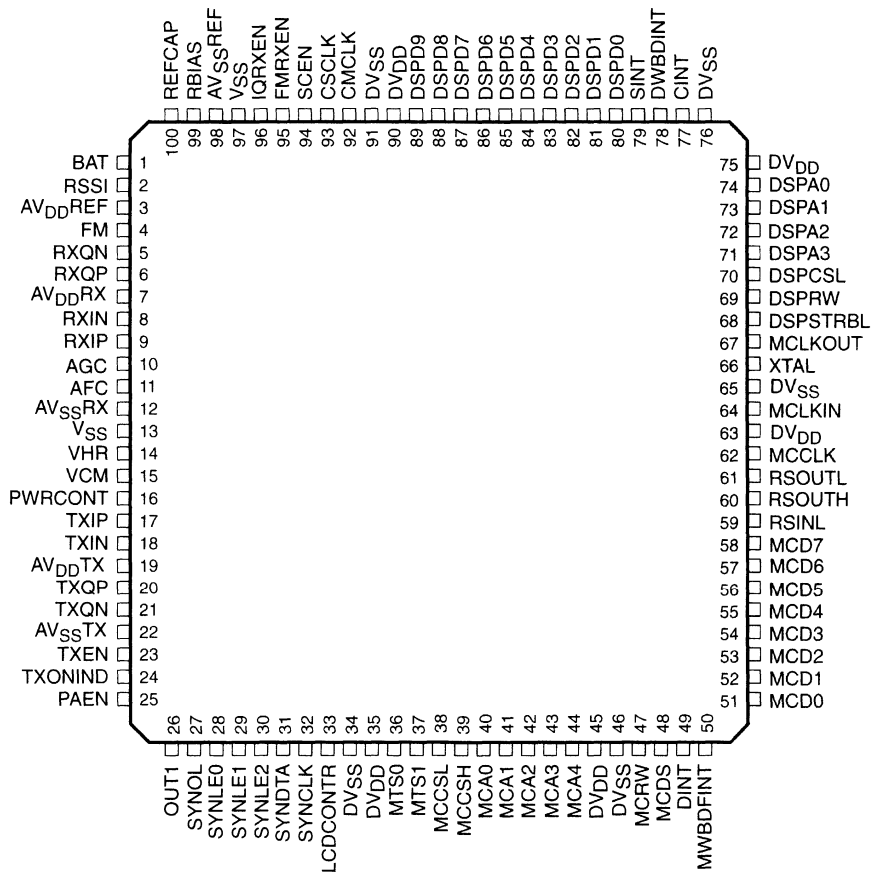
PRODUCT PREVIEW

description (continued)

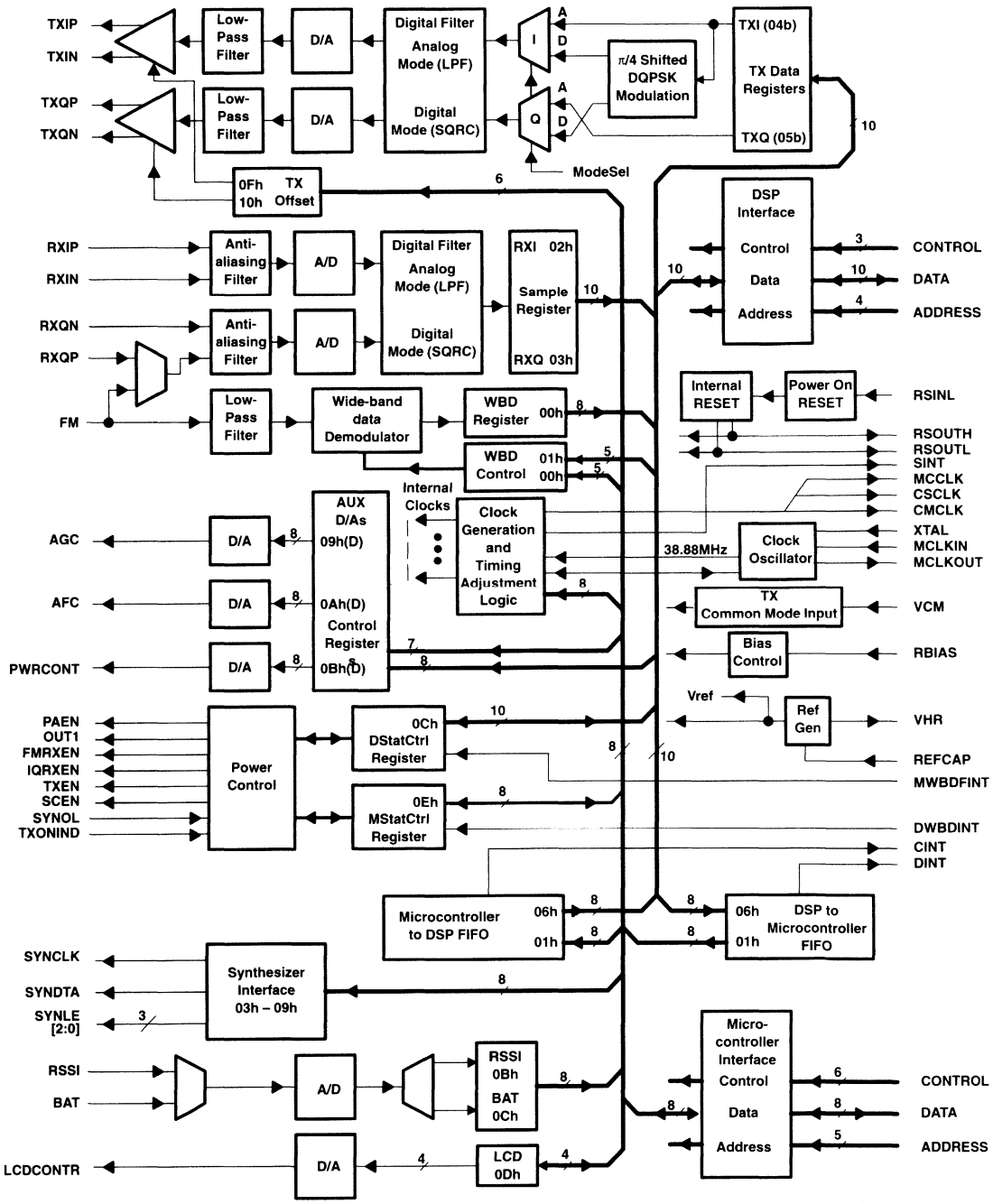
Table 1. Typical Power Consumption

OPERATING MODE		3 V	5.5 V
Analog transmitting and receiving		75 mW	275 mW
Digital receiving		60 mW	250 mW
Digital transmitting		85 mW	300 mW
Idle mode	MCLKOUT enabled	45 mW	190 mW
	MCLKOUT disabled	17 mW	96 mW
IS-136 standby (sleep mode)		15 mW	85 mW
Digital mode, 1/3 transmitting + 1/3 receiving +1/3 standby		60 mW	220 mW

PZ PACKAGE
(TOP VIEW)



functional block diagram



PRODUCT PREVIEW

Terminal Functions

RF interface analog signals

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
			RECEIVE CHANNEL
FM	4	I	Input from FM discriminator analog mode voice and wide band data
RXIN	8	I	In-phase differential negative baseband received signal
RXIP	9	I	In-phase differential positive baseband received signal
RXQN	5	I	Quadrature differential negative baseband received signal
RXQP	6	I	Quadrature differential positive baseband received signal
			TRANSMIT CHANNEL
TXIN	18	O	In-phase differential negative baseband transmit signal
TXIP	17	O	In-phase differential positive baseband transmit signal
TXQN	21	O	Quadrature differential negative baseband transmit signal
TXQP	20	O	Quadrature differential positive baseband transmit signal
			MONITORS
BAT	1	I	Battery strength monitor
RSSI	2	I	Received signal strength indicator. Used for signal strength measurements
			CONTROLS
AGC	10	O	Automatic gain control digital-to-analog converter (DAC) output
AFC	11	O	Automatic frequency control DAC output
LCDCONTR	33	O	Liquid-crystal display (LCD) contrast control DAC output
PWRCONT	16	O	Power amplifier (PA) power control DAC output
			BIAS SETTING
RBIAS	99	I	Input for bias current-setting resistor. A 100 kΩ, 1% tolerance resistor to AV_{SS} is recommended.
REFCAP	100	I	Input for reference decoupling capacitor. 3.3 µF in parallel with 470 pF is recommended.

RF interface digital signals

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
			POWER AMPLIFIER, SYNTHESIZER, AND TRANSMIT CONTROLS
PAEN	25	O	Power enable for the transmit power amplifier, active high
OUT1	26	O	User-defined general purpose data or control signal
SYNCLK	32	O	Synthesizer serial-data clock
SYNDTA	31	O	Synthesizer serial-data bit
SYNLE0	28	O	Synthesizer 0, 1, and 2 latch enables. An active high indicates the latch is enabled.
SYNLE1	29		
SYNLE2	30		
SYNOL	27	I	Synthesizer out-of-lock indicator. Active high indicates out of lock.
TXEN	23	O	Power enable signal. Enables transmit signal processing, active high
TXONIND	24	I	Transmit on indicator. Signal indicating power is applied to the power amplifier.

PRODUCT PREVIEW

Terminal Functions (Continued)

miscellaneous digital signals

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
RSINL	59	I	Reset input, active low
RSOUTH	60	O	Power on reset output, active high. On power up, RSOUTH goes high for 10 ms.
RSOUTL	61	O	Power on reset output, active low. On power up, RSOUTL goes low for 10 ms causing an internal reset of the TCM4301.
CLOCKS			
CMCLK	92	O	Codec master clock. 2.048 MHz clock provided as master clock and bit clock for speech codec.
CSCLK	93	O	Codec sample clock. 8-kHz frame synchronization pulse for speech codec. Connected to DSP for speech sample interrupts.
MCCLK	62	O	Microcontroller clock. Adjustable frequency with 1.215 MHz on powerup.
MCLKIN	64	I	Master clock input. Frequency 38.88 MHz ± 100 ppm. A crystal can be connected between MCLKIN and XTAL to provide an oscillator circuit. Alternately, XTAL can be left open and an external TTL/CMOS-level clock signal can be connected to MCLKIN.
MCLKOUT	67	O	Buffered version of MCLKIN
XTAL	66	I	Use with MCLKIN to form an oscillator circuit
POWER ENABLES			
FMRXEN	95	O	Power enable for receiver FM path, active high
IQRXEN	96	O	Power enable for receiver I/Q path, active high
SCEN	94	O	Power enable for speech codec, active high

DSP interface

TERMINAL NAME	TERMINAL NO.	I/O/Z	DESCRIPTION
CINT	77	O	Controller data interrupt. Microcontroller data interrupt (active low) sent to DSP. Caused by the microcontroller writing into the Send-C Int register location.
DSPA0	74	I	DSP 4-bit parallel address bus. DSPA3 is the MSB, and DSPA0 is the LSB.
DSPA1	73		
DSPA2	72		
DSPA3	71		
DSPCSL	70	I	DSP interface chip select, active low
DSPD0	80	I/O/Z	DSP 10-bit parallel data bus. DSPD9 is the MSB, and DSPD0 is the LSB.
DSPD1	81		
DSPD2	82		
DSPD3	83		
DSPD4	84		
DSPD5	85		
DSPD6	86		
DSPD7	87		
DSPD8	88		
DSPD9	89		
DSPRW	69	I	DSP read/write signal. DSPRW is active high for read cycles and active low for write cycles.
DSPSTRBL	68	I	DSP strobe signal, active low
DWBDINT	78	O	DSP wide-band data interrupt. Wide-band data-ready interrupt (active low) caused by WBD demodulation circuits.
SINT	79	O	Sample interrupt (active low). Operates at 40 kHz in the analog mode and 48.6 kHz in the digital mode and as sleep interrupt in the sleep mode.

PRODUCT PREVIEW

Terminal Functions (Continued)

microcontroller interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
DINT	49	O	Microcontroller interrupt request signal. DSP data-ready interrupt sent to controller. Caused by DSP writing into SEND DINT register location. DINT can be active high or low according to the levels of the MTS (1:0) signals.
MCA0	40	I	Microcontroller 5-bit parallel address bus. MCA4 is the MSB, and MCA0 is the LSB.
MCA1	41		
MCA2	42		
MCA3	43		
MCA4	44		
MCCSH	39	I	Microcontroller interface chip-select signal, active high. Chip select occurs if MCCSH is high and MCCSL is low.
MCCSL	38	I	Microcontroller interface chip-select signal, active low. Chip select occurs if MCCSH is high and MCCSL is low.
MCD0	51	I/O/Z	Microcontroller 8-bit parallel data bus. MCD7 is the MSB, and MCD0 is the LSB.
MCD1	52		
MCD2	53		
MCD3	54		
MCD4	55		
MCD5	56		
MCD6	57		
MCD7	58		
MCDS	48	I	Microcontroller data strobe. Operational characteristics are selected by MTS (1:0).
MCRW	47	I	Microcontroller read/write. Operational characteristics are selected by MTS (1:0).
MTS0	36	I	Microcontroller type select configuration control inputs. The interface is controlled by MTS (1:0) as follows: 00 – Intel™ microcontroller interface characteristics 10 – Mitsubishi™ microcontroller and Motorola microcontroller 16-bit bus interface characteristics 01 – Motorola™ microcontroller 8-bit bus characteristics 11 – Reserved
MTS1	37	I	
MWBDFINT	50	O	Microcontroller interrupt request signal. Wide-band data-ready interrupt caused by WBD demodulator in analog mode or frame interrupt sent by the DSP in digital mode. MWDBFINT can be active high or low, according to the levels of the MTS (1:0) signals.

PRODUCT PREVIEW

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Terminal Functions (Continued)

supply and reference voltages

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$AV_{DD}RX$	7	—	Analog supply voltage for RX receive path
$AV_{DD}REF$	3	—	Analog supply voltage for RX FM receive path
$AV_{DD}TX$	19	—	Analog supply voltage for TX transmit path
$AV_{SS}REF$	98	—	Analog ground for REFCAP
$AV_{SS}RX$	12	—	Analog ground for RX receive path
$AV_{SS}TX$	22	—	Analog ground for TX transmit path
DV_{DD}	35, 45, 63, 75, 90	—	Digital power supply. All supply pins must be connected.
DV_{SS}	34, 46, 65, 76, 91	—	Digital ground. All supply pins must be connected.
VCM	15	I	Voltage common mode. VCM is used to establish dc operating point for TX outputs and can be tied to VHR.
VHR	14	O	Half-rail reference voltage (VHR), approximately $0.5 \times AV_{DD}$. VHR is used to establish dc operating point for RX inputs.
V_{SS}	13, 97	—	Substrate ground

detailed description

data transfer

The interface to both the system digital signal processor and microcontroller is in the form of 2s complement.

receive section

The mode of operation is determined by the state of the MODE, FMVOX, IQRXEN, and FMRXEN bits of the DStatCtrl register, as shown in Table 2. The specifications for the receive section are included in Table 3.

Table 2. TCM4301 Receive Channel Control Signals

CONTROL SIGNAL	ANALOG MODE	DIGITAL MODE
MODE	0	1
FMVOX	1	0
IQRXEN	0	1
FMRXEN	1	0

In the digital mode (MODE=1), the receive section accepts RXIP, RXIN, RXQP, and RXQN analog inputs. These inputs are passed to continuous-time antialiasing filters (AAF), baseband filtering, and A/D conversion blocks, and then to sample registers where 10-bit registers can be read. The sample rate is 48.6 ksps.

In the analog mode (MODE = 0), the FMVOX bit of the DStatCtrl register enables or disables the Q side of the receiver channel, and the FMRXEN bit controls the external functions. In the digital mode, IQRXEN enables both the I and Q receive channels and external functions as well.

To save power, the receive I and Q channels are enabled separately. This operation occurs because in the analog mode, only the Q channel is used. When the FMVOX bit is set to 1, it controls the input multiplexer, connects the FM input to the receiver RXQP signal, and connects the RXQN to VHR. When the MODE control bit and the IQRXEN control bit are set to 1, both sides of the receive channel are enabled for use in the digital mode.

PRODUCT PREVIEW

receive section (continued)

The input signals RXIP, RXIN, and RXQP, RXQN are differential pair signals. Differential signals are used to minimize the pickup of interference and ground and supply noise, while maintaining a larger signal level. In single-ended applications, the unused RXIN and RXQN terminals must be connected to VHR or to an externally supplied bias voltage, and the input signal level must be adjusted in the RF circuitry to provide a higher level signal so that the digital output codes are properly calibrated (0.5 V peak-to-peak corresponds to full-scale digital output). In the analog mode, the RXQN input is internally referenced to VHR. Alternatively, the unused inputs can be connected to VHR and the used inputs can be capacitively coupled. Note that when the RX and FM inputs are capacitively coupled, the input pins to the TCM4301 are self-biased to VHR; no external bias is needed at the input pins.

The single-ended output of an external FM discriminator is connected to the FM pin for analog mode voice and WBD reception. The signal at this pin is conveyed to the Q side of the receiver via the multiplexer, and the other Q input is connected internally to the VHR reference voltage. The I input of the RX circuitry is disabled in the analog mode. The FM signal passes through the antialiasing filter, as specified in Table 4, before passing through the A/D converter. The signal at the FM pin is also routed directly to the WBD demodulator through a low-pass filter (LPF) with the –3 dB point at 270 kHz.

The VHR can provide a bias voltage for the received inputs when capacitively coupled from the RF section. To meet noise requirements, the VHR output should have an external decoupling capacitor connected to ground. The VHR output buffer is enabled by the OR of TXEN, FMVOX, and IQRXEN. The VHR output is high impedance otherwise.

In the digital mode, both the I and Q receive sides are enabled. Table 5 lists the receive channel frequency response.

When the I and Q sample conversion is complete and the data is placed in the RXI and RXQ sample registers, the SINT interrupt line is asserted to indicate the presence of that data. This occurs at 48.6-kHz rate in the digital mode and at 40-kHz rate in the analog mode. In the analog mode, only the RXQ conversion path is used, and the RXI path is powered down.

Table 3. RXIP, RXIN, RXQP, and RXQN Inputs (AV_{DD} = 3 V, 4.5 V, 5 V)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Common-mode input voltage range			0.3		AV_{DD}–0.3	V
Input voltage for full-scale digital output	Differential			0.5		Vp-p
	Single-ended			0.5		
Nominal operating level	Differential			0.125		Vp-p. Provides 12 dB headroom for AGC fading conditions.
	Single-ended			0.125		
Input CMRR (RXI, RXQ)			45			dB
Sampling frequency, SINT				48.6/40		Digital/Analog kHz
Receive error vector magnitude (EVM)				6%	7%	
I/Q sample timing skew		Input signal 0 – 15 kHz		50		ns
A/D resolution				10		Bits
Signal to noise-plus distortion		Input at full scale – 1 dB	50	56		dB
Integral nonlinearity		0 dB to –60 dB input		1		LSB
Gain error (I or Q channel)					±10%	
Gain mismatch between I and Q					±0.3	dB
Differential dc offset voltage					±30	mV
FM input sensitivity				2.5		Vp-p for full scale (±14 kHz deviation)
FM input dc offset (wrt VHR)					±90	mV
FM input idle channel noise					–45	dB below full scale input
FM gain error					±7%	
Power supply rejection		f = 0 kHz to 15 kHz		40		dB

PRODUCT PREVIEW

receive section (continued)

Table 4. RX Channel Frequency Response (FM Input in Analog Mode)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Frequency response	2.5 V peak-to-peak,	0 kHz to 6 kHz (see Note 1)			±0.5	dB
	2.5 V peak-to-peak,	20 kHz to 30 kHz (see Note 2)	−18			
	2.5 V peak-to-peak,	34 kHz to 46 kHz (see Note 3)	−48			
Peak-to-peak group delay distortion	2.5 V peak-to-peak,	0 kHz to 6 kHz			2	µs
Absolute channel delay	2.5 V peak-to-peak,	0 kHz to 6 kHz		400		µs

NOTES: 1. Ripple magnitude
2. Stopband
3. Stopband and multiples of stopband

Table 5. RX Channel Frequency Response (RXI, RXQ Input in Digital Mode)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Frequency response	0.125 V peak-to-peak,	0 kHz to 8 kHz (see Note 4)		±0.5	±0.75	dB
	0.125 V peak-to-peak,	8 kHz to 15 kHz (see Note 4)			±1	
	0.125 V peak-to-peak,	16.2 kHz to 18 kHz (see Note 5)	−26			
	0.125 V peak-to-peak,	18 kHz to 45 kHz (see Note 5)	−30			
	0.125 V peak-to-peak,	45 kHz to 75 kHz (see Note 5)	−46			
	0.125 V peak-to-peak,	> 75 kHz	−60			
Peak-to-peak group delay distortion	0.125 V peak-to-peak,	0 kHz to 15 kHz			2	µs
Absolute channel delay, RXI, Q IN to digital OUT	0.125 V peak-to-peak,	0 kHz to 15 kHz		325		µs

NOTES: 4. Deviation from ideal 0.35 SQRC response
5. Stopband

transmit section

The transmit section operates in two distinct modes, digital or analog. The mode of operation is determined by the MODE bit of the DStatCtrl register. In the digital mode, data is input to the transmit section by writing to the TXI register. The resulting output is a $\pi/4$ DQPSK-modulated time division multiplexed (TDM) burst. In the analog mode, the data is in the form of direct I and Q samples which are written into both the TXI and TXQ registers, then D/A converted, filtered, and output through TXIP, TXIN, TXQP, and TXQN. The I and Q outputs are zero-IF FM signals; that is, no baseband connection is necessary for FM transmission.

In the digital mode (MODE=1), the data is written into the TXI register using the SINT interrupt to synchronize the data transfer. The TCM4301 performs parallel-to-serial conversion of the bits in the TXI register and encodes the resulting bit stream as $\pi/4$ DQPSK data samples. These samples are then filtered by a digital square root raised cosine (SQRC) shaping filter with a roll-off rate of $\alpha = 0.35$ and converted to sampled analog form by two 9-bit digital-to-analog converters (DACs). The output of the DAC is then filtered by a continuous-time resistance-capacitance (RC) filter.

The TCM4301 generates a power amplifier (PA) control signal, PAEN, to enable the power supply for the PA. The start and stop times of the TDM burst are controlled by writing to a single bit, TXGO in the DSP DStatCtrl register.

In the analog mode (MODE = 0), the DSP writes 8-bit I and Q samples into the TXI and TXQ data registers at a 40-ksps rate. These writes are timed by the SINT interrupt signal. The samples are fed to a low-pass filter before D/A conversion. In the transmit analog mode, the PAEN signal is always set to 1.

The transmitter section provides differential I and Q outputs for both analog and digital modes. The differential dc offset for the TXI and TXQ outputs can be independently adjusted using the TX offset registers.

transmit section (continued)

Table 6. Transmit I and Q Channel Outputs

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Peak output voltage full scale, centered at VCM	Differential		2.24		Vp
	Single-ended		1.12		
Nominal output-level (constellation radius) centered at VCM	Differential		1.5		V
	Single-ended		0.75		
Low-level drift			±200		PPM/°C
Transmit error vector magnitude (EVM)			3%	4%	
Resolution			8		bits
S/(N+D) ratio at differential outputs		40	48		dB
Gain error (I or Q channel)			±10%	±15%	
Gain mismatch between I and Q				±0.3	dB
Gain sampling mismatch between I and Q			20		ns
Zero code error differential				±90	mV
Zero code error, each output, with respect to VCM				±90	mV
Zero code error, I to Q, with respect to other channel (differential or single-ended)				±10	mV
Load impedance, between P and N pins		10			kΩ
Load capacitance				50	pF
VCM input voltage range		1.3		$AV_{DD}-1.3$	V
Transmit offset DACs I and Q resolution			6		bits
Transmit offset DACs I and Q average step size		3	3.4	3.9	mV
Transmit offset DACs I and Q full-scale positive output			105.4		mV
Transmit offset DACs I and Q full-scale negative output			−108.8		mV
Transmit offset DACs differential nonlinearity				±1.1	LSB
Transmit offset DACs integral nonlinearity				±1.1	LSB

Modulation Error: In the digital mode, during the transmit burst, the complex output of the transmitter circuits consists of an ideal output $s = I_{ideal} + jQ_{ideal}$ + error $e = e_i + je_q$. In Table 6, the modulation error (EVM) is defined as the peak value of the magnitude of e relative to the ideal output:

$$\text{Modulation error percentage} = 100\,\frac{|e|}{|s|}\,\%$$

PRODUCT PREVIEW

transmit section (continued)

Table 7 and Table 8 shows the frequency response of the transmit section for digital and analog mode, respectively.

Table 7. Transmit Channel Frequency Response (Digital Mode)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency response	0 kHz to 8 kHz (see Note 4)			±0.3	dB
	8 kHz to 15 kHz (see Note 4)			±0.5	
	20 kHz to 45 kHz (see Note 5)	−29			
	45 kHz to 75 kHz (see Note 5)	−55			
	> 75 kHz (see Note 5)	−60			
	Any 30 kHz band centered at > 90 kHz (see Note 5)	−60			
Peak-to-peak group delay distortion	0 kHz to 15 kHz			3	µs
Absolute channel delay	0 kHz to 15 kHz		320		µs

NOTES: 4. Deviation from ideal 0.35 SQRC response
5. Stopband

Table 8. Transmit Channel Frequency Response (Analog Mode)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency response	0 kHz to 8 kHz (see Note 1)			±0.5	dB
	8 kHz to 15 kHz (see Note 1)			±0.5	
	20 kHz to 45 kHz (see Note 5)	−31			
	45 kHz to 75 kHz (see Note 5)	−70			
	> 75 kHz (see Note 5)	−70			
	Any 30 kHz band centered at > 90 kHz (see Note 5)	−70			
Peak-to-peak group delay distortion	0 kHz to 15 kHz			3	µs
Absolute channel delay	0 kHz to 15 kHz		540		µs

NOTES: 1. Ripple magnitude
5. Stopband

PRODUCT PREVIEW

transmit burst operation (digital mode)

In the digital mode, the TCM4301 performs all encoding, signal processing, and power ramping for the burst. Start and stop timing of the variable length bursts are set by means of the TXGO bit in the DStatCtrl register. The SINT interrupt output interrupts the DSP at 48.6 kHz which is T/2 interval (T = 1 symbol period = 1/24.3 kHz). The burst is initiated by the DSP writing from 1 to 5 dibits to the TXI register, a small positive delay offset value d to the base station (BST) register, and a 1 to the TXGO bit in the DStatCtrl register.

The TXGO bit is sampled on the falling edge of SINT. The TX outputs are held at zero differential voltage (each output pin is held at the voltage supplied to the VCM input pin) for 9.5 SINT periods (195.5 μs) plus BST offset delay after SINT has detected TXGO high; then the TX outputs begin to ramp to the initial π/4 DQPSK constellation value. The shape of the ramp is the transient resulting from the internal SQRC filtering. At the same time that the TX outputs are beginning to ramp, the PAEN digital output goes high. This output can be used to enable the power amplifier of a cellular radio transmitter. The TCM4301 TX outputs reach the first π/4 DQPSK constellation value (maximum effect point, MEP) 6 SINT periods (3 symbol periods) after the start of the ramp.

The bit stream to be encoded as π/4 DQPSK symbols is generated by right shifts on each SINT of the TXI register with bit 0 (LSB) used first.

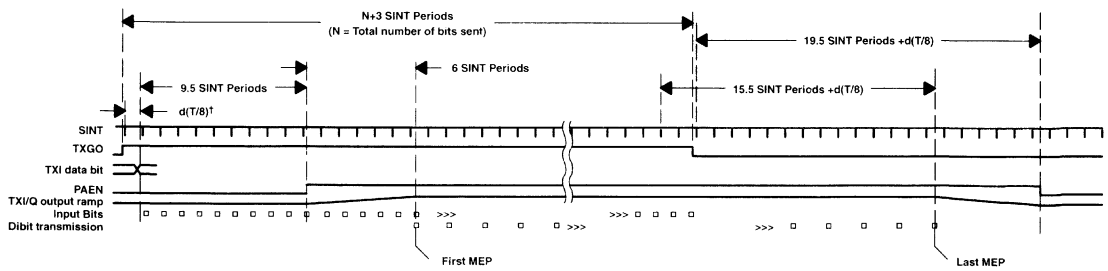
Previously written data continues to propagate through the TCM4301 internal filters until the last π/4 DQPSK constellation value (last MEP) occurs at the TX outputs 15.5 SINT periods (318.9 μs) plus BST offset delay after the last symbol occurs (2 SINT periods before TXGO goes low); then the TX outputs decay to zero differential voltage (each output at the voltage supplied to the VCM input pin). The shape of the decay is the transient resulting from the internal SQRC filtering. The TX outputs are held at zero differential voltage 6 SINT periods (3 symbol periods) after the start of the decay. At this time the PAEN digital output is set low (see Figure 1 and Figure 2).

Non-zero values of the BST offset register increase the delays of both the TX waveforms and PAEN relative to the edges of TXGO after it is internally sampled by SINT. The delays are increased in increments of 1/4 SINT (1/8 symbol period).

For delays of 1 SINT or greater, the fractional part of the delay can be achieved using the BST offset register with the remaining integer SINT delay implemented externally by delaying the writing to TXGO and TXI.

The relative timing of PAEN and the TX waveforms is not affected by the BST offset register.

The IS-136 standard describes shortened bursts and normal bursts. The two types differ in duration and number of transmitted bursts, burst length being determined by means of the TXGO bit.



† Total delay = d (SINT/4 or T/8) where d = integer value (0,1,2,3) written to the BST offset register.

Figure 1. Power Ramp-Up/Ramp-Down TIming Diagram

transmit burst operation (digital mode) (continued)

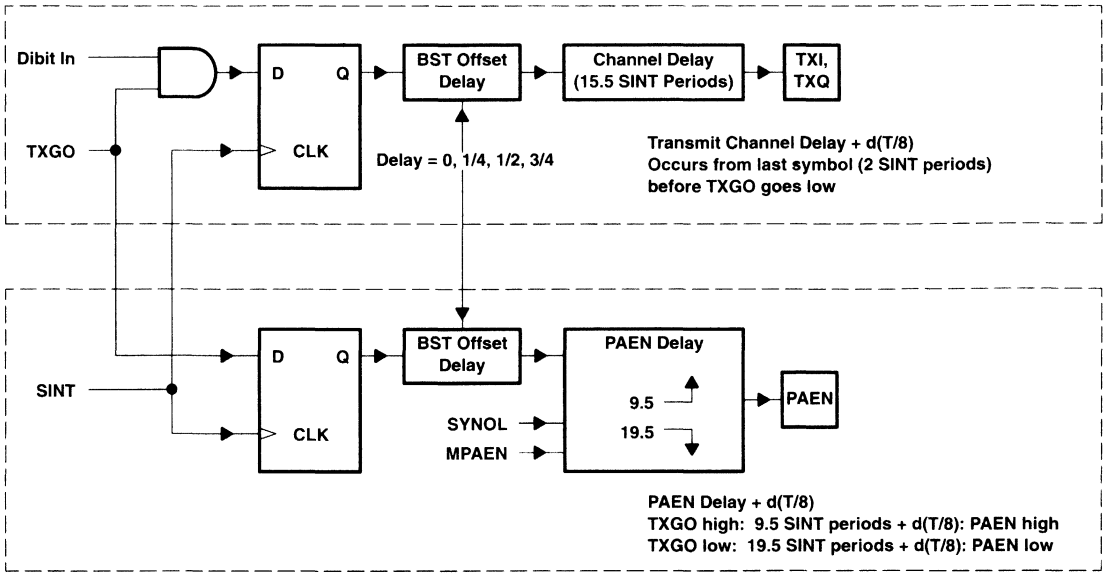


Figure 2. TX Power Ramp-Up/Ramp-Down Functional Diagram

transmit I and Q output level

In the digital mode, the output level at TXI and TXQ is controlled by the TCM4301. During the burst, but not including ramp-up or ramp-down periods, the average output level $(I^2 + Q^2)^{1/2}$ should approximate the specified value. There is no variable level control for TXI and TXQ within the TCM4301 other than the fixed ramping. In the analog mode, the output of the TCM4301 depends only on the sample values written to the TXI and TXQ registers.

There are small differences in the average output power levels between the digital and the analog modes. These differences require compensation at the system level by a small attenuation in the sample values of the analog output.

When a change in transmit power is necessary, the microcontroller can change the value sent to the PWRCONT DAC, the output of which can be connected to a voltage-controlled attenuator in the transmit path of the RF section.

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wide-band data demodulator

The wide-band data demodulator (WBDD) module demodulates the FM signal and outputs a Manchester-decoded data stream. The WBDD is used for receiving the analog control channels of forward control channel (FOCC) and forward voice control (FVC). The bit error rate (BER) performance requirements are listed in Table 9.

Table 9. Typical Bit Error Rate Performance (WBD_BW = 000)

PARAMETER	TEST CONDITIONS MEAN CNR (dB)	MIN	MAX	UNIT
Bit error rate	−5		0.4	
	0		0.279	
	5		0.143	
	10		0.056	
	15		0.0192	
	20		0.00623	
	25		0.00199	

The WBDD is controlled by the bits in the control register WBDCtrl (see Table 10).

Table 10. Bits in Control Register WBDCtrl

NAME	BIT CODE	FUNCTION
WBD_LCKD	—	Indicates whether edge detector is locked (1) or unlocked (0)
WBD_ON	—	Turns the WBDD module on/off (1/0)
WBD_BW		Sets the appropriate PLL bandwidth
	000	20 Hz
	001	39 Hz
	010	78 Hz
	011	156 Hz
	100	313 Hz
	101	625 Hz
	110	1250 Hz

WBD_LCKD: This bit can be used to reduce the effects of signal dropouts due to fading. In the Manchester-coded signal, there are two types of data edges. One type occurs at the midpoint of each data bit, and the other occurs randomly, depending on the transmitted data sequence. Inside the WBDD, an edge detector rapidly synchronizes itself to the midpoint edges when the WBD_LCKD bit is set to 0. However, if a signal dropout occurs, the edge detector may momentarily lock to the wrong edge because it cannot distinguish the midpoint edges from the data edges. A small number of additional bits may be lost in this instance.

When the WBD_LCKD bit is set to 1, the edge detector uses the WBDD internal PLL output to distinguish the correct edge. Once acquisition of data has occurred, if this bit is set to 1, the loss of bits due to signal dropouts is restricted to the fade duration only.

When the WBDD PLL is not synchronized, as at powerup, the WBD_LCKD bit must be cleared to 0 to allow edge synchronization to the data.

WBD_BW: The variable bandwidth is required for fast acquisition in the beginning using a wide bandwidth for the PLL, and a narrower bandwidth is used afterwards to reduce the likelihood of noise-causing loss of synchronization.

The WBDCtrl register is accessible by both the DSP and the microcontroller.

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wide-band data interrupts

The WBDD operates whenever WBD_ON is high, and it does not require the receive channels to be enabled. While WBD_ON is high, every 800 µs, 8 bits are placed in the WBD register, which is accessible by both the DSP and the microcontroller ports. This value should be written at the same time as WBD_ON is initially set high.

At the same time, the interrupts DWBDINT and MWBDFINT are asserted. The interrupt rate is 800 µs (8 bits/10 kHz). These interrupts are individually cleared when the WBD register is read by the corresponding processor. They can also be cleared by their respective processor by writing a 1 to the corresponding clear WBD bit.

There is one WBD control register. It can be written to by either processor port.

wide-band data demodulator: general information

The WBDD recovers the transmitter clock from the data stream, which is Manchester encoded, and decodes the data bits. Consideration at the system level is required to ensure data integrity.

The WBD stream carries with it a 10-kHz clock. The Manchester-coded data format contains a transition at the middle of every bit-clock period, which aids in clock recovery. The polarity of the transition is data-dependent. In a typical Manchester-coded WBD stream, a positive voltage for the first half of the data sequence bit time followed by a negative voltage for the second half of the data sequence bit time represents the value 0 in the data sequence. Likewise, a negative voltage followed by a transition to a positive voltage represents the value 1 in the data sequence. This is illustrated in Figure 3. The WBD stream can also be seen as the exclusive-OR of the clock and data sequence. The data sequence is in nonreturn to zero (NRZ) format.

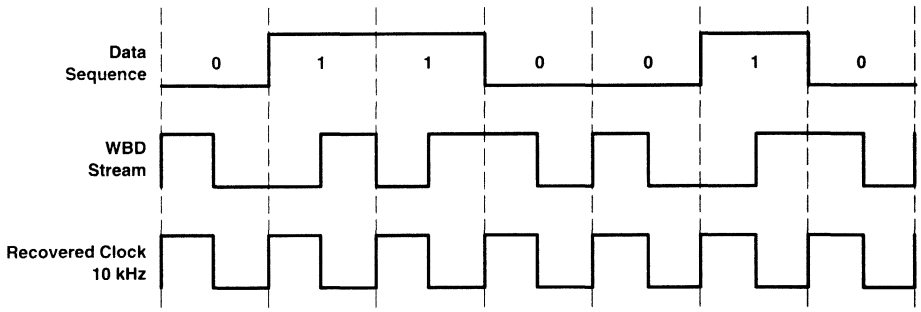

Figure 3. WBD Manchester-Coded Data Stream

auxiliary digital-to-analog converters (DACs), LCD contrast converter

Auxiliary DACs generate AFC, AGC, and power control signals for the RF system. These three D/A converters are updated when the corresponding data is received from the DSP. In fewer than 5 µs after the corresponding registers are written to, the output has settled to within 1/2 LSB of its new value (see Table 11).

The LCDCONTR output is used by the microcontroller to adjust the contrast of the liquid-crystal display (LCD). This converter is a separate 4-bit DAC.

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auxiliary digital-to-analog converters (DACs), LCD contrast converter (continued)

Table 11. Auxiliary D/A Converters

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output range	AV_{DD} > 3 V†,	AUXFS [1:0] = 00	0.2		2.5	V
	AV_{DD} > 4.5 V†,	AUXFS [1:0] = 10	0.2		4	
	AV_{DD} > 5 V†,	AUXFS [1:0] = 11	0.2		4.5	
Resolution AGC, AFC, PWRCONT DACs				8		bits
Resolution LCDCONTR DAC				4		bits
Gain + offset error (full scale) AGC, AFC, PWRCONT DAC					±5%	
Gain + offset error (full scale) LCDCONTR DAC					±8%	
Differential nonlinearity				±1.3	±2	LSB
Integral nonlinearity				±1.3	±2	LSB
Load resistance			10			kΩ
Load capacitance					50	pF

† Range settings depends only on AUXFS [1:0]. The supply voltage is not detected.

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The auxiliary DACs can be powered down. The AGC and AFC DACs have dedicated bits in the MIntCtrl register to enable the DACs. The PWRCONT DAC is enabled by the TXEN bit in the DStatCtrl register. The LCDCONTR DAC is enabled when the LCDEN bit of the LCD D/A register is set to 0, the four data bits being left justified. The AFC, AGC, and PWRCONT DACs are disabled after powerup or after a reset of the TCM4301. After powerup or reset, the default AUXFS[1:0] is 00. When the DACs are powered down, their output pins go to a high-impedance state and can tolerate any voltage present on the pin that falls within the supply range.

The slope and the corresponding output values for the auxiliary DACs are listed in Table 12 and Table 13.

Table 12. Auxiliary D/A Converters Slope (AGC, AFC, PWRCONT)

AUXFS[1:0] SETTING	SLOPE	NOMINAL LSB VALUE (V)	NOMINAL OUTPUT VOLTAGE FOR DIGITAL CODE = 128 (MIDRANGE) (V)	NOMINAL OUTPUT VOLTAGE FOR DIGITAL CODE = 256‡ (MAX VALUE) (V)
00	2.5/256	0.0098	1.25	2.5
01	Do not use	Do not use	Do not use	Do not use
10	4/256	0.0156	2	4
11	4.5/256	0.0176	2.25	4.5

‡ The maximum input code is 255. The value shown for 256 is extrapolated.

Table 13. Auxiliary D/A Converters Slope (LCDCONTR)

AUXFS[1:0] SETTING	SLOPE	NOMINAL LSB VALUE (V)	NOMINAL OUTPUT VOLTAGE FOR DIGITAL CODE = 8 (MIDRANGE) (V)	NOMINAL OUTPUT VOLTAGE FOR DIGITAL CODE = 16§ (MAX VALUE) (V)
00	2.5/16	0.1563	1.25	2.5
01	Do not use	Do not use	Do not use	Do not use
10	4/16	0.2500	2	4
11	4.5/16	0.2813	2.25	4.5

§ The maximum input code is 15. The value shown for 16 is extrapolated.

RSSI, battery monitor

The receive signal strength indicator (RSSI) and battery (BAT) strength monitor share a common register. The input source is determined by writing any value to the mapped register location for that analog-to-digital converter (see Table 14), and the result of the conversion is stored in both register locations. The conversion process is initiated when the register is written to. The CVRDY bit in the MStatCtrl register is set to 1 to show completion of the conversion process. Reading from either of the register locations causes the CVRDY bit to change to 0. The received signal strength indicator allows the mobile unit to choose the proper control channels, and to report signal levels to the base stations.

When CVRDY in the MStatCtrl register goes to 1, this indicates that the latest RSSI or battery voltage A/D conversion has been completed and can be read from the RSSI or BAT register location. CVRDY goes to 0 when the microcontroller reads either of these locations.

Table 14. RSSI/Battery A/D Converter

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input range	AV_{DD} = 3 V, 4.5 V, 5 V	0.2		2	V
Resolution			8		bits
Conversion time	AV_{DD} = 3 V, 4.5 V, 5 V		20		µs
Gain + offset error (full scale)			±4%	±5%	
Differential nonlinearity				±1.5	LSB
Integral nonlinearity				±1.5	LSB
Input resistance		1	2		MΩ

In order to save power, the entire RSSI/battery converter circuit is powered down when no A/D conversions are requested for 40 µs. The microcontroller writes to RSSI or BAT registers, causing power to be applied to the converter circuit. Power is applied to the converter circuit until the data value has been latched into the corresponding register, at which time power to the converter is removed. Data remains in the result registers after the converter is powered down.

timing and clock generation

The digital timing generation system uses a 38.88-MHz master clock, as shown in Figure 6. The upper half of the figure shows the clock generation for clocks that must be phase adjusted in order to synchronize the mobile unit with the received symbol stream in the digital mode. In the analog mode, these clocks operate without phase adjustments. The lower half of Figure 6 shows the clocks that are directly derived from the master clock.

clock generation

There are three options for generating the master clock. A fundamental crystal or third-overtone crystal with a frequency of 8 MHz can be connected between the MCLKIN and the XTAL terminals or an external clock source can be connected directly to the MCLKIN terminal. The MCLKOUT is a buffered master clock output at the same frequency as MCLKIN. MCLKOUT can be used as the source clock for other devices in the system. Setting the MCLKEN bit in the MStatCtrl register enables or disables this output. The MCLKOUT enable is synchronous to eliminate abnormal cycles of the clock output.

All output clocks are derived from the master clock (MCLKIN). The sample clocks for the digital and analog modes, the 8-kHz speech codec sample clock, and the clocks for the A/D and D/A functions are also derived from the master clock.

speech codec generation

The TCM4301 generates two clock outputs for use with speech codecs: the 2.048-MHz CMCLK and the 8-kHz CSCLK. These clocks are generated so that each CSCLK period contains exactly 256 cycles of CMCLK. Since 2.048 MHz is not an integer division of the 38.88-MHz MCLKIN, one out of every 64 CMCLK cycles is 18 MCLKIN periods long, and the remaining 63 out of 64 are 19 MCLKIN periods long. The average frequency of MCLKIN is therefore

$$\text{MCLKIN} \times \frac{\left(\frac{63}{19} + \frac{1}{18}\right)}{64} = 2.048092 \text{ MHz}$$

CSCLK is exactly CMCLK divided by 256. See Figure 4.

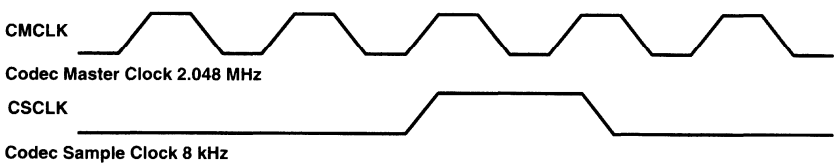

Figure 4. Codec Master and Sample Clock Timing

To save power, the codec clocks are only generated by TCM4301 when the SCEN bit of the DStatCtrl register is set high. When SCEN is low, both outputs, CSCLK and CMCLK, are held low. SCEN is also available as an output.

microcontroller clock

A variable modulus divider provides a selection of frequencies for use as a microcontroller clock. The master clock is divided by an integer from 32 to 2, giving a wide range of frequencies available to the microcontroller (1.215 MHz to 19.88 MHz). The modulus can be changed by writing to the microcontroller clock register. The output duty cycle is within the requirements of most microcontrollers, that is, from 40% to 60%. At power-on reset, the clock divider defaults to 1.215 MHz.

sample interrupt SINT

The SINT interrupt signal is the primary timing signal for the TCM4301 interface. The primary function of the SINT is to indicate the ready condition to receive or transmit data. It also conveys timing marks to allow for the synchronization of system DSP functions. In the digital mode, SINT is used in conjunction with the received sync word to track cellular system timing. The SINT can be disabled by writing a 1 to the SDIS bit of the DIntCtrl register. When enabled, the SINT operates continuously at 48.6 kHz in the digital mode and at 40 kHz in the analog mode. The SINT signal does not require an interrupt acknowledge. The SINT is active low for seven MCLKOUT cycles in both the analog mode and digital mode to guarantee capture by the DSP. The SINT signal is the sleep timer interrupt when operating in sleep mode and is the normal sample interrupt when not in sleep mode.

sleep mode timer

DSP and microcontroller registers

The sleep mode function is controlled in four TCM4301 registers. The relevant DSP registers are the sleep control register (Slp_Ctrl), the sleep compare register (Slp_Cmp), and the sleep counter register (Slp_Cntr). Address 0Eh in the DSP register map space is the [9:0] Slp_Cmp register on a write and is the [9:0] Slp_Cntr on a read. Address 0Fh is the Slp_Ctrl register. The three least significant bits, [2:0], are Slp_Cntr [12:10] on a read and Slp_Cmp [12:10] on a write. The relevant microcontroller register is the microcontroller interrupt control register (MIntCtrl), which is assigned address 0Eh in microcontroller register map space. The sleep mode bit, SM, is bit [0] in MIntCtrl. See Figure 5.

sleep counter data

The sleep counter data is 13 bits wide. The three most significant sleep counter data bits [12:10] are read via the internal DSP bus at the three least significant bits [2:0] in the sleep mode control register (Slp_Ctrl) at address 0Fh. The ten least significant sleep counter data bits [9:0] are read from the sleep counter (Slp_Cntr) at address 0Eh via the DSP bus. Two reads are needed to read the sleep counter data. The count value of the three most significant bits in address 0Fh are latched when a read is performed at address 0Eh. This feature allows the DSP to read the correct values of the three most significant bits at a later time.

sleep compare data

The sleep compare data is 13 bits wide. The three most significant sleep compare data bits [12:10] are loaded via the DSP bus by writing to the three least significant bits [2:0] of the sleep mode control register (Slp_Ctrl) at address 0Fh. The ten least significant sleep compare data bits [9:0] are written via the DSP bus to the sleep compare register (Slp_Cmp) at address 0Eh. Thus, two writes are needed to load the sleep compare data. The three most significant data bits are set to zero upon a write to the ten least significant bits.

sleep mode control register (Slp_Ctrl)

The sleep control register is 10 bits wide. The three least significant bits [2:0] are Slp_Cntr [12:10] on a read and Slp_Cmp [12:10] on a write. The remaining bits are defined as follows:

Bit [3], on Read: TMR_STS, Timer Status Bit: This bit indicates the mode status of the timer circuit. When high, the 50 Hz counter is enabled and the circuit is in sleep mode. When low, the counter is disabled. This bit is cleared during initialization.

on Write: STR_TMR, Start Timer Bit: Active high, cleared during initialization. This bit is set high by the DSP (not latched) to initiate the sleep timer and disable MCLKOUT.

NOTE: The counter is to count beginning at the edge of a 48.6-kHz clock. Thus, the 50-Hz sleep counter clock is synchronous with the 48.6-kHz clock.

Bit [4], on Read: MCSM, microcontroller sleep mode status bit. When read, this bit is the micro sleep mode bit [MIntCtrl register bit [0], sleep mode bit (SM)], echoed back to the DSP. On read, this bit can be used by the DSP to determine the cause of an SINT wakeup interrupt. When the DSP wakes up and reads the bit as set (=1), then the SINT was caused by the timer expiring (A=B). If the DSP reads the bit as reset (=0), then the SINT was caused by the microcontroller changing its sleep mode bit, SM, = 0. This bit is cleared during initialization.

on Write: STP_TMR: This bit is active high (not latched). When high, the sleep counter is stopped and reset. The DSP can then read TMR_STS to investigate the mode of the timer.

Bit [5], TEST, Test Bit. When a 1 is written to this bit, the contents of the Slp_Cmp and Slp_Ctrl registers can be read by the DSP.

microcontroller interrupt control register (MIntCtrl)

The MIntCtrl register bit [0], sleep mode bit (SM), enables the sleep mode on the microcontroller side. The reset value is 0, disabled. This bit is echoed back to the DSP and latched in bit [4] (MCSM) in the sleep control register on a read by the DSP. This microcontroller sleep mode bit is set high by the microcontroller to enable sleep mode. During sleep mode, the microcontroller can initiate an SINT wakeup interrupt to the DSP by clearing this bit. The counter continues to run until STP_TMR is set high.

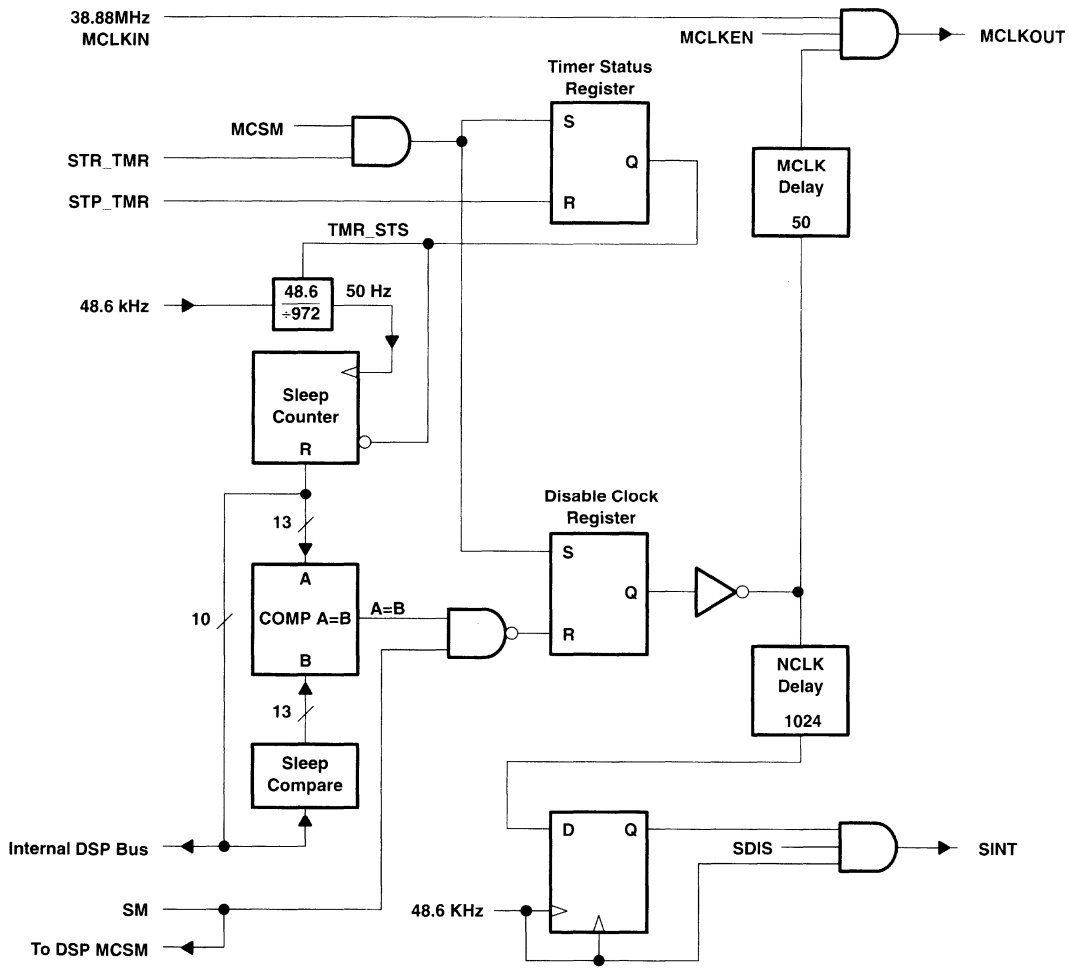

Figure 5. Sleep Mode Timer Block Diagram

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microcontroller interrupt control register (MIntCtrl) (continued)

MCLKOUT is disabled under the following conditions:

- DSP STR_TMR bit is written to with a 1, and the microcontroller sleep mode bit has been set (SM = 1). The disable function is delayed by a minimum of 50 MCLKIN clock cycles.

MCLKOUT is enabled under the following conditions:

- Microcontroller sleep mode signal is reset, SM = 0.
- Compare output is active (A = B = 0).
- TCM4301 is reset.

phase-adjustment strategy

In the digital mode IS-136 system, receiver sample timing must be phase adjusted to synchronize the A/D conversions to optimum sampling points of the received symbols, and to synchronize the mobile unit timing to the base station timing. This is done by temporarily increasing or decreasing the periods of the clocks to be adjusted. To avoid undesirable transients, each cycle of the clock being adjusted is altered by only one period of MCLKIN. A total adjustment equivalent to multiple MCLKIN periods is accomplished by altering multiple cycles of the clock being adjusted. The number of cycles altered is controlled by internal counters.

In the TCM4301 there are two clocks which must be adjusted: CMCLK and an internal 9.72-MHz clock from which SINT is derived. Each of these clocks has an associated counter that counts the number of cycles that have been lengthened or shortened by one MCLKIN period each and thus detects when the total adjustment is complete. These counters are shown in Figure 6 as Adjust Counter A and Adjust Counter B.

The magnitude of the 2s complement value written to the timing adjustment register determines the number of cycles of the clocks to be lengthened or shortened by one MCLKIN period each to achieve the total desired timing adjustment in units of MCLKIN periods. If a negative number is written, the clock periods are lengthened for the duration of the timing adjustment, resulting in a timing delay. If a positive number is written, the clock periods are shortened for the duration of the timing adjustment, resulting in a timing advance.

The divider used to generate CMCLK normally divides MCLKIN by either 19 or 18. When its period is being lengthened during a timing adjustment, MCLKIN is divided by either 20 or 19. When the CMCLK period is being shortened, MCLKIN is divided by either 18 or 17 (see the section on speech codec clock generation). The divider used to generate a 9.72-MHz divides by 4 during normal operation, by 5 when its period is being lengthened during timing adjustments, and by 3 when its period is being shortened during timing adjustments.

Because CMCLK and the 9.72-MHz internal clock have different periods, and the timing adjustments are limited to one period of MCLKIN per period of the clock, these clocks take different times to complete the entire timing adjustment. Because the total adjustment is the same number of MCLKIN periods for both clocks, the relative phases of the two clocks are the same after the adjustment as they were before.

Both adjust counters reach zero when the adjustment is complete, so there is no need to write to the timing adjustment register until another timing adjustment is required. For each write to the timing adjustment register, a single timing adjustment of the direction and magnitude requested is performed.

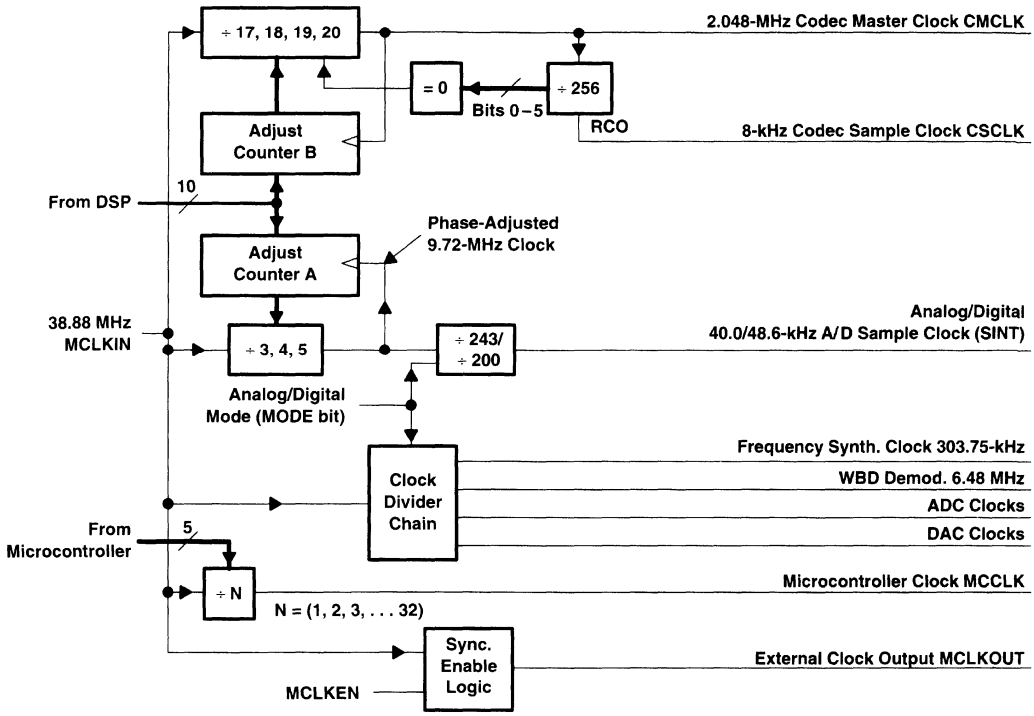

Figure 6. Timing and Clock Generation for 38.88-MHz Clock

The output of each adjustment counter is fed to a variable modulus divider. For counter A, there are three possible moduli, 3, 4, and 5. For counter B, there are four possible moduli, 17, 18, 19, and 20.

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frequency synthesizer interface

The synthesizer interface provides a means of programming three synthesizers. The synthesizer-side outputs are a data line, a clock line, and three latch enable lines that separately strobe data into each synthesizer. The control-side inputs are registers mapped into the microcontroller address space. The status of the interface can be monitored to determine when the programming operation has been completed.

The synthesizer interface is designed to be general purpose. Most of the currently available synthesizers can be accommodated by programming the interface according to the required synthesizer data and logic level formats.

The output of the synthesizer interface consists of five signals. SYNCLK is the common data clock for all attached synthesizer chips. Two control bits, CLKDIV, in SynCtrl2 control the frequency for the SYNCLK. These bits are initialized to 00, which results in MCLKIN/128 (≈304 kHz). The clock pulse has a 50% duty factor. When CLKDIV = 01, the rate is MCLKIN/64; when CLKDIV = 10, the rate is MCLKIN/32; and when CLKDIV = 11, the rate is MCLKIN/16. The serial data output SYNDTA is common to all synthesizers. Three strobe signals, SYNLE[2:0], are provided. There is one for each synthesizer chip. The attributes of this interface are controlled by means of the synthesizer control registers, SynCtrl[2,1,0]. These attributes determine:

- The polarity of the clock (rising or falling edge)
- Whether data is shifted left or right
- The number of bits sent to the synthesizer
- The timing and polarity of the latch enable bits
- The selection of which synthesizer to program

Programming of the synthesizers is accomplished by writing to four microcontroller-mapped data registers. These registers are chained to form a 32-bit data shift register that can be operated in either shift left or shift right mode. This register set can accommodate various formats of synthesizer control data. When fewer than 32 bits of data are to be transmitted, the significant data bits must be justified such that the first bit to be transferred is either the LSB or the MSB of the register set, as defined by the control register for LSB or MSB first operation. All 32 bits of the data register are transmitted each time. See Table 17 for register location. See Figure 7 for a respresentative block diagram of the frequency synthesizer interface.

frequency synthesizer interface (continued)

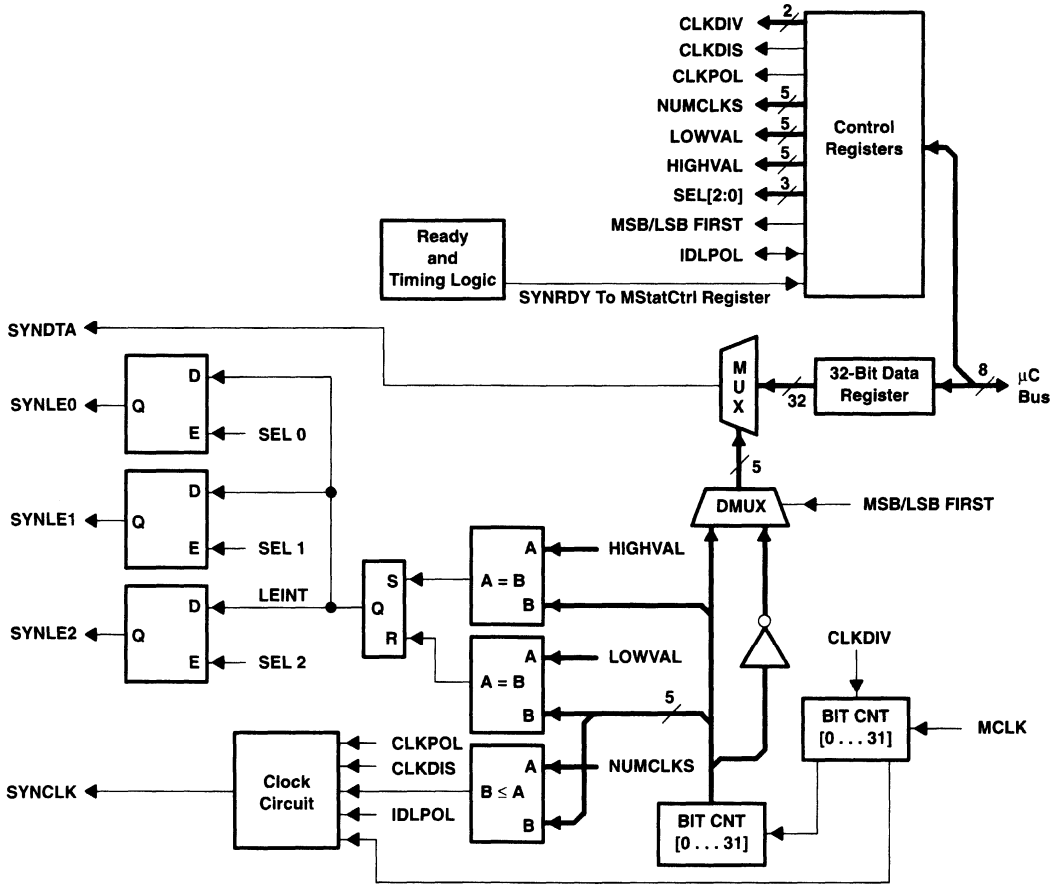

Figure 7. Synthesizer Interface Circuit Block Diagram

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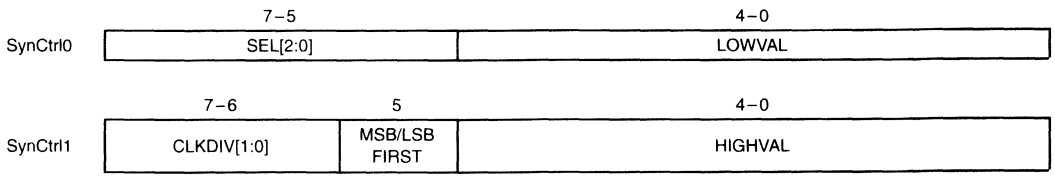
frequency synthesizer interface (continued)

The SynData0 register contains the least significant bits of the 32-bit data register. SynData3 contains the most significant bits. The bits in the SynCtrl0, SynCtrl1, and SynCtrl2 registers are allocated as shown in Figure 8.



CLKDIV1	CLKDIV0	SYNCLK RATE†
0	0	MCLKIN/128
0	1	MCLKIN/64
1	0	MCLKIN/32
1	1	MCLKIN/16

† MCLKIN is 38.88 MHz.

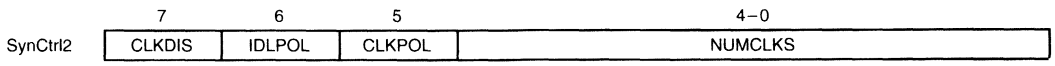


Figure 8. Contents of SynData Registers

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frequency synthesizer interface (continued)

Table 15 identifies the meaning of each of the bit fields in SynCtrl[2:0].

In the status register MStatCtrl, two bits, SYNOL and SYNRDY, are dedicated to the synthesizers. The first is an out-of-lock indicator that comes from the SYNOL input terminal. If the SYNOL input terminal is connected to the OR of the out-of-lock signals from the external synthesizers, the lock condition of the synthesizers can be monitored by reading the MStatCtrl register. A high on SYNOL also prevents the PAEN output from being asserted and forces the TXI and TXQ outputs to 0. The SYNRDY bit, active high, indicates when the synthesizer interface is idle and ready for programming. SYNRDY will indicate that the interface is idle following a programming cycle after all SYNCLK, and SYNLE events are complete. All events are complete when BIT CNT is equal to the greater of NUMCLKS, HIGHVAL, and LOWVAL; a value of 0 in NUMCLKS is the maximum value possible. When SYNRDY is low, the synthesizer interface is busy.

Controlling the synthesizer interface is straightforward. The microcontroller checks to see if the SYNRDY bit is low. When it is low, the synthesizer interface is not ready. When SYNRDY goes high, the microcontroller programs the desired information into the four registers. When the microcontroller write to the SynCtrl2 register is complete, the synthesizer interface sets the SYNRDY bit low and begins to send data, clock, and latch enable according to the format established in the registers. SYNRDY returns high when the entire operation is complete. The SynCtrl registers must be programmed in order of SynCtrl0, then SynCtrl1, and finally SynCtrl2 to assure proper synthesizer programming.

Table 15. Synthesizer Control Fields

NAME	DESCRIPTION
CLKDIV(1:0)	2 Bits. Selects rate for SYNCLK: 00=MCLK/128, 01=MCLK/64, 10=MCLK/32, 11=MCLK/16
CLKPOL	Defines the significant edge of SYNCLK that occurs in the middle of the SYNDTA bit. 0: Requires a falling edge 1: Requires a rising edge
NUMCLKS	This 5-bit field defines the total number of clock pulses that are to be produced on the SYNCLK terminal. The value written into this field is the desired number of output clock pulses, with one exception: When 32 clock pulses are desired, all zeroes are written into NUMCLKS.
CLKDIS	Defines whether the SYNCLK signal will be active during a programming cycle. 0: Requires that the SYNCLK signal is active as defined by NUMCLKS, IDLPOL, and CLKPOL. 1: Requires that the SYNCLK signal remain in the idle state as defined by IDLPOL, and CLKPOL.
HIGHVAL†	This 5-bit field defines when the strobe signal for the selected synthesizer is driven high. This number is the bit number at which the signal changes state. Bits being transferred on SYNDTA are sequentially designated 0, 1, . . . 31, independent of any MSB/LSB selection.
LOWVAL†	The value written into this 5-bit field affects the strobe signal for the selected synthesizer. This number is the bit number at which the strobe signal is driven low. The first bit transferred out of the serial interface is defined to occur at bit-time 0, independent of any MSB/LSB selection.
MSB/LSB FIRST	Writing a 0 to this bit causes the LSB (SynData0[0]) to be the first bit sent to the SYNDTA terminal of the serial synthesizer interface. Writing a 1 to this bit programs the block for MSB first operation, (SynData3[7]).
SEL[2:0]	3 Bits. Select which synthesizer strobe line is active. A 1 in any of these bits activates the corresponding latch enable.
IDLPOL	Defines the idle state polarity of the SYNCLK signal. 0: Requires that the idle state of the SYNCLK signal to be the same as the CLKPOL control bit. 1: Requires that the idle state of the SYNCLK signal to be the complement of the CLKPOL control bit.

† LOWVAL and HIGHVAL should never be assigned the same value. A particular SYNLE signal can be made to transition from a low state on the crossing of a cycle boundary to a high state as early as BIT CNT count one (1). If LOWVAL is given a value less than HIGHVAL, the selected SYNLE signal(s) will exit the programming cycle in a high state. If HIGHVAL is given a value less than LOWVAL, the selected SYNLE signal(s) will exit the programming cycle in a low state.

frequency synthesizer interface (continued)

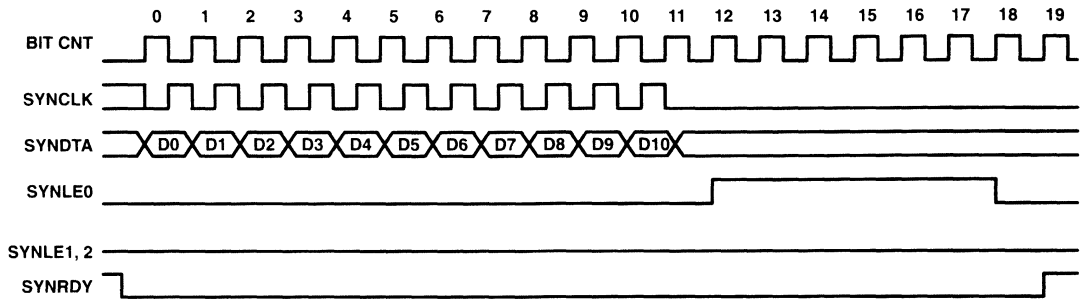
Example 1: Single Cycle, SYNCLK Activity

Example 1 depicts a single programming cycle. Of particular interest is the activity of SYNCLK. The SYNCLK signal begins the programming cycle in either a high or low logic state and completes the programming cycle in a low logic state; the idle state of SYNCLK is a logic low.

The control bit CLKDIS is set to 0, which enables the output of SYNCLK. When SYNCLK is enabled by CLKDIS = 0, SYNCLK will be enabled from a count of 0 to NUMCLKS of the BIT CNT counter. A value of 0 in NUMCLKS provides for 32 SYNCLK periods.

The significant edge polarity is controlled by CLKPOL. With CLKPOL set to 1, the significant edge of SYNCLK will be rising from a logic low to a high state and will do so in the middle of the associated SYNDTA bit.

Because the idle state polarity control bit IDLPOL is set to 1, the idle state of SYNCLK is the complement of the CLKPOL bit, which is set to 1 in Example 1. Therefore, when the BIT CNT counter reaches a value equal to NUMCLKS, SYNCLK returns to a low, idle state.



CLKDIS = 0
CLKPOL = 1
IDLPOL = 1
NUMCLKS = 10
HIGHVAL = 12
LOWVAL = 18
SEL [2:0] = 001

Figure 9. Example 1: Single Cycle SYNCLK Activity

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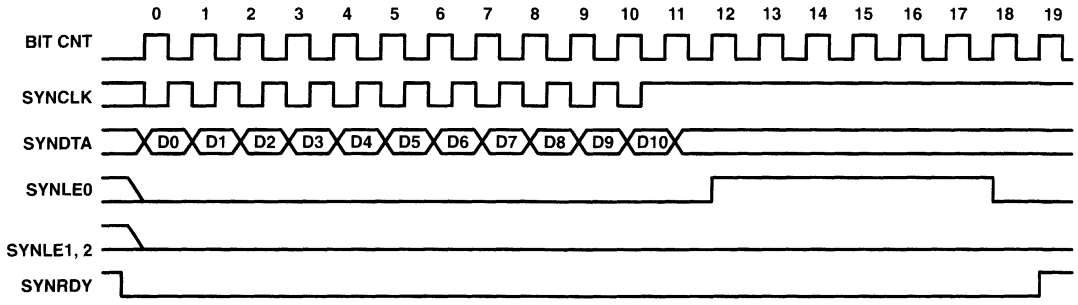
frequency synthesizer interface (continued)

Example 2: Single Cycle, SYNCLK Activity

Example 2 is similar to Example 1 with the exception of the state of control bit IDLPOL. In Example 2, CLKPOL is set to 1 and IDLPOL is set to 0. With CLKPOL = 1, the significant edge of SYNCLK will be rising from a logic low to a logic high state and will do so in the middle of the associated SYNDTA bit.

Because the idle state polarity control bit IDLPOL is set to 0, the idle state of SYNCLK is the same as the CLKPOL bit, which is set to 1 in Example 2. Therefore, when the BIT CNT counter reaches a value equal to NUMCLKS, SYNCLK remains at a high idle state.



CLKDIS = 0
CLKPOL = 1
IDLPOL = 0
NUMCLKS = 10
HIGHVAL = 12
LOWVAL = 18
SEL [2:0] = 001

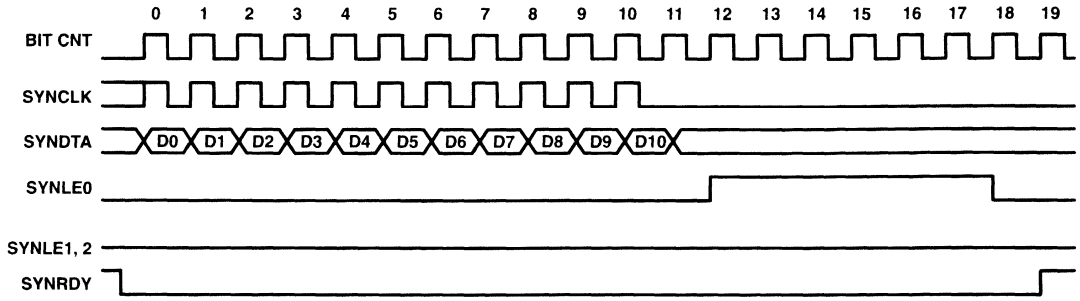
Figure 9. Example 2: Single Cycle, SYNCLK Activity (Continued)

frequency synthesizer interface (continued)

Example 3: Single Cycle, SYNCLK Activity

Example 3 is similar to Example 1. In Example 3, CLKPOL and IDLPOL are both set to 0. With CLKPOL = 0, the significant edge of SYNCLK will be falling from a logic high to a logic low state and will do so in the middle of the associated SYNDTA bit.

Because the idle state polarity control bit IDLPOL is set to 0, the idle state of SYNCLK is the same as the CLKPOL bit, which is set to 0 in Example 3. Therefore, when the BIT CNT counter reaches a value equal to NUMCLKS, SYNCLK returns to a low idle state.



CLKDIS = 0
CLKPOL = 0
IDLPOL = 0
NUMCLKS = 10
HIGHVAL = 12
LOWVAL = 18
SEL [2:0] = 001

Figure 9. Example 3: Single Cycle, SYNCLK Activity (Continued)

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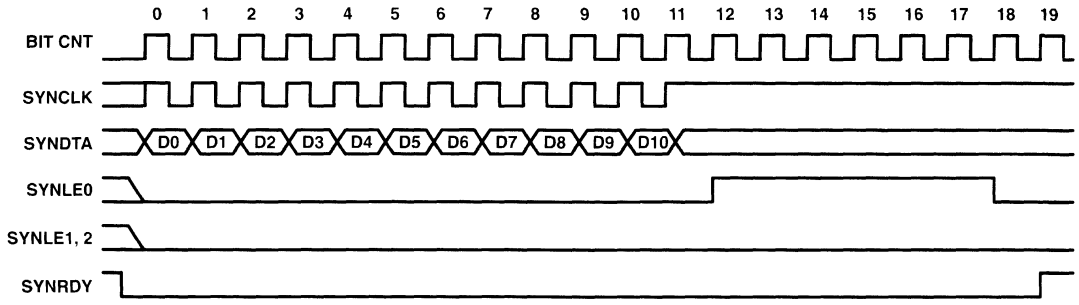
frequency synthesizer interface (continued)

Example 4: Single Cycle, SYNCLK Activity

Example 4 is similar to Example 1. In Example 4, CLKPOL is set to 0 and IDLPOL is set to 1. With CLKPOL = 0, the significant edge of SYNCLK will be falling from a logic high to a logic low state and will do so in the middle of the associated SYNDTA bit.

Because the idle state polarity control bit IDLPOL is set to 1, the idle state of SYNCLK is the complement of the CLKPOL bit, which is set to 0 in Example 4. Therefore, when the BIT CNT counter reaches a value equal to NUMCLKS, SYNCLK remains in a high idle state.



CLKDIS = 0
CLKPOL = 0
IDLPOL = 1
NUMCLKS = 10
HIGHVAL = 12
LOWVAL = 18
SEL [2:0] = 001

Figure 9. Example 4: Single Cycle, SYNCLK Activity (Continued)

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frequency synthesizer interface (continued)

Example 5: 32-Bit Data Transfer with SYNLE Activity Cycles

Example 5 depicts a 32-bit data transfer occurring in a single programming cycle followed by four cycles during which the states of SYNLE signals are manipulated.

Programming Cycle 1

Transferring 32 bits of data requires the same number of SYNCLK periods. The NUMCLKS control field is set to 0, which calls for 32 SYNCLKs during the data transfer programming cycle. The states of CLKPOL and IDLPOL call for a rising edge SYNCLK which returns to a low idle state.

During the data transfer cycle, the SYNLE signals are assumed to have been previously made low by a preceding initialization programming cycle. Because SEL [2:0] are all low, the SYNLE signals will not transition during this cycle regardless of the values of HIGHVAL and LOWVAL.

Programming Cycle 2

SEL [2:0] is set to 001, which enables a state change in the SYNLE0 signal alone. When the BIT CNT counter reaches a value equal to that of the HIGHVAL control field, SYNLE0 goes to the high state. The LOWVAL control field is set to 0. Because SYNLE0 is already at a low state when the BIT CNT counter has a counter value of 0 and LOWVAL is given a value less than HIGHVAL, the LOWVAL field has no effect on SYNLE0 during this programming cycle, and SYNLE remains in a high state at the termination of this programming cycle.

Note also the SYNCLK signal is suppressed to its idle low state by CLKDIS being set to 1 regardless of the value in the NUMCLKS field. NUMCLKS is given a value of 0, which will ensure that the 32 BIT CNT counts occur during the programming cycle.

Programming Cycle 3

SEL [2:0] is set to 001, which enables a change in the SYNLE0 signal. HIGHVAL is given a value of 1 and LOWVAL is given a value of 0. Therefore, SYNLE0 is forced low at a BIT CNT count of 0 and then returns high at a BIT CNT count of 1.

Note also that the SYNCLK signal is still suppressed to its idle low state by CLKDIS being set to 1 regardless of the value in the NUMCLKS field.

Programming Cycle 4

SEL [2:0] is set to 001, which enables a change in the SYNLE0 signal. HIGHVAL is given a value of 0 and LOWVAL is given a value of 30. Therefore, SYNLE0 is forced to a low state at a BIT CNT count of 30.

Program Cycle 1	Program Cycle 2	Program Cycle 3	Program Cycle 4
CLKDIS = 0	CLKDIS = 1	CLKDIS = 1	CLKDIS = 1
CLKPOL = 1	CLKPOL = 1	CLKPOL = 1	CLKPOL = 1
IDLPOL = 1	IDLPOL = 1	IDLPOL = 1	IDLPOL = 1
NUMCLKS = 0	NUMCLKS = 0	NUMCLKS = 0	NUMCLKS = 0
HIGHVAL = 1	HIGHVAL = 1	HIGHVAL = 1	HIGHVAL = 0
LOWVAL = 0	LOWVAL = 0	LOWVAL = 0	LOWVAL = 30
SEL [2:0] = 000	SEL [2:0] = 001	SEL [2:0] = 001	SEL [2:0] = 001

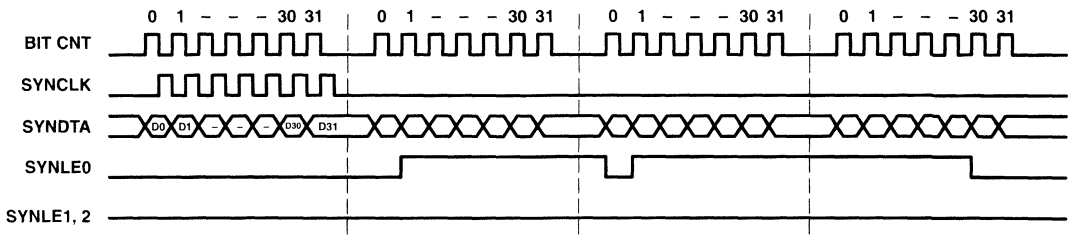

Figure 10. Example 5: 32-Bit Data Transfer with SYNLE Activity Cycles

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frequency synthesizer interface (continued)

Example 6: 32-Bit Data Transfer with SYNLE Boundary Crossing

Example 6 involves four programming cycles of which the first is used to transfer 32-bit data and the remaining three contain boundary crossing of the SYNLE signals.

Programming Cycle 1

Program cycle 1 is identical to the one in Example 5. Thirty-two bits of data are transferred with the SYNLE signals being forced to a low state at the beginning of the cycle.

Programming Cycle 2

Program cycle 2 is identical to the one in Example 5. SYNLE0 is enabled by SEL [2:0]=001 and moves from a low state to a high state when the BIT CNT counter reaches a value equal to the HIGHVAL (1) control field. Note that the LOWVAL control field is set to a value of 0 and is less than the value in the HIGHVAL control field. By this means, the SYNLE0 signal will cross the program cycle boundary in a high state.

Programming Cycle 3

SEL [2:0] is set to 110, which enables a state change in the SYNLE1 and SYNLE2 signals. Because SYNLE1 and SYNLE2 are initially in a low state and LOWVAL is less than HIGHVAL, LOWVAL has no effect on SYNLE1 and SYNLE2. However, because HIGHVAL is given a value of 1, SYNLE1 and SYNLE2 transition from a low to a high state on BIT CNT count of 1.

Programming Cycle 4

SEL [2:0] is set to 111, which enables a state change in the all SYNLE signals. Because all SYNLE signals are initially in a high state and HIGHVAL is less than LOWVAL, HIGHVAL has no effect on the SYNLE signals. However, because LOWVAL is given a value of 30, all the SYNLE signals transition from a high to a low state on BIT CNT count of 30.

Note also that the SYNCLK signal is still suppressed to its idle low state throughout program cycles 2 through 4 by CLKDIS being set to 1.

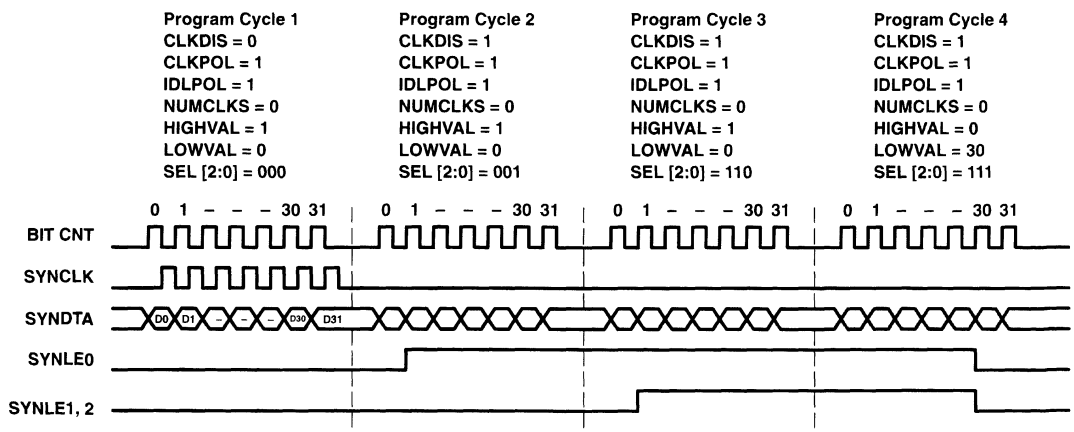

Figure 11. Example 6: 32-Bit Data Transfer with SYNLE Boundary Crossing

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power control port

For systems requiring minimum system current consumption, power can be provided to each functional part of the TCM4301 only when that function is required for proper system operation. To accomplish this, the TCM4301 provides six external power control signals accessible through the DStatCtrl and MStatCtrl registers. These signals can be used to minimize the ON time of the functional units. These power control signals are SCEN, FMRXEN, IQRXEN, TXEN, PAEN, and OUT1 (see Table 16). The polarity of each of these signals is high enable, low disable.

Table 16. External Power Control Signals

NAME	SUGGESTED EXTERNAL APPLICATION	RESET VALUE
SCEN	Speech codec (microphone/speaker interface circuit) enable	0
FMRXEN	FM demodulator enable	0
IQRXEN	I and Q receive enable. Enables QPSK demodulator and AGC amplifier	0
TXEN	Transmit enable. Enables power to the transmitter signal processing circuits: QPSK modulator, voltage-controlled amplifier, driver amplifier, PA negative bias. This signal can be used to enable these subsystems only during the TX burst in digital mode.	0
OUT1	User defined	0
PAEN	Power amplifier enable. Enables power to PA.	0

In addition to allowing control of power to external functional modules, these power control bits combined with other control bits are used to control internal TCM4301 functions. This control system is shown in Figure 12.

power control port (continued)

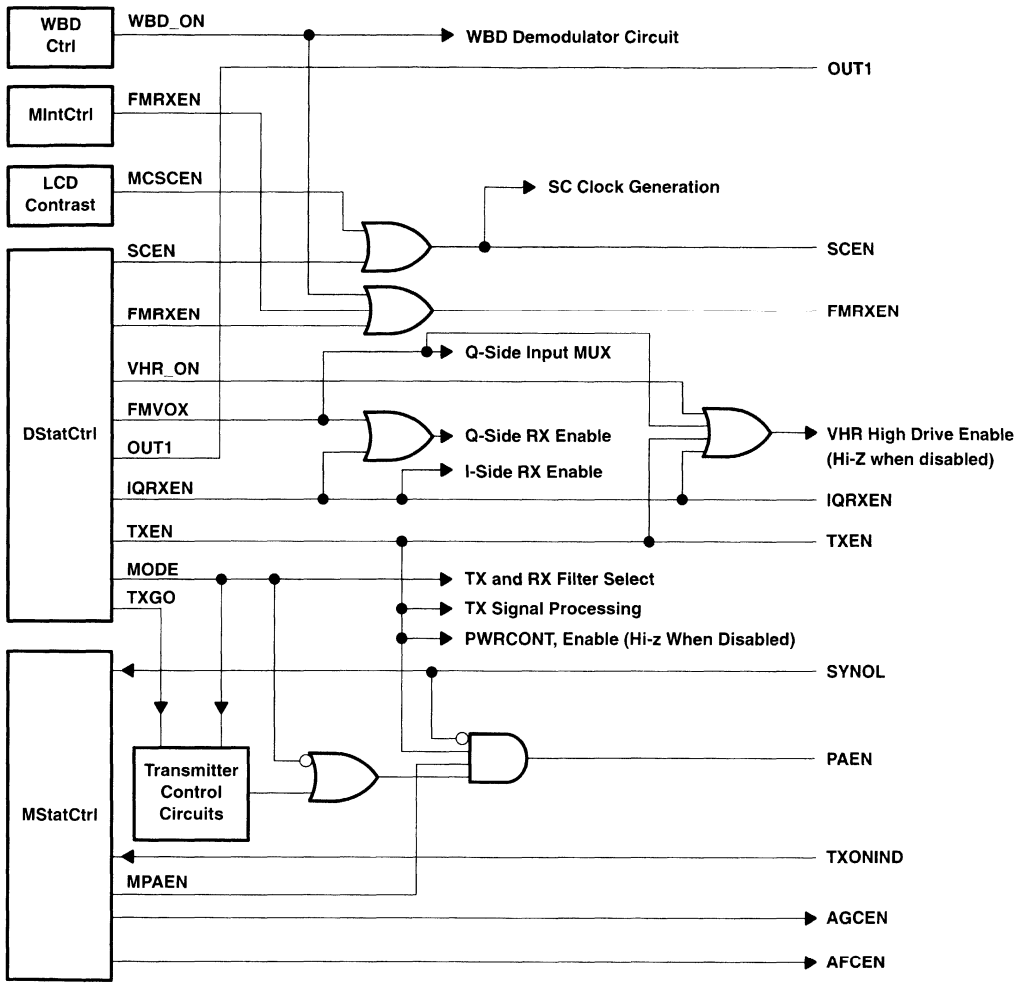

Figure 12. Internal and External Power Control Logic

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power control port (continued)

To allow for further system power savings, the TCM4301 receive I and Q channels are enabled separately because only the Q side is used in analog mode. The FMVOX bit controls the Q-side input multiplexer. When FMVOX is high, the QP side of the receiver is connected to the FM input terminal, the QN input is connected to the VHR reference voltage, and the Q side of the receiver is powered up. The MODE bit controls the Q-side filter characteristics for digital or analog mode. The IQRXEN bit enables both the I and Q receiver sides. The bit IQRXEN can be set high while still in analog mode (FMVOX high or MODE low) to allow sufficient power-up settling time for the external receiver I and Q circuits.

Setting the MODE bit low connects the RXQP to the FM input and RXQN to VHR. VHR can be enabled at any time by setting VHR_ON high.

In the digital mode (MODE bit set high), setting IQRXEN high turns on both sides of the receiver. The TXEN enables the internal TX functions. When the TXEN bit is set low, the PWRCONT output goes to a high-impedance state and the PAEN output is set low. The TXEN signal can be used to power down most of the external transmit circuits between transmit bursts.

In the analog mode, (MODE bit set low), PAEN is high whenever TXEN is active and SYNOL is low. The SYNOL input can be used as an indication to the TCM4301 that the external synthesizers are out of lock. The PAEN signal is gated by SYNOL to prevent off-channel transmissions.

The TXEN, IQRXEN, FMVOX, and MODE signals are generated by sampling the corresponding bits of the DStatCtrl register with the internal SINT. The effect of a write to the DStatCtrl register on these signals does not appear until the next SINT after the write.

microcontroller-DSP communications

The microcontroller and the DSP communicate by means of two separate 32-byte first-in first-out (FIFO) buffers. Figure 13 illustrates this scheme. The microcontroller writes to FIFO A, but data read from the same address comes from FIFO B. On the DSP side, the situation is reversed.

To send data to the DSP, the microcontroller writes data to FIFO A. To indicate to the DSP that FIFO A is ready to be read, the microcontroller writes a 1 to the Send-C bit of the microcontroller interrupt control register MIntCtrl. When this happens, the DSP interrupt line CINT goes active, signaling to the DSP that data is waiting. At the same time, the value that can be read from the Clear-C bit in the DIntCtrl register goes from 0 to 1, indicating that the interrupt is pending. When the DSP writes a 1 to the Clear-C bit, the CINT line returns to the inactive state and the value that can be read from Clear-C is 0. The microcontroller cannot deassert the CINT line.

The microcontroller-DSP communications interface is symmetric. Data sent from the DSP to the microcontroller is handled as described above, with the roles of A and B FIFOs and C and D bits and interrupts reversed. If the number of reads exceeds the number of writes from the other side, the values read are undefined.

FPREN (accessible by both the DSP and microcontroller) in the WBDCtrl register can be used to enable (active high) FIFO pointer resets. When this bit is set, the central processing unit (CPU) write pointer and the DSP read pointer are cleared whenever the CINT interrupt is cleared; and the CPU read pointer and the DSP write pointer are cleared whenever the DINT interrupt is cleared. The interrupts do not have to be active for the pointer clear to occur. In addition, these pointers are cleared whenever there is a powerup or reset.

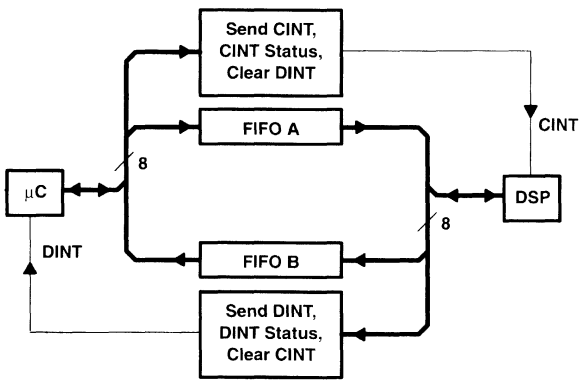

Figure 13. Microcontroller-DSP Data Buffers

microcontroller register map

The microcontroller can access 17 locations within the TCM4301. The register locations are 8 bits wide, as shown in Table 17 and Table 18.

Table 17. Microcontroller Register Map

ADDR	NAME	D7	D6	D5	D4	D3	D2	D1	D0
00h	WBDCtrl	WBD_LCKD	WBD_ON	WBD_BW			VHR_ON	M_INT_POL	FPREN
00h	WBD	MSB							LSB
01h	FIFO	MSB		FIFO A(B) Microcontroller to DSP (DSP to Microcontroller)					LSB
02h	MIntCtrl	Clear WBD	Clear-F	Clear-D	Send-C	AGCEN	AFCEN	FMRXEN	SM
03h	SynData0	MSB							LSB
04h	SynData1	MSB							LSB
05h	SynData2	MSB							LSB
06h	SynData3	MSB							LSB
07h	SynCtrl0	SEL[2:0]			LOWVAL				
08h	SynCtrl1	CLKDIV[1:0]		MSB/LSB FIRST	HIGHVAL				
09h	SynCtrl2	CLKDIS	IDLPOL	CLKPOL	NUMCLKS				
0Ah	MCClock	DSP_CLK_DIV[1:0]		MC_CLK_DIV[5:0]					
0Bh	RSSI A/D	MSB							LSB
0Ch	BAT A/D	MSB							LSB
0Dh	LCD D/A	MSB			LSD	Reserved		MCSCEN	LCDEN
0Eh	MStatCtrl	SYNOL	TXONIND	SYNRDY	MCLKEN	CVRDY	AuxFS1	AuxFS0	MPAEN
0Fh	TXI Offset	Reserved		Sign	MSB				LSB
10h	TXQ Offset	Reserved		Sign	MSB				LSB

Table 18. Microcontroller Register Definitions

ADDR	NAME	CATEGORY	R/W
00h	WBDCtrl	Wide-band data	W
00h	WBD		R
01h	FIFO	FIFO A(B) microcontroller to DSP (DSP to microcontroller)	W/(R)
02h	MIntCtrl	Interrupt/control status	R/W
03h	SynData0	Synthesizer interface	W
04h	SynData1		W
05h	SynData2		W
06h	SynData3		W
07h	SynCtrl0		W
08h	SynCtrl1		W
09h	SynCtrl2		W
0Ah	MCClock	Microcontroller clock speed	W
0Bh	RSSI A/D	RSSI level	R
0Ch	BAT A/D	Battery level monitor	R
0Dh	LCD D/A	LCD contrast control	W
0Eh	MStatCtrl	Miscellaneous status/control	R/W
0Fh	TXI Offset	Transmit dc offset compensation	W
10h	TXQ Offset		W

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wide-band data/control register

This register is used for two functions, depending on whether it is being read from or written to. When read from, the register provides the latest 8 bits of received and demodulated data to the microcontroller. When it is written to, the bits are placed into the WBDCtrl register (see Table 17) as shown here:

	7	6	5–3	2	1	0
WBDCtrl	WBD_LCKD	WBD_ON	WBD_BW[2:0]	VHR_ON	M_INT_POL	FPREN
	R/W	R/W	R/W	W	W	W

When reading the WBDCtrl register, bit 7 (MSB) is the last received data bit.

The definition of the WBDCtrl register, according to the DSP register map, is shown in Table 19.

Table 19. WBDCtrl Register

BIT	R/W	NAME	FUNCTION	RESET VALUE
9	R/W	WBD_LCKD	Wide-band data lock data. Determines whether edge detector is locked (1) or unlocked (0).	0
8	R/W	WBD_ON	Wide-band data on. Turns the WBDD module on/off (1/0).	0
7–5	R/W	WBD_BW[2:0]	Wide-band data bandwidth. Sets the appropriate PLL bandwidth. 000 : 20 Hz 001 : 39 Hz 010 : 78 Hz 011 : 156 Hz 100 : 313 Hz 101 : 625 Hz 110 : 1250 Hz	110
4	W	VHR_ON	Half-rail reference voltage is turned on/off (1/0)	0
3	W	M_INT_POL	Microcontroller Interrupt polarity bit: 0 = as defined by MTS(0:1), 1 = inverted as defined by MTS(1:0)	0
2	W	FPREN	FIFO pointer reset enable. When set(1), the read pointer in the FIFO is reset when the interrupt (CINT or DINT) is cleared. When reset(0), the read pointer in the FIFO is not acted on when the interrupt is cleared.	0
1–0	—	—	Reserved	—

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microcontroller status and control registers

MCClock:

	7–6	5–0
MCClock	DSP_CLK_DIV[1:0]	MC_CLK_DIV[5:0]
	W	W

This location is used by the microcontroller to change the speed of its own clock and the DSP clock. The division modulus is equal to a binary coded value written into MC_CLK_DIV[5:0]. Writing a 0 is prohibited. The reset value is divide by 32. The clock speed change occurs after the write completes writing to DSP_CLK_DIV[1:0] and sets the speed of MCLKOUT as follows:

DSP_CLK_DIV(1:0)	MCLKOUT CLOCK FREQUENCY
00	38.88 MHz
01	19.44 Mhz
10	9.72 MHz
11	4.86 MHz

MIntCtrl Bits [7:4]: These bit names in this field indicate the resulting action when the bit is set to 1. When these bits are being read, a 1 indicates that the corresponding interrupt is pending. A 0 indicates that the interrupt is clear. Writing a 0 into any bit location has no effect.

MIntCtrl Bits [3:1]: These bits enable power to the AGC and AFC DACs and their corresponding outputs. FMRXEN can be used to assert (set to 1) the FMRXEN external function. The reset value is 0 (off).

	7	6	5	4	3	2	1	0
MIntCtrl	Clear WBD	Clear-F	Clear-D	Send-C	AGCEN	AFCEN	FMRXEN	SM
					R/W			

MStatCtrl: This register contains various signals needed for system monitoring and control (see Table 20).

	7	6	5	4	3	2	1	0
MStatCtrl	SYNOL	TXONIND	SYNRDY	MCLKEN	CVRDY	AuxFS1	AuxFS0	MPAEN
	R	R	R	R/W	R	R/W	R/W	R/W

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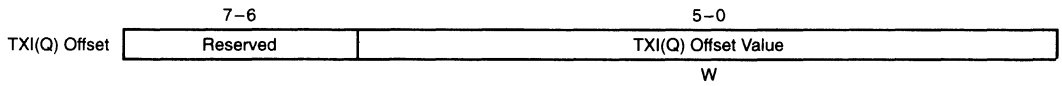
microcontroller status and control registers

Table 20. MStatCtrl Register Bits

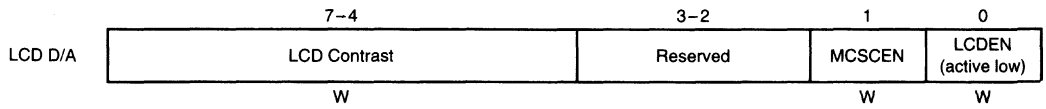
BIT	R/W	NAME	FUNCTION	RESET VALUE
7	R	SYNOL	Synthesizer out of lock. Equal to level applied to SYNOL input pin. Can be used as an input for an externally generated status signal to prevent transmission when external synthesizers are out of lock. In digital mode, when SYNOL is high, PAEN will not be asserted and no signal can be transmitted from TXIP, TXIN, TXQP, and TXQN.	Ext. pin
6	R	TXONIND	Transmitter on indicator. Equal to level applied to TXONIND input pin. Can be used to indicate power is applied to power amplifier.	Ext. pin
5	R	SYNRDY	Synthesizer interface ready to be programmed by the microcontroller. When a 1, the microcontroller can program the frequency synthesizer interface. A 0 indicates the interface circuit is busy.	1
4	R/W	MCLKEN	MCLKOUT enable. When set to 1 by the microcontroller, the 38.88-MHz master clock is sent out via MCLKOUT. Writing 0 to this bit disables MCLKOUT signal.	1
3	R	CVRDY	Conversion ready. A 1 indicates that the latest RSSI or battery voltage A/D conversion is complete and can be read from the RSSI or battery register location. Goes to 0 when microcontroller reads from either of these locations.	1
2	R/W	AuxFS[1]	Auxiliary DACs full-scale select. The auxiliary DACs are AGC, AFC, PWRCONT and also LCD CONTR DAC. The microcontroller selects the full-scale output ranges with these bits. See Table 12 and Table 13 for bit-to-output range mapping.	0
1		AuxFS[0]		0
0	R/W	MPAEN	Microcontroller PA enable. A 0 indicates the external PA enable line PAEN is prevented from going active. See Figure 12.	0

TXI Offset and TXQ Offset: These registers allow the differential offset voltages TXIP – TXIN and TXQP – TXQN to be adjusted to compensate for internal and/or external offsets. The magnitude of adjustment is D × step size, where D is a 6-bit, 2s complement integer written into bits 5–0 of these registers (see Table 6).



LCD contrast

LCD contrast register allows for 16 levels of control of terminal LCD contrast. The register is input to the LCD contrast D/A allowing control of the level of intensity of the LCD display.



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DSP register map

The register map accessible to the DSP port is shown in Table 21 and Table 22. There are 14 system addressable locations. Note that the write address of FIFO B is the same as the read address of FIFO A. Figure 14 details the connection of TCM4301 to an example DSP.

Table 21. DSP Register Map

ADDR	NAME	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00h	WBD	MSB							LSB	Reserved	
01h	WBDCtrl	WBD_LCKD	WBD_ON	WBD_BW			VHR_ON	M_INT_POL	FPREN	Reserved	
02h	RXI	Sign	MSB								LSB
03h	RXQ	Sign	MSB								LSB
04h	TXI	Sign	MSB								LSB
05h	TXQ	Sign	MSB								LSB
06h	FIFO	MSB	FIFO A(B) microcontroller to DSP (DSP to microcontroller)						LSB	Reserved	
07h	DIntCtrl	Clear WBD	SDIS	Clear-C	Send-D	Send-F	Reserved				
08h	Timing Adj	MSB									LSB
09h	AGC DAC	MSB							LSB	Reserved	
0Ah	AFC DAC	MSB							LSB	Reserved	
0Bh	PWR DAC	MSB							LSB	Reserved	
0Ch	DStatCtrl	TXGO	MODE	SCEN	FMVOX	FMRXEN	IQRXEN	TXEN	OUT1	RXOF	ALB
0Dh	BST Offset	Reserved								MSB	LSB
0Eh	Slp_Cmp	MSB									LSB
0Eh	Slp_Cntr	MSB									LSB
0Fh	Slp_Ctrl	Reserved				TEST (R/W)	STP_TMR(W) MCSM(R)	STR_TMR(W) TMR_STS(R)	Slp_Cntr[12:10](R) Slp_Cmp[12:10](W)		

Table 22. DSP Register Definitions

ADDR	NAME	CATEGORY	R/W
00h	WBD	Wide-band data	R
01h	WBDCtrl	Wide-band data control	R/W
02h	RXI	RX channel A/D results	R
03h	RXQ		
04h	TXI	Analog mode: TXI D/A data	W
		Digital mode: π/4 DQPSK modulator input data	
05h	TXQ	Analog mode: TXQ D/A data	W
		Digital mode: Not used	
06h	FIFO	FIFO A(B) microcontroller to DSP (DSP to microcontroller)	R/(W)
07h	DIntCtrl	Interrupt control/status	R/W
08h	Timing Adj	Symbol timing adjust	W
09h	AGC DAC	AGC	W
0Ah	AFC DAC	AFC	W
0Bh	PWR DAC	Power control	W
0Ch	DStatCtrl	Miscellaneous status/control	R/W
0Dh	BST Offset	TDM burst offset	W
0Eh	Slp_Cmp	Sleep compare data	W
0Eh	Slp_Cntr	Sleep counter data	R
0Fh	Slp_Ctrl	Sleep mode control	R/W

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wide-band data registers

Bit 9 of the wide-band data register is the most recently received bit.

	9–2	1–0
WBD	WB Data	Reserved
	R	

	9	8	7–5	4	3	2	1–0
WBDCtrl	WBD_LCKD	WBD_ON	WBD_BW[2:0]	VHR_ON	M_INT_POL	FPREN	Reserved
	R/W	R/W	R/W				

base station offset register

BST offset values are 00, 01, 10, and 11 corresponding to an offset value d of 0, 1, 2, and 3 respectively.

	9–2	1–0
BST	Reserved	Offset[1:0]
Offset		W

The delay in the TCM4301 TX channels is increased by the amount

$$d \times \frac{T_{SINT}}{4}$$

DSP status and control registers

DIntCtrl, Clear and Send BIts: The bit names in the DIntCtrl register indicate the action to be taken when a 1 is written to the bit. When reading these bits, a 1 indicates that the corresponding interrupt is pending. A 0 indicates that the interrupt is not pending. Writing a 0 to any bit has no effect. Writing a 1 to the clear bits clears the corresponding interrupt, and the interrupt terminal returns to its inactive level. Writing a 1 to the send bits causes the corresponding interrupt to go active.

DIntCtrl, SDIS: When a 1 is written to SDIS, the SINT interrupt going to the DSP is disabled. The disabling and re-enabling function is buffered to prevent the SINT signal from having shortened periods of output active. The SDIS bit is active (1) upon reset.

	9	8	7	6	5	4–0
DIntCtrl	Clear WBD	SDIS	Clear-C	Send-D	Send-F	Reserved
			R/W			

	9	8	7	6	5	4	3	2	1	0
DStatCtrl	TXGO	MODE	SCEN	FMVOX	FMRXEN	IQRXEN	TXEN	OUT1	RXOF	ALB
					R/W					

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DSP status and control registers (continued)

The DStatCtrl register contains various signals needed for system monitoring and control. These are described in Table 23.

Table 23. DStatCtrl Register Bits

BIT	R/W	NAME	FUNCTION	RESET VALUE
9	R/W	TXGO	Transmitter go. Used in digital mode, to initiate (1) and terminate (0) a transmit burst.	0
8	R/W	MODE	Digital (1) – Analog (0) mode select. Affects the clock dividers and the transmitter modes of operation and the Q side filter.	0
7	R/W	SCEN	Speech codec enable. (microphone/speaker interface chip.) The SCEN output pin is connected to this bit. Also enables (1) or disables (0) the internal speech codec clock generation circuits. (2.048 MHz – 8 kHz outputs)	0
6	R/W	FMVOX	FM voice enable. FMVOX = 1 enables the Q side of the internal receiver circuits and connects the receivers Q channel input to FM input pin (see Figure 12).	0
5	R/W	FMRXEN	FM receiver enable. The FMRXEN output pin is connected to this bit (see Figure 12).	0
4	R/W	IQRXEN	I and Q receiver enable. The IQRXEN output pin is connected to this bit. Enables (1), disables (0) power to the I and Q sides of the internal receiver circuits (see Figure 12).	0
3	R/W	TXEN	Transmitter enable. The TXEN output pin is connected to this bit. Enables (1), disables (0) power to the internal transmitter circuits (see Figure 12).	0
2	W	OUT1	Output 1. User defined general purpose data or control signal.	0
1	R/W	RXOF	Receive channel offset. RXOF = 1 disconnects the RXIP, RXIN, RXQP, and RXQN pins from receive channel,. and shorts internal RXIP to RXIN and RXQP to RXQN. It provides the capability of measuring dc offset of the receive channel.	0
0	R/W	ALB	Analog loop-back. ALB = 1 disconnects the RXIP, RXIN, RXQP, and RXQN pins from the internal receive channels and connects the corresponding internal signals to attenuated copies of the TXIP, TXIN, TXQP, and TXQN signals. The attenuated factor is 8.	0

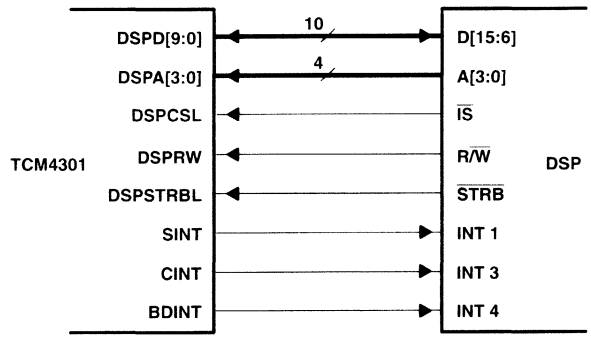

Figure 14. DSP Interface

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DSP sleep registers

Address 0Fh is decoded to be the sleep mode register (Slp_Ctrl). Bit 5 (active high) is the TEST bit and is used to allow write-only registers to be read for test purposes. Bit 4 is the stop timer bit (STP_TMR) which is written and latched. When read, this bit is the microcontroller sleep mode bit. Bit 3 is the start timer bit (STR_TMR). When a 1 is written to this bit, the MCLK delay starts. These control signals are active high and are cleared during initialization. When bit 3 is read, it is the timer status bit (TMR_STS). It indicates the mode status of the timer circuit. Bits 2, 1, and 0 are the three most significant bits of the sleep counter for reads from address 0Fh and the three most significant bits of the sleep compare register during writes to address 0Fh.

Address 0Eh is decoded to be a write-only and a read-only 10-bit register. The write-only register is the 10 least significant bits of the sleep compare register (Slp_Cmp). The read-only register is the 10 least significant bits of the sleep counter (Slp_Cntr).

When TEST = 1, reading address 0Eh returns the value of the 10 least significant bits of the sleep compare register. When address 0Fh is being read, bit 5 is the TEST bit, bit 4 is the MCSM bit, bit 3 is the TMR_STS bit, and bits 2:0 are the three most significant bits of the sleep compare register.

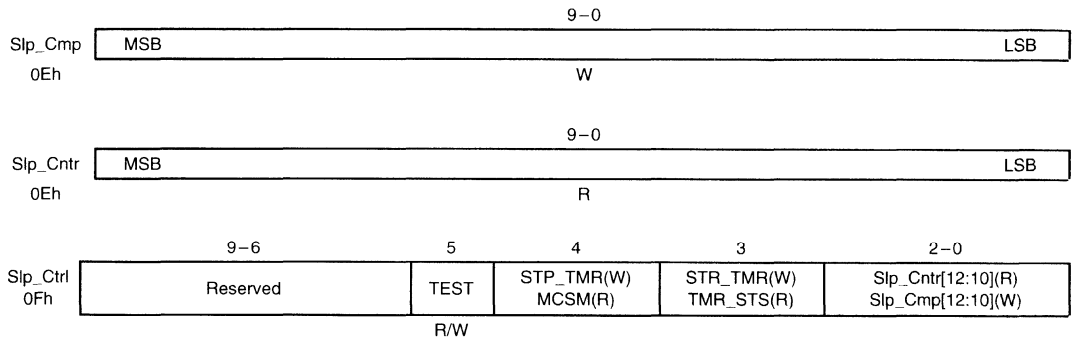

Table 24. Slp_Ctrl Register Bits

BIT	R/W	NAME	FUNCTION	RESET VALUE
9–6	N/A	Reserved		0
5	R/W	TEST	Enables write-only sleep registers to be read	0
4	R	MCSM	Microcontroller sleep mode status bit	N/A
4	W	STP_TMR	Stop timer	0
3	R	TMR_STS	Timer status bit. 1 = running, 0 = not running	N/A
3	W	STR_TMR	Start timer	N/A
2–0	R	Slp_Cntr[12:10]	Three most significant bits of the sleep counter	0
2–0	W	Slp_Cmp[12:10]	Three most significant bits of the sleep compare register	0

reset

internal reset

A low on RSINL causes the TCM4301 internal registers to assume their reset values. The power-on reset circuit also causes internal reset. However, the logic level at RSINL has no effect on reset outputs RSOUTH and RSOUTL.

power-on reset

The power-on reset (POR) is digitally implemented and provides a timed POR signal at RSOUTL and RSOUTH. The POR pulse duration is equal to 388,800 cycles of MCLKIN (10 ms). There are two outputs to provide a high reset and a low reset in order to accommodate the reset polarity requirements of any external device. The TCM4301 internal registers are reset when the POR outputs are activated. See Figure 15.

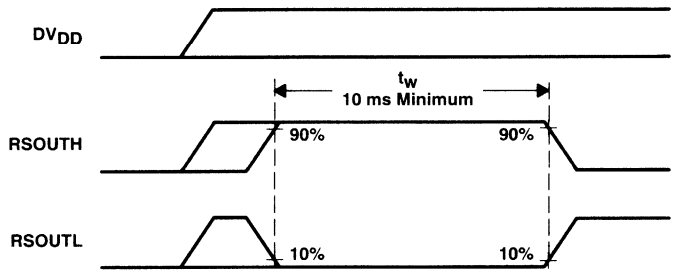

Figure 15. Power-On Reset Timing

internal reset state

After power-on reset, the TCM4301 register bits are initialized to the values shown in Table 25. The synthesizer control pins SYNCLK, SYNLE[0:2], and SYNDTA are high after reset, and the synthesizer interface circuit is in stable idle state with no SYNCLK outputs.

Table 25. Power-On Reset Register Initialization

REGISTER NAME	BIT 9	8	7	6	5	4	3	2	1	0
DIntCtrl	0	1	0	0	0	r	r	r	r	r
DStatCtrl	0	0	0	0	0	0	0	0	0	0
MIntCtrl			0	0	0	0	0	0	0	r
MStatCtrl			ext	ext	1	1	0	0	0	0
MCClock					0	0	0	0	0	0

r: reserved
ext: bit value from external pin

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microcontroller interface

The microcontroller interface of the TCM4301 is a general-purpose bus interface, which ensures compatibility with a wide range of microcontrollers, including the Mitsubshi M37700 series and most Intel and Motorola series. The interface consists of a pair of microcontroller type select (MTS[1:0]) inputs, address and data buses, as well as several input and output control signals that are designed to operate in a manner compatible with the microcontroller selected by the user.

Table 26. Microcontroller Interface Configuration

MTS1	MTS0	MODE	POLARITY	
			DS ACTIVE	INTERRUPT/OUTPUT ACTIVE
0	0	Intel	Low (separate Read and Write)	High
1	0	Motorola 16-bit and Mitsubishi	Low	Low
0	1	Motorola 8-bit	High	Low
1	1	Reserved	N/A	N/A

The microcontroller interface of the TCM4301 is designed to allow direct connection to many microcontrollers. Except for the interrupt pins, it is designed to connect to microcontrollers in the same manner as a memory device.

The internal chip select is asserted when MCCSH = 1 and MCCSL = 0.

Intel microcontroller mode of operation

When the microcontroller type select (MTS[1:0]) inputs are both held low, the TCM4301 microcontroller interface is configured into Intel mode (see Table 26). In this mode, the interface uses separate read and write control strobes and active-high interrupt signals. The processor $\overline{RD}$ and $\overline{WR}$ strobe signals should be connected to the TCM4301 MCDS signal and MCRW signal, respectively. The multiplexed address and data buses of the microcontroller must be demultiplexed by external hardware. Table 27 lists the microcontroller interface connections for Intel mode.

Table 27. Microcontroller Interface Connections for Intel Mode

TCM4301 PIN	MICROCONTROLLER PIN
MTS[1:0]	Tie to logic levels: low and low, respectively
MCCSH	Not on microcontroller; can be used for address decoding
MCCSL	Not on microcontroller; can be used for address decoding
MCD[7:0]	AD[7:0] data bus on microcontroller
MCA[4:0]	Demultiplexed address bits not on microcontroller
MCRW	$\overline{WR}$ (Active-low write data strobe)
MCDS	$\overline{RD}$ (Active-low read data strobe) MCDS configured to active-low operation by MTS[1:0]. The microcontroller bus must be demultiplexed by external hardware.
MWBDFINT	One of INT[3:0] as appropriate
DINT	One of INT[3:0] as appropriate

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Mitsubishi microcontroller mode of operation

When the microcontroller type select (MTS[1:0]) inputs are held high and low, respectively, the TCM4301 microcontroller interface is configured into Mitsubishi mode. In this mode, the interface has a single read/write control (R/$\overline{W}$) signal, an active-low data strobe (MCDS) signal, and active-low interrupt request signals. The processor $\overline{E}$ and R/($\overline{W}$) signals should be connected to the TCM4301 MCDS signal and MCRW signal, respectively. Table 28 lists the microcontroller interface connections for Mitsubishi mode.

Table 28. Microcontroller Interface Connections for Mitsubishi Mode

TCM4301 PIN	MICROCONTROLLER PIN
MTS[1:0]	Tie to logic levels: high and low, respectively
MCCSH	Not on microcontroller; can be used for address decoding
MCCSL	Not on microcontroller; can be used for address decoding
MCD[7:0]	D[7:0] data bus on microcontroller
MCA[4:0]	A[4:0]
MCRW	R/$\overline{W}$
MCDS	$\overline{E}$ (Active-low read data strobe) MCDS configured to active-low operation by MTS[1:0].
MWBDFINT	One of INT[3:0] as appropriate
DINT	One of INT[3:0] as appropriate

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Motorola microcontroller mode of operation

When the microcontroller type select MTS0 = high and MTS1 = low, the TCM4301 microcontroller interface is configured for 8-bit family (6800 family derivatives, e.g., 68HC11D3 and 68HC11G5) bus characteristics, and when the microcontroller type select MTS0 = low and MTS1 = high, the microcontroller interface is configured for 16-bit family (680 × 0 family derivatives, e.g., 68008 and 68302) characteristics. The Motorola mode makes use of a single read/write control (R/$\overline{W}$) signal and active-low interrupt request signals. The processor E (8 bit) or $\overline{DS}$ (16 bit) and (R/$\overline{W}$) control signals should be connected to the TCM4301 MCDS signal and the MCRW signal, respectively. Table 29 illustrates the connections between the TCM4301 and an 8-bit Motorola processor. Table 30 illustrates the connections between the TCM4301 and a 16-bit Motorola processor.

Table 29. Microcontroller Interface Connections for Motorola Mode (8 Bit)

TCM4301 PIN	MICROCONTROLLER PIN
MTS[1:0]	Tie to logic levels: low and high, respectively
MCCSH	Not on microcontroller; can be used for address decoding
MCCSL	Not on microcontroller; can be used for address decoding
MCD[7:0]	PC[7:0] data bus on microcontroller
MCA[4:0]	Demultiplexed address output. PF[4:0] on microcontroller for nonmultiplexed machines (e.g., 68CH11G5) and not on micro for multiplexed bus machines (e.g., 68HC11D3).
MCRW	R/$\overline{W}$
MCDS	E (Active-high data strobe) MCDS configured to active-high operation by MTS[1:0].
MWBDFINT	$\overline{IRQ}$ and/or $\overline{NMI}$ as appropriate
DINT	$\overline{IRQ}$ and/or $\overline{NMI}$ as appropriate

Table 30. Microcontroller Interface Connections for Motorola Mode (16 Bit)

TCM4301 PIN	MICROCONTROLLER PIN
MTS[1:0]	Tie to logic levels: high and low, respectively
MCCSH	Not on microcontroller; can be used for address decoding
MCCSL	Not on microcontroller (68000, 68008) $\overline{CS1}$, $\overline{CS2}$, or $\overline{CS3}$ (68302)
MCD[7:0]	D[7:0] data bus on microcontroller
MCA[4:0]	A[4:0] (68008) A[5:1] (68000, 68302)
MCRW	R/$\overline{W}$
MCDS	$\overline{DS}$ (active-low data strobe) (68008) $\overline{LDS}$ (active-low data strobe) (68000, 68302) MCDS configured to active-low operation by MTS[1:0]
MWBDFINT	$\overline{IACK7}$, $\overline{IACK6}$, or $\overline{IACK1}$ (68302) Not on microcontroller (68000, 68008)
DINT	One of INT[3:0] as appropriate

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range: DV_{DD} (see Notes 6 and 7): Condition 1 . . . . . V_{SS} −0.3 to +6 V
Condition 2 . . . . . V_{SS} −0.3 to AV_{DD} +0.3 V
AV_{DD} (see Notes 7 and 8): Condition 1 . . . . . V_{SS} −0.3 to +6 V
Condition 2 . . . . . V_{SS} −0.3 to DV_{DD} +0.3 V
Input voltage range, V_I: Digital signals . . . . . V_{SS} −0.3 to DV_{DD} +0.3 V
Analog signals . . . . . V_{SS} −0.3 to AV_{DD} +0.3 V
Output voltage range, V_O: Digital signals . . . . . V_{SS} to DV_{DD}
Analog signals . . . . . V_{SS} to AV_{DD}
Continuous total power dissipation . . . . . See Dissipation Table
Operating free-air temperature range, T_A . . . . . −40°C to 85°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 6. Voltage values are with respect DV_{SS}.
7. Maximum voltage is the minimum of the two conditions.
8. Voltage values are with respect to AV_{SS}.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR (T_{JA}) ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
PZ	2222 mW	45°C/W	889 mW

recommended operating conditions

			MIN	MAX	UNIT
DV_{DD}	Supply voltage		3	5.5	V
V_{IH}	High-level input voltage	Digital	0.7 DV_{DD}	DV_{DD}+0.3	V
V_{IL}	Low-level input voltage	Digital	0	0.3 DV_{DD}	V
V_{OH}	High-level output voltage	Digital	0.7 DV_{DD}	DV_{DD}	V
V_{OL}	Low-level output voltage	Digital	0	0.5	V
I_{OH}	High-level output current at 3 V	Digital	2		mA
I_{OL}	Low-level output current at 3 V	Digital	2		mA
I_{OH}	High-level output current at 5 V	Digital	2		mA
I_{OL}	Low-level output current at 5 V	Digital	2		mA
T_A	Operating free-air temperature		−40	85	°C

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electrical characteristics power consumption over full range of operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Analog transmitting and receiving		DV_{DD} = 3 V,	AV_{DD} = 3 V		75		mW
		DV_{DD} = 5.5 V,	AV_{DD} = 5.5 V		275		
Digital receiving		DV_{DD} = 3 V,	AV_{DD} = 3 V		60		mW
		DV_{DD} = 5.5 V,	AV_{DD} = 5.5 V		250		
Digital transmitting		DV_{DD} = 3 V,	AV_{DD} = 3 V		85		mW
		DV_{DD} = 5.5 V,	AV_{DD} = 5.5 V		300		
Idle mode	MCLKOUT enabled	DV_{DD} = 3 V,	AV_{DD} = 3 V		45		mW
	MCLKOUT disabled	DV_{DD} = 3 V,	AV_{DD} = 3 V		17		
	MCLKOUT enabled	DV_{DD} = 5.5 V,	AV_{DD} = 5.5 V		190		
	MCLKOUT disabled	DV_{DD} = 5.5 V,	AV_{DD} = 5.5 V		96		
IS-136 standby (sleep mode)		DV_{DD} = 3 V,	AV_{DD} = 3 V		15		mW
		DV_{DD} = 5.5 V,	AV_{DD} = 5.5 V		85		
Digital mode, 1/3 transmitting +1/3 receiving + 1/3 standby		DV_{DD} = 3 V,	AV_{DD} = 3 V		60		mW
		DV_{DD} = 5.5 V,	AV_{DD} = 5.5 V		220		

† All typical values are at T_A = 25°C

reference characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$V_{OH(VHR)}$	High-level output voltage		0.5 AV_{DD}–0.2		0.5 AV_{DD}+0.2	V
r_O	Output resistance	FMVOX or IQRXEN or TXEN = high		80	100	Ω
		FMVOX or IQRXEN or TXEN = low	15	40		kΩ

‡ All typical values are at DV_{DD} = 5 V, AV_{DD} = 5 V, and T_A = 25°C

terminal impedance

FUNCTION	TERMINAL NAME	MIN	TYP§	MAX	UNIT
Receive channel input impedance (single-ended)	RXIP/N and RXQP/N	40	70		kΩ
Transmit channel output impedance (single-ended)	TXIP/N and TXQP/N	40	50	100	Ω
FM input	WBD	25	200		kΩ
MCLKOUT	MCLKOUT @ 3.3 V		240		Ω
	MCLKOUT @ 5 V		180		

§ All typical values are at DV_{DD} = 5 V, AV_{DD} = 5 V, and T_A = 25°C, unless otherwise specified.

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MCLKOUT timing requirements

		MIN	NOM	MAX	UNIT
t_{wH}	Pulse duration high	9	10	12	ns
t_{wL}	Pulse duration low	9	10	12	ns
t_r	Rise time	2	3	4	ns
t_f	Fall time	2	3	4	ns

NOTE: Tested with 15 pF loading on MCLKOUT.

PARAMETER MEASUREMENT INFORMATION

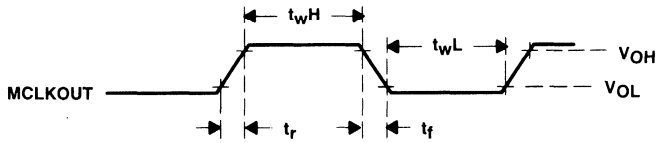

Figure 16. MCLKOUT Timing Diagram

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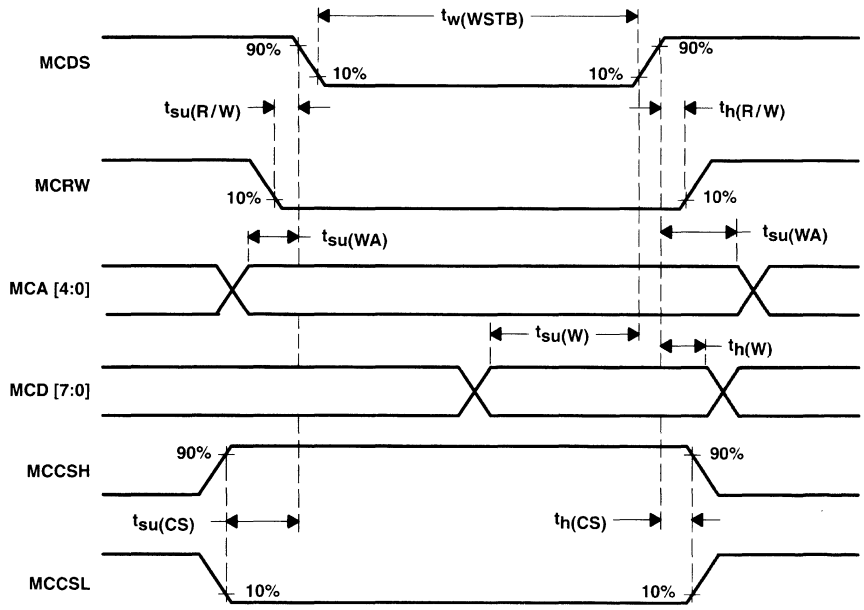
PARAMETER MEASUREMENT INFORMATION

TCM4301 to microcontroller interface timing requirements (Mitsubishi write cycle)

PARAMETER			ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(R/W)}$	Setup time, read/write	Read/write (MCRW) stable before falling edge of strobe (MCDS)	$TRW_{(SU)}$	0		ns
$t_{h(R/W)}$	Hold time, read/write	Read/write (MCRW) stable after rising edge of strobe (MCDS)	$TRW_{(HO)}$	10		ns
$t_{su(WA)}$	Setup time, write address	Address (MCA) stable before falling edge of strobe (MCDS)	$TWA_{(SU)}$	0		ns
$t_{h(WA)}$	Hold time, write address	Address (MCA) stable after rising edge of strobe (MCDS)	$TWA_{(HO)}$	10		ns
$t_{su(W)}$	Setup time, write data	Data stable (MCD) before rising edge of strobe (MCDS)	$TWD_{(SU)}$	14		ns
$t_{h(W)}$	Hold time, write data	Data stable (MCD) after rising edge of strobe (MCDS)	$TWD_{(HO)}$	0		ns
$t_{w(WSTB)}$	Pulse duration, write strobe	Write strobe pulse width	$TWR_{(STB)}$	60		ns
$t_{h(CS)}$	Hold time, chip select	Chip select (MCCSH and MCCSL) stable before rising edge of strobe (MCDS)	$TCS_{(HO)}$	0		ns
$t_{su(CS)}$	Setup time, chip select	Chip select stable (MCCSH and MCCSL) before falling edge of strobe (MCDS)	$TCS_{(SU)}$	0		ns

NOTE: Timings based upon Mitsubishi 37732S4 (16 MHz) and Mitsubishi 3772S4L (8 MHz).



NOTE: Chip selection is defined as both MCCS and MCDS active.

Figure 17. Microcontroller Interface Timing Requirements (Mitsubishi Configuration Write Cycle, MTS[1:0] = 10)

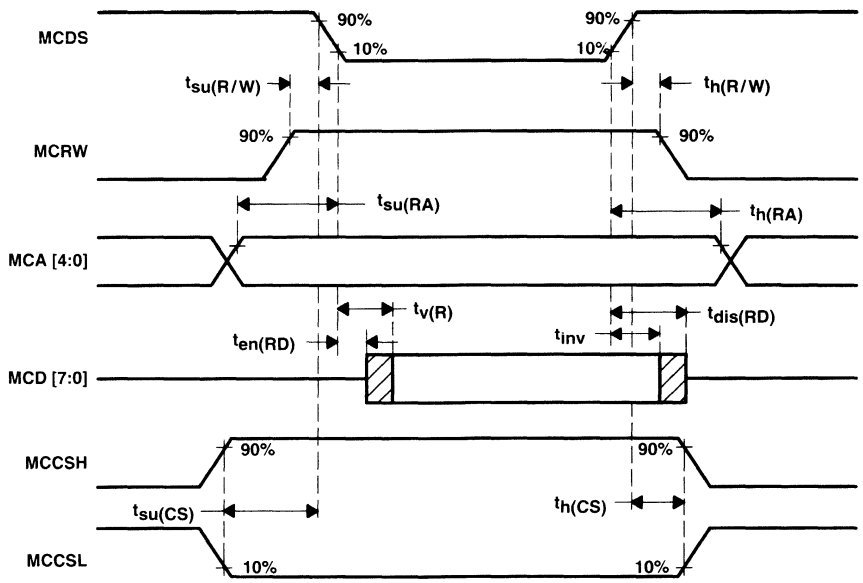
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

TCM4301 to microcontroller interface timing requirements (Mitsubishi read cycle)

PARAMETER			ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(R/W)}$	Setup time, read/write	Read/write (MCRW) stable before falling edge of strobe (MCDS)	$TRW_{(SU)}$	0		ns
$t_{h(R/W)}$	Hold time, read/write	Read/write (MCRW) stable after rising edge of strobe (MCDS)	$TRW_{(HO)}$	10		ns
$t_{su(RA)}$	Setup time, read address	Read address (MCS) stable before falling edge of strobe (MCDS)	$TRA_{(SU)}$	0		ns
$t_{h(RA)}$	Hold time, read address	Read address (MCA) stable after rising edge of strobe (MCDS)	$TRA_{(HO)}$	10		ns
$t_{en(RD)}$	Enable time, read data	Falling edge of strobe (MCDS) to TCM4301 driving data bus (MCD)	$TRD_{(EN)}$	10		ns
$t_{v(R)}$	Read data valid time	Falling edge of strobe (MCDS) to valid data (MCD)	$TRD_{(DV)}$		50	ns
t_{inv}	Data invalid time	Data (MCD) invalid after rising edge of strobe (MCDS)	$TRD_{(INV)}$		10	ns
$t_{dis(RD)}$	Disable time, read data	TCM4301 releases data bus after rising edge of strobe (MCDS)	$TRD_{(DIS)}$		28	ns
$t_{h(CS)}$	Hold time, chip select	Chip select (MCCSH and MCCSL) stable before rising edge of strobe (MCDS)	$TCS_{(HO)}$	0		ns
$t_{su(CS)}$	Setup time, chip select	Chip select stable (MCCSH and MCCSL) before falling edge of strobe (MCDS)	$TCS_{(SU)}$	0		ns

NOTE: Timings based upon Mitsubishi 37732S4 (16 MHz) and Mitsubishi 3772S4L (8 MHz).



NOTE: Chip selection is defined as both MCCS and MCDS active.

Figure 18. Microcontroller Interface Timing Requirements (Mitsubishi Configuration Read Cycle, MTS[1:0] = 10)

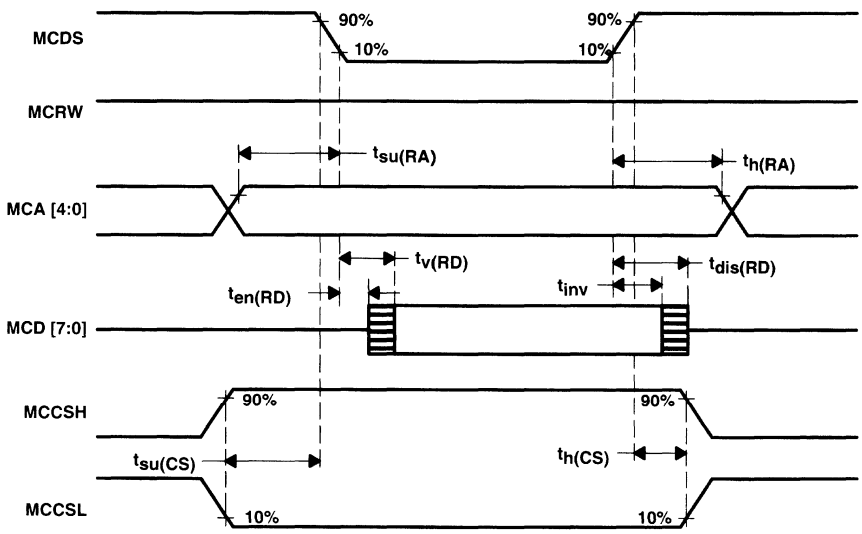
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

TCM4301 to microcontroller interface timing requirements (Intel read cycle)

PARAMETER			ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(RA)}$	Setup time, read address	Read address (MCA) stable before falling edge of strobe (MCDS)	$TRA_{(SU)}$	0		ns
$t_{h(RA)}$	Hold time, read address	Read address (MCA) stable after rising edge of strobe (MCDS)	$TRA_{(HO)}$	10		ns
$t_{en(RD)}$	Enable time, read data	Falling edge of strobe (MCDS) to TCM4301 driving data bus (MCD)	$TRD_{(EN)}$	10		ns
$t_{v(RD)}$	Valid time, read data	Falling edge of strobe (MCDS) to valid data (MCD)	$TRD_{(DV)}$		50	ns
t_{inv}	Data invalid time	Data (MCD) invalid after rising edge of strobe (MCDS)	$TRD_{(INV)}$		10	ns
$t_{dis(RD)}$	Disable time, read data	TCM4301 releases data bus after rising edge of strobe (MCDS)	$TRD_{(DIS)}$		28	ns
$t_{su(CS)}$	Setup time, chip select	Chip select (MCCSH and MCCSL) stable before falling edge of strobe (MCDS)	$TCS_{(SU)}$	0		ns
$t_{h(CS)}$	Hold time, chip select	Chip select (MCCSH and MCCSL) stable before rising edge of strobe (MCDS)	$TCS_{(HO)}$	0		ns

NOTE: Timings based upon Intel 80C186 (16 MHz)



NOTE: Chip selection is defined as both MCCS and MCDS active.

Figure 19. Microcontroller Interface Timing Requirements (Intel Configuration Read Cycle, MTS[1:0] = 00)

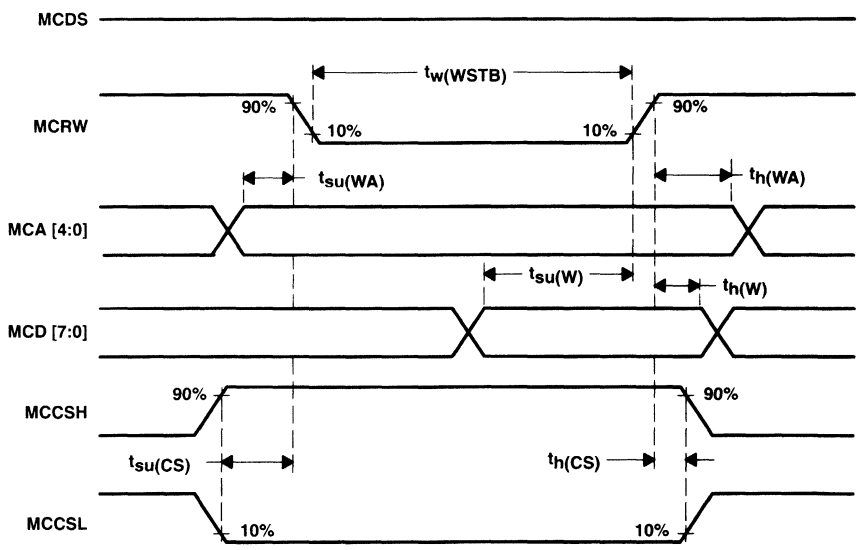
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

TCM4301 to microcontroller interface timing requirements (Intel write cycle)

PARAMETER			ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(WA)}$	Setup time, write address	Address (MCA) stable before falling edge of strobe (MCRW)	$TWA_{(SU)}$	0		ns
$t_{h(WA)}$	Hold time, write address	Address (MCA) stable after rising edge of strobe (MCRW)	$TWA_{(HO)}$	10		ns
$t_{su(W)}$	Setup time, write data	Data stable (MCD) before rising edge of strobe (MCRW)	$TWD_{(SU)}$	14		ns
$t_{h(W)}$	Hold time, write data	Data stable (MCD) after rising edge of strobe (MCRW)	$TWD_{(HO)}$	0		ns
$t_{w(WSTB)}$	Pulse duration, write strobe	Write strobe pulse width	$TWR_{(STB)}$	60		ns
$t_{su(CS)}$	Setup time, chip select	Chip select (MCCSH and MCCSL) stable before falling edge of strobe (MCRW)	$TCS_{(SU)}$	0		ns
$t_{h(CS)}$	Hold time, chip select	Chip select (MCCSH and MCCSL) stable before rising edge of strobe (MCRW)	$TCS_{(HO)}$	0		ns

NOTE: Timings based upon Intel 8C186 (16 MHz).



NOTE: Chip selection is defined as both MCCS and MCRW active.

Figure 20. Microcontroller Interface Timing Requirements (Intel Configuration Write Cycle, MTS[1:0] = 00)

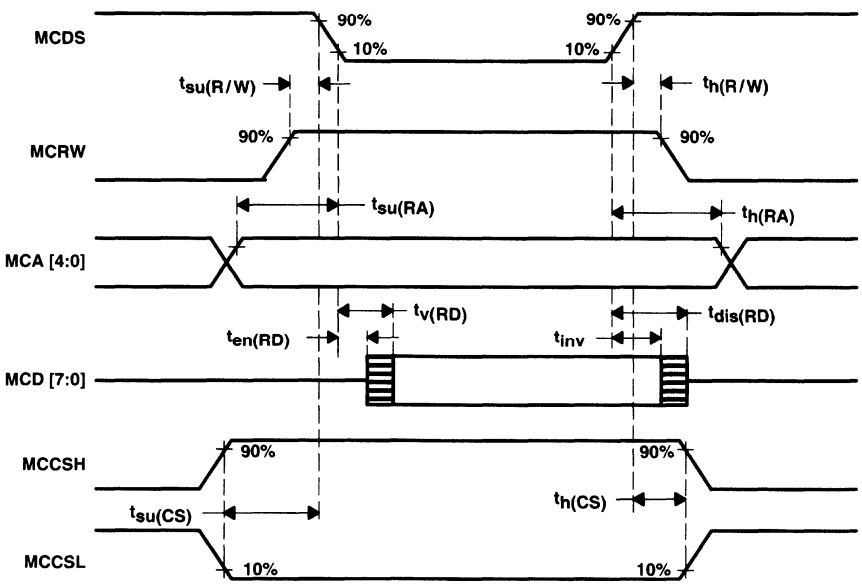
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

TCM4301 to microcontroller interface timing requirements (Motorola 16-bit read cycle)

PARAMETER			ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(R/W)}$	Setup time, read/write	Read/write (MCRW) stable before falling edge of strobe (MCDS)	$TRW_{(SU)}$	0		ns
$t_{h(R/W)}$	Hold time, read/write	Read/write (MCRW) stable after rising edge of strobe (MCDS)	$TRW_{(HO)}$	10		ns
$t_{su(RA)}$	Setup time, read address	Read address (MCA) stable before falling edge of strobe (MCDS)	$TRA_{(SU)}$	0		ns
$t_{h(RA)}$	Hold time, read address	Read address (MCA) stable after rising edge of strobe (MCDS)	$TRA_{(HO)}$	10		ns
$t_{en(RD)}$	Enable time, read data	Falling edge of strobe (MCDS) to TCM4301 driving data bus (MCD)	$TRD_{(EN)}$	10		ns
$t_{v(RD)}$	Valid time, read data	Falling edge of strobe (MCDS) to valid data (MCD)	$TRD_{(DV)}$		50	ns
t_{inv}	Data invalid time	Data (MCD) invalid after rising edge of strobe (MCDS)	$TRD_{(INV)}$		10	ns
$t_{dis(RD)}$	Disable time, read data	TCM4301 releases data bus after rising edge of strobe (MCDS)	$TRD_{(DIS)}$		28	ns
$t_{h(CS)}$	Hold time, chip select	Chip select (MCCSH and MCCSL) stable before falling edge of strobe (MCDS)	$TCS_{(HO)}$	0		ns
$t_{su(CS)}$	Setup time, chip select	Chip select stable (MCCSH and MCCSL) before rising edge of strobe (MCDS)	$TCS_{(SU)}$	0		ns

NOTE: Timings based upon Motorola 68HC000 (16.67 MHz) and Motorola 68302 (16 MHz).



NOTE: Chip selection is defined as both MCCS and MCDS active.

Figure 21. Microcontroller Interface Timing Requirements (Motorola 16-Bit Read Cycle, MTS[1:0] = 10)

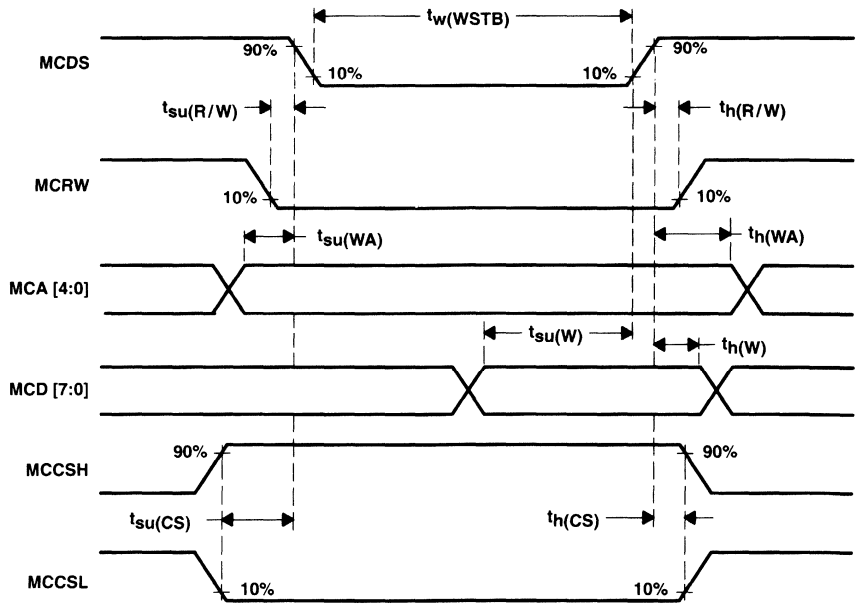
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

TCM4301 to microcontroller interface timing requirements (Motorola 16-bit write cycle)

PARAMETER			ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(R/W)}$	Setup time, read/write	Read/write (MCRW) stable before falling edge of strobe (MCDS)	$TRW_{(SU)}$	0		ns
$t_{h(R/W)}$	Hold time, read/write	Read/write (MCRW) stable after rising edge of strobe (MCDS)	$TRW_{(HO)}$	10		ns
$t_{su(WA)}$	Setup time, write address	Address (MCA) stable before falling edge of strobe (MCDS)	$TWA_{(SU)}$	0		ns
$t_{h(WA)}$	Hold time, write address	Address (MCA) stable after rising edge of strobe (MCDS)	$TWA_{(HO)}$	10		ns
$t_{su(W)}$	Setup time, write data	Data stable (MCD) before rising edge of strobe (MCDS)	$TWD_{(SU)}$	14		ns
$t_{h(W)}$	Hold time, write data	Data stable (MCD) after rising edge of strobe (MCDS)	$TWD_{(HO)}$	0		ns
$t_{w(WSTB)}$	Pulse duration, write strobe	Write strobe pulse width	$TWR_{(STB)}$	60		ns
$t_{h(CS)}$	Hold time, chip select	Chip select (MCCSH and MCCSL) stable before falling edge of strobe (MCDS)	$TCS_{(HO)}$	0		ns
$t_{su(CS)}$	Setup time, chip select	Chip select (MCCSH and MCCSL) stable before rising edge of strobe (MCDS)	$TCS_{(SU)}$	0		ns

NOTE: Timings based upon Motorola 68HC000 (16.67 MHz) and Motorola 68302 (16 MHz).



NOTE: Chip selection is defined as both MCCS and MCDS active.

Figure 22. Microcontroller Interface Timing Requirements (Motorola 16-Bit Write Cycle, MTS[1:0] = 10)

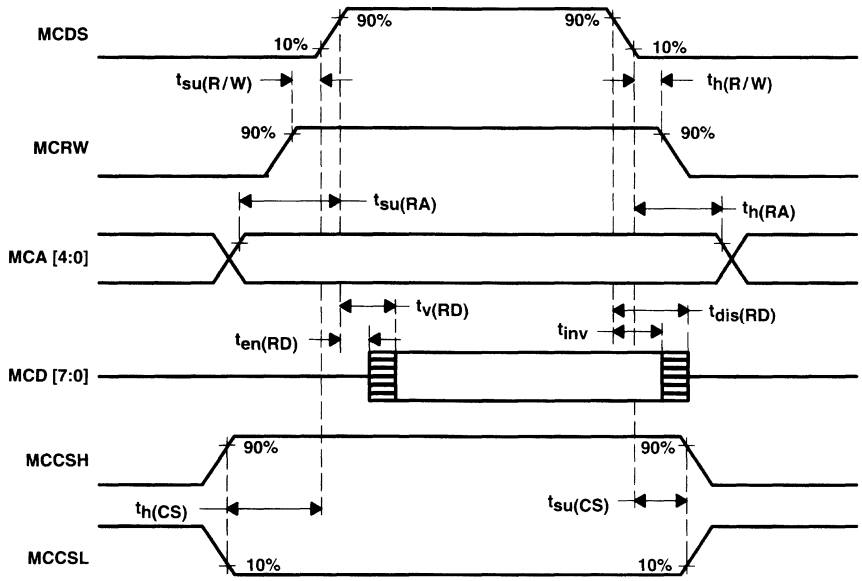
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

TCM4301 to microcontroller interface timing requirements (Motorola 8-bit read cycle)

PARAMETER			ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(R/W)}$	Setup time, read/write	Read/write (MCRW) stable before rising edge of strobe (MCDS)	$TRW_{(SU)}$	0		ns
$t_{h(R/W)}$	Hold time, read/write	Read/write (MCRW) stable after falling edge of strobe (MCDS)	$TRW_{(HO)}$	10		ns
$t_{su(RA)}$	Setup time, read address	Read address (MCA) stable before rising edge of strobe (MCDS)	$TRA_{(SU)}$	0		ns
$t_{h(RA)}$	Hold time, read address	Read address (MCA) stable after falling edge of strobe (MCDS)	$TRA_{(HO)}$	10		ns
$t_{en(RD)}$	Enable time, read data	Rising edge of strobe (MCDS) to TCM4301 driving data bus (MCD)	$TRD_{(EN)}$	10		ns
$t_{v(RD)}$	Valid time, read data	Rising edge of strobe (MCDS) to valid data (MCD)	$TRD_{(DV)}$		50	ns
t_{inv}	Data invalid time	Data (MCD) invalid after falling edge of strobe (MCDS)	$TRD_{(INV)}$		10	ns
$t_{dis(RD)}$	Disable time, read data	TCM4301 releases data bus after falling edge of strobe (MCDS)	$TRD_{(DIS)}$		28	ns
$t_{h(CS)}$	Hold time, chip select	Chip select (MCCSH and MCCSL) stable before falling edge of strobe (MCDS)	$TCS_{(HO)}$	0		ns
$t_{su(CS)}$	Setup time, chip select	Chip select (MCCSH and MCCSL) stable before rising edge of strobe (MCDS)	$TCS_{(SU)}$	0		ns

NOTE: Timings based upon Motorola 68HC11D3 (3 MHz) and Motorola 68HC11G5 (2.1 MHz).



NOTE: Chip selection is defined as both MCCS and MCDS active.

Figure 23. Microcontroller Interface Timing Requirements (Motorola 8-Bit Read Cycle, MTS[1:0] = 01)

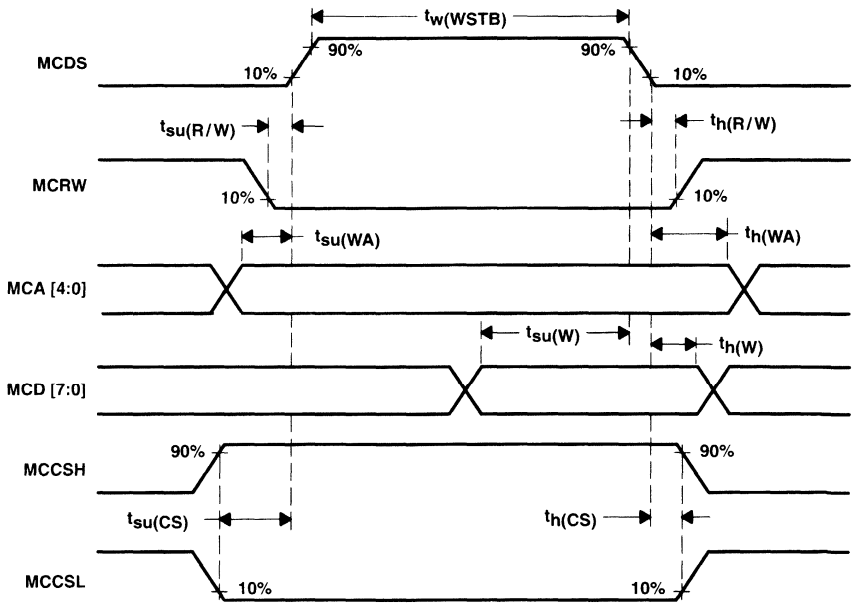
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

TCM4301 to microcontroller interface timing requirements (Motorola 8-bit write cycle)

PARAMETER			ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(R/W)}$	Setup time, read/write	Read/write (MCRW) stable before rising edge of strobe (MCDS)	$TRW_{(SU)}$	0		ns
$t_{h(R/W)}$	Hold time, read/write	Read/write (MCRW) stable after falling edge of strobe (MCDS)	$TRW_{(HO)}$	10		ns
$t_{su(WA)}$	Setup time, write address	Address (MCA) stable before rising edge of strobe (MCDS)	$TWA_{(SU)}$	0		ns
$t_{h(WA)}$	Hold time, write address	Address (MCA) stable after falling edge of strobe (MCDS)	$TWA_{(HO)}$	10		ns
$t_{su(W)}$	Setup time, write data	Data stable (MCD) before falling edge of strobe (MCDS)	$TWD_{(SU)}$	14		ns
$t_{h(W)}$	Hold time, write data	Data stable (MCD) after falling edge of strobe (MCDS)	$TWD_{(HO)}$	0		ns
$t_{w(WSTB)}$	Pulse duration, write strobe	Write strobe pulse width	$TWR_{(STB)}$	60		ns
$t_{h(CS)}$	Hold time, chip select	Chip select (MCCSH and MCCSL) stable before rising edge of strobe (MCDS)	$TCS_{(HO)}$	0		ns
$t_{su(CS)}$	Setup time, chip select	Chip select (MCCSH and MCCSL) stable before falling edge of strobe (MCDS)	$TCS_{(SU)}$	0		ns

NOTE: Timings based upon Mitsubishi 37732S4 (16 MHz) and Mitsubishi 3772S4L (8 MHz).



NOTE: Chip selection is defined as both MCCS and MCDS active.

Figure 24. Microcontroller Interface Timing Requirements (Motorola 8-Bit Write Cycle, MTS[1:0] = 01)

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

switching characteristics, TCM4301 to DSP Interface (write cycle)

PARAMETER			ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(R/W)}$	Setup time, read/write	Read/write (DSPRW) stable before falling edge of strobe (DSPSTRBL)	$TRW_{(SU)}$	0		ns
$t_{h(R/W)}$	Hold time, read/write	Read/write (DSPR W) stable after rising edge of strobe (DSPSTRBL)	$TRW_{(HO)}$	0		ns
$t_{su(CS)}$	Setup time, chip select	Chip select stable (DSPCSL) before falling edge of strobe (DSPSTRBL)	$TCS_{(SU)}$	0		ns
$t_{h(CS)}$	Hold time, chip select	Chip select (DSPCSL) stable after rising edge of strobe (DSPSTRBL)	$TCS_{(HO)}$	0		ns
$t_{su(WA)}$	Setup time, write address	Address (DSPA) stable before falling edge of strobe (DSPSTRBL)	$TWA_{(SU)}$	0		ns
$t_{h(WA)}$	Hold time, write address	Address (DSPA) stable after rising edge of strobe (DSPSTRBL)	$TWA_{(HO)}$	0		ns
$t_{su(W)}$	Setup time, write data	Data stable (DSPD) before rising edge of strobe (DSPSTRBL)	$TWD_{(SU)}$	3		ns
$t_{h(W)}$	Hold time, write data	Data stable (DSPD) after rising edge of strobe (DSPSTRBL)	$TWD_{(HO)}$	0		ns
$t_{w(WSTB)}$	Pulse duration, write strobe	Write strobe pulse width	$TWR_{(STB)}$	25		ns

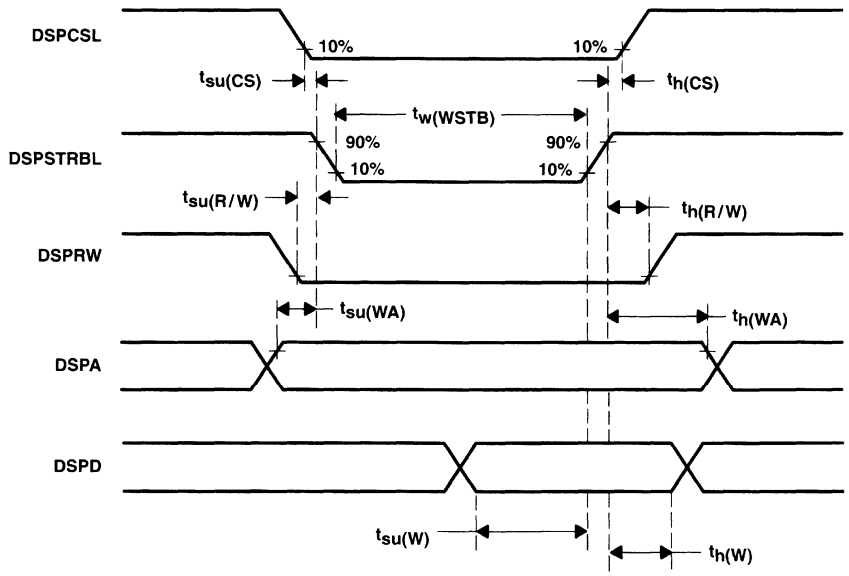


Figure 25. TCM4301 to DSP Interface (Write Cycle)

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

switching characteristics, TCM4301 to DSP Interface (read cycle)

PARAMETER			ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(R/W)}$	Setup time, read/write	Read/write (DSPRW) stable before falling edge of strobe (DSPSTRBL)	$TRW_{(SU)}$	0		ns
$t_{h(R/W)}$	Hold time, read/write	Read/write (DSPRW) stable after rising edge of strobe (DSPSTRBL)	$TRW_{(HO)}$	0		ns
$t_{su(CS)}$	Setup time, chip select	Chip select stable (DSPCSL) before falling edge of strobe (DSPSTRBL)	$TCS_{(SU)}$	0		ns
$t_{h(CS)}$	Hold time, chip select	Chip select (DSPCSL) stable after rising edge of strobe (DSPSTRBL)	$TCS_{(HO)}$	0		ns
$t_{su(RA)}$	Setup time, read address	Read address (DSPA) stable before strobe (DSPSTRBL) goes low	$TWA_{(SU)}$	0		ns
$t_{h(RA)}$	Hold time, read address	Read address (DSPA) stable after strobe (DSPSTRBL) goes high	$TWA_{(HO)}$	0		ns
$t_{en(R)}$	Enable time, read data	Falling edge of strobe (DSPSTRBL) to TCM4301 driving data bus (DSPD)	$TRD_{(EN)}$	0		ns
$t_{d(DV)}$	Delay read data valid time	Falling edge of strobe (DSPSTRBL) to valid data (DSPD)	$TRD_{(DV)}$		50	ns
$t_{h(R)}$	Hold time, read data	Data (DSPD) invalid after rising edge of strobe (DSPSTRBL)	$TRD_{(INV)}$	5		ns
$t_{dis(R)}$	Disable time, read data	TCM4301 releases data bus after rising edge of strobe (DSPSTRBL)	$TRD_{(DIS)}$		12	ns

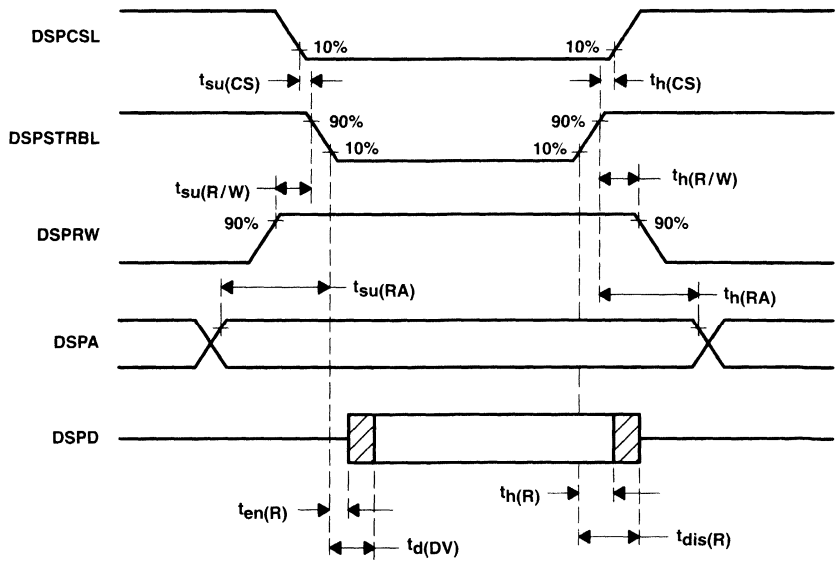


Figure 26. TCM4301 to DSP Interface (Read Cycle)

PRODUCT PREVIEW

TCM4400
GSM/DCS BASEBAND AND VOICE A/D AND D/A RF INTERFACE CIRCUIT

SLWS029 – JUNE 1996

- **Applications Include GSM 900 and DCS 1800 Cellular Telephones**
- **80-Pin TQFP Package**
- **Single 3-V Supply Voltage**
- **Internal Voltage Reference**
- **Extended RF Control Voltages**
- **Advanced Power Management**
- **GSM-DAI Interface**
- **MCU and DSP Serial Interface**
- **Five Ports Auxiliary A/D**
- **Meets JTAG Testability Standard (IEEE Std 1131.1-1990)**
- **Baseband Codec-GMSK Modulator with On-Chip Burst Buffer**
- **Voice Codec Features: Microphone Amplifier and Bias Source, Programmable Gain Amplifiers, Volume Control and Side-Tone Control**

description

The TCM4400 Global System for Mobile Communication (GSM) baseband RF interface circuit is designed for GSM 900 and DCS 1800 European digital cellular telecommunication systems. It includes a complete set of functions to perform the interface and processing of voice signals, generate baseband in-phase (I) and quadrature (Q) signals, and control the signals between a digital signal processor (DSP) and associated RF circuits.

The TCM4400 includes a second serial interface intended for use with a microcontroller. Through this interface, a microcontroller can access all the internal registers that can be accessed through the DSP digital serial interface. This option is intended for applications in which part of the L1 software is implemented in the microcontroller.

A 4-pin parallel port is dedicated to the full control of the digital audio interface (DAI) to the GSM system simulator that consists of system simulator reset (SSRST) control, clock generation, and rate adaptation with the DSP.

The voice processing portion of the device includes microphone and earphone amplifiers, analog-to-digital (A/D) and digital-to-analog (D/A) converters, speech digital filtering, and a serial port.

The baseband processing portion of the device includes a 2-channel uplink path, a 2-channel downlink path, a serial port, and a parallel port. The uplink path performs Gaussian minimum shift keying (GMSK) modulation, D/A conversion, and has smoothing filters to provide the external RF circuit with I and Q baseband signals. The downlink path performs antialiasing, A/D conversion, and channel separation filtering of the baseband I and Q signals. The serial port allows baseband data exchange with the DSP, and the parallel port controls precise timing signals.

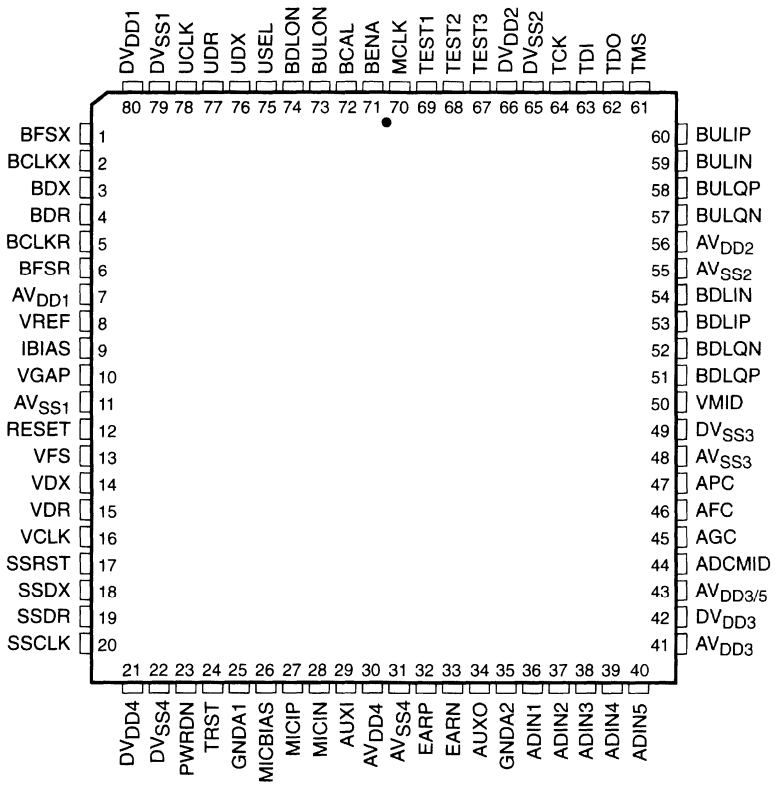
Auxiliary RF functions such as automatic frequency control (AFC), automatic gain control (AGC), power control, and analog monitoring are also implemented in the TCM4400. Internal functional blocks of the device can be separately and automatically powered down with GSM RF windows.

PRODUCT PREVIEW

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

80-Pin TQFP PACKAGE
(TOP VIEW)



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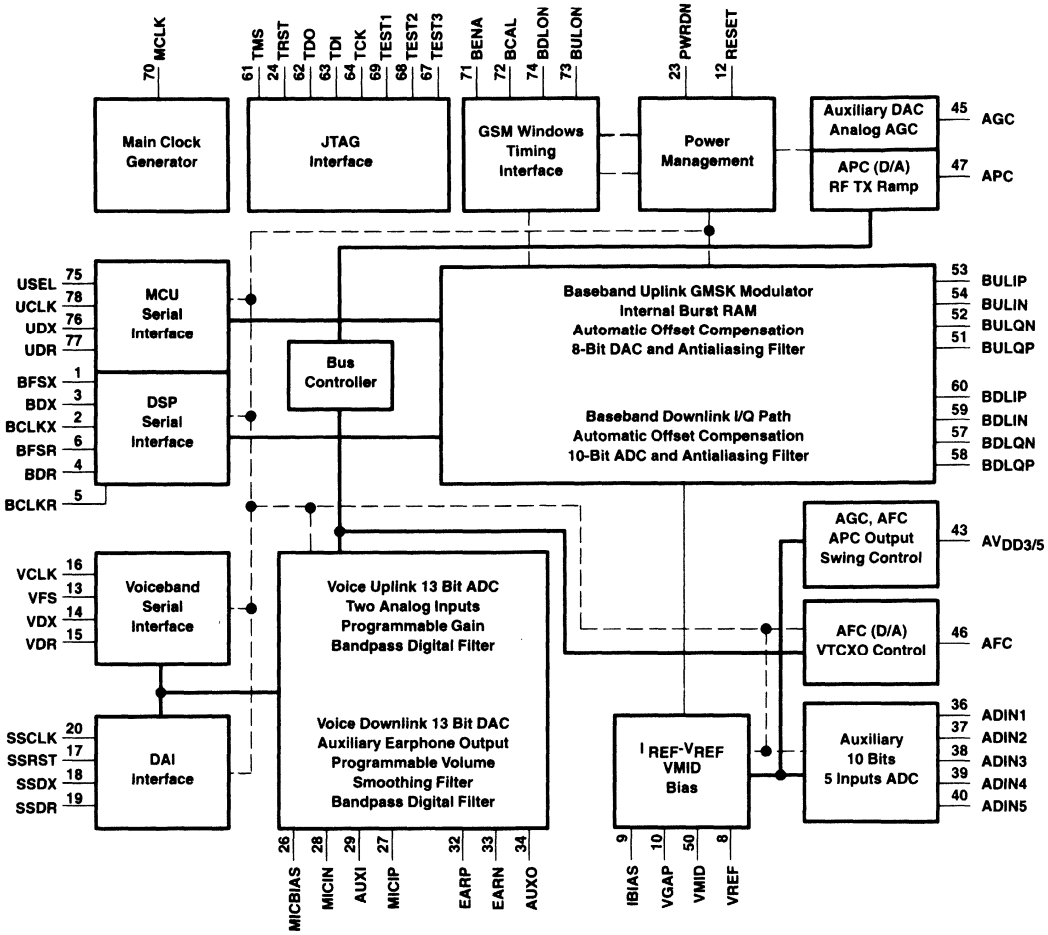
functional block diagram



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Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ADCMID	44	I/O	Reference voltage of auxiliary A/D converters; decoupling only (analog)
ADIN1	36	I	Auxiliary 10-bit ADC input 1 (analog)
ADIN2	37	I	Auxiliary 10-bit ADC input 2 (analog)
ADIN5	40	I	Auxiliary 10-bit ADC input 3 (analog)
ADIN4	39	I	Auxiliary 10-bit ADC input 4 (analog)
ADIN3	38	I	Auxiliary 10-bit ADC input 5 (analog)
AFC	46	O	Automatic frequency control DAC output (analog)
AGC	45	O	Automatic gain control DAC output (analog)
APC	47	O	Automatic power control DAC output (analog)
AUXI	29	I	Auxiliary (high-level) speech signal input (analog)
AUXO	34	O	Auxiliary downlink (voice codec) amplifier output — single-ended (analog)
AV_{DD1}	7		Analog positive power supply (bandgap, internal common-mode generator, bias current generator).
AV_{DD2}	56		Analog positive power supply (baseband CODEC)
AV_{DD3}	41		Analog positive power supply (auxiliary RF functions)
$AV_{DD3/5}$	43		Analog positive power supply (auxiliary RF functions) — can be in the 3-V to 5-V range
AV_{DD4}	30		Analog positive power supply (voice codec)
AV_{SS1}	11		Analog negative power supply (bandgap, internal common-mode generator, bias current generator).
AV_{SS2}	55		Analog negative power supply (baseband CODEC)
AV_{SS3}	48		Analog negative power supply (auxiliary RF functions)
AV_{SS4}	31		Analog negative power supply (voice codec)
BCAL	72	I	Baseband uplink or downlink offset calibration enable (timing interface)
BCLKR	5	I/O	DSP serial interface clock input — this clock signal is provided by the DSP or the TCM4400 (digital).
BCLKX	2	O	DSP serial interface clock output. The frequency is the same as MCLK (digital).
BDR	4	I	DSP serial interface serial data input (digital)
BDX	3	O	DSP serial interface serial data output (digital)
BENA	71	I	Burst transmit or receive enable (depends on status of BULON and BDLON) (digital)
BDLON	74	I	Power on of baseband downlink (timing interface)
BFSR	6	I	DSP serial interface receive frame synchronization input (digital)
BFSX	1	O	DSP serial interface transmit frame synchronization output (digital)
BDLIN	54	I	In-phase baseband input (–) — downlink path (analog)
BDLIP	53	I	In-phase baseband input (+) — downlink path (analog)
BDLQN	52	I	Quadrature baseband input (–) — downlink path (analog)
BDLQP	51	I	Quadrature baseband input (+) — downlink path (analog)
BULIN	59	O	In-phase baseband output (–) — uplink path (analog)
BULIP	60	O	In-phase baseband output (+) — uplink path (analog)
BULON	73	I	Serial clock input (serial interface) (digital)
BULQN	57	O	Quadrature baseband output (–) — uplink path (analog)
BULQP	58	O	Quadrature baseband output (+) — uplink path (analog)
DV_{DD1}	80		Digital positive power supply (baseband and timing serial interfaces)
DV_{DD2}	66		Digital positive power supply (baseband CODEC)
DV_{DD3}	42		Digital positive power supply (auxiliary RF functions)
DV_{DD4}	21		Digital positive power supply (voiceband codec and serial interface)
DV_{SS1}	79		Digital negative power supply (baseband and timing serial interfaces)

PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
DV_{SS2}	65		Digital negative power supply (baseband CODEC)
DV_{SS3}	49		Digital negative power supply (auxiliary RF functions)
DV_{SS4}	22		Digital negative power supply (voiceband codec and serial interface)
EARN	33	O	Earphone amplifier output (–) (analog)
EARP	32	O	Earphone amplifier output (+) (analog)
GNDA1	25		Analog signal ground for the microphone amplifier and auxiliary input
GNDA2	35		Signal return (ground) for AUXO output
IBIAS	9	I/O	Internal bias reference current adjust — adjust with external resistor (analog)
MCLK	70	I	Master system clock input (13 MHz) (digital)
MICBIAS	26	I	Microphone bias supply output — also used to decouple bias supply with external capacitor (analog)
MICIP	27	I	Microphone amplifier input (+) (analog)
MICIN	28	I	Microphone amplifier input (–) (analog)
PWRDN	23	I	Powerdown mode control input (digital)
RESET	12	I	Device global hardware reset — pull to ground to reset (digital)
SSCLK	20	O	DAI interface external 104 kHz clock output (digital)
SSDR	19	I	DAI interface data transfer input — connect to GSM-SS TDAI (digital)
SSDX	18	O	DAI interface data transfer output — connect to GSM-SS RDAI (digital)
SSRST	17	I	DAI interface reset input (digital)
TCK	64	I	Scan test clock (digital)
TDI	63	I	Scan path input (for testing purposes) (digital)
TDO	62	I	Scan path output (for testing purposes) (digital)
TEST1	69	I/O	Test I/O (digital)
TEST2	68	I/O	Test I/O (digital)
TEST3	67	O	Test output (digital)
TMS	61	I	JTAG test mode select (digital)
TRST	24	I	JTAG serial interface reset — pull to ground to reset (digital)
UCLK	78	I	MCU interface clock input (digital)
UDR	77	I	MCU interface data transfer input (digital)
UDX	76	O	MCU interface data transfer output (digital)
USEL	75	I	MCU serial interface select (digital)
VCLK	16	O	Voiceband serial interface clock output (digital)
VDR	15	I	Voiceband serial interface receive data input (digital)
VDX	14	O	Voiceband serial interface transmit data output (digital)
VFS	13	O	Voiceband serial interface transmit frame synchronization output (digital)
VGAP	10	I/O	Bandgap reference voltage — decouple with external capacitor (analog)
VMID	50	O	Midrail voltage output — serves as reference common-mode voltage for RF device when directly dc coupled (analog)
V_{REF}	8	I/O	Reference voltage — decouple with external capacitor (analog)

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, AV_{DD}, DV_{DD} (see Note 1) . . . . . −0.3 to 6 V
Maximum voltage on any input, V_I max . . . . . V_{DD} +0.3 V / V_{SS} −0.3 V
Storage temperature, T_{stg} . . . . . −65°C to 150°C
Maximum junction temperature, T_J . . . . . +150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage measurements with respect to GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage range (AV_{DD}, DV_{DD})	2.7		3.3	Vdc
Supply extended voltage range for RF blocks ($AV_{DD}3/5$)	2.7		5.25	Vdc
Operating temperature range	−25		+85	°C
Digital I/O voltage with respect to DV_{SS}	−0.3		DV_{DD} + 0.3	Vdc
Analog I/O voltage with respect to AV_{SS}	−0.3		AV_{DD} + 0.3	V
Difference between any AV_{DD} or DV_{DD}			0.3	V
Typical low-level output current with digital pad lower than 0.1 V (CMOS)	500			µA
Typical low-level output current with digital pad lower than 0.4 V (TTL)	2			µA
Typical high-level output current with digital pad higher than V_{DD}–0.1 V (CMOS)	–700			µA
Typical high-level output current with digital pad higher than V_{DD}–0.4 V (TTL)	−3			mA
Minimum high-level input voltage, V_{IH}	0.8			V
Maximum low level input voltage, V_{IL}			0.3	V
High impedance state output current (pullup)		15		µA
Load resistance	10			kΩ
Load capacitance			50	pF
Maximum external load capacitance		33		nF
Current capability at MICBIAS nominal audio level of 2.5 V		0 to 0.5		mA

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voltage references

REFERENCE	VOLTAGE	DEFINITION
VGAP	1.22 V	Band gap used for all other references
VREF	1.75 V	Voltage reference of GMSK internal ADC and DAC
VMID	$AV_{DD}2/2$	Common-mode reference for uplink/downlink GMSK
MICBIAS	2 V / 2.5 V	Microphone-driving voltage
ACDMID	1.75 V	Voltage reference of the auxiliary ADCs

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

baseband uplink path

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I and Q D/A converters resolution			8		bit
Dynamic range on each output	Centered on internal reference		V_{VREF}		Vpp
Differential output dynamic range	BULQP-BULQN or BULIP-BULIN		2 x V_{VREF}		Vpp
Output load resistance, differential		10			kΩ
Output load capacitance, differential		50			pF
Output common-mode voltage	Programmable by bit SELVMID		$V_{DD}/2$ or 1.35 ±0.1		V

dc accuracy – uplink path

PARAMETER	MIN	TYP	MAX	UNIT
Offset error before calibration		±50		mV
Offset error after calibration		±5		mV
Offset correction range		±100		mV

dynamic parameters – uplink path

PARAMETER		MIN	TYP	MAX	UNIT
Maximum output modulation spectrum	±400 kHz		−65		dB
	±600 kHz		−70		dB
	±800 kHz		−70		dB
Absolute gain relative to VREF	VREF		±1		dB

smoothing filters characteristics – uplink path

PARAMETER		MIN	TYP	MAX	UNIT
Group delay	0 Hz to 100 kHz		1.5		µs

I and Q channels gain and phase matching – uplink path

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gain matching between channels	0 Hz to 96 kHz			±0.15		dB
Phase matching between channels	0 Hz to 96 kHz			0.5°		
I and Q gain unbalance		Programmable		0		dB
				0.25		
				0.50		
				0.75		

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baseband uplink path global characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GMSK phase error	peak			6°		
	rms			1.5°		
Power supply rejection						dB
Supply current for uplink path	active			2		mA
	power-down	Maximum value		10		µA

timing requirements of baseband uplink path

programmable delays – uplink path (see Figure 1)

			MIN	NOM	MAX	UNIT†
t_{su1}	Setup time, BENA↑ before APC↑	Bits DELU of register BULRUDEL	0		15	1/4-bit
t_{h1}	Hold time, ramp-down from BENA low	Bits DELD of register BULRUDEL	0		15	1/4-bit
t_{t1}	Transition time, APC	Bit APCSPD = 0	0		64	1/16-bit
		Bit APCSPD = 1				1/8-bit

† Bit is relative to GSM bit = 1/270 kHz. Units can be a fractional part of the GSM bit as noted.

fixed delays – uplink path (see Figure 1)

			MIN	NOM	MAX	UNIT†
t_{su2}	Setup time, BULON↑ to BCAL↑		15			µs
t_{w1}	Pulse duration, BCAL high				132	µs
t_{su3}	Setup time, BCAL low before BENA↑		0			µs
t_{w2}	Pulse duration, BENA high	N effective duration of burst Controlled by BENA		N–32		1/4-bit
t_{h2}	Hold time, modulation low after BENA low			32		bit
t_{h3}	Hold time, BULON↓ after APC low		1			bit
	Input-to-output modulator delay	(Digital delay of modulator)		1.5		bit

† Bit is relative to GSM bit = 1/270 kHz. Units can be a fractional part of the GSM bit as noted.

timing requirements of baseband downlink path (see Figure 2)

			MIN	NOM	MAX	UNIT†
t_{su4}	Setup time, BDLON↑ to BCAL↑		5			µs
t_{w3}	Pulse duraton, BCAL				60	µs
t_{su5}	Setup time BCAL low before BENA↑		0			µs
t_{w4}	Pulse duration, BENA high	N effective duration of burst controlled by BENA		N		1/4-bit
t_{su6}	Setup time, BENA↑ before DATAOUT VALID				28	µs
t_{h4}	Hold time, DATAOUT VALID after BENA↓				3.7	µs
t_{h5}	Hold time, BDLON low after BENA low		0			µs

† Bit is relative to GSM bit = 1/270 kHz. Units can be a fractional part of the GSM bit as noted.

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baseband downlink path

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic range on each input	Centered on Internal Reference		V_{VREF}		Vpp
Differential input dynamic range	BDLQP–BDLQN or DLIP–DLIN		$2V_{VREF}$		Vpp
Input resistance at BDLQP–BDLQN or BDLIP–BDLIN			200		kΩ
Input capacitance at BDLQP–BDLQN or BDLIP–BDLIN					pF
Common-mode input voltage		–10%	$V_{DD}/2$	+10%	V
Range of digital output data	Maximum digital code value		±21060		

dc accuracy – downlink path

PARAMETER	MIN	TYP	MAX	UNIT
Offset error before calibration		60		LSB
Offset error after calibration		±1		LSB
Offset correction range		full scale		

dynamic parameters – downlink path

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic range			66		dB
Signal to noise plus distortion, whole downlink path			62		dB
Absolute gain relative to V_{VREF}			±1		dB

channel characteristics

frequency response – downlink path

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency response of the total chain with values referenced to 67.708 kHz	0 Hz		–0.2		0.2	dB
	67.5 kHz		–0.2		0.2	dB
	96 kHz		–4		0.3	dB
	135 kHz				–40	dB
	200 kHz				–40	dB
	400 kHz				–40	dB

group delay – downlink path

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Group delay	0 Hz to 100 kHz			28		µs

I and Q channels matching – downlink path

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gain matching between channels	0 Hz to 96 kHz			±0.5		dB
Delay matching between channels	0 Hz to 96 kHz			5		ns

baseband downlink path global characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power supply rejection, 0 Hz –100 kHz band						dB
Supply current for downlink path	active			10		mA
	power-down			2		µA

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automatic power control

power D/A converter

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Integral nonlinearity	Best fitting of linearity with the shaper at full scale maximum		+/–2		LSB
Differential nonlinearity			+/–1		LSB
Settling time			10		µs

shaper DAC

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Integral nonlinearity	Best fitting of linearity		+/–1		LSB
Settling time			1		µs
Minimum voltage swing (AV_{DD3}/5 = 3 V)	APCSWG_config bit = 0		2		V
Minimum voltage swing (AV_{DD3}/5 = 5 V)	APCSWG_config bit = 1		4		V
Load resistance			10		KΩ
Load capacitance			50		pF
Power consumption active (AV_{DD3}/5 = 3 V)			2.1		mW
Power consumption active (AV_{DD3}/5 = 5 V)			7.1		mW
Maximum power consumption, power-down, 3-V and 5-V			0.01		µW

auxillary ADC

monitoring

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Integral nonlinearity (best fitting)		Input signal range < 0.95 V_{VREF}			±4	LSB
Differential nonlinearity		Input signal range < 0.95 V_{VREF}			±2	LSB
Integral nonlinearity (best fitting)		Input signal range > 0.95 V_{VREF}				LSB
Differential nonlinearity		Input signal range > 0.95 V_{VREF}				LSB
Full-scale accuracy				5		LSB
Conversion time				10		µs
Input range				0 to V_{VREF}		V
Input leakage current				10		µA
Input capacitance				25		pF
Supply current for ADC	active			500		µA
	power-down			<1		µA

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AGC characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Integral nonlinearity	Best fitting line		±2		LSB
Differential nonlinearity			±2		LSB
Settling time	From AUXAGC load		100		µs
Output swing ($AV_{DD3/5}$ = 3 V ± 10%)		2			V
Offset voltage with code 000 (3 V ± 10%)			0.2		V
Output swing ($AV_{DD3/5}$ = 5 V ± 5%)		4			V
Offset voltage with code 000 (5 V ± 5%)			0.4		V

AFC characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Sampling frequency, f_S			2		MHz
			1		MHz
			0.5		MHz
			0.25		MHz
Minimum resolution	Depending on quartz characteristics		13		bit
Integral nonlinearity from 0 to 80% output range	Best fitting line		±0.5		LSB
Differential nonlinearity from 0 to 80% output range			±0.5		LSB
Settling time			1		µs
DC power-supply sensitivity	Over power supply range		TBD		%
Internal output resistance	Programmable value		25 or 50		kΩ
Minimum voltage swing (AV_{DD} = 3 V)	AFCSWG_config bit = 0		2		V
Minimum voltage swing (AV_{DD} = 5 V)	AFCSWG_config bit = 1		4		V
Power consumption when device is active (typical)	f_S = 2 MHz (V_{DD} = 3 V)		0.7		mW
	f_S = 1 MHz		0.6		mW
	f_S = 0.5 MHz		0.54		mW
	f_S = 0.25 MHz				mW

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voice uplink path

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum input range (MICP – MICN)		Inputs 3 dBm0 (maximum digital sample amplitude)		32.5		mVrms
Nominal reference level (MICP – MICN)		from maximum value		–10		dBm0
Input resistance (MICP – MICN)				100		kΩ
DC level at MICBIAS		+/– 10% precision value		2 or 2.5		V
Maximum input range at AUXI				320		mVrms
Nominal reference level at AUXI		From maximum value		–10		dBm0
Minimum input resistance at AUXI			100	300		kΩ
PGA gain range		With 1-dB steps	–7.4		16.6	dB
Frequency response	100 Hz	Value obtained at nominal level		–37.4		dB
	150 Hz			–25.9		dB
	200 Hz			–16.5		dB
	300 Hz			–1.46		dB
	1000 Hz	Reference point is 1000 Hz		0		dB
	2000 Hz			–0.58		dB
	3000 Hz			–0.77		dB
	3400 Hz			–1		dB
	3600 Hz			–12.4		dB
	3800 Hz			–23.3		dB
	4000 Hz			–35		dB
	>4600 Hz			>–52		dB

psophometric SNR vs signal level uplink path

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal level	3 dBm0			35		dB
	0 dBm0			40		dB
	–5 dBm0			42		dB
	–10 dBm0			45		dB
	–20 dBm0			42		dB
	–30 dBm0			40		dB
	–40 dBm0			30		dB
	–45 dBm0			25		dB
Gain tracking error		Over the range +3 dBm0 to – 45 dBm0 at 1 kHz with reference –10 dBm0				dB
Maximum idle channel noise	300 Hz –3 kHz			–72		dBm0
Maximum group delay distortion	300 Hz – 3 kHz					ms
Crosstalk with the downlink path		Downlink path loaded with 30 Ω		–66		dB

global characteristicsfor voice uplink path

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power supply rejection, 0 Hz –100 kHz band						dB
Supply current for voice uplink	active			3		mA
	power-down			2		µA

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voice downlink path

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum output swing (EARP – EARN)	with 5% distortion and with 150 Ω			3.92		Vpp
	with 5% distortion and with 30 Ω			1.5		Vpp
Minimum output resistive load		Depending on the output swing	150	30		Ω
Maximum output capacitive load				100		pF
Earpiece mute switch attenuation				40		dB
Programmable volume control		Maximum volume control		0		dB
				–6		dB
		Typical audio level		–12		dB
				–18		dB
				–24		dB
		Mute		<–40		dB
Maximum output swing (AUXO), 5% distortion, maximum		Load = 1 kΩ		1.96		Vpeak
Minimum output resistive load		ac coupled		1		kΩ
Maximum output capacitive load				100		pF
Total signal to noise ratio (AUXO)		Maximum at 1 kHz over 300 Hz – 3 kHz			2%	
Idle noise (AUXO)		300 Hz – 3 kHz			–77	dB
Audio delay (AUXO)				<1		ms
Mute switch attenuation (AUXO)				<–40		dB
Frequency response	100 Hz			–5.8		dB
	150 Hz			–3.6		dB
	200 Hz			–2.5		dB
	300 Hz			–1.4		dB
	1000 Hz	Reference point		0		dB
	2000 Hz			–0.6		dB
	3000 Hz			–0.15		dB
	3400 Hz			–0.35		dB
	3600 Hz			–9.0		dB
	3800 Hz			–21.0		dB
	4000 Hz			–32.0		dB
	>4600 Hz			–60.0		dB
Maximum distortion at 1 kHz with 30 Ω		V_{IN} = 0.1 Vrms		1%		
		V_{IN} = 1 Vrms		2%		
		V_{IN} = 1.5 Vrms		5%		
Programmable gain amplifier		By 1-dB steps	–6	6		dB
Gain tracking error		Over the range +3 dBm0 to –30 dBm0 at 1 kHz with reference –10 dBm0		±0.25		dB
		Over the range –31 dBm0 to –45 dBm0 at 1 kHz with reference –10 dBm0		±0.50		dB
Idle channel noise, 0 Hz –30 KHz				–71		dBm
Power supply rejection, 0 Hz –100 kHz		In the band				dB
Supply current for voice downlink	active			7.4		mA
	power-down			2		µA
Side-tone gain range		With 3 dB steps	–17		1	dB
Side-tone mute				–60		dB

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psophometric SNR vs signal level downlink path

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal level	–45 dBm0			25		dB
	–40 dBm0			30		dB
	–30 dBm0			40		dB
	–20 dBm0			42		dB
	–10 dBm0			45		dB
	–3 dBm0			42		dB
	0 dBm0			35		dB

supply current

PARAMETER		MIN	NOM	MAX	UNIT
Deep power down	13 MHz clock applied; PWRDN active; Band-gap voltage reference off				µA
Power down with AFC	AFC programmed with internal 50 kΩ and 1 MHz clock		1		mA
AFC + GMSK – Rx			3		mA
Audio + GMSK – Tx + APC + AFC	transmit burst		13		mA
Audio + GMSK – Rx + AFC	receive burst		21		mA

voice timing requirements (see Figure 5)

PARAMETER		MIN	NOM	MAX	UNIT
VCLK	VCLK signal frequency		520		kHz
VCLK	VCLK duty cycle (±10%)		50%		
t_{h6}	Hold time, VFS↓ after VCLK low		100		ns
t_{h7}	Hold time, VDR↓ after VCLK low		100		ns
t_{h8}	Hold time, VDX high after VCLK high		100		ns
t_{su7}	Setup time, VFS↑ before VCLK low		100		ns
t_{su8}	Setup time, VDX↓ before VCLK low		100		ns
t_{su9}	Setup time, VDR high before VCLK low		100		ns

MCU serial interface timing requirements (see Figure 3)

PARAMETER		MIN	NOM	MAX	UNIT
t_{su10}	Setup time, UCLK↓ before USEL↓		20		ns
t_{v1}	Hold time, UDX valid after USEL↓		20		ns
t_{v2}	Hold time, UDX valid after UCLK↑		20		ns
t_{h9}	Sequential transfer delay between 16-bit word acquisition t_W pulsduration, USEL high			3000	ns
t_{h10}	Hold time, UCLK↑ after USEL↓		20		ns
t_{h11}	Hold time, UCLK↑ after USEL↑		20		ns
t_{su11}	Setup time, data valid before UCLK↓		20		ns
t_{h12}	Hold time, data valid after UCLK↓		20		ns
$t_c$max	Cycle time, ULCK	77			ns

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master clock timing requirements

PARAMETER	MIN	NOM	MAX	UNIT
Master clock signal frequency		13		MHz
Master clock duty cycle	40%		60%	
Maximum peak-to-peak amplitude			1.3	V
Minimum peak-to-peak amplitude	0.5			V
Common-mode input voltage	V_{SS} +0.5		V_{DD} –0.5	V

PARAMETER MEASUREMENT INFORMATION

uplink timing considerations

Figure 1 shows the timing diagram for the uplink operation.

Timing for power-up, offset calibration, data transmission, and power ramp-up are driven by control bits applied to BULON (base uplink on), BCAL (calibration) and BENA (enable). The burst content including guard bits, tail bits, and data bits is sent by the DSP by way of the DSP interface and then stored by the TCM4400 in a burst buffer. Transmission start is indicated by the control bit ENA when the BULON is active. The transmission, sequencing, and power ramp-up are then controlled by an on-chip burst sequencer with a one-quarter-bit timing accuracy. For a detailed description of the baseband in length path, see the functional description of the baseband uplink path in the Principles of Operation section.

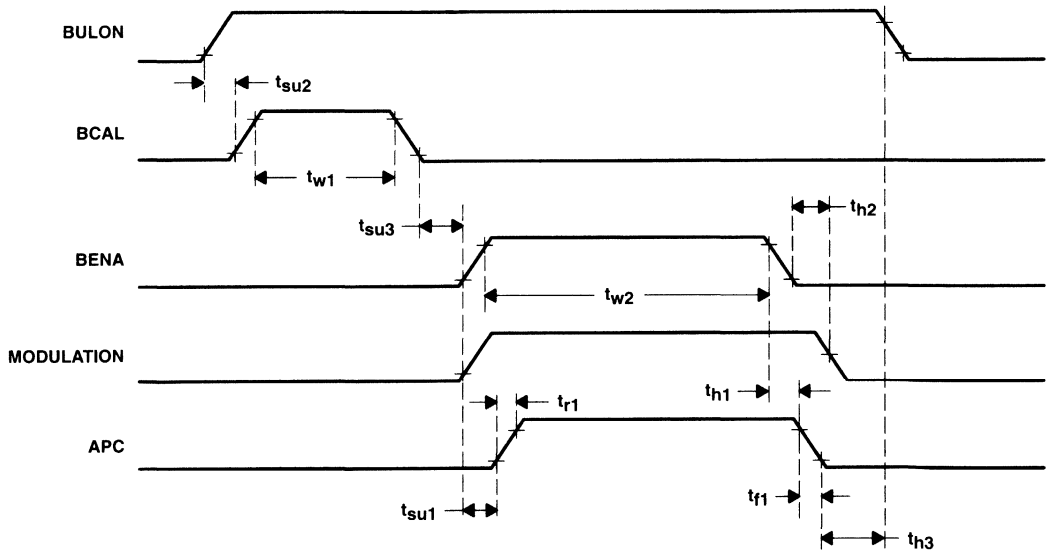

Figure 1. Uplink Timing Diagram

PRODUCT PREVIEW

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downlink timing considerations

Figure 2 shows the timing diagram for downlink operation.

Timing control of the baseband downlink path is controlled by bits DLON (downlink on), BCAL (calibration) and BENA (enable) when BDLON is active (see the topic, timing control and interface). BDLON controls the power up of the baseband downlink path, BCAL controls the start and duration of the autocalibration sequence, and BENA controls the beginning and the duration of data transmission to the DSP, using the DSP serial interface.

The power-down sequence is controlled with two bits, the first bit (BBDLW of PWDNWIN register) determines whether the baseband downlink path can be powered down with external GSM receive window activation (BDLON); the second bit (BBDLPD of PWDNWIN register) controls the activation of the baseband downlink path. See the topic, power-down functional description, for more details about power-down control.

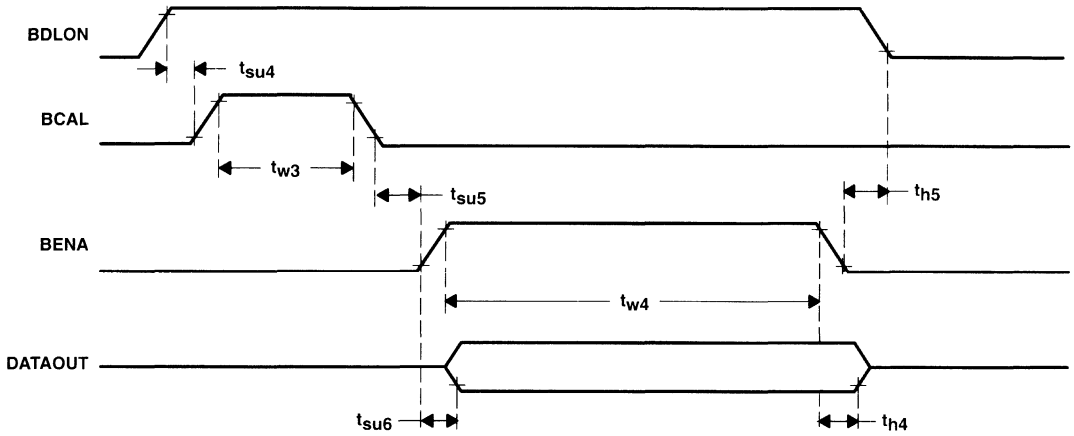

Figure 2. Downlink Timing Sequence

PARAMETER MEASUREMENT INFORMATION

microcontroller serial interface timing considerations

Figure 3 shows the timing diagram for the microcontroller serial interface.

The microcontroller serial interface is designed to be compliant with 8-bit standard synchronous serial ports. The microcontroller operates on 16-bit words; this interface consists of four pins.

UCLK: A clock provided by the microcontroller to the GSM baseband and voice A/D and D/A conversion.

UDR: An input terminal of the GSM baseband and voice A/D and D/A components intended for reception of data.

UDX: An output terminal of the GSM baseband and voice A/D and D/A components intended for transmission of data.

USEL: An input terminal of the GSM baseband and voice A/D and D/A components intended for activation of the serial interface.

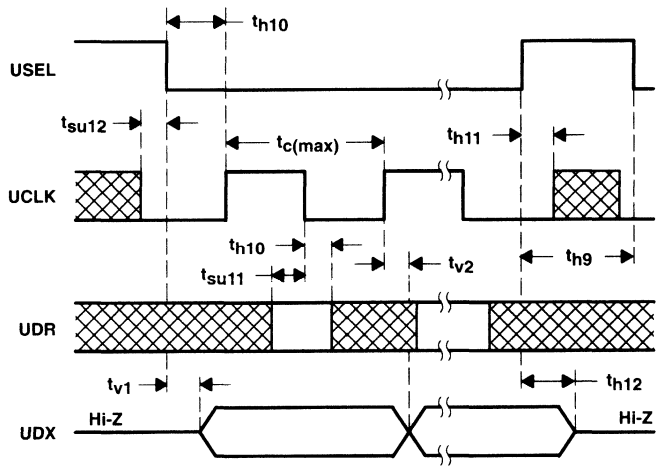

Figure 3. Microcontroller Serial Interface Timing Waveforms

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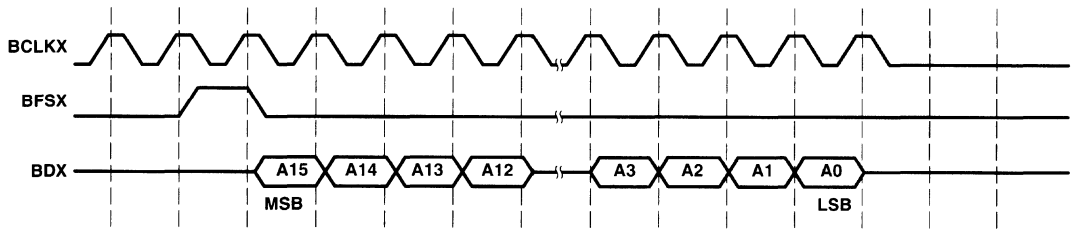
DSP Serial port timing considerations

Figure 4 shows the timing diagram for DSP serial port operation.

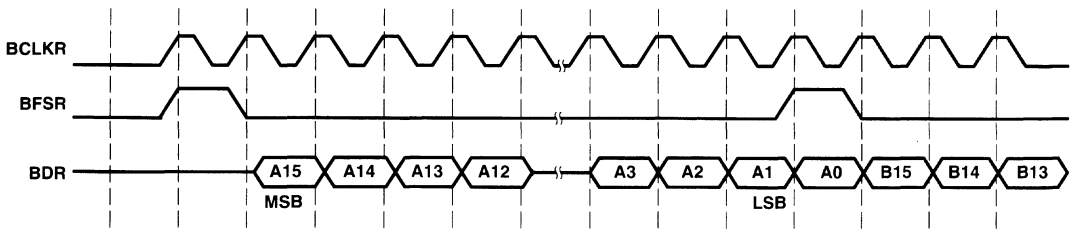
Six pins are used for the serial port interface, see Figure 14. The terminal BCLKR is an I/O port for the serial clock used to control the reception of the data BDR. At reset BCLKR is configured as an output and the clock frequency is set to MCLK/3 (4.333 MHz with MCLK = 13 MHz), the clock signal is running permanently. The port BCLKR can be reconfigured as an input by programming an internal register. In this case BCLKR is provided by the DSP and can run in burst mode to reduce power consumption. The receive frame synchronization (BFSR) is used to identify the beginning of a data packet transfer on port BDR.

The transmitted serial data (BDX) is the serial data input; the transmit frame synchronization (BFSX) is used to initiate the transmission of data. The transmit clock (BCLKX) is provided by the GSM baseband and voice A/D and D/A converters with a frequency of MCLK. The downlink data bus (BFSX, BCLKX, BDX) can be driven to VSS or placed in high-impedance when no data is to be transferred to the DSP. The bit BCLKDIR of the register BCTLREG controls the direction of the BCLKR clock.

As with the voice serial interface, an extra clock cycle must be generated since the last 16-bit word received on the DSP serial interface is latched on the next two falling BCLKR edge, following the least significant bit (LSB). As for the voice serial interface, one extra clock period is generated on the BCLKX before the first synchronization BFSX of downlink data sequence.



(a) Burst-Mode Serial Port Transmit Operation



(b) Burst-Mode Serial Port Receive Operation

Figure 4. DSP Serial Port Timings

PARAMETER MEASUREMENT INFORMATION

voiceband serial interface timing considerations

Figure 5 shows the timing diagram for both transmit and receive voiceband serial interface operation.

The signal VCLK is the output serial clock used to control the transmission or reception of the data (see Figure 9). The transmitted serial data (VDX) is the serial data output; the frame synchronization (VFS) is used to initiate the transfer of transmit and receive data. The received data (VDR) is the serial data input.

Each serial port includes four registers that include the data transmit register (DXR), the data receive register (DRR), the transmit shift register (XSR) and the receive shift register (RSR).

The voice serial interface has the same structure and timing diagram as the serial interface; one extra cycle is generated before VFS and two extra cycles are generated after the LSB.

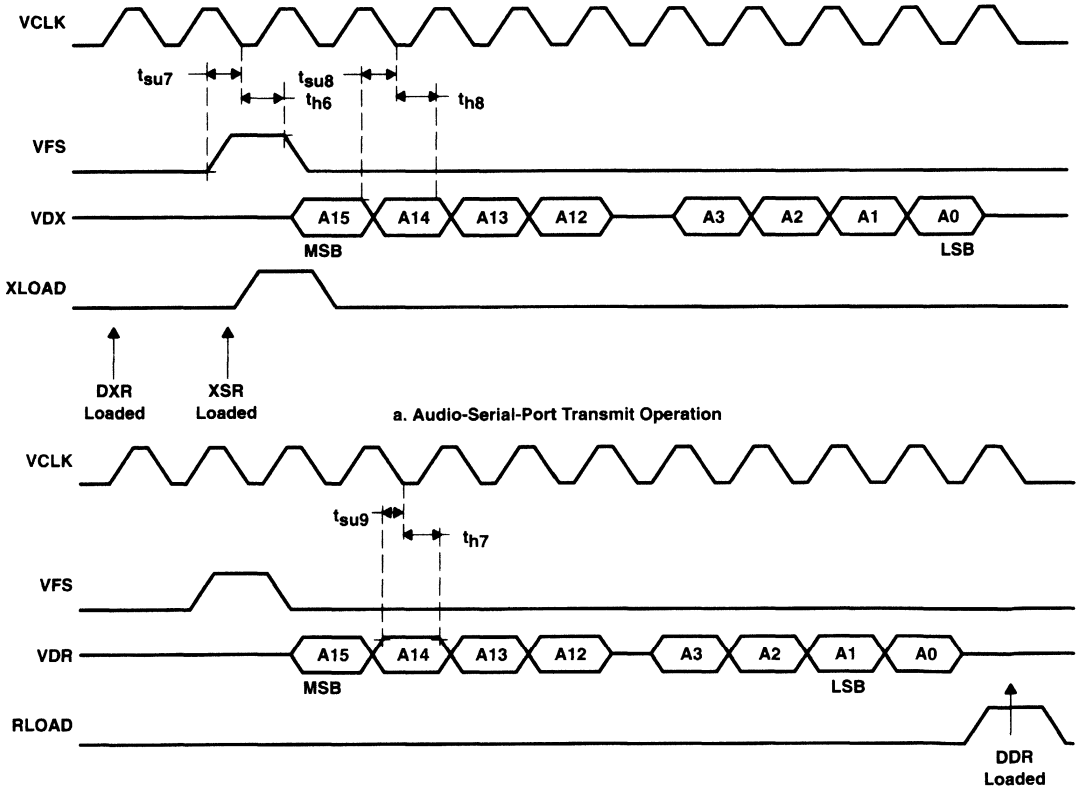


Figure 5. Voiceband Serial Interface Timing Waveforms

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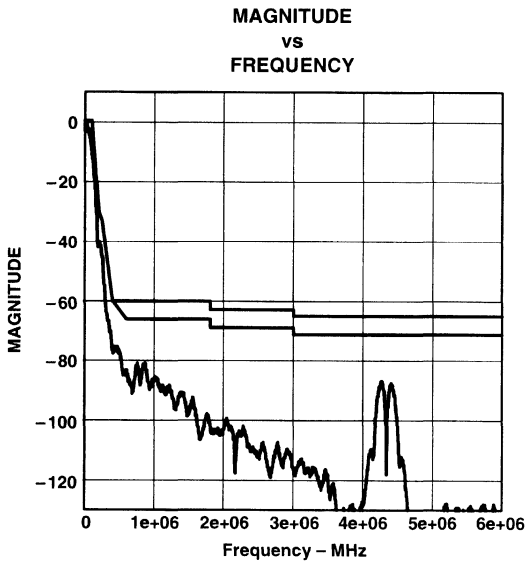
PRINCIPLE OF OPERATION

baseband uplink path

Instead of the traditional transmit and receive terms, which can be confusing when describing a cellular telephone 2-way communication, the terms uplink meaning from a user device to a remote station and downlink meaning from a remote station, whether earthbound or satellite, are used to indicate the signal-flow direction.

The modulator circuit in the baseband uplink path performs the Gaussian minimum shift keying (GMSK) in accordance with the GSM specification 5.04. The data to be modulated flows from the DSP through the serial interface, it is differentially encoded, and it is applied to the input of the GMSK modulator. The GMSK modulator is implemented with digital logic and a sin/cos look-up table in ROM, and it generates the I and Q components (words) with an interpolation ratio of 16.

These digital I and Q words are sampled at a 4.33 MHz rate and applied to the inputs of a pair of high-speed 8-bit DACs. The analog outputs are then processed by second-order Bessel filters to reduce image frequencies due to sampling and to obtain a spectrum consistent with GSM specification 05.05 (see Figure 6).



NOTE A: Conformance with GSM Rec 05.05: simulated spectrum of an infinite modulation of random data with a Blackman Harris analysis window.

Figure 6. Typical GSM Modulation Spectrum

Full-differential buffered signals are available at ULIP, ULIN, ULQP, and ULQN. These signals are suitable for use in the RF circuit for generating a phase-modulated signal of the form:

$$s(t) = A \cos(2 \pi fc\, t + \text{Phi}(t, \text{alpha}))$$

where fc is the RF carrier frequency and Phi (t, alpha) is the phase component generated by the GMSK modulator from the differential encoded data.

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baseband uplink path (continued)

Timing for power up, offset calibration, data transmission, and power ramp-up are driven by control bits applied to BULON (base uplink on), BCAL (calibration) and BENA (enable) (see Figure 1). The entire content of a burst, including guard bits, tail bits, and data bits is sent by the DSP using the DSP interface and then stored by the TCM4400 in a burst buffer. Transmission start is indicated by the control bit ENA when the BULON is active. The transmission, sequencing, and power ramp-up are then controlled by an on-chip burst sequencer having a one-quarter-bit timing accuracy (see Figure 7).

The burst length is determined by the time during which the BENA signal is active. Effective burst length is equal to the duration of BENA + 32 one-quarter bits. The tail of the burst is controlled internally, which means that the modulation is maintained for 32 one-quarter bits after BENA turns off to generate the ramp-down sequence and complete modulation.

For each burst, the power control level can be controlled by writing the power level value using the serial interfaces, into the power register of the auxiliary RF power control circuitry. The power ramp-up and ramp-down sequences are controlled by the burst sequencer while the shape of the power control is generated internally by dedicated circuitry, which drives the power control 5-bit and 8-bit D/A converters.

To minimize phase error, the I and Q channel dc-offset can be minimized using offset calibration. Each channel includes an offset register in which a value corresponding to the required dc offset is stored, controlling the dc offset of the I channel and Q channel D/A converters. This value is set by a calibration sequence. Starting and stopping the calibration sequence is controlled by the control bit BCAL using the timing interface when BULON is active. During the calibration sequence, the digital value of I and Q is forced to zero so that only the offset register value drives the D/A converters and a low-offset comparator senses the dc level at the BULIP/BULIN and BULQP/BULQN outputs and modifies the content of the offset registers to minimize the dc offset (see Figure 7).

The power-down function is controlled with two bits. The first bit (BBULW of the PWDNRG1 register), determines whether the baseband uplink path can be powered down with external GSM transmit window activation (BULON). The second bit (BBULPD of the PWDNWIN register) controls the activation of the baseband uplink path. See the topic, powerdown functional description, for more details about power-down control.

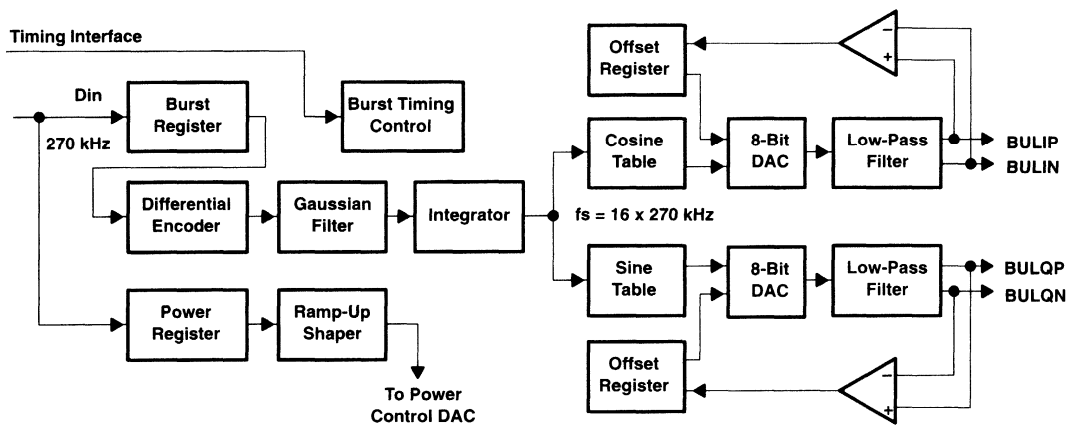

Figure 7. Functional Structure Of The Baseband Uplink Path

PRINCIPLES OF OPERATION

baseband downlink path

The baseband downlink path includes two identical circuits for processing the baseband I and Q components generated by the RF circuits. The first stage of the downlink path is a continuous-time second-order antialiasing filter (see Figure 8) that prevents aliasing due to sampling in the A/D converter. This filter also serves as an adaptation stage (input impedance and common-mode level) between external world and on-chip circuitry.

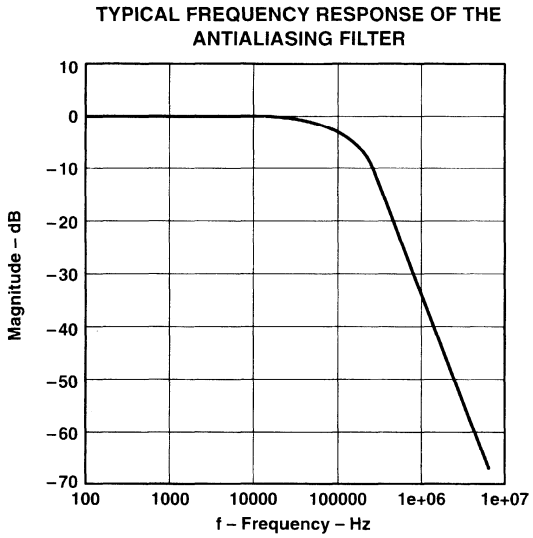

Figure 8. Antialiasing Filter

The antialiasing filter is followed by a third-order sigma-delta modulator that performs A/D conversion at a sampling rate of 6.5 MHz. The A/D converter provides 3-bit words that are fed to a digital filter (see Figure 9) that performs the decimation by a ratio of 24 to lower the sampling rate down to 270.8 KHz and the channel separation by providing enough rejection of the adjacent channels to allow the demodulation performances required by the GSM specification. Figure 10 shows the frequency response curve for the downlink digital filter and Figure 11 shows the in-band response curve for the same digital filter.

The baseband downlink path includes an offset register in which the value representing the channel dc offset is stored; this value is subtracted from the output of the digital filter before transmitting the digital samples to the DSP using the serial interface. Upon reset, the offset register is loaded with 0 and updated with the BCAL calibrating signal (see Figure 2).

The content of the offset register results from a calibration sequence. The input BDLIP is shorted with the input BDLIN, and the input BDLQP is shorted with the input BDLQN. The digital outputs are evaluated and the values are stored in the corresponding offset registers in accordance with the dc offset of the GSM baseband and voice A/D and D/A downlink path. When the external autocalibration sequence is selected, the inputs BDLIP and BDLIN and the inputs BDLQP and BDLQN remain connected to the external circuitry. The digital outputs are evaluated and the values stored into the corresponding offset registers take in to account the dc offset of the external circuitry.

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baseband downlink path (continued)

Timing control of the baseband downlink path is controlled by bits DLON (downlink on), BCAL (calibration) and BENA (enable) when BDLON is active (see topic, timing control and interface). BDLON controls the power up of the baseband downlink path, BCAL controls the start and duration of the autocalibration sequence, and BENA controls the beginning and the duration of data transmission to the DSP by using the DSP serial interface.

The power-down sequence is controlled with two bits, the first bit (BBDLW of PWDNWIN register) determines whether the baseband downlink path can be powered down with external GSM receive window activation (BDLON); the second bit, BBDLPD of register PWDNWIN, controls the activation of the baseband downlink path. See the topic, power-down functional description, for more details about power-down control.

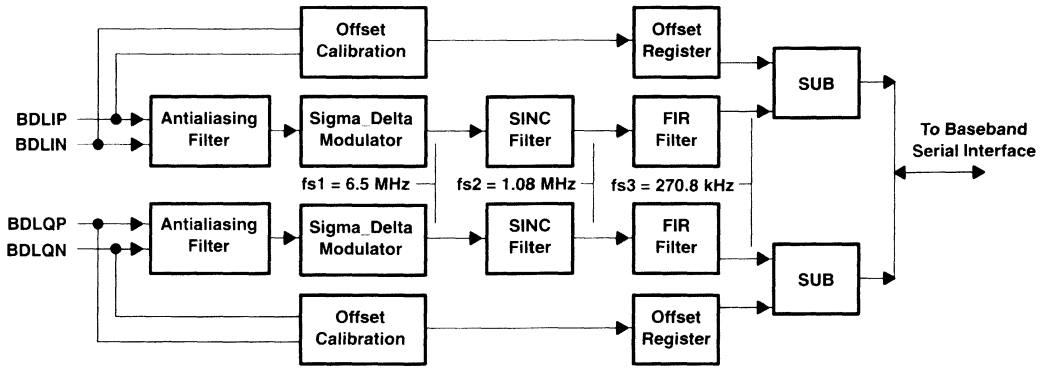

Figure 9. Functional Structure of the Baseband Downlink Path

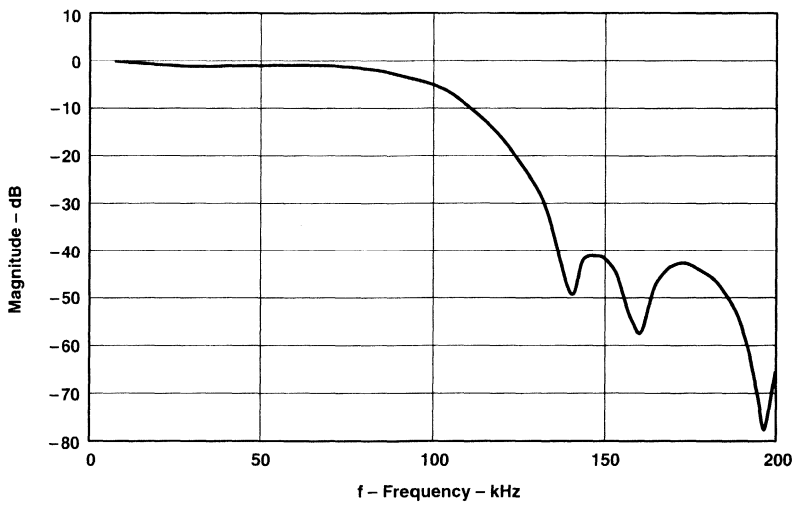

Figure 10. Downlink Digital Filter Frequency Response

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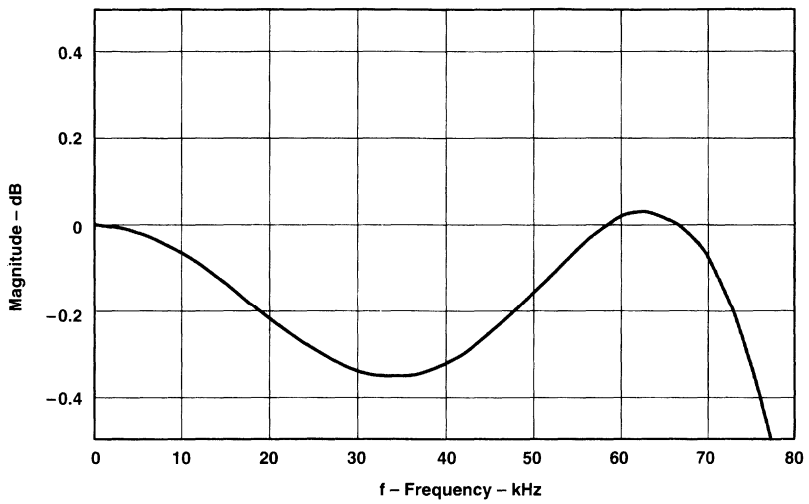

Figure 11. Downlink Digital Filter In-band Response

auxiliary RF functions

The auxiliary RF functions include the following:

- Automatic frequency control
- Automatic gain control
- RF power control
- Monitoring

Each of these functions is discussed in the following paragraphs.

automatic frequency control (AFC)

The automatic frequency control function consists in a DAC converter optimized for high resolution dc conversion. The AFC digital interface includes two registers that can be written using the serial interfaces. The content of these registers control a 13-bit DAC whose purpose is to correct frequency shifts of the oscillator maintaining the master clock frequency in a 0.1 ppm range.

To optimize the AFC function depends on the type of oscillator used and whether its sampling frequency is programmable. This means that the lower the selected frequency the lower the resolution and power consumption. Using a high-quality resonance oscillator filter permits the AFC circuit to operate at low frequency. Thus, a low-cost oscillator permits operation at a higher internal frequency to ensure 13-bit resolution.

The AFC value is programmed with registers AUXAFC1 and AUXAFC2. The internal resistance and output voltage swing selection is controlled with bit AFZ of AUXCTL2 register. Power down is controlled with two bits: the first bit, AFCPN of AUXCTL1 register, determines whether the AFC can be powered down from the external PWRDN terminal; the second bit, AFCPD of AUXCTL1 register, controls the activation of the the AFC function. See the topic, power-down functional description for more details about power-down control.

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automatic frequency control (continued)

The auxiliary analog functions of the GSM baseband A/D and D/A conversions are independently powered from the $AV_{DD3/5}$ external terminal. The AFC output voltage swing is programmable to provide the largest possible voltage range. This configuration is programmed with bit AFCZ of AUXCTRL2 register.

auxiliary analog converter (automatic gain control (AGC))

The auxiliary analog converter control function includes a register which can be written to using the serial interfaces and a 10-bit D/A converter that provides a control signal to set the gain of the RF section receive amplifier. The 10-bit D/A converter is accessed through the internal register AUXAGC.

Power down is controlled with two bits, the first bit (AAGCW of AUXCTL2 register) determines whether the AAGC can be powered down with the external GSM receive window activation (BDLON), the second bit (AGCPD of AUXCTL2 register) controls the activation of AGC function. See the topic, power-down functional description for more details about power-down control.

The auxiliary analog functions of the GSM baseband A/D and D/A conversions are independently powered from the $AV_{DD3/5}$ external terminal. The AGC output-voltage swing is programmable to provide the largest possible voltage range. This configuration is programmed with bit AGCSWG of AUXCTL2 register.

RF power control

The RF power control section includes a register that is written to using the serial interfaces. The content of this register is processed using an 8-bit D/A converter and determines the gain of the RF section power amplifier.

The reference of the 8-bit D/A converter (accessed by register AUXAPC) is provided by the ramp-up-shaper D/A converter which is a 5-bit D/A converter controlled by the APCRAM registers located in random access memory (RAM). This area of RAM contains sixty-four 10-bit words which are read from address 0 through address 62 during the ramp-up sequence and from 63 through 1 during the ramp-down sequence at a rate of 4 MHz when bit APCSPD is at zero or at a rate of 2 MHz when bit APCSPD is at 1. The ramp-up parameters are obtained from the five least significant bits of the RAM words. The ramp-down parameters are obtained from the most, significant bits of the RAM words. Content of address 0 must be identical with the content of address 1. Content of address 62 must be identical with content of address 63.

This RAM is loaded once and its content determines the shape of the ramp-up and ramp-down control signal, which means these control signals can be adapted to the response of the power amplifier used in the RF section. The shape and timing of ramp-up and ramp-down waveforms are independent.

Timing of the ramp-up and ramp-down sequences is controlled internally; however, programming of the delay register allows adjusting the power-control start time in a 4-bit range in 1/4-bit steps. The contents of the delay register are referenced to the BENA signal, which determines the beginning of the burst-signal modulation. This feature allows adjusting the timing of the control signal versus the I and Q components within 1/4-bit accuracy as defined in the specification GSM 05.05.

When APC is in power-down mode, the analog output is driven to V_{SS}. During inactivity periods, the APC output is switched to V_{SS} to give low-current consumption to the power amplifier (drain cutoff current of the RF amplifier); during activity periods, the binary value 00000 of the pulse shaper locks the APC driver.

Power down is controlled with two bits, the first bit (APCW of AUXCTL2 register) determines whether the APC can be powered down by activating external GSM transmit window activation (BULON); the second bit (APCPD of AUXCTL2 register) controls the activation of APC function. See the topic, power-down functional description, for more details about power-down control. The auxiliary analog functions of the GSM baseband A/D and D/A conversions are independently powered from the $AV_{DD3/5}$ terminal. The APC output-voltage swing is programmable to provide the largest voltage range. This configuration is programmed with bit APCSWG of the AUXCTRL2 register.

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monitoring

The monitoring section includes a 10-bit A/D converter and one result-register which allows monitoring of five external analog values such as the temperature and the battery voltage. The selection of the input and reading of the control registers is done using the serial interfaces.

The selection of the input channel is done with the bits ADCCH0 – ADCCH2 of the AUXCTL1 register; the data is read from the AUXADC register. Power down is controlled with two bits, the first bit (ADCPN of AUXCTL1 register) determines whether the A/D converter can be powered down from the external PWRDN terminal; the second bit (ADCPD of AUXCTL1 register) controls the activation of the A/D conversion function. See the topic, power down functional description, for more details about power-down control.

Conversion is started with a write access to the AUXCTL1 register. During the conversion, the ADCEOC bit of BSTATUS register stays at 1 and resets to 0 when the converted data is loaded in to the AUXADC register. This way the power consumption of the main parts of the converter is limited to the useful part of the conversion time.

voice codec

The voice coder/decoder (codec) circuitry processes analog audio components in the uplink path and applies this signal to the voice signal interface for eventual baseband modulation. In the downlink path, the codec circuitry changes voice-component data received from the voice serial interface into analog audio. The following paragraphs describe these uplink/downlink functions in more detail.

voice uplink path

The voice uplink path includes two input stages, refer to Figure 12. The first one is a microphone amplifier, compatible with an electret microphone containing a FET-buffer with open-drain output, has a gain of typically 27 dB, and provides an external voltage of 2 V to 2.5 V to bias the microphone. The auxiliary audio input can be used as an alternative source for a higher level speech signal. This stage performs single-ended to differential conversion and provides a gain of 6 dB. When auxiliary audio input is used, the microphone input is disabled and powered down.

The resulting fully differential signal is fed to a programmable gain amplifier that allows adjustment of the level of the speech signal to the dynamic range of the A/D converter, which is determined by the value of the internal voltage reference. Programmable gain can be set from –12 dB to +12 dB in 1-dB steps and is programmed with bits VULPG to VULPG4 of VBCTL1 register.

Analog to digital conversion is made with a third-order sigma-delta modulator whose sampling rate is 1 MHz. Output of the A/D converter is fed to a speech digital filter which performs the decimation down to 8 KHz and band limits the signal with both a low-pass and high-pass transfer functions. The speech samples are then transmitted to the DSP using the voice serial interface at a rate of 8 kHz.

Programmable functions of the voice uplink path, power-up, input selection and gain are controlled by the DSP or the MCU using the serial interfaces. The uplink voice path can be powered down with the bit VULON of the VBCTL1 internal register.

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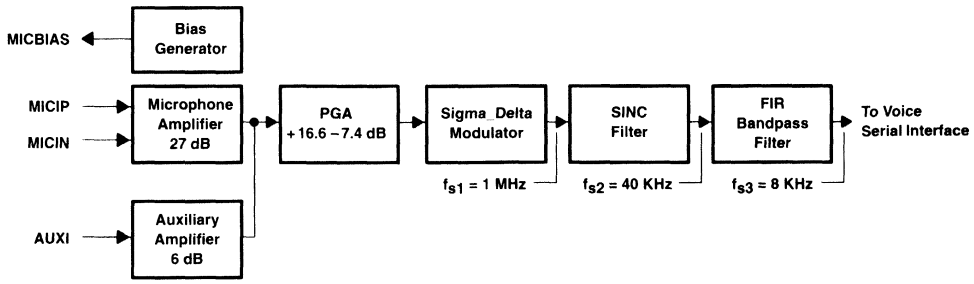

Figure 12. Uplink Path Block Diagram

voice downlink path

The voice downlink path receives speech samples at an 8-kHz rate from the voice serial interface and converts them to analog signals to drive the external speech transducer.

The digital speech coming from the voice serial interface is first fed to a speech-digital finite-duration impulse response (FIR) filter, which has two functions (see Figure 13). The first function is to interpolate the input signal and increase the sampling rate form 8 kHz up to 1 MHz to permit D/A conversion by an oversampling digital modulator. The second function is to band limit the speech signal using both low-pass and high-pass transfer functions.

The interpolated and band-limited signal is fed to a second-order sigma-delta modulator and sampled at 1 MHz to generate a 1-bit oversampled signal that drives a 1-bit D/A converter.

Due to the oversampling conversion, the analog signal obtained at the output of the one-bit D/A converter is mixed with high frequency noise. This noise is filtered by a switched-capacitor third-order low-pass filter and the remaining signal is fed to a programmable gain amplifier (PGA) to adjust the volume control. Volume control is done in 6-dB steps from 0 dB through –24 dB; in the mute state, attenuation is higher than 40 dB. A fine adjustment of gain is possible from –6 to +6 dB in 1-dB steps to calibrate the system, depending on the earphone characteristics. This configuration is programmed using the VBCTL2 register.

The PGA output is fed to two output stages: The earphone amplifier that provides a full differential signal on the terminals EARP/EARN and an auxiliary output amplifier that provides a single-ended signal on terminal AUXO. The downlink voice path can be powered down with bit VDLON of the VBCTL2 internal register.

A side-tone path is connected between the output of the voice uplink PGA and the input of the voice downlink PGA. This path provides seven programmable gains (+1 dB, –2dB, –5 dB, –8 dB, –11 dB, –14 dB, –17 dB) and one mute position. Side-tone path gain can be selected by programming bit at register address 23.

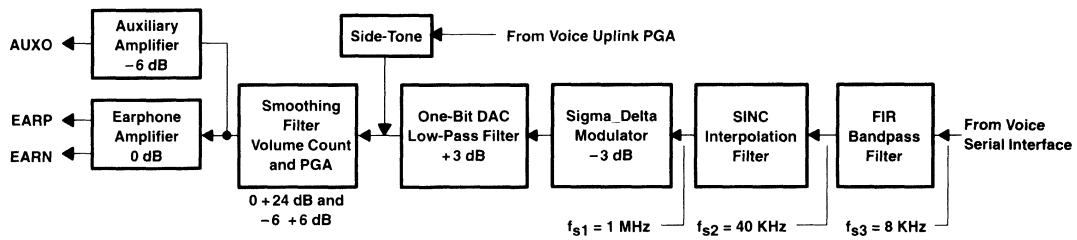

Figure 13. Downlink Path Block Diagram

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DAI interface

This digital audio interface (DAI) consists of four terminals: SSRST, SSCLK, SSDR, and SSDX. It is compatible with the digital audio interface described in the GSM Recommendatioin 11.10. This interface is designed to offer minimum CPU overhead during audio tests and speech transcoding tests, and to minimize the extra hardware and the number of external terminals of the mobile system (MS). With this interface the DSP does not have to deal with rate adaptation. In normal operation the DSP works with a 8-kHz sampling rate with a 16-bit word format and frame synchronization, but the DAI interface works with an 8-kHz sampling rate with a 13-bit word format without frame synchronization. The DSP (or the MCU) does not have real time constraints with SSRST since the reset of the internal transmitters is done automatically.

power-down functional description

During periods of time it is possible to disable some functions in order to lower the TCM4400 power consumption. For example, it is possible to disable the internal functions dedicated to radio transmission during GSM-idle mode. It is also possible to disable the internal demodulator path during transmit window.

There are three ways to control the power consumption of the internal blocks as described in following paragraphs.

direct control with internal register

With this method these internal blocks are power down:

- DAI GSM tests: bit DAION of register VBCTL3
- Transmit and receive voice path: bit VULON of register VBCTL1 and bit VDLON of register VBCTL2

radio window activation control

With this method these internal blocks are powered up with the control of two bits. The first bit enables the window control of the block activity, the second bit enables the power down.

First bit: If cleared to 0, the function is powered down with the control of the corresponding GSM window (BDLON/BULON terminal) and with the control of the second bit. If this first bit is set to 1, the power down is only controlled by the second bit.

Second bit: This bit is functionally associated with the first one. When this bit is loaded with 0, the function is in power-down mode.

During transmit windows designated with the activity of the BULON terminal:

- Automatic power control (APC): bits APCW and APCPD of register AUXCTL2 are paired.
- Baseband uplink path: bits BBULW and BBULPD of register PWDNRG1 are paired.
- External reference voltage buffers VMID: bits VMIDW and VMIDPD are paired.

During receive windows designated with activity of the BDLON terminal:

- Analog automatic gain control (AAGC): bits AAGCW and AAGCPD of register AUXCTL2 are paired.
- Baseband downlink path: bits BBDLW and BBDLPD of register PWDNRG1 are paired.

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external terminal PWRDN control

With this method these internal blocks are powered up with the control of two bits. The first bit enables the external terminal PWRDN control of the block activity, the second bit enables the power down.

First bit: If cleared to 0, the function is powered down with the control of PWRDN terminal and with the control of the second bit. If this first bit is set to 1, the power down is only controlled by the second bit.

Second bit: This bit is functionally associated with the first one. When this bit is loaded with 0, the function is in power-down mode.

- For the digital serial interface to the DSP: bits BBSIPN and BBSIPD of register PWDNRG2 are paired.
- For the timing interface: bits TIMGPN and TIMGPD of register PWDNRG2 are paired.
- For the auxiliary A/D converters: bits ADCPN and ADCPD of register AUXCTL1 are paired.
- For the automatic frequency control (AFC) block: bits AFCPN and AFCPD of register AUXCTL1 are paired.
- For the external reference voltage buffers MICBIAS: bits VREFPN and VREFPD of register PWDNRG2 are paired.
- For the internal reference band-gap buffers: bit VGAPPN determines whether or not that the bandgap power down is under control of the PWRDN bit.

DSP voiceband serial interface

Voiceband serial digital interface consists in a bidirectional serial port. Both receive and transmit operations are double buffered, thus allowing a continuous communication stream. The serial port is fully static and, thus, functions with any arbitrary low clocking frequency.

The transfer mode available on this port is:

Clock frequency	520 kHz	16-bit data packet	frame synchronization

VCLK is the output serial clock used to control the transmission or reception of the data, (see Figure 5). VCLK can run in burst mode or continuous mode, depending on the VCLKMODE bit. The transmitted serial data (VDX) is the serial data output; the frame synchronization (VFS) is used to initiate the transfer of transmit and receive data. The received data (VDR) is the serial data input

Each serial port includes four registers, which are the data transmit register (DXR), the data receive register (DRR), the transmit shift register (XSR), and the receive shift register (RSR).

The voice serial interface has the same structure and timing diagram as the serial interface. One extra cycle is generated before VFS and two extra cycles are generated after the least significant bit (see Figure 5).

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voltage references

Voltage and current generators are integrated inside the GSM converter. Some additional components are required for the decoupling and regulation of the internal references. In addition, the internal buffers are automatically shut down with the corresponding functions being powered down.

There are five terminals reserved for voltage references decoupling and use: VGAP, IBIAS, VREF, MICBIAS and VMID (refer to Table 1):

VGAP: This terminal is connected to the internal band gap reference voltage. It must be externally connected to a 0.1-µF capacitor. The band gap drives the current generator and the voltage reference. This bandgap may be down powered by PWRDN pin depending on bit VGAPPN of register PWDNRG2.

IBIAS: This terminal is connected to the current reference. It must be externally connected to a 100 kΩ resistor. As this block is connected to the AFC function, the power down is controlled with similar means. The current generator is shut down with the same bits of the band gap: one bit for the power down selection of a hardware solution (with the external PWRDN terminal).

VREF: This terminal is connected to the internal reference voltage. It must be externally connected to a 0.1-µF capacitor. This band gap may be down powered with the control of the bits VREFPN and VREFPD of the register PWDNRG2. This voltage reference is internally connected to three buffers corresponding to the blocks of speech downlink, speech uplink and GMSK downlink. The two first blocks are down powered with the inactivity of the corresponding speech blocks. This last block is shut down outside the radio downlink activations.

MICBIAS: This buffer is destined to drive an electret-type microphone. The output voltage can be chosen by software (bit MICBIAS of VBCTL1 register) between the value 2 V to 2.5 V.

VMID: This buffer gives the $V_{DD}/2$ or 1.35 V common-mode output voltage of the baseband uplink path. This voltage value is selected with the SELVMID bit.

Table 1. Voltage References

REFERENCE	VOLTAGE	DEFINITION
VGAP	1.22 V	Band gap used for all other references
VREF	1.75 V	Voltage reference of GMSK internal ADC and DAC
VMID	$AV_{DD2}/2$	Common-mode reference for uplink/downlink GMSK
MICBIAS	2 V / 2.5 V	Microphone-driving voltage
ACDMID	1.75 V	Voltage reference of the auxiliary ADCs

MCU serial baseband digital interface

The GSM baseband and voice A/D and D/A conversion provide two digital serial 16-bit interfaces intended for use with the DSP and a microcontroller device. Through this interface a microcontroller can access all the internal registers that can be accessed through the DSP digital serial interface.

This option is intended for application in which part of layer-1 software is implemented into the microcontroller and needs access to some functions implemented into the GSM baseband and voice A/D and D/A conversion circuitry.

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serial interface

The microcontroller serial interface is designed to be compliant with 8-bit standard synchronous serial ports. This interface consists of four terminals (see Figure 3 for timing diagram).

UCLK: A clock provided by the microcontroller to GSM baseband and voice A/D and D/A conversion.

UDR: An input terminal of the GSM baseband and voice A/D and D/A components intended for reception of data.

UDX: An output terminal of the GSM baseband and voice A/D and D/A components intended for transmission of data.

USEL: An input terminal of GSM baseband and voice A/D and D/A components intended for activation of the serial interface.

When USEL = V_{DD}, the serial interface is deactivated and UDX is placed in a high-impedance state. A high level on USEL resets the internal serial interface, the 16-bit transfers must be completed with USEL = V_{SS}.

The external MCU initiates data transfer by driving the selection terminal and sending a clock signal. For both the GSM baseband and voice A/D and D/A components, the MCU data is shifted out of the shift registers on one edge of the clock and latched into the shift registers on the opposite clock edge.

As a result, both controllers send and receive data simultaneously. For the MCU portion, the software determines whether the data is meaningful or dummy data. On the GSM Baseband and voice A/D and D/A conversion portion, dummy data is that data with all zeroes.

The 16-bit word data format is identical to the BSP data format. After a read-register command, there is a sequential transfer delay between two 16-bit word acquisitions to let the internal sequencer extract the data going from internal registers to the serial shift register.

Three internal bits control the data serial flow as follows:

- UDIR determines whether data is transferred with MSB or LSB first.
- UPOL determines the polarity of the clock
- UPHA determines the insertion of a half-clock period in the data serial flow.

With UPOL and UPHA there are four clock schemes (see Table 2):

- Falling edge without delay — The MCU serial interface transmits data on the falling edge of the UCLK and receives data on the rising edge of the UCLK
- Falling edge with delay — The MCU serial interface transmits data one half-cycle ahead of the falling edge of the UCLK and receive data on the falling edge of the UCLK
- Rising edge without delay — The MCU serial interface transmits data on the rising edge of the UCLK and receive data on the falling edge of the UCLK
- Rising edge with delay — The MCU serial interface transmits data one half-cycle ahead of the rising edge of the UCLK and receive data on the rising edge of the UCLK

Table 2. Microcontroller Clocking Schemes

UPOL	UPHA	MCU Clocking Scheme
1	1	Falling edge without delay
1	0	Falling edge with delay
0	1	Rising edge without delay
0	0	Rising edge with delay

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DSP/MCU serial interface

The DSP/MCU serial interface is used not only to configure the GSM baseboard and voice A/D and D/A conversion but also to transmit data to the DSP during downlink burst reactions. The following paragraphs describe the operation of the serial interface in more detail.

DSP serial digital interface

The DSP serial digital interface (Figure 14) is used to transfer the baseband transmit and receive data, and is also used to access all internal programming registers of the device (baseband codec, voice codec and auxiliary RF functions). The format for the serial interface is 16 bits.

The baseband serial digital interface is a bidirectional (transmit/receive) serial port. Both receive and transmit operations are double buffered and permit a continuous communication stream (16-bit data packets). The serial port is fully static and functions with any arbitrary, low-clocking frequency.

Six terminals are used for the serial port interface (see Figure 4 for timing diagram). BCLKR is an I/O port for the serial clock used to control the reception of the data BDR. At reset BCLKR is configured as an output and the clock frequency is set to MCLK/3 (4.333 MHz with MCLK = 13 MHz), the clock signal is running permanently. The port BCLKR can be reconfigured as an input by programming an internal register. In this case BCLKR is provided by the DSP and can run in burst mode to reduce power consumption. The receive frame synchronization (BFSR) is used to identify the beginning of a data packet transfer on port BDR.

The transmitted serial data (BDX) is the serial data input; the transmit frame synchronization (BFSX) is used to initiate the transmission of data. The transmit clock (BCLKX) is provided by the GSM baseband and voice A/D and D/A converters with a MCLK frequency. The clock signal BCLKX can run in burst mode or continuous mode, depending on the BCLKMODE bit. The downlink data bus (BFSX, BCLKX, BDX) can be driven to VSS or placed in a high-impedance state when no data is to be transferred to the DSP. The bit BCLKDIR of the register BCTLREG controls the direction of the BCLKR clock.

As with the voice serial interface, on extra clock cycle must be generated because the last 16-bit word received on the DSP serial interface is latched on the next two falling BCLKR edges following the LSB. As for the voice serial interface, one extra clock period is generated on the BCLKX before the first synchronization BFSX of the downlink data sequence.

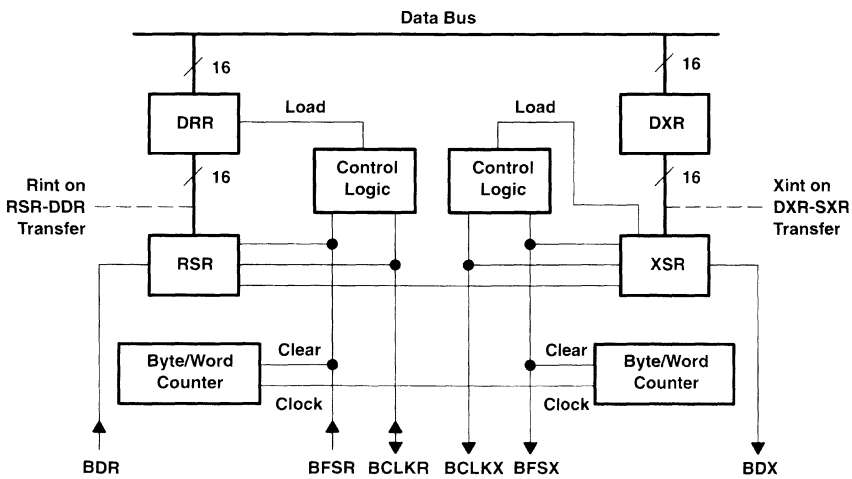

Figure 14. DSP Serial Port

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DSP/MCU serial interface operation and format

The DSP/MCU serial interface is used to both configure the GSM baseband and voice A/D and D/A converters (read and write operation in internal registers) and transmist RF data to the DSP during reception of a burst by the downlink path of the GSM baseband and voice A/D and D/A circuitry.

During reception of a burst (bit DLR of the status register is 1) and DSP serial interface and associated internal bus are dedicated to the transfer of RF data from the GSM baseband A/D and D/A converters to the DSP. During this period only a write operation of internal registers can be done through the DSP serial interface. However, all registers can be accessed by the serial MCU interface.

During transmission of a burst (bit ULX of the status register is 1) no read or write operation can be done in the registers of the baseband uplink part of the GSM baseband, APC RAM, and APC shape register.

Writing or reading registers using the serial interface is done by transferring 16-bit words to the serial interface. Each word is split into three fields as shown in Table 3.

Table 3. Read/Write Data Word

DATA										ADDRESS					R/W
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	1 / 0

When writing to internal registers observe the following convention:

Bit 0 : It indicates a write operation at zero .

Bits 1 to 5 : This field contains the address of the register to be accessed.

Bits 6 to 15 : This field contains the data to be written into the internal register.

When reading from internal registers observe the following convention:

Bit 0 : At 1 it indicates a read operation.
Bits 1 to 5 : This field contains the address of the register to be accessed.
Bits 6 to 15 : This field is an irrelevant status in a read request operation.

Read operation from the downlink baseband codec is done using the TX part of the DSP/MCU serial interface in the following 16-bit word format given in Table 4.

Table 4. 16-Bit Word Format

DATA										ADDRESS					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A4	A3	A2	A1	A0	0

During reception of a burst, transfer of RF data from the downlink baseband codec is done using the transmit part of the DSP serial interface in the following 16-bit word format: As the I and Q samples are coded with 16-bit words, the data rate is 270833 x 16 x 2 which equals 8.66 Mbps. Since the digital clock MCLK is 13 MHz, transfer is done at 13 Mbps in burst mode. During burst reception the DSP serial interface is idled about 33% of the time.

Table 5. Format of 16-Bit Word Transfer

DATA															I / Q
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

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DSP/MCU serial interface registers

The following internal register buffers are accessed using the DSP/MCU serial interface during manual operation of the TCM4400.

baseband uplink ramp delay register

Each bit position of the baseband uplink ramp-delay register is given in Table 6.

Table 6. Uplink Ramp-Delay Register

BULRUDEL: BASEBAND UPLINK RAMP DELAY REG.								ADDRESS :1							R/W
RESERVD	IBUFPTR	DELD3	DELD2	DELD1	DELD0	DELU3	DELU2	DELU1	DELU0	0	0	0	0	1	1 / 0
R = 0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<— ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<—VALUE AT RESET					

DELU0 to DELU3 : Value of the delay of ramp-up start versus the rising edge of BENA.

DELD0 to DELD3 : Value of the delay of ramp-down start versus the falling edge of BENA.

IBUFPTR : Writing a 1 in this bit initializes the pointer of the burst buffer to the base address.

RESERVD : Reserved bits for testing purposes

R/W : A 1 indicates a read operation; a 0 indicates a write operation.

baseband uplink data buffer

The baseband uplink data buffer is used to transmit the uplink burst data. The uplink data buffer contents are shown in Table 7.

Table 7. Uplink Data Buffer

BULDATA: BASEBAND UPLINK DATA BUFFER										ADDRESS: 2 (16 WORDS)					W
BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7	BIT8	BIT9	0	0	0	1	0	0
BIT10	BIT11	BIT12	BIT13	BIT14	BIT15	BIT16	BIT17	BIT18	BIT19	0	0	0	1	0	0
BIT20	BIT21	BIT22	BIT23	BIT24	BIT25	BIT26	BIT27	BIT28	BIT29	0	0	0	1	0	0
BIT30	BIT31	BIT32	BIT33	BIT34	BIT35	BIT36	BIT37	BIT38	BIT39	0	0	0	1	0	0
BIT40	BIT41	BIT42	BIT43	BIT44	BIT45	BIT46	BIT47	BIT48	BIT49	0	0	0	1	0	0
BIT50	BIT51	BIT52	BIT53	BIT54	BIT55	BIT56	BIT57	BIT58	BIT59	0	0	0	1	0	0
BIT60	BIT61	BIT62	BIT63	BIT64	BIT65	BIT66	BIT67	BIT68	BIT69	0	0	0	1	0	0
BIT70	BIT71	BIT72	BIT73	BIT74	BIT75	BIT76	BIT77	BIT78	BIT79	0	0	0	1	0	0
BIT80	BIT81	BIT82	BIT83	BIT84	BIT85	BIT86	BIT87	BIT88	BIT89	0	0	0	1	0	0
BIT90	BIT91	BIT92	BIT93	BIT94	BIT95	BIT96	BIT97	BIT98	BIT99	0	0	0	1	0	0
BIT100	BIT101	BIT102	BIT103	BIT104	BIT105	BIT106	BIT107	BIT108	BIT109	0	0	0	1	0	0
BIT110	BIT111	BIT112	BIT113	BIT114	BIT115	BIT116	BIT117	BIT118	BIT119	0	0	0	1	0	0
BIT120	BIT121	BIT122	BIT123	BIT124	BIT125	BIT126	BIT127	BIT128	BIT129	0	0	0	1	0	0
BIT130	BIT131	BIT132	BIT133	BIT134	BIT135	BIT136	BIT137	BIT138	BIT139	0	0	0	1	0	0
BIT140	BIT141	BIT142	BIT143	BIT144	BIT145	BIT146	BIT147	BIT148	BIT149	0	0	0	1	0	0
BIT150	BIT151	BIT152	BIT153	BIT154	BIT155	BIT156	BIT157	BIT158	BIT159	0	0	0	1	0	0
W	W	W	W	W	W	W	W	W	W	<—ACCESS TYPE					
1	1	1	1	1	1	1	1	1	1	<—VALUE AT RESET					

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baseband uplink data buffer (continued)

Bit 0 – Bit 159 are the bits composing the sequence of the transmitted burst, bit 0 is transmitted first. For a normal burst, the uplink data buffer is loaded as follows:

Bit0 to Bit3	: 4 guard bits
Bit4 to Bit6	: 3 tail bits
Bit7 to Bit66	: 58 data bits
Bit67 to Bit92	: 26 training sequence bits
Bit93 to Bit92	: 58 training sequence bits
Bit151 to Bit153	: 3 tail bits
Bit154 to Bit159	: 6 guard bits

At reset and after each transmission, the burst buffer is reinitialized with guard bits (all bits = 1).

baseband uplink I and Q offset registers

The baseband uplink I and Q offset register contain the offset values for the I and Q components, respectively, as shown in Tables 8 and 9.

Table 8. Uplink I Offset Register

BULIOFF: BASEBAND UPLINK I OFFSET REGISTER										ADDRESS: 3					R/W
RESERVD	ULIOFF8	ULIOFF7	ULIOFF6	ULIOFF5	ULIOFF4	ULIOFF3	ULIOFF2	ULIOFF1	ULIOFF	0	0	0	1	1	1/0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<–ACCESS TYPE					
0	1	1	1	1	1	1	1	1	1	<–VALUE AT RESET					

ULIOFF0 to ULIOFF1 : Integration bits during calibration (to minimize sensitivity to noise)
ULIOFF2 to ULIOFF8 : Value of the offset on I channel
RESERVD : Reserved bits for testing purposes
R/W : A 1 indicates a read operation; a 0 indicates a write operation

Table 9. Uplink Q Offset Register

BULQOFF: BASEBAND UPLINK Q OFFSET REGISTER										ADDRESS: 4					R/W
RESERVD	ULQOFF8	ULQOFF7	ULQOFF6	ULQOFF5	ULQOFF4	ULQOFF3	ULQOFF2	ULQOFF1	ULQOFF0	0	0	1	0	0	1/0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<–ACCESS TYPE					
0	1	1	1	1	1	1	1	1	1	<–VALUE AT RESET					

ULQOFF0 to ULQOFF1 : Integration bits during calibration (to minimize sensitivity to noise)
ULQOFF2 to ULQOFF8 : Value of the offset on Q channel
RESERVD : Reserved bits for testing purposes
R/W : A 1 indicates a read operation; a 0 indicates a write operation

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baseband uplink I and Q D/A conversion registers

The I and Q component values generated by the I and Q uplink D/A converter during the conversion of analog data are written to and read from the uplink I and Q D/A converter registers as shown in Tables 10 and 11.

Table 10. Uplink I DAC Register

BULIDAC: BASEBAND UPLINK I DAC REGISTER										ADDRESS: 6					R/W
RESERVD	RESERVD	ULIDAC7	ULIDAC6	ULIDAC5	ULIDAC4	ULIDAC3	ULIDAC2	ULIDAC1	ULIDAC0	0	0	1	1	0	1/0
R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<–ACCE0S TYPE					
0	0	0	0	0	0	0	0	0	0	<–VALUE AT RESET					

ULIDAC0 to ULIDAC7: Data applies to D/A converter of I channel

RESERVD: Reserved bits for testing

R/W: A 1 indicates a read operation; a 0 indicates a write operation

Table 11. Uplink Q DAC Register

BULQDAC: BASEBAND UPLINK Q DAC REGISTER										ADDRESS: 5					R/W
RESERVD	RESERVD	ULQDAC7	ULQDAC6	ULQDAC5	ULQDAC4	ULQDAC3	ULQDAC2	ULQDAC1	ULQDAC0	0	0	1	0	1	1/0
R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<–ACCESS TYPE					
0	0	0	1	1	1	1	1	1	1	<–VALUE AT RESET					

ULIDAC0 TO ULIDAC7: Data is applied to the D/A converter of the Q channel

RESERVD: Reserved bits for testing

R/W: A 1 indicates a read operation; a 0 indicates a write operation

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power down register No. 2

The values in each bit position of power-down register No. 2 have the meaning outlined in Table 12.

Table 12. PWDNGR2 Register

PWDNRG2: REGISTER FOR POWERING DOWN										ADDRESS: 8					R/W
RESERVD	RESERVD	TIMGPN	TIMGPD	BBSIPN	BBSIPD	VGAPPN	CHGUP	VREFPN	VREFPD	0	1	0	0	0	1/0
R = 0	R = 0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<–ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<–VALUE AT RESET					

VREFPN: If cleared to 0, the internal reference voltage is powered down under the control of terminal PWRDN and bit VREFPD. If bit VREFPD is set to 1, the power down is only controlled by bit VREFPD.

VREFPD: This bit is functionally associated with bit VREFPD.

VGAPPN: If cleared to 0, the intenal reference VGAP is powered down under the control of terminal PWRDN. If this bit is set to 1, the VGAP is not placed in power-down mode.

TIMGPN: If cleared to 0, the timing interface is powered down under the control of terminal PWRDN.

TIMGPD: If this bit is set to 1, the power down is only controlled by bit TIMGPD. This bit is functionally associated with bit TIMGPN. When this bit is 1, timing interface is active and in the power-down mode.

BBSIPN: If cleared to 0, the baseband serial interface is powered down under the control of terminal PWRDN. If this bit is set to 1, the power down is only controlled by bit BBSIPD.

BBSIPD: This bit is functionally associated with bit BBSIPN. When this bit is set to 1, baseband serial interface is in power-down mode.

CHGUP: This bit is used for testing purposes to accelerate the band-gap settling time.

RESRVD: Reserved bits for testing purpose.

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power down register No. 1

The values in each bit position of power down register No. 1 have the meaning outlined in Table 13.

Table 13. PWDNRG1 Register

PWDNRG1: REGISTER FOR POWERING DOWN										ADDRESS: 7					R/W
SELVMID	BALOOP	VMIDW	VMIDPD	BBULW	BBULPD	BBDLW	BBDLPD	EXTCAL	BBRST	0	0	1	1	1	1/0
R = 0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<–ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<–VALUE AT RESET					

BBRST: This is the digital reset of the baseband codec, the RAM is set to 1 and the memory of the digital filter is cleared to 0.

EXTCAL: Downlink autocalibration mode (at 0: autocalibration; at 1: external calibration)

BBULW: If cleared to 0, the baseband uplink path is powered down under the control of the GSM transmit window (BULON terminal). If this bit is set to 1, the power down in only controlled by bit BBULPD.

BBULPD: This bit is functionally associated with bit BBULW. When this bit is set to 1, the baseband uplink path is in power-down mode.

BBDLW: If cleared to 0, the baseband downlink path is powered down under the control of GSM receive window (BDLON terminal). If this bit is set to 1, the power down is only controlled by bit BBDLPD.

BBDLPD: This bit is functionally associated with bit BBDLW. When this bit is set to 1, the baseband downlink path is in power-down mode.

VMIDW: If cleared to 0, the VMID output driver is powered down under the control of GSM transmit window (BULON terminal). If this bit is set to 1, the power down is only controlled by bit VMIDPD.

VMIDPD: This bit is functionally associated and paired with bit VMIDW. When VMIDW bit is set to 1, the VMID output driver is active. When VMIDPD bit is set to 1, the VMID output driver is in power-down mode.

BALOOP: When set to 1, the internal analog loop of I and Q uplink terminals are connected to I and Q downlink terminals.

SELVMID: When cleared to 0, this sets the common-mode voltage of the baseband uplink and VMID at $V_{DD}/2$; when set to 1, these voltages are set to 1.35 V.

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baseband control register (see Table 14)

The values in the baseband control register bit positions determine whether the data is shifted left or right. Note that the microcontroller unit (MCU) clocking scheme determines on which edge of the clock that data is received or transmitted using the serial interface.

Table 14. Baseband Control Register

BCTLREG: BASEBAND CONTROL REGISTER										ADDRESS: 9					R/W
RESERVD	RESERVD	RESERVD	MCLKBP	BCLKMODE	BIZBUS	BCLKDIR	UDIR	UPHA	UPOL	0	1	0	0	1	1/0
R = 0	R = 0	R = 0	R = 0	R = 0	R/W	R/W	R/W	R/W	R/W	<–ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<–VALUE AT RESET					

UDIR: This bit determines whether the data is shifted in from right (see serial register description) to left, LSB first (bit value 0), or from left to right, MSB first (bit value 1).

BCLKMODE: When cleared to 0, BLCKX runs in the burst mode; when set to 1, BCLKX is continuous

MCLKBP: When cleared to 0, UCLK signal passes through the clock slicer; when set to 1, the clock slicer is bypassed (in this case, the signal at the MCLK terminal must be digital).

MCU clocking schemes

Falling edge without delay: The MCU seriel interface transmits data on the falling edge of the UCLK and receives data on the rising edge of UCLK.

Falling edge with delay: The MCU serial interface transmits data one half-cycle ahead of the falling edge of the UCLK and receives data on the falling edge of the UCLK.

Rising edge without delay: The MCU serial interface transmits data on the rising edge of the UCLK and receives data on the falling edge of the UCLK.

Rising edge with delay: The MCU serial interface transmits data one half-cycle ahead of the rising edge of the UCLK and receives data on the rising edge of UCLK.

Table 15. MCU Clocking Schemes

UPOL	UPHA	MCU clocking scheme
1	1	Falling edge without delay
1	0	Falling edge with delay
0	1	Rising edge without delay
0	0	Rising edge with delay

BCLKDIR: Direction of the BCLKR port.

BIZBUS: When set to 1, BDX, BCLKX, BFSX are in hi-Z when there is nothing to transfer to the DSP; when cleared to 0, DBX, BCLKX, BFSX are set to V_{SS} when there is nothing to transfer to the DSP.

RESRVD: Reserved bits for testing purpose

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voiceband uplink control register

The values in the voiceband uplink control reigister bit positions control not only the power level of the audio in the uplink path but also set the gain of the PGA from –12 dB to 12 dB in 1 dB steps. Bit MICBIAS and VULMIC and VULAUX are shifted by one position to the left. This is shown in Table 16.

Table 16. Voiceband Uplink Control Register

VBCTL1: VOICEBAND UPLINK CONTROL REGISTER										ADDRESS: 10					R/W
RESERVD	MICBIAS	VULMIC	VULAUX	VULPG4	VULPG3	VULPG2	VULPG1	VULPG0	VULON	0	1	0	1	0	1/0
R = 0	R = 0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<–ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<–VALUE AT RESET					

VULON: Power on the uplink path of the audio codec

VULAUX: Enables the auxiliary input amplifier if bit VULON is 1

VULMIC: Enables the microphone input amplifier if bit VULON is 1

MICBIAS: When MICBIAS = 0, the analog bias for the electret microphone and external decoupling is driven to 2 V; when the value is 1, the bias is 2.5 V.

RESERVD: Reserved for testing

VULPG (0 to 4): Gain of the voice-uplink programmable gain amplifier (–6 dB to 6 dB in 1 dB step), see Table 17.

Table 17. Uplink PGA Gain

VULPG 4	VULPG 3	VULPG 2	VULPG 1	VULPG 0	ABS GAIN	PGA RELATIVE GAIN
1	0	0	0	0	4.6 dB	–12 dB
1	0	1	1	1	4.6 dB	–11 dB
1	1	0	0	0	4.6 dB	–10 dB
1	1	0	0	1	4.6 dB	–9 dB
1	1	0	1	0	4.6 dB	–8 dB
1	1	0	1	1	4.6 dB	–7 dB
0	0	0	0	0	4.6 dB	–6 dB
0	0	0	0	1	4.6 dB	–5 dB
0	0	0	1	0	4.6 dB	–4 dB
0	0	0	1	1	4.6 dB	–3 dB
0	0	1	0	0	4.6 dB	–2 dB
0	0	1	0	1	4.6 dB	–1 dB
0	0	1	1	0	4.6 dB	0 dB
0	0	1	1	1	4.6 dB	1 dB
0	1	0	0	0	4.6 dB	2 dB
0	1	0	0	1	4.6 dB	3 dB
0	1	0	1	0	4.6 dB	4 dB
0	1	0	1	1	4.6 dB	5 dB
0	1	1	0	0	4.6 dB	6 dB
1	0	0	0	1	4.6 dB	7 dB
1	0	0	1	0	4.6 dB	8 dB
1	0	0	1	1	4.6 dB	9 dB
1	0	1	0	0	4.6 dB	10 dB
1	0	1	0	1	4.6 dB	11 dB
1	0	1	1	0	4.6 dB	12 dB

PRINCIPLES OF OPERATION

voiceband downlink control register

The values in the voiceband downlink control register bit positions control the audio power level in the downlink path. Earphone volume is set (three bits VOLCTL0 –VOLCTL2) and PGA gain is set from –6 dB to 6 dB in 1 dB steps. This is shown in Table 18.

Table 18. Voiceband Downlink Control Register

VBCTL2: VOICEBAND DOWNLINK CONTROL REGISTER										ADDRESS: 11	R/W
VDLAUX	VDLEAR	VOLCTL2	VOLCTL1	VOLCTL0	VDLG3	VDLG2	VDLG1	VDLG0	VDLON	0 1 0 1 1	1 / 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<–ACCESS TYPE	
0	0	0	0	0	0	0	0	0	0	<–VALUE AT RESET	

VDLON: Power on of the downlink path of the audio codec

VDLEAR: Enables the earphone amplifier if the bit VDLON is 1

VDLAUX: Enables the auxiliary output amplifier if the bit VDLON is 1

VDLG (0 to 3) 1dB: Gain of the voice-downlink programmable gain amplifier (–6 dB to 6 dB in 1-dB steps), see Table 19.

Table 19. Downlink PGA Gain

	VDLG3	VDLG2	VDLG1	VDLG0	RELATIVE GAIN
0	0	0	0	0	–6 dB
1	0	0	0	1	–5 dB
2	0	0	1	0	–4 dB
3	0	0	1	1	–3 dB
4	0	1	0	0	–2 dB
5	0	1	0	1	–1 dB
6	0	1	1	0	0 dB
7	0	1	1	1	1 dB
8	1	0	0	0	2 dB
9	1	0	0	1	3 dB
10	1	0	1	0	4 dB
11	1	0	1	1	5 dB
12	1	1	0	0	6 dB
13	1	1	0	1	–6 dB
14	1	1	1	0	–6 dB
15	1	1	1	1	–6 dB

VOLCTL (0 to 2): Volume control (0, –6 ,–12, 18, –24, Mute), see Table 20.

Table 20. Volume Control Gain Settings

	VOLCTL2	VOLCTL1	VOLCTL0	RELATIVE GAIN
0	0	1	0	0 dB
1	1	1	0	–6 dB
2	0	0	0	–12 dB
3	1	0	0	–18 dB
4	0	1	1	–24 dB
5	1	0	1	Mute
6	0	0	1	Mute
7	1	1	1	Mute

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voiceband control register

The values in the voiceband control register have the meaning shown in Table 21.

Table 21. Voiceband Control Register

VBCTL3: VOICEBAND CONTROL REGISTER										ADDRESS: 12					R/W
RESERVD	RESERVD	VCLKMODE	DAIMD1	DAIMD0	VDAI	DAION	VALOOP	VIZBUS	VRST	0	1	1	0	0	1 / 0
R = 0	R = 0	R /W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<–ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<–VALUE AT RESET					

VALOOP: When set to 1, the internal analog loop of output samples are sent to the audio input terminal; standard audio paths are connected together, and auxiliary audio paths are connected together.

VIZBUS: When set to 1, VFS, VCLK, VDX are put in a hi-Z state when there is nothing to transfer to the DSP, when cleared to 0, VFS and VCLK are put in V_{SS} when there is nothing to transfer to the DSP, and the VDX bus drives an undefined value (value depends on the previous serial data transfers).

VRST: Resets the digital parts of the audio codec (digital filter and modulator).

DAION: When cleared to 0, the DAI block is in power down; when set to 1, the DAI block is active.

VDAI: Writing a 1 to this bit starts the SSCLK (104 kHz DAI clock) on reception of the first sample. This bit is automatically reset to 0 by SSRST after reception of the last sample.

RESERVD: Reserved bits for testing

DAIMD (0–1): DAI mode selection as given in Table 22.

VCLKMODE When cleared to 0, allows selection of VCLK in burst mode. When set to 1, allows-selection of VCLK in continuous mode.

Table 22. DAI Mode Selection

DAIMD1	DAIMD0	DAI MODE
0	0	Normal operation (no tested device using DAI)
0	1	Test of speech decoder / DTX functions (downlink)
1	0	Test of speech encoder / DTX functions (uplink)
1	1	Test of acoustic devices and A/D and D/A (voice path)

PRINCIPLES OF OPERATION

auxiliary functions control register No. 1

The bit values in the auxiliary functions control register No. 1 resets the APC generator or the AFC modulator, selects the A/D counter input, and selects the AFC sampling frequency. This is shown in Table 23.

Table 23. AUX Functions Control Register No. 1

UXCTL1: AUXILIARY FUNCTIONS CONTROL REGISTER										ADDRESS: 13	R/W
AFCPN	AFCPD	ADCPN	ADCPD	AFCCK1	AFCCK0	ADCCH2	ADCCH1	ADCCH0	ARST	0 1 1 0 1	1/0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<–ACCESS TYPE	
0	0	0	0	0	0	0	0	0	0	<–VALUE AT RESET	

ARST: Reset of the digital parts of the auxiliary functions (APC generator and AFC modulator).

ADCCH(0 to 2): Selection of the input of the A/D converter, see Table 24.

Table 24. A/D Converter Selection

ADCCH2	ADCCH1	ADCCH 0	A/D CONVERTER INPUT SELECTION
0	0	0	A/D conversion of ADIN1
0	0	1	A/D conversion of ADIN2
0	1	0	A/D conversion of ADIN3
0	1	1	A/D conversion of ADIN4
1	0	0	A/D conversion of ADIN5
1	0	1	A/D conversion of ADIN5
1	1	0	A/D conversion of ADIN5
1	1	1	A/D conversion of ADIN5

AFCCK(0 To 1): Selection of the sampling frequency of the AFC, see Table 25.

Table 25. AFC Selection

AFCCK 1	AFCCK 0	AFC INTERNAL FREQUENCY
0	0	0.25 MHz
0	1	0.50 MHz
1	0	1 MHz
1	1	2 MHz

AFCPN: If cleared to 0, the AFC block is powered down under the control of the PWRDN terminal. If this bit is set to 1, the power down is only controlled by bit AFCPD.

AFCPD: This bit is functionally associated and paired with bit AFCPN. When the AFCPN bit is 1, the AFC block is active. When the AFCPD bit is set to 1, the AFCPD block is in power-down mode.

ADCPN: If cleared to 0, the auxiliary ADC block is powered down when under the control of PWRDN.

If this bit is set to 1, the power down is only controlled by bit ADCPD.

ADCPD: This bit is functionally associated and paired with bit ADCPN. When the ADCPN bit is set to 1, an auxiliary ADC is active. When the ADCPD bit is set to 1, the auxiliary ADCPD is in power-down mode.

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PRINCIPLES OF OPERATION

automatic frequency control register (No. 1 and No. 2)

There are two AFC control registers; each is 10 bits wide. AFC control register No. 1 contains the least significant bit of the AFC D/A converter output. AFC control register No. 2 contains the most significant bit of the AFC D/A converter input. See Table 26 and 27. The AFC value is loaded after successive writes of AFC MSB and AFC LSB.

Table 26. AFC Control Register 1

AUXAFC1: AUTOMATIC FREQUENCY CONTROL REG1										ADDRESS: 14	R/W
BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	0 1 1 1 0	1/0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<–ACCESS TYPE	
0	0	0	0	0	0	0	0	0	0	<–VALUE AT RESET	

BIT9 to BIT0: LSB input of the 13-bit AFC D/A converter in 2's complement.

Table 27. AFC Control Register 2

AUXAFC2: AUTOMATIC FREQUENCY CONTROL REG2										ADDRESS: 15	R/W
RESREVD	RESREVD	RESREVD	RESREVD	RESREVD	RESREVD	RESREVD	BIT12	BIT11	BIT10	0 1 1 1 1	1/0
R = 0	R = 0	R = 0	R = 0	R = 0	R = 0	R = 0	R/W	R/W	R/W	<–ACCESS TYPE	
0	0	0	0	0	0	0	0	0	0	<–VALUE AT RESET	

BIT12 to BIT10: MSB Input of the 13-bit AFC D/A converter in 2's complement.

automatic power control register

The values in the automatic power control (APC) register set the operating conditions for the APC circuit, see Table 28.

Table 28. APC Register

AUXAPC: AUTOMATIC POWER CONTROL REGISTER										ADDRESS: 16	R/W
RESERVD	RESERVD	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	1 0 0 0 0	1/0
R = 0	R = 0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<–ACCESS TYPE	
0	0	0	0	0	0	0	0	0	0	<–VALUE AT RESET	

BIT7 to BIT0: Input of the 8-bit level APC DAC.

RESERVD: Reserved bits for testing

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automatic frequency control register (No. 1 and No. 2) (continued)

The content of the APC RAM describes the shape of the ramp-up and ramp-down control, see Table 29.

Table 29. APC Ramp Control

APCRAM: AUTOMATIC POWER CONTROL RAM										ADDRESS: 17 (64 Words)					W
RDWN WORD0 (5 BIT)					RUP WORD0 (5 BIT)					1	0	0	0	1	0
RDWNWORD1 (5BIT)					RUP WORD 21(5 BIT)					1	0	0	0	1	0
///////					///////					//////	//////	//////	//////	//////	//////
///////					///////					//////	//////	//////	//////	//////	//////
RDWNWORD62 (5BIT)					RUP WORD 62 (5 BIT)					1	0	0	0	1	0
RDWNWORD63 (5BIT)					RUP WORD 63(5 BIT)					1	0	0	0	1	0
W	W	W	W	W	W	W	W	W	W	<——ACCESS TYPE					
X	X	X	X	X	X	X	X	X	X	<——VALUE AT RESET					

Actual shape values (5 bits long) are contained in the shape D/A converter input register as shown in Table 30.

Table 30. Shape DAC Input Register

APCSHAP: SHAPE DAC INPUT REGISTER										ADDRESS: 18					R/W
RESERVD	RESERVD	RESERVD	RESERVD	RESERVD	BIT4	BIT3	BIT2	BIT1	BIT0	1	0	0	1	0	1/0
R = 0	R = 0	R = 0	R = 0	R = 0	R/W	R/W	R/W	R/W	R/W	<–ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<–VALUE AT RESET					

BIT4 to BIT0: Input of the 5-bit APC DAC.

RESERVD: Reserved bits for testing

analog AGC control register

The AGC control register is 10-bits wide and controls operations of the analog AGC circuit as shown in Table 31.

Table 31. Analog AGC Gain Control Register

AUXAAGC: ANALOG AUTOMATIC GAIN CONTROL REGISTER										ADDRESS: 19					R/W
BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	1	0	0	1	1	1/0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<–ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<–VALUE AT RESET					

BIT9 to BIT0: Input of the 10-bit AAGC DAC.

RESERVD: Reserved bits testing

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auxiliary functions control register No. 2 (see Table 32)

The values in the auxiliary function control register No. 2 set the operation parameters as decribed below:

AFCZ: Selection of internal resistance of AFC driver. When AFCZ is 1, the resistance is 50 kΩ. When AFZ is 0, the resistance is 25 kOhm. The largest swing is obtained with 50 kΩ.

APCSCD: When cleared to 0, the APC clock is at 4 MHz; when set to 1, the APC clock is at 2 MHz.

AGCSWG: Selection of the swing of the AAGC output: 0 corresponds to a 0 V to 1.1 V swing; 1 corresponds to 0 V to 3.3 V swing

APCSWG: Selection of the swing of the APC output: 0 corresponds to a 0-V to 3-V swing; 1 corresponds to 0-V to 5-V swing

IAPCPTR: Setting to 1 initializes the pointer of the APC RAM to the base address.

AAGCW: If cleared to 0, the automatic gain control path is powered down with the control of GSM receive window (BDLON terminal) and AAGCPD bit. If the AAGCPD bit is set to 1, the power down is controlled by AAGCPD bit.

AAGCPD: This bit is functionally associated with AAGCW bit. When this bit is set to 1, the automatic gain control path is in power-down mode.

APCW: If 0, the RF Power Control path is down powered with the control of GSM transmit window (BULON) and with the control of APCPD bit. If the APCPD bit is set to 1, power down is only controlled by APCPD bit.

APCPD: This bit is functionally associated with BBULW bit. When this bit is set to 1, the RF power control path is in power-down mode.

Table 32. AUX Functions Control Register No. 2

AUXCTL2: AUXILIARY FUNCTIONS CONTROL REGISTER										ADDRESS: 20					R/W
AGCW	AGCPD	APCW	APCPD3	IAPCTR	RESERVD	APCSWG	AGCSWG	APCSPD	AFCZ	1	0	1	0	0	1/0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<–ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<–VALUE AT RESET					

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auxiliary A/D converter output register

This register is read-only, but when there is an attempt to write into it, A/D conversion starts see Table 33. When the A/D conversion is finished, the AUXADC register is loaded and the A/D converter is automatically down powered. During the conversion process the ADCEOC bit of the BSTATUS register is set. This bit is reset automatically after AUXADC is loaded.

Table 33. AUX A/D Converter Output Register

AUXADC: AUXILIARY A/D CONVERTER OUTPUT REGISTER										ADDRESS: 21					R
BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	1	0	1	0	1	1/0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<–ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<–VALUE AT RESET					

BIT9 to BIT0: Output of the 10-bit monitoring ADC.

baseband status register

The baseband status register stores the baseband status as decribed in Table 34.

Table 34. Baseband Status Register

BSTATUS: BASEBAND STATUS REGISTER										ADDRESS: 22					R
RESERVD	ADCEOC	RAMPTR	BUFPTR	ULON	ULCAL	ULX	DLON	DLCAL	DLR	1	0	1	1	0	1
R = 0	R	R	R	R	R	R	R	R	R	<–ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<–VALUE AT RESET					

DLR: This bit is set to 1 during conversion of a burst in the downlink path.

DLCAL: This bit is set to 1 during offset calibration of the downlink path.

DLON: When is set to 1, it indicates that the downlink path is in powered on.

ULX: This bit is set to 1 during transmission of the burst in the uplink path.

ULCAL: This bit is set to 1 during offset calibration of the uplink path.

ULON: When set to 1, it indicates that the uplink path is in powered on.

BUFPTR: When set to 1, it indicates that the pointer of the burst buffer is at address zero.

RAMPTR: When set to 1, it indicates that the pointer of the APC RAM is at address zero.

ADCEOC: (ADC–end of conversion) when this bit is set to 1, an ADC conversion is in process.

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voiceband control register 4 (address 23)

Voiceband control register 4 (VBCTL4) is a read/write register (see Table 35) and contains the four programming bits of of VDLST as shown in Table 36.

Table 35. Voiceband Control Register 4

VBCTL4: VOICEBAND CONTROL REGISTER 4										ADDRESS: 23					R/W
RESERVD	RESERVD	RESERVD	RESERVD	RESERVD	RESERVD	VDLST3	VDLST2	VDLST1	VDLST0	1	0	1	1	1	1/0
R=0	R=0	R=0	R=0	R=0	R=0	R/W	R/W	R/W	R/W	<–ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<–VALUE AT RESET					

Table 36. VDLST Status

VDLST3	VDLST2	VDLST1	VDLST0	SIDE TONE GAIN
1	0	0	0	Mute
0	1	1	0	–17 dB
0	0	1	0	–14 dB
0	1	1	1	–11 dB
0	0	1	1	–8 dB
0	0	0	0	–5 dB (nominal)
0	1	0	0	–2 dB
0	0	0	1	+1 dB
0	1	0	1	+1 dB

baseband uplink register (address 24)

The baseband uplink register (BULCTL) is a 3-bit register (see Table 37) that permits mismatch compensation in the RF transmit mixer. Gain mismatches of 0 dB, –0.25 dB, –0.5 dB, and –0.25 dB are permitted between the I and Q channel as shown in Table 38.

Table 37. Uplink Register BULCTL

BULCTL: BASEBAND UPLINK CONTROL REGISTER										ADDRESS: 24					R/W
RESERVD	RESERVD	RESERVD	RESERVD	RESERVD	RESERVD	RESERVD	IQSEL	G1	G0	1	1	0	0	0	1/0
R=0	R=0	R=0	R=0	R=0	R=0	R=0	R/W	R/W	R/W	<–ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<–VALUE AT RESET					

Table 38. BLKCTL Register

BIT2	BIT1	BIT0	GAIN I	GAIN Q
IQSEL	G1	G0		
0	0	0	0 dB	0 dB
0	0	1	–0.25 dB	0 dB
0	1	0	–0.50 dB	0 dB
0	1	1	–0.75 dB	0 dB
1	0	0	0 dB	0 dB
1	0	1	0 dB	– 0.25 dB
1	1	0	0 dB	–0.50 dB
1	1	1	0 dB	–0.75 dB

PRINCIPLES OF OPERATION

timing and interface

Accurate timing control of baseband uplink and downlink paths is performed using the timing serial interface. The timing interface is a parallel asynchronous port with four control signals, refer to Figure 15. The BDLON bit controls power on the downlink path of the baseband codec; the BULON bit controls power on the uplink path of the baseband codec, and the BCAL bit controls the calibration of the active parts of the baseband codec selected by BULON or BDLON.

The BENA bit controls the transmission of the reception of burst depending on which part of the baseband codec is selected by the signals BULON or BDLON. These asynchronous inputs are internally synchronized with the uplink and downlink internal clocks and stored in timing register TR. The timing register, TR, is a 6-bit register containing the bits defined in Table 39.

Table 39. 6-Bit TR Register

BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
ULON	ULCAL	ULSEND	DLON	DLCAL	DLREC

TR bit signification

ULON: If set to 1, this bit turns on the uplink path of the baseband codec; if cleared to 0, the uplink path is in power-down mode.

ULCAL: When this bit is set to 1, the uplink offset autocalibration is active.

ULSEND: A transition from 0 to 1 of ULSEND initiates the emission of a burst. The burst informations data, burst length, and power level need to be loaded in the corresponding registers using the serial interface.

DLON: If set at 1, this bit turns on the downlink path of the baseband codec; if cleared to 0, the downlink path is in power-down mode.

DLCAL: When this bit is set at 1, the downlink offset autocalibration is active.

DLREC: A transition from 0 to 1 of DLREC initiates the transmission of data from the baseband codec to the DSP using the serial interface.

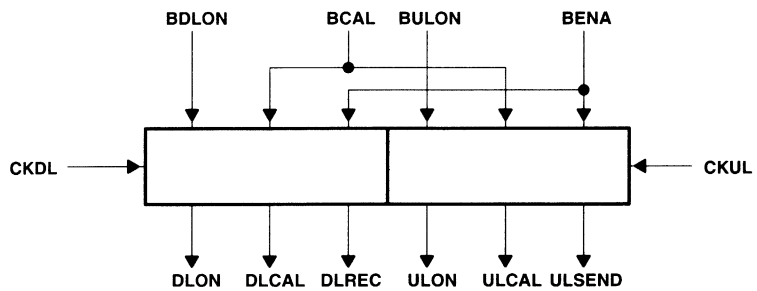

Figure 15. Timing Interface

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9 Digital Signal Processors

- High-Performance Static CMOS Technology
- Includes the T320C2xLP Core CPU
- 16-Bit Timer
- Instruction Cycle Time

'C203	'C209
50 ns @ 5 V	50 ns @ 5 V
35 ns @ 5 V	35 ns @ 5 V
25 ns @ 5 V	
35 ns @ 3 V	
50 ns @ 3 V	

- Source Compatible With TMS320C25
- Upwardly Compatible to TMS320C5x Devices
- TMS320C203 100-Pin PZ Package
- TMS320C209 80-Pin PN Package
- Three external Interrupts
- Boot-Loader Option ('C203 Only)
- TMS320C2xx Integrated Memory:
  - 544 × 16 Words of On-Chip Dual Access Data RAM ('C2xx)
  - 4K × 16 Words of On-Chip Single Access Program/Data RAM ('C209 Only)
  - 4K × 16 Words of On-Chip Program ROM ('C209 Only)
- 224K × 16-Bit Maximum Addressable External Memory Space (64K Program, 64K Data, 64K I/O, and 32K Global)
- 32-Bit ALU/Accumulator
- 16 × 16-Bit Multiplier With a 32-Bit Product
- Block Moves for Data, Program, I/O Port Space
- TMS320C2xx Peripherals:
  - On-Chip 16-Bit Timer
  - 1 Wait State Software Programmable to Each Space ('C209 Only)
  - 0 – 7 Wait States Software Programmable to Each Space ('C203 Only)
  - On-Chip Oscillator
  - One Synchronous Serial Port With Four Level Deep FIFOs ('C203 Only)
  - Full-Duplex Asynchronous Serial Port (UART) ('C203 Only)
- Input Clock Options:
  - ×1, ×2, ×4, ÷2 ('C203)
  - ×2 ÷2 ('C209)
- Support of Hardware Wait States
- Power Down IDLE Mode
- Scan-Based Emulation
- 1.1 mA/MIPS at 3 V

ADVANCE INFORMATION

description

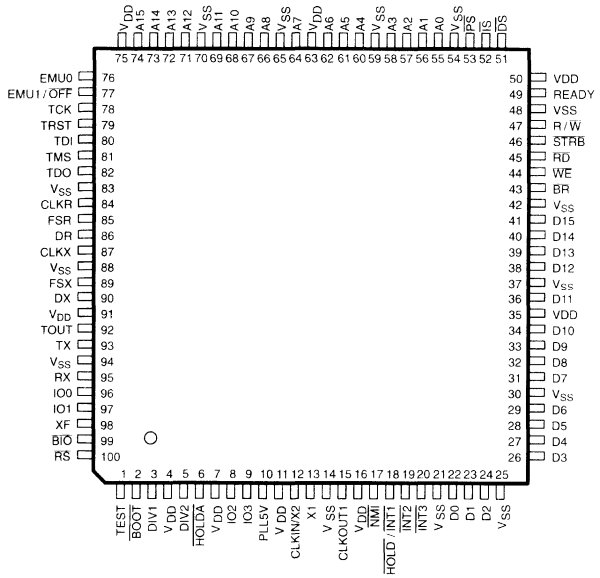
The TMS320C2xx generation of Texas Instruments TMS320 digital signal processors (DSPs) is fabricated with static CMOS integrated circuit technology, and their architectural design is based upon that of the TMS320C5x series, optimized for low power operation (see Table 1).The combination of advanced Harvard architecture, on-chip peripherals, on-chip memory, and a highly specialized instruction set is the basis of the operational flexibility and speed of the 'C2xx devices.

The TMS320C203 is packaged in a 100-pin PZ package while the TMS320C209 is packaged in an 80-pin PN package.

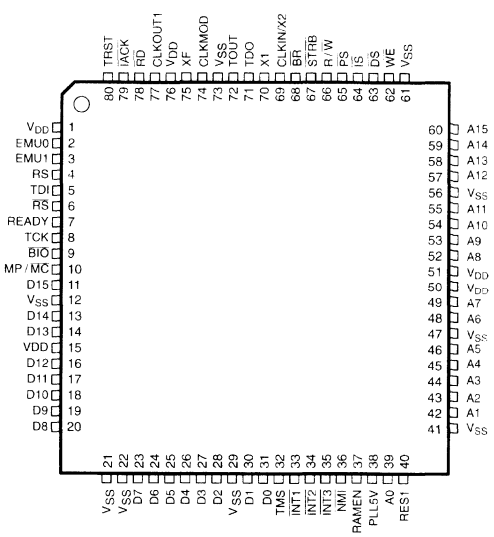
The 'C2xx generation offers these advantages:

- Enhanced TMS320 architectural design for increased performance and versatility
- Advanced integrated-circuit processing technology for increased performance
- Source code for the 'C2xx DSPs is software-compatible with the 'C1x and 'C2x DSPs and is upwardly compatible with fifth-generation DSPs ('C5x)
- New static-design techniques for minimizing power consumption and increasing radiation tolerance

PZ PACKAGE
(TOP VIEW)



PN PACKAGE
(TOP VIEW)



description (continued)

Table 2 provides a comparison of the devices in the 'C2xx generation. It shows the capacity of on-chip RAM and ROM memories, number of serial and parallel I/O ports, execution time of one machine cycle, and type of package with total pin count.

Table 1. Low Power Dissipation

POWER	TMS320C203	TMS320C209
3 V	1.1 ma/MIPS	N/A
5 V	1.9 ma/MIPS	1.9 ma/MIPS

Table 2. Characteristics of the TMS320C2xx Processors

TMS320C2XX DEVICES	ON-CHIP MEMORY			I/O PORTS		POWER SUPPLY (V)	CYCLE TIME (NS)	PACKAGE TYPE PIN COUNT
	RAM		ROM					
	DATA	DATA/ PROG	PROG	SERIAL	PARALLEL			
TMS320C203	288	256	0	2	64K	3/5	50/35/25	PZ 100-PIN
TMS320C209	288	4K + 256	4K	0	64K	5	50/35	PN 80-PIN

ADVANCE INFORMATION

TMS320C203 Interface Signals

PIN NAME	PIN NO.	I/O/Z†	DESCRIPTION
DATA AND ADDRESS BUSES			
D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	41 40 39 38 36 34 33 32 31 29 28 27 26 24 23 22	I/O/Z	Parallel data bus D15(MSB) through D0 (LSB). Multiplexed to transfer data between the TMS320C2xx and external data/program memory or I/O devices. Placed in the high-impedance state when not outputting (R/$\overline{W}$ high) or $\overline{RS}$ when asserted. They go into the high-impedance state when $\overline{OFF}$ is active low.
A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	74 73 72 71 69 68 67 66 64 62 61 60 58 57 56 55	O/Z	Parallel data bus A15(MSB) through A0 (LSB). Multiplexed to address external data/program memory or I/O devices. These signals go into the high-impedance state when $\overline{OFF}$ is active low.
MEMORY CONTROL SIGNALS			
$\overline{PS}$	53	O/Z	Program select signal. $\overline{PS}$ is always high unless low level asserted for communicating to off-chip program space. PS goes into the high-impedance state when $\overline{OFF}$ is active low.
$\overline{DS}$	51	O/Z	Data select signal. $\overline{DS}$ is always high unless low level asserted for communicating to off-chip program space. $\overline{DS}$ goes into the high-impedance state when $\overline{OFF}$ is active low.
$\overline{IS}$	52	O/Z	I/O space select signal. $\overline{IS}$ is always high unless low level asserted for communicating to input/output ports. $\overline{IS}$ goes into the high-impedance state when $\overline{OFF}$ is active low.
READY	49	I	Data ready input. READY indicates that an external device is prepared for the bus transaction to be completed. If the device is not ready (READY low), the TMS320C203 waits one cycle and checks READY again. If READY is not used it should be pulled high.
R/$\overline{W}$	47	O/Z	Read/write signal. R/$\overline{W}$ indicates transfer direction when communicating to an external device. Normally in read mode (high), unless low level is asserted for performing a write operation. R/$\overline{W}$ goes into the high-impedance state when $\overline{OFF}$ is active low.
$\overline{RD}$	45	O/Z	Read select indicates an active, external read cycle and can connect directly to the output enable ($\overline{OE}$) of external devices. $\overline{RD}$ is active on all external program, data, and I/O reads. $\overline{RD}$ goes into the high-impedance state when $\overline{OFF}$ is active low.
$\overline{WE}$	44	O/Z	Write enable. The falling edge of $\overline{WE}$ indicates that the device is driving the external data bus (D15–D0). Data can be latched by an external device on the rising edge of $\overline{WE}$. $\overline{WE}$ is active on all external program, data, and I/O writes. $\overline{WE}$ goes into the high-impedance state when $\overline{OFF}$ is active low.

† I = input, O = output, Z =high impedance

ADVANCE INFORMATION

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TMS320C203 Interface Signals (Continued)

PIN NAME	PIN NO.	I/O/Z†	DESCRIPTION
			MEMORY CONTROL SIGNALS (CONTINUED)
$\overline{STRB}$	46	O/Z	Strobe signal. $\overline{STRB}$ is always high unless asserted low to indicate an external bus cycle. $\overline{STRB}$ goes into the high-impedance state when $\overline{OFF}$ is active low.
			MULTI-PROCESSING SIGNALS
$\overline{BR}$	43	O/Z	Bus request signal. $\overline{BR}$ is asserted when a global data memory access is initiated. $\overline{BR}$ goes into the high-impedance state when $\overline{OFF}$ is active low.
$\overline{HOLDA}$	6	O/Z	Hold acknowledge signal. $\overline{HOLDA}$ indicates to the external circuitry that the processor is in a hold state and that the address, data, and memory control lines are in the high-impedance state so that they are available to the external circuitry for access of local memory. $\overline{HOLDA}$ goes into the high-impedance state when $\overline{OFF}$ is active low.
XF	98	O/Z	External flag output (latched software-programmable signal). XF is used for signalling other processors in multiprocessing configurations or as a general-purpose output pin. XF goes into the high-impedance state when $\overline{OFF}$ is active low.
$\overline{BIO}$	99	I	Branch control input. When polled by BIOZ instruction, if $\overline{BIO}$ is low, the TMS320C203 executes a branch. If $\overline{BIO}$ is not used it should be pulled high.
IO0 IO1 IO2 IO3	96 97 8 9	I/O/Z	Software controlled Input/output pins via the asynchronous serial port register (ASPCR). At reset these pins are configured as inputs. These can be used as general purpose input/output pins or as handshake control for the UART. IO0–IO3 go into the high-impedance state when $\overline{OFF}$ is active low.
			INITIALIZATION, INTERRUPTS, AND RESET OPERATIONS
$\overline{RS}$	100	I	Reset input. $\overline{RS}$ causes the TMS320C203 to terminate execution and forces the program counter to zero. When $\overline{RS}$ is brought high, execution begins at location 0 of program memory after 16 cycles. $\overline{RS}$ affects various registers and status bits.
TEST	1	I	Reserved input pin. Do not connect to this pin.
$\overline{BOOT}$	2	I	Microprocessor mode select pin. When $\overline{BOOT}$ is high the device accesses off-chip memory. If $\overline{BOOT}$ is low, the on-chip bootloader transfers data from external global data space to external RAM program space.
$\overline{NMI}$	17	I	Nonmaskable interrupt. $\overline{NMI}$ is an external interrupt that cannot be masked via the INTM or the IMR. When $\overline{NMI}$ is activated, the processor traps to the appropriate vector location. If $\overline{NMI}$ is not used, it should be pulled high.
$\overline{HOLD}$/$\overline{INT1}$ $\overline{INT2}$ $\overline{INT3}$	18 19 20	I	External user interrupts. Prioritized and maskable by the interrupt mask register (IMR) and the interrupt mode bit (INTM). Can be polled and reset via the interrupt flag register (IFR). If these signals are not used, they should be pulled high. $\overline{INT1}$/$\overline{HOLD}$ can select a hold mode where the address, data, and control lines are 3-stated. $\overline{HOLD}$ has priority over $\overline{INT1}$ at reset.
			OSCILLATOR, PLL, AND TIMER SIGNALS
TOUT	92	O	Timer output. TOUT signals a pulse when the on-chip timer counts down past zero. The pulse is a CLKOUT1 cycle wide. TOUT goes into the high-impedance state when $\overline{OFF}$ is active low.
CLKOUT1	15	O/Z	Master clock ouput signal. The CLKOUT1 high pulse signifies the logic phase while the low pulse signifies the latch phase.
CLKIN/X2 X1	12 13	I O	Input clock. CLKIN/X2 is the input clock to the device. X1 is either multiplied and phase-locked using the PLL operation or can bypass the PLL and operate in a divide-by-two mode. As X2, the pin operates as the oscillator input with X1 being the oscillator output.
DIV1 DIV2	3 5	I	DIV1 and DIV2 provide clock mode inputs. DIV1–DIV2 should not be changed unless the $\overline{RS}$ signal is active.

† I = input, O = output, Z =high impedance

TMS320C203 Interface Signals (Continued)

PIN NAME	PIN NO.	I/O/Z†	DESCRIPTION
OSCILLATOR, PLL, AND TIMER SIGNALS (CONTINUED)			
PLL5V	10	I	PLL operating at 5 V. When the device is operated at 5 V, PLL5V should be strapped high. When operating at 3 V, PLL5V should be strapped low.
SERIAL PORT AND UART SIGNALS			
CLKX	87	I/O	Transmit clock. CLKX is a clock signal for clocking data from the DX (data receive register) to the DX pin data transmit pin. The CLKX can be an input if the MCM bit in the SSPCR is set to 0. CLKX can also be driven by the device at one-half of the CLKOUT1 frequency when MCM = 1. If the serial port is not being used, CLKX can be sampled as an I/O pin via the IN1 bit of the SSPCR register. CLKX goes into the high-impedance state when OFF is active low. Value at reset is as an input.
CLKR	84	I	Receive clock input. External clock signal for clocking data from the DR (data receive) pin into the RSR (serial port shift register). CLKR must be present during serial port transfers. If the serial port is not being used, CLKR can be sampled as an input via the IN0 bit of the SSPCR.
FSR	85	I	Frame synchronization pulse for receive input. The falling edge of the FSR pulse initiates the data receive process beginning the clocking of the RSR. FSR goes into the high-impedance state when OFF is active low.
FSX	89	I/O	Frame synchronization pulse for transmit input/ouput. The falling edge of the FSR pulse initiates the data-transmit process beginning the clocking of the RSR. Following reset, FSX is an input. FSX can be selected by software to be an output when the TXM bit in the serial control registers, SSPCR is set to 1. FSX goes into the high-impedance state when OFF is active low.
DR	86	I	Serial data receive input. Serial data is received in the receive shift register (RSR) via DR.
DX	90	O	Serial port transmit output. Serial data transmitted from the transmit shift register (XSR) via DX. Placed in the high-impedance state when not transmitting and also when OFF is active low.
TX	93	O	Asynchronous transmit pin.
RX	95	I	Asynchronous receive pin.
TEST SIGNALS			
TRST	79	I	JTAG test reset. TRST, when active high, gives the JTAG-scan system control of the operations of the device. If TRST is not connected or driven low, the device operates in its functional mode, and the JTAG signals are ignored.
TCK	78	I	JTAG test clock. TCK is normally a free-running clock signal with a 50% duty cycle. The changes on TAP (test access port) input signals (TMS and TDI) are clocked into the TAP controller, instruction register, or selected test data register on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK.
TMS	81	I	JTAG test mode select. TMS is clocked into the TAP controller on the rising edge of TCK.
TDI	80	I	JTAG test data input. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO	82	O/Z	JTAG test data output. The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance state except when scanning of data is in progress.
EMU0	76	I/O/Z	Emulator pin 0. When $\overline{\text{TRST}}$ is driven low, this pin must be high for activation of the $\overline{\text{OFF}}$ condition. When $\overline{\text{TRST}}$ is driven high, this pin is used as an interrupt to or from the emulator system and is defined an input/output via JTAG scan.
EMU1/$\overline{\text{OFF}}$	77	I/O/Z	Emulator pin 1. Emulator pin 1 disables all outputs. When $\overline{\text{TRST}}$ is driven high, EMU1/$\overline{\text{OFF}}$ is used as an interrupt to or from the emulator system and is defined as input/output via JTAG scan. When $\overline{\text{TRST}}$ is driven low, this pin is configured as $\overline{\text{OFF}}$. EMU1/$\overline{\text{OFF}}$, when active low, puts all output drivers in the high-impedance state. Note that $\overline{\text{OFF}}$ is used exclusively for testing and emulation purposes (not for multiprocessing applications). Thus, for $\overline{\text{OFF}}$ condition, the following apply: $\overline{\text{TRST}}$ = 0 EMU0 = 1 EMU/$\overline{\text{OFF}}$ = 0

† I = input, O = output, Z =high impedance

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TMS320C203 Interface Signals (Continued)

PIN NAME	PIN NO.	I/O/Z†	DESCRIPTION
SUPPLY PINS			
V_{DD}	4 7 11 16 35 50 63 75 91	PWR	Power.
V_{SS}	14 21 25 30 37 42 48 54 59 65 70 83 88 94	GND	Ground.

† I = input, O = output, Z =high impedance

TMS320C209 Pin Functions

PIN NAME	PIN NO.	I/O/Z†	DESCRIPTION
			ADDRESS AND DATA BUSES
D15	11	I/O/Z	Parallel data bus D15 (MSB) through D0 (LSB). D15–D0 are multiplexed to transfer data between the core CPU and external data/program memory or I/O devices. D15–D0 are placed in the high-impedance state when not outputting or when $\overline{RS}$ is asserted. They also go into the high-impedance state when $\overline{OFF}$ is active low. D15–D0 are also used in external DMA access of the on-chip single-access RAM.
D14	13		
D13	14		
D12	16		
D11	17		
D10	18		
D9	19		
D8	20		
D7	23		
D6	24		
D5	25		
D4	26		
D3	27		
D2	28		
D1	30		
D0	31		
A15	60	O/Z	Parallel address bus A15 (MSB) through A0 (LSB). A15–A0 are multiplexed to address external data/program memory or I/O. A15–A0 go into the high-impedance state when $\overline{OFF}$ is active low. A15–A0 are used as inputs for external DMA access of the on-chip single-access RAM.
A14	59		
A13	58		
A12	57		
A11	55		
A10	54		
A9	53		
A8	52		
A7	49		
A6	48		
A5	46		
A4	45		
A3	44		
A2	43		
A1	42		
A0	39		
			MEMORY CONTROL SIGNALS
$\overline{DS}$	63	O/Z	Data select signal. $\overline{DS}$ is always high unless low level asserted for communicating to off-chip program space. $\overline{DS}$ goes into the high-impedance state when $\overline{OFF}$ is active low.
$\overline{PS}$	65	O/Z	Program select signal. $\overline{PS}$ is always high unless low-level asserted for communicating to off-chip program space. $\overline{PS}$ goes into the high-impedance state when $\overline{OFF}$ is active low.
$\overline{IS}$	64	O/Z	I/O space select signal. $\overline{IS}$ is always high unless low level asserted for communicating to I/O ports. $\overline{IS}$ goes into the high-impedance state when $\overline{OFF}$ is active low.
READY	7	I	Data-ready input. READY indicates that an external device is prepared for the bus transaction to be completed. If READY is not (READY low), the TMS320C209 waits one cycle and checks READY again. If READY is not used it should be pulled high.
R/$\overline{W}$	66	O/Z	Read/write signal. R/$\overline{W}$ indicates transfer direction when communicating to an external device. Normally in read mode (high), unless low-level is asserted for performing a write operation. R/$\overline{W}$ goes into the high-impedance state when $\overline{OFF}$ is active low.
$\overline{STRB}$	67	O/Z	Strobe signal. $\overline{STRB}$ is always high unless asserted low to indicate an external bus cycle. $\overline{STRB}$ goes into the high-impedance state when $\overline{OFF}$ is active low.
$\overline{RD}$	78	O/Z	Read select. $\overline{RD}$ indicates an active, external read cycle and can connect directly to the output enable ($\overline{OE}$) of external devices. $\overline{RD}$ is active on all external program, data, and I/O reads. $\overline{RD}$ goes into the high-impedance state when $\overline{OFF}$ is active low.

† I = input, O = output, Z =high impedance

ADVANCE INFORMATION

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TMS320C209 Pin Functions (Continued)

PIN NAME	PIN NO.	I/O/Z†	DESCRIPTION
			MEMORY CONTROL SIGNALS (CONTINUED)
$\overline{WE}$	62	O/Z	Write enable. The falling edge of $\overline{WE}$ indicates that the device is driving the external data bus (D15–D0). Data can be latched by an external device on the rising edge of $\overline{WE}$. $\overline{WE}$ is active on all external program, data, and I/O writes. $\overline{WE}$ goes into the high-impedance state when $\overline{OFF}$ is active low.
RAMEN	37	I	RAM enable. RAMEN enables the 4K × 16 words of on-chip RAM.
			MULTIPROCESSING SIGNALS
$\overline{BR}$	68	O/Z	Bus request signal. $\overline{BR}$ is asserted during access of external global data memory space. $\overline{BR}$ can be used to extend the data memory address space by up to 32K words. $\overline{BR}$ goes into the high-impedance state when $\overline{OFF}$ is active low.
$\overline{BIO}$	9	I	Branch control input. $\overline{BIO}$ is polled by BIOZ instruction. If $\overline{BIO}$ is low, the TMS320C209 executes a branch. If $\overline{BIO}$ is not used, it should be pulled high.
XF	75	O/Z	External flag output (latched software-programmable signal). XF is used for signaling other processors in multiprocessing configurations or a general-purpose output pin.
$\overline{IACK}$	79	O/Z	Interrupt acknowledge signal. $\overline{IACK}$ indicates receipt of an interrupt and that the program counter is fetching the interrupt vector location designated by A15–A0. $\overline{IACK}$ also goes into the high-impedance state when $\overline{OFF}$ is active low.
			INITIALIZATION, INTERRUPT, AND RESET OPERATIONS
$\overline{INT1}$ $\overline{INT2}$ $\overline{INT3}$	33 34 35	I	External-user interrupts. $\overline{INT1}$–$\overline{INT3}$ are prioritized and maskable by the interrupt-mask register and the interrupt-mode bit. If $\overline{INT1}$–$\overline{INT3}$ are not used they should be pulled high.
$\overline{NMI}$	36	I	Nonmaskable interrupt. $\overline{NMI}$ is an external interrupt that cannot be masked via the INTM or the IMR. When $\overline{NMI}$ is activated, the processor traps to the appropriate vector location. If $\overline{NMI}$ is not used, it should be pulled high.
RS $\overline{RS}$	4 6	I	Reset input. $\overline{RS}$ and RS cause the TMS320C209 to terminate execution and force the program counter to 0. When $\overline{RS}$ is brought high, execution begins at location 0 of program memory after 16 cycles. $\overline{RS}$ affects various registers and status bits.
MP/$\overline{MC}$	10	I	Microprocessor/microcontroller mode-select pin. If MP/$\overline{MC}$ is low, the on-chip ROM is mapped into program space. When MP/$\overline{MC}$ is high, the device accesses off-chip memory.
			OSCILLATOR/TIMER SIGNALS CLKIN1/2
CLKOUT1	77	O/Z	Master clock output signal. CLKOUT1 cycles at the machine-cycle rate of the CPU. The internal machine cycle is bounded by the rising edges of CLKOUT1. CLKOUT1 goes into the high-impedance state when $\overline{OFF}$ is active low.
CLKMOD	74	I	Clock input mode. CLKMOD (when high) enables the clock doubler and phase lock loop on the clock input signal. If the internal oscillator is not used, X1 should be left unconnected.
CLKIN/X2 X1	69 70	I	Clock input. The clock input to CLKIN/X2 operates at half of the internal machine rate if the phase lock loop (PLL) is enabled (CLKMOD high), or twice the internal machine rate if the PLL is disabled. As X2, the pin operates as the oscillator input with X1 being the oscillator output.
TOUT	72	O	Timer output. TOUT signals a pulse when the on-chip timer counts down past zero. The pulse is a CLKOUT1 cycle wide.
PLL5V	38	I	PLL operating at 5 V. When PLL5V is operated at 5 V, PLL5V should be strapped high.
RES1	40	I	Reserved input pin. Do not connect to RES1.

† I = input, O = output, Z =high impedance

TMS320C209 Pin Functions (Continued)

PIN NAME	PIN NO.	I/O/Z†	DESCRIPTION
			TEST SIGNALS
TCK	8	I	JTAG test clock. TCK is normally a free-running clock signal with a 50% duty cycle. The changes on TAP (test access port) input signals (TMS and TDI) are clocked into the TAP controller, instruction register, or selected test-data register on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK.
TDI	5	I	JTAG test data input. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO	71	O/Z	JTAG test data output. The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance state except when scanning of data is in progress. TDO goes into the high-impedance state when $\overline{OFF}$ is active low.
TMS	32	I	JTAG test mode select. TMS is clocked into the TAP controller on the rising edge of TCK.
TRST	80	I	JTAG test reset. TRST, when active high, gives the JTAG scan system control of the operations of the device. If TRST is not connected or driven low, the device operates in its functional mode, and the JTAG signals are ignored.
EMU0 EMU1	2 3	I/O/Z	Emulator pin 0. When $\overline{TRST}$ is driven low, this pin must be high for activation of the $\overline{OFF}$ condition. When $\overline{TRST}$ is driven high, this pin is used as an interrupt to or from the emulator system and is defined an input/output via JTAG scan. Emulator pin 1. Emulator pin 1 disables all outputs. When $\overline{TRST}$ is driven high, EMU1/$\overline{OFF}$ is used as an interrupt to or from the emulator system and is defined as input/output via JTAG scan. When $\overline{TRST}$ is driven low, this pin is configured as $\overline{OFF}$. EMU1/$\overline{OFF}$, when active low, puts all output drivers in the high-impedance state
			SUPPLY PINS
V_{DD}	1 15 50 51 76	PWR	Power.
V_{SS}	12 21 22 29 41 47 56 61 73	PWR	Ground.

† I = input, O = output, Z =high impedance

ADVANCE INFORMATION

functional block diagram of 'C2xx internal hardware

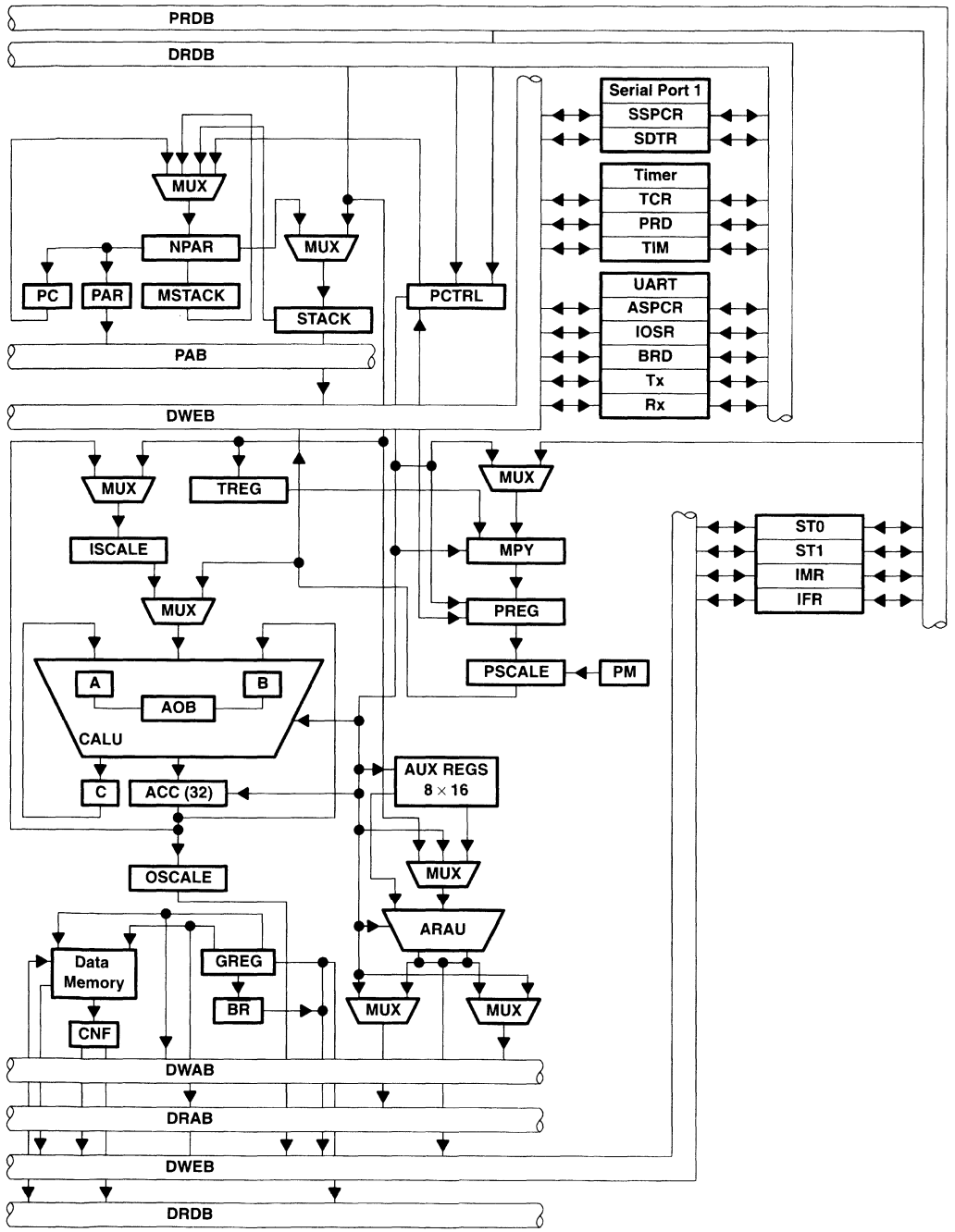

Table 3. Legend for C2xx Block Diagram

SYMBOL	NAME	DESCRIPTION
A	A Input	A input of the two operand CALU. A feeds ACC back to the CALU operations.
AOB	CALU Operation	Identifies the operation of A to B in the CALU. The O can be an arithmetic or logical operation as defined by the operator selection for the current instruction.
ACC	Accumulator	32-bit register that stores the results and provides input for subsequent CALU operations. Also includes shift and rotate capabilities.
ARAU	Auxiliary Register Arithmetic Unit	An unsigned, 16-bit arithmetic unit used to calculate indirect addresses using the auxiliary registers as inputs and outputs.
AUX REGS	Auxiliary Register 0–7	These 16-bit registers are used as pointers to anywhere within the data space address range. They are operated upon by the ARAU and are selected by the ARP, auxiliary register pointer. AR0 can also be used as an index value for AR updates of more than one and as a compare value to AR(ARP).
B	B Input	B input of the two operand CALU. B feeds the 32-bit input (from ISCALE or PSCALE) to the CALU operations.
$\overline{BR}$	Bus Register Signal	$\overline{BR}$ is asserted during access of the external global data memory space. READY is asserted to the device when the global data memory is available for the bus transaction. $\overline{BR}$ can be used to extend the data memory address space by up to 32K words.
C	Carry	Register carry output from CALU. C is feed back into the CALU for extended arithmetic operation. The C bit resides in ST1, status register 1 and can be tested in conditional instructions. C is also used in accumulator shifts and rotates.
CALU	Central Arithmetic Logic Unit	32-bit wide main arithmetic logic unit for the TMS320C2xx core. The CALU executes 32-bit operations in a single machine cycle. CALU operates on data coming from ISCALE or PSCALE with data from ACC and provides status results to PCTRL.
CNF	On-Chip RAM Configuration Control Bit	If set to 0, the reconfigurable data dual-access RAM blocks are mapped to data space; otherwise, they are mapped to program space.
DRAB	Data Read Address Bus	16-bit bus that provides the address for data read operations. DRAB is driven by the TMS320C2xx core.
DRDB	Data-Read Bus	16-bit bus for data-space read data. DRDB is driven by memories or the logic interface.
DWAB	Data-Write Bus	16-bit bus that provides the address for data-write operations. DWAB is driven by the TMS320C2xx core.
DWEB	Data-Write Bus	16-bit bus for data-space write data. DWEB is driven by the TMS320C2xx core.
GREG	Global Memory Allocation Register	GREG specifies the size of the global data memory space.
IMR	Interrupt Mask Register	IMR individually masks or enables the seven interrupts.
IFR	Interrupt Flag Register	The 7-bit IFR indicates that the TMS320C2xx has latched an interrupt from one of the seven maskable interrupts.
INTM	Interrupt Mode Bit	When set to 0, all unmasked interrupts are enabled. When set to 1, all maskable interrupts are disabled.
INT#	Interrupt Traps	A total of 32 interrupts via hardware and/or software are available.
ISCALE	Input Data-Scaling Shifter	16 to 32-bit barrel left shifter. ISCALE shifts incoming 16-bit data 0 to16 positions left relative to the 32-bit output within the fetch cycle therefore not cycle overhead required for input scaling operations.
MPY	Multiplier	16 × 16-bit Multiplier to a 32-bit product. MPY executes multiplication in a single cycle. Operates either signed or unsigned 2s complement arithmetic multiply.
MSTACK	Micro Stack	MSTACK provides temporary storage for the address of the next instruction to be fetched when program address-generation logic is used to generate sequential addresses in data space.
MUX	Multiplexer	Multiplexes buses to a common input.
NPAR	Next Program Address	NPAR holds the program address to be driven out PAB on the next cycle.

Table 3. Legend for C2xx Block Diagram (Continued)

SYMBOL	NAME	DESCRIPTION
OSCALE	Output Data-Scaling Shifter	32 to 16-bit barrel left shifter. OSCALE shifts the 32-bit accumulator output 0 to 7 bits left for quantization management and outputs either the 16-bit high or low half of the shifted 32-bit data to DWEB.
PAB	Program Address Bus	16-bit bus that provides the address for program space reads and writes. PAB is driven by the TMS320C2xx core.
PAR	Program Address	PAR holds the address currently being driven on PAB for as many cycles as it takes to complete all memory operations scheduled for the current machine cycle.
PC	Program Counter	Increments the value from NPAR to provide sequential addresses for instruction fetching and sequential data transfer operations.
PCTRL	Program Controller	PCTRL decodes instruction, manages the pipeline, stores status, and decodes conditional operations.
PM	Product Register Shift Mode Bit	These two bits identify which of the four shift modes (0, 1, 4, -6) will be used by PSCALE. PM resides in ST1.
PRDB	Program Read Data Bus	16-bit bus for program space read data. PRDB is driven by the memories or the logic interface.
PREG	Product Register	32-bit register holds results of 16 × 16 multiply.
PSCALE	Product-Scaling Shifter	0, 1 or 4-bit left shift or 6-bit right shift of multiplier product. The left shift options are used to manage the additional sign bits resulting from the 2s complement multiply. The right shift option is used to scale down the number to manage overflow of product accumulation in the CALU. PSCALE resides in the path from the 32-bit product shifter and either the CALU or the DWEB and requires no cycle overhead.
TREG	Temporary Register	16-bit register holds one of the operands for the multiply operations. TREG holds dynamic shift count for LACT, ADDT, and SUBT instructions. TREG holds dynamic bit position for BITT instruction.
SSPCR	Synchronous Serial Port Control Register	Control register for selecting the mode of operation of the serial port.
SDTR	Synchronous Serial Port Transmit and Receive Register	Data transmit and receive register.
TCR	Timer-Control Register	TCR contains the control bits that define the divide-down ratio, start/stop the timer, and reload the period. Also contained in TCR is the current count in the prescaler. Reset initializes the timer-divide-down ratio to 0 and starts the timer.
PRD	Timer-Period Register	PRD contains the 16-bit period that is loaded into the timer counter when the counter borrows or when the reload bit is activated. Reset initializes the PRD to 0xFFFF.
TIM	Timer-Counter Register	TIM contains the current 16-bit count of the timer. Reset initializes the TIM to 0xFFFF.
UART	Universal Asynchronous Receive Transmit	Asynchronous serial port.
ASPCR	Asynchronous Serial Port Control Register	ASPCR controls the asynchronous serial port operation.
IOSR	I/O Status Register	IOSR detects current levels (and changes with inputs) on pins IO0–IO3 and status of UART.
BRD	Baud Rate Divisor	Used to set the baud rate of the UART.

Table 3. Legend for C2xx Block Diagram (Continued)

SYMBOL	NAME	DESCRIPTION
ST0 ST1	Status Register	Contain the status of various conditions and modes. These registers can be stored into and loaded from data memory, thus allowing the status of the machine to be saved and restored.
IMR	Interrupt Mask Registers	IMR individually masks or enables the seven interrupts.
IFR	Interrupt Flag Register	IFR indicates that the T320C2xLP core has latched an interrupt pulse from one of the maskable interrupts.
STACK	Stack	A block of memory used for storing return addresses for subroutines and interrupt service routines, or for storing data. The 'C2xx stack is 16-bits wide and eight levels deep.

architectural overview

The 'C2xx advanced Harvard-type architecture maximizes the processing power by maintaining two separate memory bus structures, program and data, for full-speed execution. This multiple bus allows both reading data and instructions simultaneously. Instructions support data transfers between the two spaces. This architecture permits coefficients stored in program memory to be read in RAM, eliminating the need for a separate coefficient ROM. This, coupled with a four-deep pipeline, allows the TMS320C2xx to execute most instructions in a single cycle.

status and control registers

Two status registers, ST0 and ST1, contain the status of various conditions and modes. These registers can be stored into data memory and loaded from data memory, thus allowing the status of the machine to be saved and restored for subroutines.

The load status register (LST) instruction is used to write to ST0 and ST1. The store status register (SST) instruction is used to read from the ST0 and ST1 except the INTM bit which is not affected by the LST instruction). The individual bits of these registers can be set or cleared when using the SETC and CLRC instructions. Figure 1 shows the organization of status registers ST0 and ST1, indicating all status bits contained in each. Several bits in the status registers are reserved and read as logic 1s. Refer to Table 4 for status register field definitions.

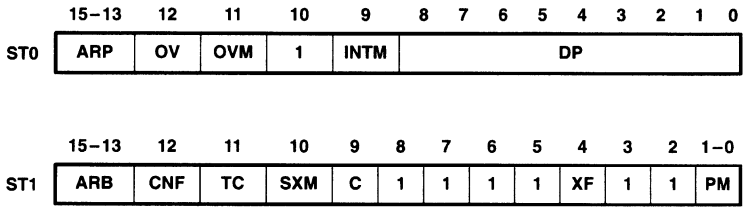

Figure 1. Status and Control Register Organization

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Table 4. Status Register Field Definitions

FIELD	FUNCTION
ARB	Auxiliary register pointer buffer. Whenever the ARP is loaded, the old ARP value is copied to the ARB except during an LST instruction. When the ARB is loaded via an LST #1 instruction, the same value is also copied to the ARP.
ARP	Auxiliary register pointer. ARP selects the AR to be used in indirect addressing. When the ARP is loaded, the old ARP value is copied to the ARB register. ARP can be modified by memory-reference instructions when using indirect addressing, and by the LARP, MAR, and LST instructions. The ARP is also loaded with the same value as ARB when an LST #1 instruction is executed.
C	Carry Bit. C is set to 1 if the result of an addition generates a carry, or reset to 0 if the result of a subtraction generates a borrow. Otherwise, C is reset after an addition or set after a subtraction, except if the instruction is ADD or SUB with a 16-bit shift. In these cases the ADD can only set and the SUB only reset the carry bit, but cannot affect it otherwise. The single bit shift and rotate instructions also affect C, as well as the SETC, CLRC, and LST #1 instructions. Branch instructions have been provided to branch on the status of C. C is set to 1 on a reset.
CNF	On-chip RAM configuration control bit. If CNF is set to 0, the re-configurable data dual access RAM blocks are mapped to data space; otherwise, they are mapped to program space. The CNF can be modified by the SETC CNF, CLRC CNF, and LST #1 instructions. $\overline{RS}$ sets the CNF to 0.
DP	Data memory page pointer. The 9-bit DP register is concatenated with the 7 LSBs of an instruction word to form a direct memory address of 16 bits. DP can be modified by the LST and LDP instructions.
INTM	Interrupt mode bit. When INTM is set to 0, all unmasked interrupts are enabled. When set to 1, all maskable interrupts are disabled. INTM is set and reset by the SETC INTM and CLRC INTM instructions. $\overline{RS}$ and $\overline{IACK}$ also set INTM. INTM has no effect on the unmaskable $\overline{RS}$ and $\overline{NMI}$ interrupts. Note that INTM is unaffected by the LST instruction. This bit is set to 1 by reset. It is also set to 1 when a maskable interrupt trap is taken.
OV	Overflow flag bit. As a latched overflow signal, OV is set to 1 when overflow occurs in the ALU. Once an overflow occurs, the OV remains set until a reset, BCND/D on OV/NOV, or LST instructions clear OV.
OVM	Overflow mode bit. When OVM is set to 0, overflowed results overflow normally in the accumulator. When set to 1, the accumulator is set to either its most positive or negative value upon encountering an overflow. The SETC and CLRC instructions set and reset this bit, respectively. LST may also be used to modify the OVM.
PM	Product shift mode. If these two bits are 00, the multiplier's 32-bit product is loaded into the ALU with no shift. If PM = 01, the PREG output is left-shifted one place and loaded into the ALU, with the LSB zero-filled. If PM = 10, PREG output is left-shifted by four bits and loaded into the ALU, with the LSB's zero-filled. PM = 11 produces a right shift of six bits, sign-extended. Note that the PREG contents remain unchanged. The shift takes place when transferring the contents of the PREG to the ALU. PM is loaded by the SPM and LST #1 instructions. PM is cleared by $\overline{RS}$.
SXM	Sign-extension mode bit. SXM = 1 produces sign extension on data as it is passed into the accumulator through the scaling shifter. SXM = 0 suppresses sign extension. SXM does not affect the definitions of certain instructions; e.g., the ADDS instruction suppresses sign extension regardless of SXM. SXM is set by the SETC SXM and reset by the CLRC SXM instructions, and can be loaded by the LST #1. SXM is set to 1 by reset.
TC	Test / control flag bit. TC is affected by the BIT, BITT, CMPR, LST #1, and NORM instructions. TC is set to a 1 if a bit tested by BIT or BITT is a 1, if a compare condition tested by CMPR exists between AR(ARP) and AR0, if the exclusive-OR function of the two MSBs of the accumulator is true when tested by a NORM instruction. The conditional branch, call, and return instructions can execute based on the condition of TC.
XF	XF pin status bit. XF indicates the state of the XF pin, a general-purpose output pin. XF is set by the SETC XF and reset by the CLRC XF instructions. XF is set to 1 by reset.

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central processing unit

The TMS320C2xx central processing unit (CPU) contains a 16-bit scaling shifter, a 16x16-bit parallel multiplier, a 32-bit arithmetic logic unit (CALU), a 32-bit accumulator, and additional shifters at the outputs of both the accumulator and the multiplier. This section describes the CPU components and their functions. The functional block diagram (page 10) shows the components of the CPU.

input scaling shifter

The TMS320C2xx provides a scaling shifter with a 16-bit input connected to the data bus and a 32-bit output connected to the CALU. This shifter operates as part of the path of data coming from program or data space to the CALU and requires no cycle overhead. It is used to align the 16-bit data coming from memory to the 32-bit CALU. This is necessary for scaling arithmetic as well as aligning masks for logical operations.

input scaling shifter (continued)

The scaling shifter produces a left shift of 0 to 16 on the input data. The LSBs of the output are filled with zeros; the MSBs may be either filled with zeros or sign-extended, depending upon the value of the SXM bit (sign-extension mode) of status register ST1. The shift count is specified by a constant embedded in the instruction word or by a value in TREG. The shift count in the instruction allows for specific scaling or alignment operations specific to that point in the code. The TREG base shift allows the scaling factor to be adaptable to the system's performance.

multiplier

The TMS320C2xx uses a 16x16-bit hardware multiplier that is capable of computing a signed or an unsigned 32-bit product in a single machine cycle. All multiply instructions, except the MPYU (multiply unsigned) instruction, perform a signed multiply operation. That is, two numbers being multiplied are treated as 2s-complement numbers, and the result is a 32-bit 2s-complement number. There are two registers associated with the multiplier:

- 16-bit temporary register (TREG) that holds one of the operands for the multiplier, and
- 32-bit product register (PREG) that holds the product.

Four product shift modes (PM) are available at the PREG's output (PSCALE). These shift modes are useful for performing multiply/accumulate operations, performing fractional arithmetic, or justifying fractional products. The PM field of status register ST1 specifies the PM shift mode, as shown in Table 5.

Table 5. PSCALE Product Shift Modes

PM	SHIFT	DESCRIPTION
00	no shift	Product feed to CALU or data bus with no shift.
01	left 1	Removes the extra sign bit generated in a 2s-complement multiply to produce a Q31 product.
10	left 4	Removes the extra 4 sign bits generated in a 16x13 2s-complement multiply to a produce a Q31 product when using the multiply by a 13-bit constant.
11	right 6	Scales the product to allow up to 128 product accumulation without the possibility of accumulator overflow.

The product can be shifted one bit to compensate for the extra sign bit gained in multiplying two 16-bit 2s-complement numbers (MPY). A four-bit shift is used in conjunction with the MPY instruction with a short immediate value (13 bits or less) to eliminate the four extra sign bits gained in multiplying a 16-bit number by a 13-bit number. Finally, the output of PREG can be right-shifted 6 bits to enable the execution of up to 128 consecutive multiply/accumulates without the possibility of overflow.

The LT (load TREG) instruction normally loads TREG to provide one operand (from the data bus), and the MPY (multiply) instruction provides the section operand (also from the data bus). A multiplication can also be performed with a 13-bit immediate operand when using the MPY instruction. A product is then obtained every two cycles. When the code is executing multiple multiplies and product sums, the CPU supports the pipelining of the TREG load operations with CALU operations using the previous product. These pipeline operations run in parallel with loading the TREG include: load ACC with PREG (LTP); add PREG to ACC (LTA); add PREG to ACC and shift TREG input data (DMOV) to next address in data memory (LTD); and subtract PREG from ACC (LTS).

Two multiply/accumulate instructions (MAC and MACD) fully utilize the computational bandwidth of the multiplier, allowing both operands to be processed simultaneously. The data for these operations can be transferred to the multiplier each cycle via the program and data buses. This facilitates single-cycle multiply/accumulates when used with repeat (RPT) instruction. In these instructions, the coefficient addresses are generated by program address generation (PAGEN), while the data addresses are generated by data address generation (DAGEN). This allows the repeated instruction to sequentially access the values from the coefficient table and step through the data in any of the indirect addressing modes.

multiplier (continued)

The MACD instruction, when repeated, supports filter constructs (weighted running averages) so that as the sum-of-products is executed, the sample data is shifted in memory to make room for the next sample and to throw away the oldest sample.

The MPYU instruction performs an unsigned multiplication, which greatly facilitates extended-precision arithmetic operations. The unsigned contents of TREG are multiplied by the unsigned contents of the addressed data memory location, with the result placed in PREG. This allows the operands of greater than 16 bits to be broken down into 16-bit words and processed separately to generate products of greater then 32-bits. The SQRA (square/add) and SQRS (square/subtract) instructions pass the same value to both inputs of the multiplier for squaring a data memory value.

After the multiplication of two 16-bit numbers, the 32-bit product is loaded into the 32-bit product register (PREG). The product from PREG may be transferred to the CALU or to data memory via the SPH (store product high) and SPL (store product low). Note: the transfer of PREG to either the CALU or data bus passes through the PSCALE shifter and is therefore affected by product shift mode defined by PM. This is important when saving PREG in an interrupt service routine context save as the PSCALE shift effects cannot be modeled in the restore operation. PREG can be cleared by executing the MPY #0 instruction. The product register can be restored by loading the saved low half into TREG and executing a MPY #1. The high half is then loaded using the LPH instruction.

central arithmetic logic unit

The TMS320C2xx central arithmetic logic unit (CALU) implements a wide range of arithmetic and logical functions, the majority of which execute in a single clock cycle. This ALU is referred to as central to differentiate it from a second ALU used for indirect address generation called the ARAU. Once an operation is performed in the CALU, the result is transferred to the accumulator (ACC) where additional operations, such as shifting, may occur. Data that is input to the CALU may be scaled by ISCALE when coming from one of the data buses (DRDB or PRDB) or scaled by PSCALE when coming from the multiplier.

The CALU is a general-purpose arithmetic/logic unit that operates on 16-bit words taken from data memory or derived from immediate instructions. In addition to the usual arithmetic instructions, the CALU can perform Boolean operations, facilitating the bit manipulation ability required for a high-speed controller. One input to the CALU is always provided from the accumulator, and the other input may be provided from the Product Register (PREG) of the multiplier or the output of the scaling shifter (that has been read from data memory or from the ACC). After the CALU has performed the arithmetic or logical operation, the result is stored in the accumulator.

The TMS320C2xx supports floating-point operations for applications requiring a large dynamic range. The NORM (normalization) instruction is used to normalize fixed-point numbers contained in the accumulator by performing left shifts. The four bits of the TREG define a variable shift through the scaling shifter for the LACT/ADDT/SUBT (load/add to /subtract from accumulator with shift specified by TREG) instructions. These instructions are useful in floating-point arithmetic where a number needs to be de normalized, i.e., floating-point to fixed-point conversion. They are also useful in execution of an automatic gain control (AGC) going into a filter. The BITT (bit test) instruction provides testing of a single bit of a word in data memory based on the value contained in the four LSB's of TREG.

The CALU overflow saturation mode may be enabled/disabled by setting/resetting the OVM bit of ST0. When the CALU is in the overflow saturation mode and an overflow occurs, the overflow flag is set and the accumulator is loaded with either the most positive or the most negative value representable in the accumulator, depending upon the direction of the overflow. The value of the accumulator upon saturation is 07FFFFFFh (positive) or 080000000h (negative). If the OVM (overflow mode) status register bit is reset and an overflow occurs, the overflowed results are loaded into the accumulator with modification. (Note that logical operations cannot result in overflow.)

central arithmetic logic unit (continued)

The CALU can execute a variety of branch instructions that depend on the status of the CALU and accumulator. These instructions can be conditionally executed based on any meaningful combination of these status bits. For overflow management these conditions include the OV (branch on overflow) and EQ (branch on accumulator equal to zero). In addition, the BACC (branch to address in accumulator) instruction provides the ability to branch to an address specified by the accumulator (computed goto). Bit test instructions (BIT and BITT), which do not affect the accumulator, allow the testing of a specified bit of a word in data memory.

The CALU also has an associated carry bit that is set or reset depending on various operations within the device. The carry bit allows more efficient computation of extended-precision products and additions or subtractions. It is also useful in overflow management. The carry bit is affected by most arithmetic instructions as well as the single-bit shift and rotate instructions. It is not affected by loading the accumulator, logical operations, or other such non-arithmetic or control instructions.

The ADDC (add to accumulator with carry) and SUBB (subtract from accumulator with borrow) instructions provided use the previous value of carry in their addition/subtraction operation.

The one exception to operation of the carry bit is in the use of ADD with a shift count of 16 (add to high accumulator) and SUB with a shift count of 16 (subtract from high accumulator) instructions. This case of the ADD instruction can set the carry bit only if a carry is generated, and this case of the SUB instruction can reset the carry bit only if a borrow is generated; otherwise, neither instruction affects it.

Two conditional operands, C and NC, are provided for branching, calling, returning, and conditionally executing based upon the status of the carry bit. The SETC, CLRC, and LST #1 instructions also can be used to load the carry bit. The carry bit is set to one on a hardware reset.

accumulator

The 32-bit accumulator is the registered output of the CALU. It can be split into two 16-bit segments for storage in data memory. Shifters at the output of the accumulator provide a left-shift of 0 to 7 places. This shift is performed while the data is being transferred to the data bus for storage. The contents of the accumulator remain unchanged. When the post-scaling shifter is used on the high word of the accumulator (bits 16–31), the MSB's are lost and the LSB's are filled with bits shifted in from the low word (bits 0–15). When the post-scaling shifter is used on the low word, the LSB's are zero filled.

The SFL and SFR (in-place one-bit shift to the left/right) instructions and the ROL and ROR (rotate to the left/right) instructions implement shifting or rotating of the contents of the accumulator through the carry bit. The SXM bit affects the definition of the SFR (shift accumulator right) instruction. When SXM=1, SFR performs an arithmetic right shift, maintaining the sign of the accumulator data. When SXM=0, SFR performs a logical shift, shifting out the LSBs and shifting in a zero for the MSB. The SFL (shift accumulator left) instruction is not affected by the SXM bit and behaves the same in both cases, shifting out the MSB and shifting in a zero. Repeat (RPT) instructions may be used with the shift and rotate instructions for multiple-bit shifts.

auxiliary registers and auxiliary-register arithmetic unit (ARAU)

The 'C2xx provides a register file containing eight auxiliary registers (AR0–AR7). The auxiliary registers are used for indirect addressing of the data memory or for temporary data storage. Indirect auxiliary-register addressing allows placement of the data memory address of an instruction operand into one of the auxiliary registers. These registers are referenced with a 3-bit auxiliary register pointer (ARP) that is loaded with a value from 0 through 7, designating AR0 through AR7, respectively. The auxiliary registers and the ARP can be loaded from data memory, the ACC, the product register, or by an immediate operand defined in the instruction. The contents of these registers can also be stored in data memory or used as inputs to the central arithmetic logic unit (CALU).

auxiliary registers and auxiliary-register arithmetic unit (ARAU) (continued)

The auxiliary register file (AR0–AR7) is connected to the auxiliary register arithmetic unit (ARAU). The ARAU can autoindex the current auxiliary register while the data memory location is being addressed. Indexing either by ±1 or by the contents of the AR0 register can be performed. As a result, accessing tables of information does not require the CALU for address manipulation; thus, the CALU is free for other operations in parallel.

memory

The 'C2xx implements three separate address spaces for program memory, data memory, and I/O. Each space accommodates a total of 64K 16-bit words. Within the 64K words of data space, the 256 to 32K words at the top of the address range can be defined to be external global memory in increments of powers of two, as specified by the contents of the global memory allocation register (GREG). Access to global memory is arbitrated using the global memory bus request ($\overline{BR}$) signal.

On the 'C2xx, the first 96 (0–5Fh) data memory locations are allocated for memory-mapped registers or reserved. This memory-mapped register space contains various control and status registers including those for the CPU.

TMS320C209 (only)

The mask-programmable ROM is located in program memory space. Customers can arrange to have this ROM programmed with contents unique to to any particular application. The ROM is enabled or disabled by the state of the MP/$\overline{MC}$ control input upon resetting the device. The ROM occupies the lowest block of program memory when enabled. When disabled, these addresses are located in the device's external program memory space.

The 'C209 devices provide two types of RAM: single-access RAM (SARAM) and dual-access RAM (DARAM). The single-access RAM requires a full machine cycle to perform a read or a write. However, this is not one large RAM block in which only one access per cycle is allowed. It is made up of 2K-word size-independent RAM blocks and each one allows one CPU access per cycle. The CPU can read or write one block while accessing another block at the same time. The 'C209 processor supports multiple accesses to its SARAM in one cycle as long as they go to different RAM blocks. With an understanding of this structure, code and data can be appropriately arranged to improve code performance.

The 'C2xx dual-access RAM (DARAM) allows writes to and reads from the RAM in the same cycle without the address restrictions of the SARAM. The dual-access RAM is configured in three blocks: block 0 (B0), block 1 (B1), and block 2 (B2). Block 1 is 256 words in data memory and block 2 is 32 words in data memory. Block 0 is a 256-word block which can be configured as data or program memory. The SETC CNF (Configure B0 as data memory) and CLRC CNF (Configure B0 as program memory) instructions allow dynamic configuration of the memory maps through software. When using Block 0 as program memory, instructions can be downloaded from external program memory into on-chip RAM and then executed.

TMS320C203 (only)

When using on-chip RAM, or high-speed external memory, the 'C2xx runs at full speed with no wait states. The ability of the DARAM to allow two accesses to be performed in one cycle coupled with the parallel nature of the 'C2xx architecture enables the device to perform three concurrent memory accesses in any given machine cycle. Externally, the READY line can be used to interface the 'C2xx to slower, less expensive external memory. Downloading programs from slow off-chip memory to on-chip RAM can speed processing while cutting system costs.

memory (continued)

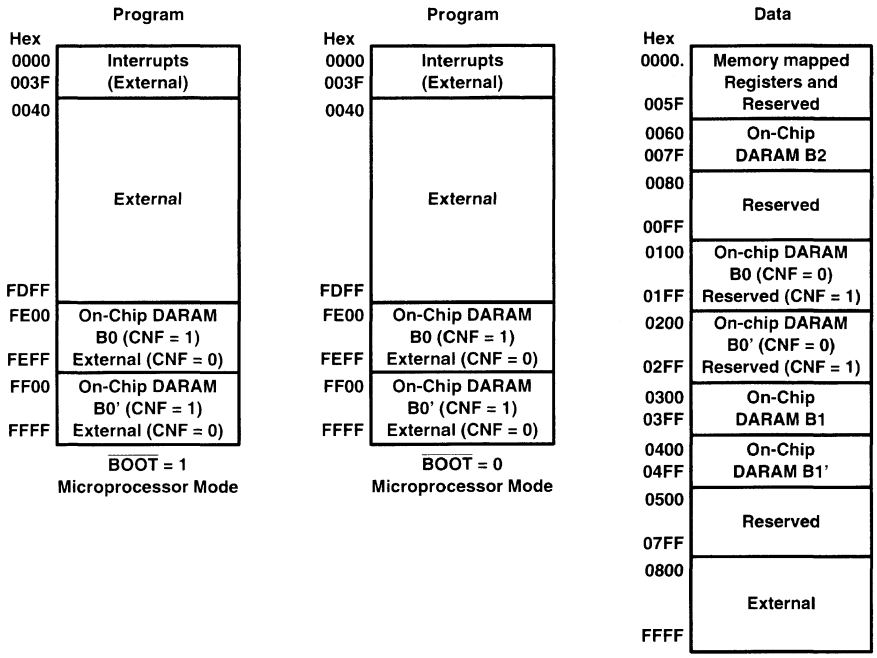

Figure 2. TMS320C203 Memory Map

Table 6. TMS320C203 Memory Map Configurations†

$\overline{\text{BOOT}}$	CNF	ON-CHIP			OFF-CHIP		
		PROGRAM	DATA	I/O	PROGRAM	DATA	I/O‡
0	0	—	0–7FF	FF00–FFFF	1000–FFFF	800–FFFF	0–FEFF
0	1	FE00–FFFF	0–7FF	FF00–FFFF	1000–FDFF	800–FFFF	0–FEFF
1	0		0–7FF	FF00–FFFF	1000–FFFF	800–FFFF	0–FEFF
1	1	FE00–FFFF	0–7FF	FF00–FFFF	1000–FDFF	800–FFFF	0–FEFF

† Internal I/O locations 0FFE0h–0FFFFh are dedicated to the timer, serial port control, wait state generator registers, and reserved space.
‡ FF00–FF0F are reserved for test purposes and should not be used.

The TMS320C203 includes three registers mapped to internal data space and twelve registers mapped to internal I/O space. Figure 2 and Tables 5 and 7 describe these registers and show their respective addresses. In the table, DS refers to data space and IS refers to input/output ports.

memory (continued)

Both of the TMS320C2xx devices include 544 × 16 words of dual-access RAM. The 'C209 device includes 4K × 16 words of single-access RAM, and 4K × 16 words of ROM integrated with CPU. Figure 2 and Tables 6 and 8 show the mapping of these memory blocks and the appropriate control bits and pins for the 'C209 and 'C203, respectively. For the 'C209 devices Figure 3 and Table 7 show the effects of the memory-control pins MP/$\overline{\text{MC}}$ and RAMEN and control bit CNF on the mapping of the respective memory spaces to on-chip or off-chip.

For the 'C203 devices, Figure 2 and Tables 5 and 7 show the effects of the memory-control pins $\overline{\text{BOOT}}$ and control bit CNF on the mapping of the respective memory spaces to on-chip or off-chip.

Table 7. TMS320C209 On-Chip Memory Map

DESCRIPTION OF MEMORY BLOCK	DATA ADDRS	PROG ADDRS	MP/ $\overline{\text{MC}}$	CNF BIT	RAMEN
4K × 16 words of factory-masked ROM		0	low		
256 × 16 words dual-access RAM (B0)	0x100† 0x200†			0	
256 × 16 words dual-access RAM (B0)		0xFE00† 0xFF00†		1	
256 × 16 words dual-access RAM (B1)	0x300† 0x400†				
32 × 16 words dual-access RAM (B2)	0x60				
4096 × 16 words dual-access RAM	0x1000	0x1000			high

† Both of the addresses in each of these address pairs point to the same block of memory.

Table 8. TMS320C203 On-Chip Memory Map

DESCRIPTION OF MEMORY BLOCK	DATA ADDRS	PROG ADDRS	$\overline{\text{BOOT}}$	CNF BIT
On-chip bootloader		0	low	
256 × 16 words dual-access RAM (B0)	0x100‡ 0x200‡			0
256 × 16 words dual-access RAM (B0)		0xFE00‡ 0xFF00‡		1
256 × 16 words dual-access RAM (B1)	0x300‡ 0x400‡			
32 × 16 words dual-access RAM (B2)	0x60			

‡ Both of the addresses in each of these address pairs point to the same block of memory.

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memory (continued)

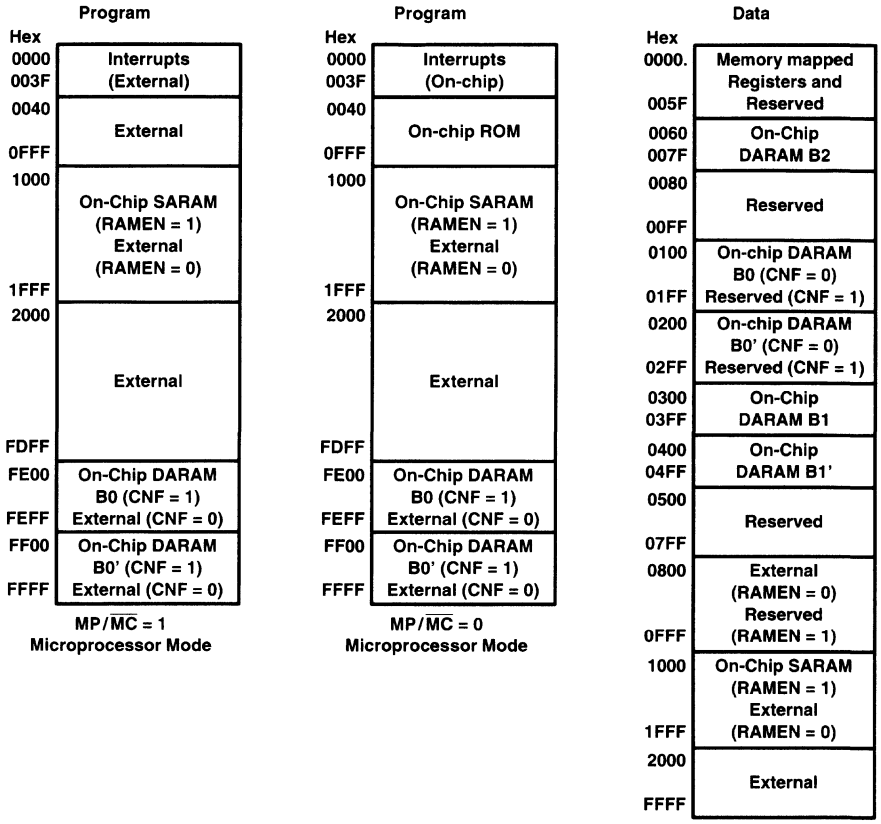

Figure 3. TMS320C209 Memory Map

ADVANCE INFORMATION

memory (continued)

Table 9. TMS320C209 Memory Map Configurations

MP/$\overline{MC}$	RAMEN	CNF	ON-CHIP			OFF-CHIP		
			PROGRAM	DATA	I/O	PROGRAM	DATA	I/O†
0	1	0	0–1FFF	0–1FFF	FFF0–FFFF	2000–FFFF	2000–FFFF	0–FFEF
0	1	1	0–1FFF FE00–FFFF	0–1FFF	FFF0–FFFF	2000–FDFF	2000–FFFF	0–FFEF
0	0	0	0–0FFF	0–07FF	FFF0–FFFF	1000–FFFF	0800–FFFF	0–FFEF
0	0	1	0–0FFF FE00–FFFF	0–07FF	FFF0–FFFF	1000–FDFF	0800–FFFF	0–FFEF
1	1	0	1000–1FFF	0–1FFF	FFF0–FFFF	0–FFF 2000–FFFF	2000–FFFF	0–FFEF
1	1	1	1000–1FFF FE00–FFFF	0–1FFF	FFF0–FFFF	0–FFF 2000–FDFF	2000–FFFF	0–FFEF
1	0	0		0–07FF	FFF0–FFFF	0–FFFF	0800–FFFF	0–FFEF
1	0	1	FE00–FFFF	0–07FF	FFF0–FFFF	0–FDFF	0800–FFFF	0–FFEF

† FF00–FF0F are reserved for test purposes and should not be used.
‡ Internal I/O locations 0FFF0h–0FFFFh are dedicated to the timer, wait state generator registers, and reserved space.

memory (continued)

Table 10. TMS320C203 Memory and I/O Internally Mapped Registers

NAME	ADDRESS	DESCRIPTION
IMR	DS@0004	Interrupt-mask register. IMR individually masks or enables the seven interrupts. Bit 0 shares the external interrupt pins $\overline{INT1}$ and $\overline{HOLD}$. $\overline{INT2}$ and $\overline{INT3}$ share bit 1. Bit 2 ties to the timer interrupt, $\overline{TINT}$. Bits 3 and 4, $\overline{RINT}$ and $\overline{XINT}$, respectively, are for the synchronous serial port, SSP. Bit 5, $\overline{TXRXINT}$ shares the transmit and receive interrupts for the asynchronous serial port, ASP. Bit 6 is reserved for monitor mode emulation operations and should always be set to 0 except in conjunction with emulation monitor operations. Bits 7–15 are not used in the TMS320C203. IMR is set to 0 at reset.
GREG	DS@0005	Global-memory-allocation register. GREG specifies the size of the global memory space. GREG is set to 0 at reset.
IFR	DS@0006	Interrupt-flag register. IFR indicates that the TMS320C203 has latched an interrupt from one of the seven maskable interrupts. Bit 0 shares the external interrupt $\overline{INT1}$ and $\overline{HOLD}$. $\overline{INT2}$ and $\overline{INT3}$ share bit 1. Bit 2 ties to the timer interrupt, $\overline{TINT}$. Bits 3 and 4, $\overline{RINT}$ and $\overline{XINT}$, respectively, are for the synchronous serial port, SSP. Bit 5, $\overline{TXRXINT}$ shares the transmit and receive interrupts for the asynchronous serial port, ASP. Bit 6 is reserved for monitor mode emulation operations and should always be set to 0 except in conjunction with emulation monitor operations. Writing a 1 to the respective interrupt bit clears an active flag and the respective pending interrupt. Writing a 1 to an inactive flag has no effect. Bits 7–15 are not used in the TMS320C203. IMR is set to 0 at reset.
CLK	IS@FFE8	CLKOUT1 on or off. At reset, this bit is configured as a zero for the CLKOUT1 pin to be active. If CLKOUT1 is a 1, CLKOUT1 pin is turned off.
IC	IS@FFEC	Interrupt control register. IC is used to determine which interrupt is active since $\overline{INT1}$ and $\overline{HOLD}$ share an interrupt vector as do $\overline{INT1}$ and $\overline{INT3}$. A portion of this register is for mask/unmask (similar to IMR) and another portion is for pending interrupts (similar to IFR). At reset, all bits are zeroed, enabling HOLD mode. The MODE bit is used by the hold generating circuit to determine if a $\overline{HOLD}$ or $\overline{INT1}$ is active.
SDTR	IS@FFF0	Synchronous serial port (SSP) transmit and receive register.
SSPCR	IS@FFF1	Synchronous serial port control register.
ADTR	IS@FFF4	Asynchronous serial port (ASP) transmit and receive register.
ASPCR	IS@FFF5	Asynchronous serial port control register. ASPCR controls the asynchronous serial port operation.
IOSR	IS@FFF6	I/O status register. IOSR detects current levels (and changes with inputs) on pins IO0–IO3 and status of UART.
BRD	IS@FFF7	Baud rate divisor. Used to set baud rate of UART.
TCR	IS@FFF8	Timer-control register. TCR contains the control bits that define the divide-down ratio, start/stop the timer, and reload the period. Also contained in TCR is the current count in the prescaler. Reset initializes the timer-divide-down ratio to 0 and starts the timer.
BRD	IS@FFF9	Timer-period register. PRD contains the 16-bit period that is loaded into the timer counter when the counter borrows or when the reload bit is activated. Reset initializes the PRD to 0xFFFF.
TIM	IS@FFFA	Timer-counter register. TIM contains the current 16-bit count of the timer. Reset initializes the TIM to 0xFFFF.
WSGR	IS@FFFC	Wait-state-generator register. WSGR contains 12 control bits to enable 0, . . . ,7 wait states to program, data, and I/O space. Reset initializes the WSGR to 0x0FFFh.

Table 11. TMS320C209 Memory-Mapped Registers

NAME	ADDRESS	DESCRIPTION
IMR	DS@0004	Interrupt mask register. IMR individually masks or enables the seven interrupts. The lower three bits align to the three external interrupt pins (bit 0 ties to $\overline{INT1}$, bit 1 to $\overline{INT2}$, bit 2 to $\overline{INT3}$). Bit 3 ties to the timer interrupt. Bits 4 and 5 are not used in the TMS320C209. Bit 6 is reserved for monitor mode emulation operations and should always be set to 0 except in conjunction with emulation monitor operations. Bits 7–15 are not used in the TMS320C209. IMR is set to 0 at reset.
GREG	DS@0005	Global memory allocation register. GREG specifies the size of the global memory space. GREG is set to 0 at reset.
IFR	DS@0006	Interrupt flag register. IFR indicates that the T320C2xLP core has latched an interrupt pulse from one of the maskable interrupts. The lower three bits align to the three external interrupt pins (bit 0 ties to INT1N, bit 1 to INT2N, bit 2 to INT3N). Bit 4 ties to the timer interrupt. Bits 5 and 6 are not used in the TMS320C209. Bit 7 is reserved for monitor mode emulation operations and should always be set to 0 except in conjunction with emulation monitor operations. A 1 indicates an active interrupt in the respective interrupt location. Writing a 1 to the respective interrupt bit clears an active flag and the respective pending interrupt. Writing a 1 to an inactive flag has no affect. IFR is set to 0 at reset.
TCR	IS@FFFC	Timer control register. TCR contains the control bits that define the divide down ratio, start/stop the timer, and reload the period. Also contained in TCR is the current count in the prescaler. Reset initializes the timer divide down ratio to 0 and starts the timer.
PRD	IS@FFFD	Timer period register. PRD contains the 16-bit period that is loaded into the timer counter when the counter borrows or when the reload bit is activated. Reset initializes the PRD to 0xFFFF.
TIM	IS@FFFE	Timer counter register. TIM contains the current 16-bit count of the timer. Reset initializes the TIM to 0xFFFF.
WSGR	IS@FFFF	Wait state generator register. WSGR contains the three control bits to enable a single wait state each of program, data, and I/O space as well as the address visibility enable bit. Reset initializes WSGR to 0xF.

external interface

The TMS320C2xx can address up to 64K × 16 words of memory or registers in each of the program, data, and I/O spaces. On-chip memory, when enabled, removes some of this off-chip range. In data space, the high 32K words can be dynamically mapped either local or global using the GREG register as described in the *TMS320C2xx User's Guide*. A data-memory access mapped as global asserts $\overline{BR}$ low (with timing similar to the address bus) (see Table 8).

The CPU of the TMS320C2xx schedules a program fetch, data read, and data write on the same machine cycle. This is because from on-chip memory the CPU can execute all three of these operations in the same cycle. However, the external interface multiplexes the internal buses to one address and one data bus. The external interface sequences these operations to complete first the data write, then the data read, and finally the program read.

The 'C2xx supports a wide range of system interfacing requirements. Program, data, and I/O address spaces provide interface to memory and I/O, thus maximizing system throughput. The full 16-bit address and data bus, along with the $\overline{PS}$, $\overline{DS}$, and $\overline{IS}$ space select signals, allow addressing of 64K 16-bit words in each of the three spaces.

I/O design is simplified by having I/O treated the same way as memory. I/O devices are mapped into the I/O address space using the processor's external address and data buses in the same manner as memory-mapped devices.

The 'C2xx external parallel interface provides various control signals to facilitate interfacing to the device. The R/$\overline{W}$ output signal is provided to indicate whether the current cycle is a read or a write. The $\overline{STRB}$ output signal provides a timing reference for all external cycles. For convenience, the device also provides the $\overline{RD}$ and the $\overline{WE}$ output signals, which indicate a read and a write cycle, respectively, along with timing information for those cycles. The availability of these signals minimizes external gating necessary for interfacing external devices to the 'C2xx.

external interface (continued)

Interface to memory and I/O devices of varying speeds is accomplished by using the READY line. When transactions are made with slower devices, the 'C2xx processor waits until the other device completes its function and signals the processor via the READY line. Once a ready indication is provided back to the 'C2xx from the external device, execution continues. **On the 'C209 device, the READY line is required (active high) to complete reads or writes to internal I/O-mapped registers.**

The bus request ($\overline{BR}$) signal is used in conjunction with the other 'C2xx interface signals to arbitrate external global memory accesses. Global memory is external data memory space in which the $\overline{BR}$ signal is asserted at the beginning of the access. When an external global memory device receives the bus request, it responds by asserting the READY signal after the global memory access is arbitrated and the global access is completed.

The TMS320C2xx supports zero-wait state reads on the external interface. However, to avoid bus conflicts, writes take two cycles. This allows the TMS320C2xx to buffer the transition of the data bus from input to output (or output to input) by a half cycle. In most systems, TMS320C2xx ratio of reads to writes is significantly large to minimize the overhead of the extra cycle on writes.

Wait states can be generated when accessing slower external resources. The wait states operate on machine-cycle boundaries and are initiated either by using READY or using the software wait-state generator. READY can be used to generate any number of wait states.

interrupts and subroutines

The 'C2xx implements four general-purpose interrupts, $\overline{INT3}$–$\overline{INT1}$, along with reset ($\overline{RS}$) and the nonmaskable interrupt ($\overline{NMI}$) which are available for external devices to request the attention of the processor. Internal interrupts are generated by the serial port (RINT and XINT) ('C203 only), by the timer (TINT), UART, TXRXINT ('C203 only), and by the software-interrupt (TRAP, INTR and NMI) instructions. Interrupts are prioritized with $\overline{RS}$ having the highest priority, followed by $\overline{NMI}$, and timer ('C209) or UART ('C203) having the lowest priority. Additionally, any interrupt except $\overline{RS}$ and $\overline{NMI}$ can be individually masked with a dedicated bit in the interrupt mask register (IMR) and can be cleared, set, or tested using its own dedicated bit in the interrupt flag register (IFR). The reset and NMI functions are not maskable.

All interrupt vector locations are on two-word boundaries so that branch instructions can be accommodated in those locations if desired.

A built-in mechanism protects multicycle instructions from interrupts. If an interrupt occurs during a multicycle instruction, the interrupt is not processed until the instruction completes execution. This mechanism applies to instructions that are repeated (using the RPT instruction) and to instructions that become multicycle because of wait states.

Each time an interrupt is serviced or a subroutine is entered, the PC is pushed onto an internal hardware stack, providing a mechanism for returning to the previous context. The stack contains eight locations, allowing interrupts or subroutines to be nested up to eight levels deep.

reset

The TMS320C203 provides an active-low reset ($\overline{RS}$) only, while the TMS320C209 provides both an RS and an $\overline{RS}$.

RS and $\overline{RS}$, the TMS320C209 resets, are not synchronized. A minimum pulse duration of six cycles assures that an asynchronous reset signal resets the device. Either RS or $\overline{RS}$ can reset the device with RS being active high and $\overline{RS}$ being active low. The TMS320C2xx fetches its first instruction approximately sixteen cycles after the rising edge of $\overline{RS}$ (either 'C203 or 'C209) or falling edge of RS ('C209 only).

reset (continued)

Please note that the reset action halts all operations whether complete or not. Therefore, the state of the system and its data cannot be maintained through the reset operation. For example, if the device is writing to an external resource when the reset is initiated, the write is aborted. This can and will corrupt data in system resources. Therefore it is necessary to reinitialize the system after a reset.

power-down modes

The 'C2xx implements several power-down modes in which the 'C2xx core enters a dormant state and dissipates considerably less power. A power-down mode is invoked either by executing the IDLE instruction or by driving the $\overline{\text{HOLD}}$ ('C203 only) input low. When the $\overline{\text{HOLD}}$ signal initiates the power-down mode, on-chip peripherals continue to operate; this power-down mode is terminated when $\overline{\text{HOLD}}$ goes inactive ('C203 only).

While the 'C2xx is in a power-down mode, all of its internal contents are maintained; this allows operation to continue unaltered when the power-down mode is terminated. All CPU activities are halted when the IDLE instruction is executed, but the CLKOUT1 pin remains active depending on status of IC register ('C203 only). The peripheral circuits continue to operate, allowing peripherals such as serial ports and timers to take the CPU out of its powered-down state. A power-down mode, when initiated by an IDLE instruction, is terminated upon receipt of an interrupt.

software-controlled wait-state generator

Due to the fast cycle time of the TMS320C2xx devices, it is often necessary to operate with wait states to interface with external logic and memory. For many systems, one wait state is adequate.

TMS320C209

When operating the TMS320C209 at full speed, it is difficult to respond fast enough to provide a READY-based wait state for the first cycle. For this reason, the TMS320C209 includes a simple software-controlled wait-state generator to provide the first wait state.

The software-controlled wait-state generator can be programmed to generate the first wait state for a given external space. The WSGR has four bits: AVIS, DATA, PROG, and IO. The wait-state generator inserts a wait state to a given memory space if the respective bit is set to 1, regardless of the condition of the READY signal. Then READY can be used to further extend wait states. The AVIS bit differs from the other WSGR bits because it doesn't generate a wait state but enables the address-visibility mode of the '320C209. This mode allows the internal program address to be presented to the address bus when this bus is not used for an external access. The WSGR bits are initially set to 1 by reset so that the device can operate from slow memory. After initialization, the AVIS bit should be set to 0 for production systems to reduce power and noise. The WSGR register (shown in Figure 4 and NO TAG) resides at I/O port 0xFFFF.

3	2	1	0
AVIS	ISWS	DSWS	PSWS

Figure 4. TMS320C209 Wait-State Generator Control Register (WSGR)

ADVANCE INFORMATION

software-controlled wait-state generator

Table 12. 'C209 Wait-State Generator Control Register (WSGR)

TERMINAL	NAME	DESCRIPTION
0	PSWS	External program-space wait state on. When active, PSWS = 1 applies one wait state to all reads to off-chip program space (writes always take at least two cycles regardless of PSWS or READY). The memory cycle can be further extended using the READY signal. However, the READY signal does not override the wait state generated by PSWS. This bit is set to 1 (active) by reset (RS or $\overline{RS}$).
1	DSWS	External data-space wait state on. When active, DSWS = 1 applies one wait state to all reads to off-chip data space (writes always take at least two cycles regardless of DSWS or READY). The memory cycle can be further extended using the READY signal. However, the READY signal does not override the wait state generated by DSWS. This bit is set to 1 (active) by reset (RS or $\overline{RS}$).
2	ISWS	External input-/output-space wait state on. When active, ISWS = 1 applies one wait state to all reads to off-chip I/O space (write always takes at least two cycles regardless of ISWS or READY). The memory cycle can be further extended using the READY signal. However, the READY signal does not override the wait state generated by ISWS. This bit is set to 1 (active) by reset (RS or $\overline{RS}$).
3	AVIS	Address visibility. When active high, AVIS presents the internal program address out of the logic-interface address bus if the bus is not currently used in an external memory operation. The internal address is presented to provide a trace mechanism of internal code operation. Therefore, the memory-control signals are not active. AVIS is set to 1 (active) by reset (RS or $\overline{RS}$). AVIS should be deactivated in production systems to reduce system power and noise.

TMS320C203

The software wait-state generator can be programmed to generate between 0 and seven wait states for a given space. The WSGR has 12 bits: three DATA, six PROGRAM, and three I/O. The wait state generator inserts a wait state(s) to a given memory space based on the value of the three bits, regardless of the condition of the READY signal. The READY signal can be used to extend wait state further. All bits are set to 1 at reset so that the device can operate from slow memory from reset. The WSGR register (shown in Figure 5 and Table 13 and Table 14) resides at I/O port 0xFFFF.

15–12	11 10 9	8 7 6	5 4 3	2 1 0
Reserved	ISWS	DSWS	PSUWS	PSLWS
0	W	W	W	W

Figure 5. TMS320C203 Wait-State Generator Control Register (WSGR)

Table 13. TMS320C203 Wait-State(s) Programming

BITS 11, 8, 5, 2	BITS 10, 7, 4, 1	BITS 9, 6, 3, 0	WAIT-STATES FOR PROGRAM, DATA, AND I/O
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

TMS320C203 (continued)

Table 14. 'C203 Wait-State Generator Control Register (WSGR)

BITS	NAME	DESCRIPTION
2–0	PSLWS	External program-space wait states (lower). PSLWS determines that between 0,. . .,7 wait states are applied to all reads and writes to off-chip lower program space address (0h-7FFFh). The memory cycle can be further extended using the READY signal. The READY signal does not override the wait states generated by PSWS. These bits are set to 1 (active) by reset, ($\overline{RS}$).
5–3	PSUWS	External program-space wait states (upper). PSUWS determines that between 0,. . .,7 wait states are applied to all reads and writes to off-chip upper program space address (8000h-0FFFFh). The memory cycle can be further extended using the READY signal. The READY signal does not override the wait states generated by PSWS. These bits are set to 1 (active) by reset, ($\overline{RS}$).
8–6	DSWS	External data space wait states. DSWS determines that between 0,. . .,7 wait states are applied to all reads and writes to off-chip data space. The memory cycle can be further extended using the READY signal. The READY signal does not override the wait states generated by DSWS. These bits are set to 1 (active) by reset, ($\overline{RS}$).
11–9	ISWS	External input / output-space wait state. DSWS determines that between 0,. . .,7 wait states are applied to all reads and writes to off-chip I/O space. The memory cycle can be further extended using the READY signal. The READY signal does not override the wait states generated by ISWS. These bits are set to 1 (active) by reset, ($\overline{RS}$).
15–12	X	Don't care.

timer

The 'C2xx features a 16-bit timing circuit with a 4-bit prescaler. This timer clocks between one-half and one thirty-second the machine rate of the device itself, depending upon the programmable timer's divide-down ratio. This timer can be stopped, restarted, reset, or disabled by specific status bits.

The timer can be used to generate CPU interrupts periodically. The timer is decremented by one at every CLKOUT1 cycle. A timer interrupt (TINT) and a pulse equal to the duration of a CLKOUT1 cycle on the external TOUT pin are generated each time the counter decrements to zero. The timer thus provides a convenient means of performing periodic I/O or other functions.

TMS320C209 input clock options

The TMS320C209 includes two clock options. The first option (÷2) operates the CPU at half the input clock rate. The second option (×2) doubles the input clock and phase locks the output clock with the input clock. The ÷2 mode is enabled by tying the CLKMOD pin low. The ×2 mode is enabled by tying the CLKMOD pin high.

The clock doubler option of the 'C209 uses an internal phase lock loop (PLL). The PLL requires approximately 1000 cycles to lock. The rising edge of $\overline{RS}$ (or falling edge of RS) must be delayed until at least three cycles after the PLL has stabilized. Likewise, the modes cannot be dynamically switched because the internal clock generator can generate minimal clock pulse with violations. The $\overline{RS}$ or RS signals should be in their active state if the CLKMOD pin is changed.

TMS320C203 input clock options

The TMS320C203 provides multiple clock modes of: ÷2, ×1, ×2, ×4. The clock mode configuration cannot be dynamically changed without executing another reset. The operation of the PLL circuit is affected by the operating voltage of the device. If the device is operating at 5 V then the PLL5V signal should be tied high. For 3 V operation, PLL5V should be tied low.

synchronous serial port (TMS320C203 only)

A full duplex (bidirectional 16 bit on-chip synchronous serial port provides direct communication with serial devices such as codecs, serial A/D (analog to digital) converters, and other serial systems. The interface signals are compatible with codecs and many other serial devices. The serial port can also be used for intercommunication between processors in multiprocessing applications.

Both receive and transmit operations have a four deep first in first out (FIFO). The advantage of having a FIFO is a to alleviate the CPU from being loaded with the task of servicing a transmit or receive data on every interrupt, allowing a continuous communications stream of 16-bit data packets. The continuous mode provides operation that once initiated requires no further frame synchronization pulses when transmitting at maximum packet frequency. The maximum transmission rate for both transmit and receive operations is CPU divided by two or CLKOUT1(frequency)/2. Therefore, the maximum rate at 25 ns is 20 Mbit/s and 14.28 Mbit/s at 35 ns. The serial port is fully static and functions arbitrarily at low clocking frequencies. When the serial ports are in reset the device can be configured to shut off the serial port internal clocks, allowing the device to run in a lower power mode of operation.

Three signals are necessary to connect the transmit pins of the transmitting device with the receive pins of the receiving device for data transmission. The transmitted serial data signal (DX) sends the actual data. The transmit frame synchronization signal (FSX) initiates the transfer (at the beginning of the packet), and the transmit clock signal (CLKX) clocks the bit transfer. The corresponding pins on the receive device are DR, FSR and CLKR, respectively.

asynchronous serial port ('C203 only)

The asynchronous serial port is full–duplexed and transmits and receives 8-bit data only. For transmit and receive there is one start bit and configurable one or two stop bits via the asynchronous serial port control register (ASPCR). Double-buffering or transmit/receive data is used in all modes. Baud rate generation uses the BRD baud rate divisor register to obtain baud rate. The maximum baud rate is 2.5 Mbit/s at 250000 characters per second (at 25 ns instruction cycle time).

TMS320C2xx scan-based emulation

TMS320C2xx devices use scan-based emulation for code- and hardware-development support. Scan-based emulation allows the emulator to control the processor in the system without the use of intrusive cables to the full pinout of the device.

multiprocessing ('C203 only)

The flexibility of the 'C2xx allows configurations to satisfy a wide range of system requirements; the device can be used in a variety of system configurations, including but not limited to the following:

- A standalone processor
- A multiprocessor with devices in parallel
- A slave/host multiprocessor with global memory space
- A peripheral processor interfaced via processor-controlled signals to another device

For multiprocessing applications, the 'C2xx has the capability of allocating global memory space and communicating with that space via the $\overline{BR}$ and ready control signals. Global memory is data memory shared by more than one device. Global memory access must be arbitrated. The 8-bit memory-mapped global memory allocation register (GREG) specifies part of the 'C2xx's data memory as global external memory. The contents of the register determine the size of the global memory space. If the current instruction addresses an operand within that space, $\overline{BR}$ is asserted to request control of the bus. The length of the memory cycle is controlled by the READY line.

The 'C203 supports direct memory access (DMA) to its external program, data, and I/O spaces using the $\overline{HOLD}$ and $\overline{HOLDA}$ signals. Another device can take complete control of the 'C2xx's external memory interface by asserting $\overline{HOLD}$ low. This causes the 'C2xx to to place its address, data, and control lines in the high-impedance state and assert $\overline{HOLDA}$.

instruction set

The 'C2xx microprocessor implements a comprehensive instruction set that supports both numeric-intensive signal processing operations and general-purpose applications, such as multiprocessing and high-speed control. Source code for the 'C1x and 'C2x DSPs is upward compatible with the 'C2xx.

For maximum throughput, the next instruction is prefetched while the current one is being executed. Because the same data lines are used to communicate to external data, program, or I/O space, the number of cycles an instruction requires to execute varies depending upon whether the next data operand fetch is from internal or external memory. Highest throughput is achieved by maintaining data memory on chip and using either internal or fast external program memory.

addressing modes

The 'C2xx instruction set provides four basic memory-addressing modes: direct, indirect, immediate and register.

In direct addressing, the instruction word contains the lower seven bits of the data-memory address. This field is concatenated with the nine bits of the data-memory page pointer (DP) to form the 16-bit data-memory address. Thus, in the direct-addressing mode, data memory is effectively paged with a total of 512 pages, each page containing 128 words.

Indirect addressing accesses data memory through the auxiliary registers. In this addressing mode, the address of the instruction operand is contained in the currently selected auxiliary register. Eight auxiliary registers (AR0–AR7) provide flexible and powerful indirect addressing. To select a specific auxiliary register, the auxiliary register pointer (ARP) is loaded with a value from 0 to 7 for AR0 through AR7, respectively.

addressing modes (continued)

There are seven types of indirect addressing: autoincrement or autodecrement, postindexing by either adding or subtracting the contents of AR0, single-indirect addressing with no increment or decrement, and bit-reversed addressing (used in FFTs) with increment or decrement. All operations are performed on the current auxiliary register in the same cycle as the original instruction, following which the current auxiliary register and ARP can be modified.

In immediate addressing, the actual operand data is provided in a portion of the instruction word or words. There are two types of immediate addressing: long and short. In short immediate addressing, the data is contained in a portion of the bits in a single-word instruction. In long immediate addressing, the data is contained in the second word of a two-word instruction. The immediate-addressing mode is useful for data that does not need to be stored or used more than once during the course of program execution, such as initialization values, constants, etc.

The register-addressing mode uses operands in CPU registers either explicitly, such as with a direct reference to a specific register, or implicitly with instructions that intrinsically reference certain registers. In either case, operand reference is simplified because 16-bit values can be used without specifying a full 16-bit operand address or immediate value.

repeat feature

The repeat function can be used with instructions (as defined in Table 16) such as multiply/accumulates (MAC and MACD), block moves (BLDD and BLPD), I/O transfers (IN/OUT), and table read/writes (TBLR/TBLW). These instructions, although normally multicycle, are pipelined when the repeat feature is used, and they effectively become single-cycle instructions. For example, the table-read instruction may take three or more cycles to execute, but when the instruction is repeated, a table location can be read every cycle.

The repeat counter (RPTC) is loaded with the addressed data memory location if direct or indirect addressing is used, an 8-bit immediate value if short immediate addressing is used. The RPTC register is loaded by the RPT instruction. This results in a maximum of N + 1 executions of a given instruction. RPTC is cleared by reset. Once a repeat instruction (RPT) is decoded, all interrupts including $\overline{\text{NMI}}$ (except reset) are masked until the completion of the repeat loop. However, the device responds to the $\overline{\text{HOLD}}$ signal while executing an RPT loop.

instruction set summary

This section summarizes the opcodes of the instruction set for the 'C2xx digital signal processors. This instruction set is a superset of the 'C1x and 'C2x instruction sets. The instructions are arranged according to function and are alphabetized by mnemonic within each category. The symbols in Table 8 are used in the instruction set opcode table (Table 16). The Texas Instruments 'C2xx assembler accepts 'C2x instructions.

The number of words that an instruction occupies in program memory is specified in column 3 of Table 16. Several instructions specify two values separated by a slash mark (/) for the number of words. In these cases, different forms of the instruction occupy a different number of words. For example, the ADD instruction occupies one word when the operand is a short immediate value or two words if the operand is a long immediate value.

The number of cycles that an instruction requires to execute is in column 3 of Table 16. All instructions are assumed to be executed from internal program memory (RAM) and internal data dual-access memory. The cycle timings are for single-instruction execution, not for repeat mode.

Table 15. Opcode Symbols

SYMBOL	DESCRIPTION
A	Address
ACC	Accumulator
ACCB	Accumulator buffer
ARX	Auxiliary register value (0–7)
BITX	4-bit field specifies which bit to test for the BIT instruction
BMAR	Block-move address register
DBMR	Dynamic bit-manipulation register
I	Addressing-mode bit
II...II	Immediate operand value
INTM	Interrupt-mode flag bit
INTR#	Interrupt vector number
N	Field for the XC instruction, indicating the number of instructions (one or two) to execute conditionally
PREG	Product register
PROG	Program memory
RPTC	Repeat counter
SHF, SHFT	3/4 bit shift value
TC	Test-control bit
T P	Two bits used by the conditional execution instructions to represent the conditions TC, NTC, and BIO. T P Meaning 0 0 $\overline{\text{BIO}}$ low 0 1 TC = 1 1 0 TC = 0 1 1 None of the above conditions
TREGn	Temporary register n (n = 0, 1, or 2)
Z L V C	4-bit field representing the following conditions: Z: ACC = 0 L: ACC < 0 V: Overflow C: Carry A conditional instruction contains two of these 4-bit fields. The 4-LSB field of the instruction is a 4-bit mask field. A 1 in the corresponding mask bit indicates that the condition is being tested. The second 4-bit field (bits 4–7) indicates the state of the conditions designated by the mask bits as being tested. For example, to test for ACC ≥ 0, the Z and L fields are set while the V and C fields are not set. The next 4-bit field contains the state of the conditions to test. The Z field is set to indicate testing the condition ACC = 0, and the L field is reset to indicate testing the condition ACC ≥ 0. The conditions possible with these 8 bits are shown in the BCND, CC, and XC instructions. To determine if the conditions are met, the 4-LSB bit mask is ANDed with the conditions. If any bits are set, the conditions are met.

Table 16. TMS320C2xx Instruction Set Summary

C2xx MNEMONIC	DESCRIPTION	WORDS/ CYCLES	OPCODE MSB			LSB
ABS	Absolute value of accumulator	1/1	1011	1110	0000	0000
ADD	Add to accumulator with shift	1/1	0010	SHFT	IADD	RESS
ADDC	Add to accumulator with carry	1/1	0110	000	IADD	RESS
ADD	Add to high accumulator	1/1	0110	0001	IADD	RESS
	Add to accumulator short immediate	1/1	1011	1000	8BIT	CNST
	Add to accumulator long immediate with shift	2/2	1011	1111	1001	SHFT
			16-Bit Constant			
ADDS	Add to low accumulator with sign extension suppressed	1/1	0110	0010	IADD	RESS
ADDT	Add to accumulator with shift specified by T register	1/1	0110	0011	IADD	RESS
ADRK	Add to auxiliary register short immediate	1/1	0111	1000	8BIT	CNST
AND	AND with accumulator	1/1	0110	1110	IADD	RESS
AND	AND immediate with accumulator with shift	2/2	1011	1111	1011	SHFT
			16-Bit Constant			
	AND immediate with accumulator with shift of 16	2/2	1011	1110	1000	0001
			16-Bit Constant			
APAC	Add P register to accumulator	1/1	1011	1110	0000	0100
B	Branch unconditionally	2/4	0111	1001	IADD	RESS
			Branch Address			
BACC	Branch to address specified by accumulator	1/4	1011	1110	0010	0000
			Branch Address			
BANZ	Branch on auxiliary register not zero	2/4/2	0111	1011	IADD	RESS
			Branch Address			
BCND	Branch if TC bit ≠ 0	2/4/2	1110	0001	0000	0000
			Branch Address			
	Branch if TC bit = 0	2/4/2	1110	0010	0000	0000
			Branch Address			
	Branch on carry	2/4/2	1110	0011	0001	0001
			Branch Address			
	Branch if accumulator ≥ 0	2/4/2	1110	0011	1000	1100
			Branch Address			
	Branch if accumulator > 0	2/4/2	1110	0011	0000	0100
			Branch Address			
	Branch on I/O status low	2/4/3	1110	0000	0000	0000
			Branch Address			
	Branch if accumulator ≤ 0	2/4/2	1110	0011	1100	1100
			Branch Address			
BIT	Test bit	1/1	0100	BITx	IADD	RESS
BITT	Test bit specified by TREG	1/1	0110	1111	IADD	RESS
BLDD	Block move from data memory to data memory source immediate	2/3	1010	1000	IADD	RESS
			Branch Address			
	Block move from data memory to data memory destination immediate	2/3	1010	1001	IADD	RESS
			Branch Address			
BLPD	Block move from program memory to data memory	2/3	111	0011	IADD	RESS
			Branch Address			

Table 16. TMS320C2xx Instruction Set Summary (Continued)

C2xx MNEMONIC	DESCRIPTION	WORDS/ CYCLES	OPCODE MSB LSB
BCND	Branch if accumulator < 0	2/4/2	1110 0011 0100 0100 Branch Address
	Branch on no carry	2/4/2	1100 0011 0000 0001 Branch Address
	Branch if no overflow	2/4/2	1110 0011 0000 0010 Branch Address
	Branch if accumulator ≠ 0	2/4/2	1110 0011 0000 1000 Branch Address
	Branch on overflow	2/4/2	1110 0011 0010 0010 Branch Address
	Branch if accumulator = 0	2/4/2	1110 0011 1000 1000 Branch Address
CALA	Call subroutine indirect	1/4	1011 1110 0011 0000
CALL	Call subroutine	2/4	0111 1010 1ADD RESS Routine Address
CC	Conditional call subroutine	2/4/2	1110 10TP ZLVC ZLVC Routine Address
CMPL	Complement accumulator	1/1	1011 1110 0000 0001
CMPR	Compare auxiliary register with auxiliary register AR0	1/1	1011 1111 0100 01CM
CLRC	Configure block as data memory	1/1	1011 1110 0100 0100
SETC	Configure block as program memory	1/1	1011 1110 0100 0101
	Disable interrupt	1/1	1011 1110 0100 0001
DMOV	Data move in data memory	1/1	0111 0111 IADD RESS
CLRC	Enable interrupt	1/1	1011 1110 0100 0000
IDLE	Idle until interrupt	1/1	1011 1110 0010 0010
IN	Input data from port	2/2	1010 1111 IADD RESS 16BIT I/O PORT ADR S
INTR	Software interrupt	1/4	1011 1110 011I
LACC	Load accumulator with shift	1/1	0001 SHFT 1ADD RESS
LACL	Load accumulator immediate short	1/1	1011 1001 8BIT CNST
LACT	Load accumulator with shift specified by T register	1/1	0110 1011 IADD RESS
LACC	Load accumulator long immediate with shift	2/2	1011 1111 1000 SHFT 16-Bit Constant
LAR	Load auxiliary register	1/2	0000 0ARx IADD RESS
	Load auxiliary register short immediate	1/2	1011 0ARx 8BIT CNST
MAR	Load auxiliary register pointer	1/1	1000 1011 1000 1ARx
LDP	Load data-memory page pointer	1/2	0000 1101 IADD RESS
LDP	Load data-memory page pointer immediate	1/2	1011 110P AGE P OINT
LPH	Load high-P register	1/1	0111 0101 IADD RESS
LAR	Load auxiliary register long immediate	2/2	1011 1111 0000 1ARx 16-Bit Constant
LST	Load status register ST0	1/2	0000 1110 IADD RESS
	Load status register ST1	1/2	0000 1111 IADD RESS

ADVANCE INFORMATION

Table 16. TMS320C2xx Instruction Set Summary (Continued)

C2xx MNEMONIC	DESCRIPTION	WORDS/ CYCLES	OPCODE			
			MSB			LSB
LT	Load TREG	1/1	0111	0011	IADD	RESS
LTA	Load TREG and accumulate previous product	1/1	0111	0000	IADD	RESS
LTD	Load TREG, accumulate previous product, and move data	1/1	0111	0010	IADD	RESS
LTP	Load TREG and store P register in accumulator	1/1	0111	0001	IADD	RESS
LTS	Load TREG and subtract previous product	1/1	0111	0100	IADD	RESS
MAC	Multiply and accumulate	2/3	1010	0010	IADD	RESS
				16-Bit Constant		
MACD	Multiply and accumulate with data move	2/3	1010	0011	IADD	RESS
				16-Bit Constant		
MAR	Modify auxiliary register	1/1	1000	1011	IADD	RESS
MPY	Multiply (with TREG, store product in P register)	1/1	0101	0100	IADD	RESS
	Multiply immediate	1/1	110C	CNST	ANTx	xxxx
MPYA	Multiply and accumulate previous product	1/1	0101	0000	IADD	RESS
MPYS	Multiply and subtract previous product	1/1	0101	0001	IADD	RESS
MPYU	Multiply unsigned	1/1	0101	0101	IADD	RESS
NEG	Negate accumulator	1/1	1011	1110	0000	0010
NMI	Nonmaskable interrupt	1/4	1011	1110	0101	0010
NOP	No operation	1/1	1000	1011	0000	0000
NORM	Normalize contents of accumulator	1/1	1010	0000	IADD	RESS
OR	OR with accumulator	1/1	0110	1101	IADD	RESS
	OR immediate with accumulator with shift	2/2	1011	1111	1100	SHFT
				16-Bit Constant		
	OR immediate with accumulator with shift of 16	2/2	1011	1110	1000	0010
				16-Bit Constant		
OUT	Output data to port	2/3	0000	1100	IADD	RESS
			16BIT	I/O	PORT	ADRS
PAC	Load accumulator with P register	1/1	1011	1110	0000	0011
POP	Pop top of stack to low accumulator	1/1	1011	1110	0011	0010
POPD	Pop top of stack to data memory	1/1	1000	1010	IADD	RESS
PSHD	Push data-memory value onto stack	1/1	0111	0110	IADD	RESS
PUSH	Push low accumulator onto stack	1/1	1011	1110	0011	1100
CLRC	Reset carry bit	1/1	1011	1110	0100	1110
RETC	Conditional return from subroutine	1/4/2	1110	11TP	ZLVC	ZLVC
RET	Return from subroutine	1/4	1110	1111	0000	0000
ROL	Rotate accumulator left	1/1	1011	1110	0000	1100
ROR	Rotate accumulator right	1/1	1011	1110	0000	1101
CLRC	Reset overflow mode	1/1	1011	1110	0100	0010
	Reset sign-extension mode	1/1	1011	1110	0100	0110
	Reset test/control flag	1/1	1011	1110	0100	1010
	Reset external flag	1/1	1011	1110	0100	1100
RPT	Repeat instruction as specified by data-memory value	1/1	0000	1011	IADD	RESS
RPT	Repeat instruction as specified by immediate value	1/1	1011	1011	REPE	ATxx
SACH	Store high accumulator with shift	1/1	1001	1SHF	IADD	RESS

Table 16. TMS320C2xx Instruction Set Summary (Continued)

C2xx MNEMONIC	DESCRIPTION	WORDS/ CYCLES	OPCODE MSB			LSB
SACL	Store low accumulator with shift	1/1	1001	0SHF	IADD	RESS
SAR	Store auxiliary register	1/1	1000	OARx	IADD	RESS
SBRK	Subtract from auxiliary register short immediate	1/1	0111	1100	8BIT	CNST
SETC	Set carry bit	1/1	1011	1110	0100	1111
SFL	Shift accumulator left	1/1	1011	1110	0000	1001
SFR	Shift accumulator right	1/1	1011	1110	0000	1010
SETC	Set overflow mode	1/1	1011	1110	0100	0011
SPAC	Subtract P register from accumulator	1/1	1011	1110	0000	0101
SPH	Store high-P register	1/1	1000	1101	IADD	RESS
SPL	Store low-P register	1/1	1000	1100	IADD	RESS
SPM	Set P register output shift mode	1/1	1011	1111	IADD	RESS
SQRA	Square and accumulate	1/1	0101	0010	IADD	RESS
SQRS	Square and subtract previous product from accumulator	1/1	0101	0011	IADD	RESS
SST	Store status register ST0	1/1	1000	1110	IADD	RESS
SST	Store status register ST1	1/1	1000	1111	IADD	RESS
SPLK	Store long immediate to data memory	2/2	1010	1110	IADD	RESS
			16-Bit Constant			
SSXM	Set sign-extension mode	1/1	1011	1110	0100	0111
SETC	Set test/control flag	1/1	1011	1110	0100	1011
SUB	Subtract from accumulator long immediate with shift	2/2	1011	1111	1010	SHFT
			16-Bit Constant			
	Subtract from accumulator with shift	1/1	0011	SHFT	IADD	RESS
	Subtract from high accumulator	1/1	0110	0101	IADD	RESS
	Subtract from accumulator short immediate	1/1	1011	1010	8BIT	CNST
SUBB	Subtract from accumulator with borrow	1/1	0110	0100	IADD	RESS
SUBC	Conditional subtract	1/1	0000	1010	IADD	RESS
SUBS	Subtract from low accumulator with sign extension suppressed	1/1	0110	0110	IADD	RESS
SUBT	Subtract from accumulator with shift specified by TREG	1/1	0110	0111	IADD	RESS
SETC	Set external flag	1/1	1010	0110	IADD	RESS
TBLR	Table read	1/3	1010	0111	IADD	RESS
TBLW	Table write	1/3	1011	1110	0101	0001
TRAP	Software interrupt	1/4	1011	1110	0101	0001
XOR	Exclusive-OR with accumulator	1/1	0110	1100	IADD	RESS
	Exclusive-OR immediate with accumulator with shift	2/2	1011	1111	1101	SHFT
			16-Bit Constant			
	Exclusive-OR immediate with accumulator with shift of 16	2/2	1011	1110	1000	0011
			16-Bit Constant			
LACL	Zero accumulator	1/1	1011	1001	0000	0000
	Zero low accumulator and load high accumulator	1/1	0110	1010	IADD	RESS
	Zero low accumulator and load low accumulator with no sign extension	1/1	0110	1001	IADD	RESS
ZALR	Zero low accumulator and load high accumulator with rounding	1/1	0110	1000	IADD	RESS

ADVANCE INFORMATION

development support

Texas Instruments offers an extensive line of development tools for the 'C2xx generation of DSPs, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of 'C2xx-based applications:

Software Development Tools:
Assembler/Linker
Simulator
Optimizing ANSI C Compiler
Application Algorithms
C/Assembly Debugger and Code Profiler

Hardware Development Tools:
Emulator XDS510 (supports 'C2xx multiprocessor system debug)

The *TMS320 Family Development Support Reference Guide* (SPRU011D) contains information about development support products for all TMS320 family member devices, including documentation. Refer to this document for further information about TMS320 documentation or any other TMS320 support products from Texas Instruments. There is also an additional document, the *TMS320 Third Party Support Reference Guide* (SPRU052), which contains information about TMS320-related products from other companies in the industry. To receive copies of TMS320 literature, contact the Literature Response Center at 800/477-8924.

See Table 17 for complete listings of development support tools for the 'C2xx. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

Table 17. TMS320C2xx Development Support Tools

DEVELOPMENT TOOL	PLATFORM	PART NUMBER
	Software	
Compiler/Assembler/Linker	SPARC	TMDS3242555-08
Compiler/Assembler/Linker	PC-DOS™	TMDS3242855-02
Assembler/Linker	PC-DOS, OS/2™	TMDS3242850-02
Simulator	PC-DOS, WIN	TMDS3245851-02
Simulator	SPARC	TMDS3245551-01
Digital Filter Design Package	PC-DOS	DFDP
Debugger/Emulation Software	PC-DOS, OS/2, WIN	TMDS3240120
Debugger/Emulation Software	SPARC™	TMDS3240620
	Hardware	
XDS-510 XL Emulator	PC-DOS, OS/2	TMDS00510
XDS-510 WS Emulator	SPARC	TMDS00510WS

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SPARC is a trademark of SPARC International, Inc.
PC-DOS and OS/2 are trademarks of International Business Machines Corp.
XDS is a trademark of Texas Instruments Incorporated.

device and development support tool nomenclature

To designate the stages in the product development cycle, Texas Instruments assigns prefixes to the part numbers of all TMS320 devices and support tools. Each TMS320 member has one of three prefixes: TMX, TMP, and TMS. Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS). This development flow is defined below.

Device Development Evolutionary Flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications.

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification.

TMS Fully-qualified production device

Support Tool Development Evolutionary Flow:

TMDX Development support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully qualified development support product

TMX and TMP devices and TMDX development support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development support tools have been fully characterized, and the quality and reliability of the device has been fully demonstrated. Texas Instruments standard warranty applies.

Predictions show that prototype devices (TMX or TMP) will have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate is still undefined. Only qualified production devices are to be used.

ADVANCE INFORMATION

device and development support tool nomenclature (continued)

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, N, FN, or GB) and temperature range (for example, L). The following figures provide a legend for reading the complete device name for any TMS320 family member.

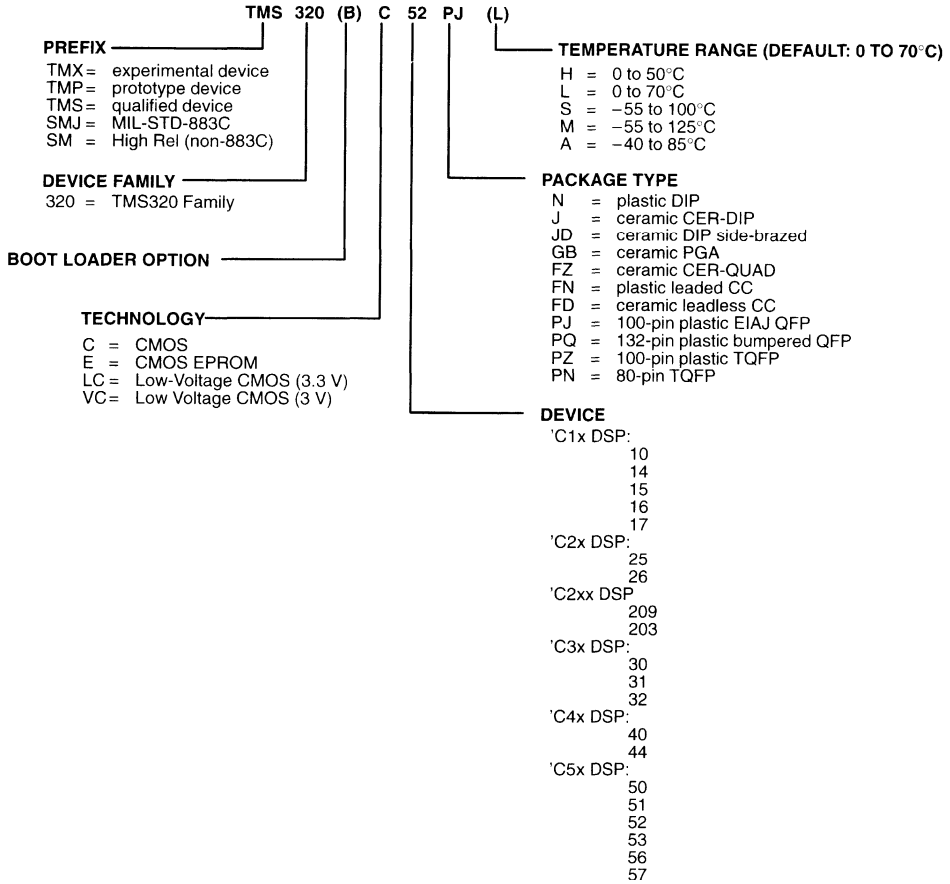

Figure 6. TMS320 Device Nomenclature

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device and development support tool nomenclature (continued)

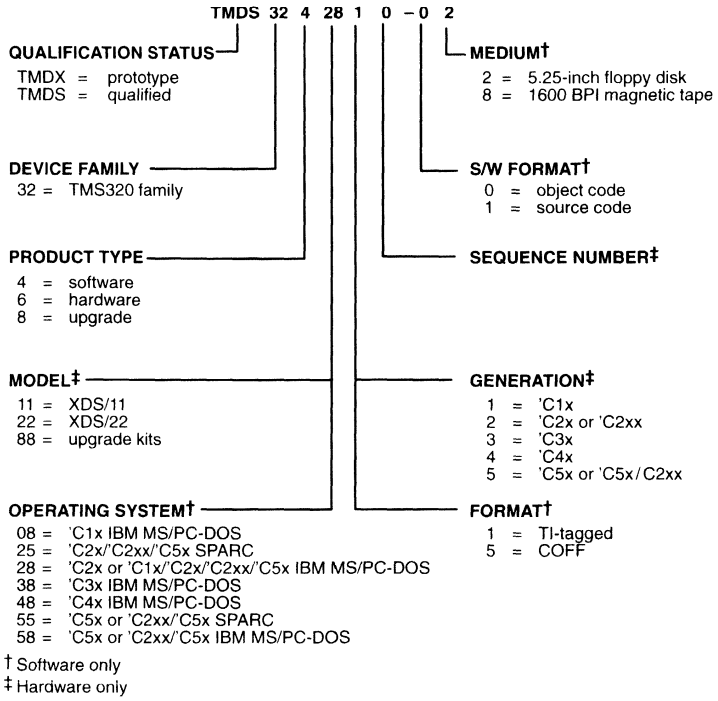


Figure 7. TMS320 Development Tool Nomenclature

documentation support

Extensive documentation supports all of the TMS320 family generations of devices from product announcement through applications development. The types of documentation available include data sheets, such as this document, with design specifications, complete user's guides for all devices and development support tools, and three volumes of the publication *Digital Signal Processing Applications with the TMS320 Family.*

The application book series describes hardware and software applications, including algorithms, for fixed and floating point TMS320 family devices. The *TMS320C2xx User's Guide,* which describes in detail the 2xx-generation TMS320 products, is also currently available.

A series of DSP textbooks is published by Prentice-Hall and John Wiley & Sons to support digital signal processing research and education. The TMS320 newsletter, *Details on Signal Processing*, is published quarterly and distributed to update TMS320 customers on product information. The TMS320 DSP bulletin board service (BBS) provides access to a wealth of information pertaining to the TMS320 family, including documentation and source and object code for many DSP algorithms and utilities. The BBS can be reached at 713/274-2323.

ADVANCE INFORMATION

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) ('320C2xx only)†

Supply voltage range, V_{DD} (see Note 1) . . . . . – 0.3 V to 7 V
Input voltage range . . . . . – 0.3 V to 7 V
Output voltage range . . . . . – 0.3 V to 7 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

TMS320C2xx recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	CLKIN	3		V_{DD} + 0.3	V
		$\overline{RS}$, CLKR, CLKX, RX, DR (203 only)	2			
		All others	2		V_{DD} + 0.3	
V_{IL}	Low-level input voltage	CLKIN	– 0.3		0.7	V
		$\overline{RS}$, CLKR, CLKX, RX, DR (203 only)			0.8	
		All others	– 0.3		0.8	
I_{OH}	High-level output current				– 300	μA
I_{OL}	Low-level output current				2	mA
T_C	Case temperature		0		85	°C

ADVANCE INFORMATION

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) ('320VC2xx only)†

Supply voltage range, V_{DD} (see Note 2) . . . . . – 0.3 V to 5 V
Input voltage range . . . . . – 0.3 V to 5 V
Output voltage range . . . . . – 0.3 V to 5 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: All voltage values are with respect to V_{SS}.

TMS320VC2xx recommended operating conditions

	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		2.7	3	3.3	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	CLKIN	2		V_{DD} + 0.3	V
		$\overline{RS}$, CLKR, CLKX, RX, DR (203 only)	0.7 V_{DD}			
		All others	1.8		V_{DD} + 0.3	
V_{IL}	Low-level input voltage	CLKIN	– 0.3		0.5	V
		$\overline{RS}$, CLKR, CLKX, RX, DR (203 only)			0.2 V_{DD}	
		All others	– 0.3		0.6	
I_{OH}	High-level output current				– 300	µA
I_{OL}	Low-level output current				2	mA
T_C	Case temperature		0		85	°C

ADVANCE INFORMATION

TMS320C2xx electrical characteristics over recommended ranges of supply voltage and operating free-air temperature @ 5 V

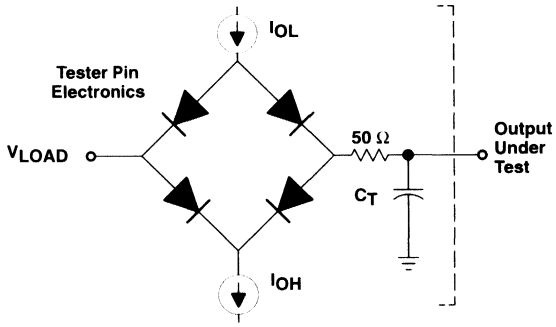
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	5-V operation, I_{OH} = MAX	2.4			V
V_{OL}	Low-level output voltage	5-V operation, I_{OH} = MAX			0.6	V
I_I	Input current	$V_I = V_{DD}$ or 0 V	– 10		10	μA
I_{OZ}	Off-state output current	$V_O = V_{DD}$ or 0 V			± 5	μA
I_{DD}	Supply current, core CPU	5-V operation, f_x = 80 MHz		76		mA
C_i	Input capacitance			15		
C_o	Output capacitance			15		

TMS320VC2xx electrical characteristics over recommended ranges of supply voltage and operating free-air temperature @ 3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	3-V operation, I_{OH} = MAX	2			V
V_{OL}	Low-level output voltage	3-V operation, I_{OH} = MAX			0.4	V
I_I	Input current	$V_I = V_{DD}$ or 0 V	– 10		10	μA
I_{OZ}	Off-state output current	$V_O = V_{DD}$ or 0 V			± 5	μA
I_{DD}	Supply current, core CPU	3-V operation, f_x = 57 MHz		32		mA
C_i	Input capacitance			15		pF
C_o	Output capacitance			15		pF

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



Where: I_{OL} = 2 mA (all outputs)
I_{OH} = 400 μA (all outputs)
V_{LOAD} = 1.5 V
C_T = 60-pF typical load-circuit capacitance

Figure 8. Test Load Circuit

signal-transition levels

The data in this section is shown for both the 5-V version ('C2xx) and the 3.0-V version ('VC2xx). In each case, the 5-V data is shown followed by the 3-V data in parentheses. TTL-output levels are driven to a minimum logic-high level of 2.4 V (2 V) and to a maximum logic-low level of 0.6 V (0.4 V). Figure 9 shows the TTL-level outputs.

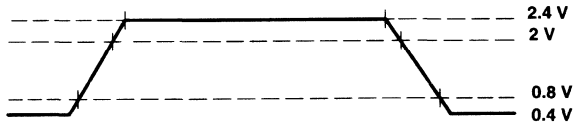


Figure 9. TTL-Level Outputs

TTL-output transition times are specified as follows:

- For a *high-to-low transition*, the level at which the output is said to be no longer high is 2 V (1.8 V) and the level at which the output is said to be low is 1 V (0.8 V).
- For a *low-to-high transition*, the level at which the output is said to be no longer low is 1 V (0.8 V) and the level at which the output is said to be high is 2 V (1.6 V).

Figure 10 shows the TTL-level inputs.

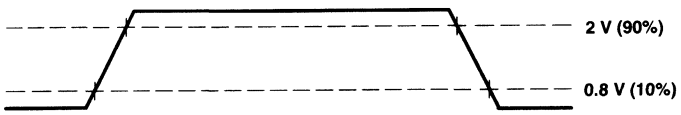


Figure 10. TTL-Level Inputs

TTL-compatible input transition times are specified as follows:

- For a *high-to-low transition* on an input signal, the level at which the input is said to be no longer high is 2 V (1.8 V) and the level at which the input is said to be low is 0.8 V (0.4 V).
- For a *low-to-high transition* on an input signal, the level at which the input is said to be no longer low is 0.8 V (0.4 V) and the level at which the input is said to be high is 2 V (1.8 V).

ADVANCE INFORMATION

CLOCK CHARACTERISTICS AND TIMING

TMS320C209 clock options

PARAMETER	CLKMOD
Internal divide by two with external crystal	0
PLL multiply by two	1

TMS320C203 clock options

PARAMETER	DIV2	DIV1
Internal divide by two with external crystal	0	0
PLL multiply by one	0	1
PLL multiply by two	1	0
PLL multiply by four	1	1

internal divide-by-two clock option with external crystal

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN. The frequency of CLKOUT1 is one-half the crystal's oscillating frequency. The crystal should be in either fundamental or overtone operation and parallel resonant, with an effective series resistance of 30 ohms and a power dissipation of 1 mW; it should be specified at a load capacitance of 20 pF. Note that overtone crystals require an additional tuned-LC circuit. Figure 11 shows an external crystal (fundamental frequency) connected to the on-chip oscillator.

TMS320C2xx timing at V_{pp} = 5 V with the PLL circuit disabled, divide-by-two mode

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
f_x	Input clock frequency	T_C = 0° C to 85° C	0†		80 57.14 40.96	MHz
C1, C2	Load capacitance			10		pF

† This device utilizes a fully static design and, therefore, can operate with input clock cycle time ($t_{c(CI)}$) approaching infinity. The device is characterized at frequencies approaching 0 Hz, but is tested at f_{clk} = 6.7 MHz to meet device test time requirements.

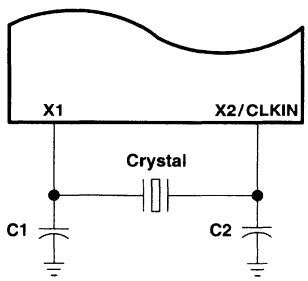


Figure 11. Internal Clock Option

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TMS320C2xx timing at V_{DD} = 5 V with the PLL circuit disabled, divide-by-two mode (continued)

TMS320C2xx switching characteristics over recommended operating conditions [H = 0.5 $t_{c(CO)}$]

PARAMETER		'320C2XX-40			'320C2XX-57			'320C2XX-80			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(CO)}$	Cycle time, CLKOUT1	48.8	$2t_{c(CI)}$	†	35	$2t_{c(CI)}$	†	25	$2t_{c(CI)}$	†	ns
$t_{d(CIH-CO)}$	Delay time, CLKIN high to CLKOUT1 high/low	1	11	20	1	11	20	1	9	18	ns
$t_{f(CO)}$	Fall time, CLKOUT1		5			5			4		ns
$t_{r(CO)}$	Rise time, CLKOUT1		5			5			4		ns
$t_{w(COL)}$	Pulse duration, CLKOUT1 low	H – 2	H	H + 2	H – 2	H	H + 2	H – 2	H	H + 2	ns
$t_{w(COH)}$	Pulse duration, CLKOUT1 high	H – 2	H	H + 2	H – 2	H	H + 2	H – 2	H	H + 2	ns

† This device is implemented in static logic and therefore can operate with $t_{c(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz, but is tested at $t_{c(CI)}$ = 300 ns to meet device test time requirements.

TMS320C2xx timing requirements over recommended operating conditions

		'320C2XX-40		'320C2XX-57		'320C2XX-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(CI)}$	Cycle time, CLKIN	25	†	17.5	†	12.5	†	ns
$t_{f(CI)}$	Fall time, CLKIN		5		5		4	ns
$t_{r(CI)}$	Rise time, CLKIN		5		5		4	ns
$t_{w(CIL)}$	Pulse duration, CLKIN low	11	†	8	†	5	†	ns
$t_{w(CIH)}$	Pulse duration, CLKIN high	11	†	8	†	5	†	ns

† This device is implemented in static logic and therefore can operate with $t_{c(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz, but is tested at $t_{c(CI)}$ = 150 ns to meet device test time requirements.

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TMS320VC2xx† timing at V_{DD} = 3 V with the PLL circuit disabled, internal divide-by-two mode

NAME	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
f_x	Input clock frequency	T_C = 0°C to 85°C	0‡	40.96	MHz

† TMS320VC2xx refers to the 3.0 V version of the TMS320C2xx

‡ This device is implemented in static logic and therefore can operate with $t_{c(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz, but is tested at f_x = 6.7 MHz to meet device test time requirements.

TMS320VC2xx switching characteristics over recommended operating conditions [H = 0.5 $t_{c(CO)}$]

PARAMETER		'320VC2XX-40			'320VCXX-57			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(CO)}$	Cycle time, CLKOUT1	50	$2_{c(CI)}$	‡	35	$2t_{c(CI)}$	‡	ns
$t_{d(CIH-CO)}$	Delay time, CLKIN high to CLKOUT1 high/low	3	11	20	1	11	20	ns
$t_{f(CO)}$	Fall time, CLKOUT1		5			5		ns
$t_{r(CO)}$	Rise time, CLKOUT1		5			5		ns
$t_{w(COL)}$	Pulse duration, CLKOUT1 low	H – 3	H	H + 2	H – 2	H	H + 2	ns
$t_{w(COH)}$	Pulse duration, CLKOUT1 high	H – 3	H	H + 2	H – 2	H	H + 2	ns

‡ This device is implemented in static logic and therefore can operate with $t_{c(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz, but is tested at $t_{c(CI)}$ = 300 ns to meet device test time requirements.

TMS320VC2xx timing requirements over recommended operating conditions

		'320VC2XX-40		'320VC2XX-57		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(CI)}$	Cycle time, CLKIN	25	‡	17.5	‡	ns
$t_{f(CI)}$	Fall time, CLKIN		5		5	ns
$t_{r(CI)}$	Rise time, CLKIN		5		5	ns
$t_{w(CIL)}$	Pulse duration, CLKIN low	9	‡	8	‡	ns
$t_{w(CIH)}$	Pulse duration, CLKIN high	9	‡	8	‡	ns

‡ This device is implemented in static logic and therefore can operate with $t_{c(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz, but is tested at $t_{c(CI)}$ = 150 ns to meet device test time requirements.

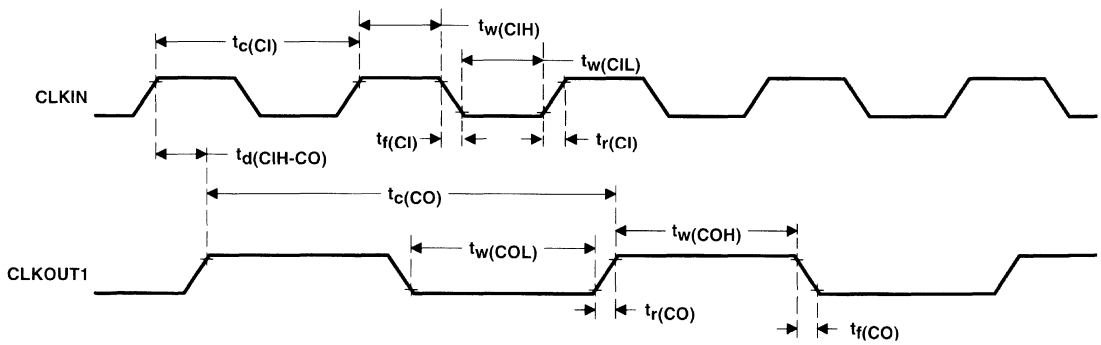

Figure 12. CLKIN-to-CLKOUT Timing Without PLL (using ÷2 clock option)

timing with the PLL circuit enabled x2 mode

NAME	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
f_x	Input clock frequency	T_C = 0°C to 85°C, 3 V	5	14.25	MHz
		T_C = 0°C to 85°C, 5 V	5	20	MHz

switching characteristics over recommended operating conditions @ 5 V [H = 0.5$t_{c(CO)}$]

PARAMETER		'320C2XX-40			'320C2XX-57			'320C2XX-80			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(CO)}$	Cycle time, CLKOUT1	50		100	35		75	25		55	ns
$t_{d(CIH-CO)}$	Delay time, CLKIN high to CLKOUT1 high/low	3	8	18	3	8	18	1	8	16	ns
$t_{f(CO)}$	Fall time, CLKOUT1		5			5			4		ns
$t_{r(CO)}$	Rise time, CLKOUT1		5			5			4		ns
$t_{w(COL)}$	Pulse duration, CLKOUT1 low	H – 2	H	H + 2	H – 2	H	H + 2	H – 2	H	H + 2	ns
$t_{w(COH)}$	Pulse duration, CLKOUT1 high	H – 2	H	H + 2	H – 2	H	H + 2	H – 2	H	H + 2	ns
t_p	Transition time, PLL synchronized after CLKIN supplied			1000			1000			1000	cycles

timing requirements over recommended operating conditions @ 5 V

		'320C2XX-40		'320C2XX-57		'320C2XX-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(CI)}$	Cycle time, CLKIN multiply by one	50	100	35	75	25	75	ns
	Cycle time, CLKIN multiply by two	100	200	70	200	50	150	ns
$t_{f(CI)}$	Fall time, CLKIN		4		4		4	ns
$t_{r(CI)}$	Rise time, CLKIN		4		4		4	ns
$t_{w(CIL)}$	Pulse duration, CLKIN low	16	95	14	95	11	95	ns
$t_{w(CIH)}$	Pulse duration, CLKIN high	16	95	14	95	11	95	ns

switching characteristics over recommended operating conditions @ 3 V

		'320C2XX-40			'320C2XX-57			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(CO)}$	Cycle time, CLKOUT1	50	$2t_{c(CI)}$	75	35	$2t_{c(CI)}$	75	ns
$t_{d(CIH-CO)}$	Delay time, CLKIN high to CLKOUT1 high/low	3	8	18	3	8	118	ns
$t_{f(CO)}$	Fall time, CLKOUT1		5			5		ns
$t_{r(CO)}$	Rise time, CLKOUT1		5			5		ns
$t_{w(COL)}$	Pulse duration, CLKOUT low	H – 2	H	H + 2	H – 2	H	H + 2	ns
$t_{w(COH)}$	Pulse duration, CLKOUT high	H – 2	H	H + 2	H – 2	H	H + 2	ns
t_p	Transition time, PLL synchronized after CLKIN supplied			1000			1000	cycles

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timing requirements over recommended operating conditions @ 3 V

		'320C2XX-40		'320C2XX-57		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(CI)}$	Cycle time, CLKIN multiply by one	50	75	35	75	ns
	Cycle time, CLKIN multiply by two	100	150	70	200	ns
$t_{f(CI)}$	Fall time, CLKIN		5		4	ns
$t_{r(CI)}$	Rise time, CLKIN		5		4	ns
$t_{w(CIL)}$	Pulse duration, CLKIN low	15	95	15	95	ns
$t_{w(CIH)}$	Pulse duration, CLKIN high	15	95	15	95	ns

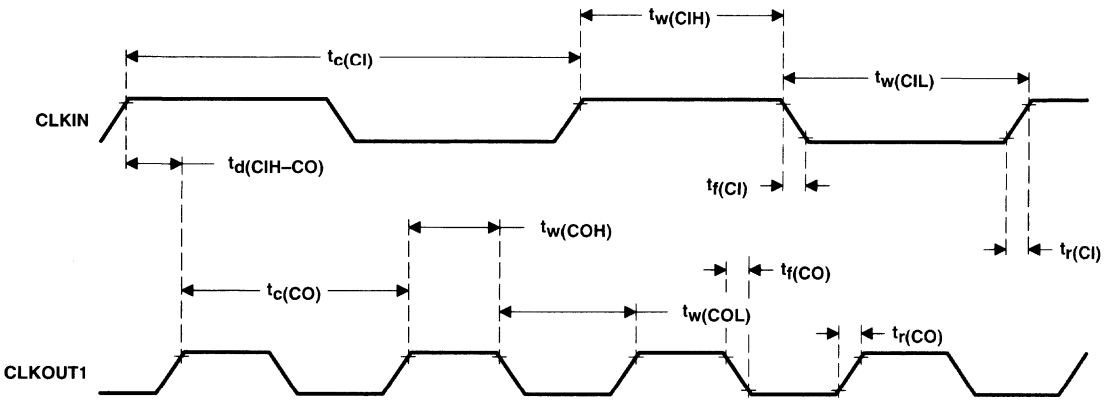

Figure 13. CLKIN-to-CLKOUT Timing With PLL (using ×2 clock option)

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PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols used are created in accordance with JEDEC Standard 100-A. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

A	A[15:0]	MS	Memory strobe pins $\overline{IS}$, $\overline{DS}$ or $\overline{PS}$
CI	CLKIN/X2	R	READY
C0	CLKOUT1	RD	Read cycle or $\overline{RD}$
D	D[15:0]	RS	RESET pins RS or $\overline{RS}$
IN	INT[3:1] or $\overline{INTx}$	W	Write cycle or $\overline{WE}$

Lowercase subscripts and their meanings are:

a	access time
c	cycle time (period)
d	delay time
f	full time
h	hold time
r	rise time
su	setup time
t	transition time
v	valid time
w	pulse duration (width)

The following letters and symbols and their meanings are:

H	High
L	Low
V	Valid
Z	High impedance
X	Unknown, changing, or don't care level

general notes on timing parameters

All output signals from the TMS320C2xx devices (including CLKOUT1) are derived from an internal clock such that all output transitions for a given half cycle occur with a minimum of skewing relative to each other.

The signal combinations shown in the following timing diagrams may not necessarily represent actual cycles. For actual cycle examples, refer to the appropriate cycle description section of this data sheet.

ADVANCE INFORMATION

MEMORY AND PERIPHERAL INTERFACE TIMING

memory and parallel I/O interface read timing

A15–A0, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, $\overline{RW}$, and $\overline{BR}$ timings are all included in the timings referenced to A15–A0 except when in transition between read and write operations where $\overline{PS}$, $\overline{DS}$, and $\overline{IS}$ pulse high [see $t_{w(NSN)}$].

switching characteristics over recommended operating conditions @ 5 V [H = 0.5$t_{c(CO)}$]

PARAMETER		'320C2XX-40		'320C2XX-57		'320C2XX-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{su(A)RD}$	Setup time, address valid before $\overline{RD}$ low	H – 7		H – 5		H – 5		ns
$t_{h(A)RD}$	Hold time, address valid after $\overline{RD}$ high	– 6		– 6		– 6		ns
$t_{d(CO-A)}$	Delay time, address valid after CLKOUT1 low		8		8		8	ns
$t_{h(A)CO}$	Hold time, address valid after CLKOUT1 low	– 2		– 2		– 2		ns
$t_{d(CO-RD)}$	Delay time, CLKOUT1 high/low to $\overline{RD}$ low/high	0	6	0	6	0	6	ns
$t_{d(CO-S)}$	Delay time, CLKOUT1 low to $\overline{STRB}$ low/high †	– 1	4	0	5	0	5	ns
$t_{w(RDL)}$	Pulse duration, $\overline{RD}$ low (no wait states)	H – 3	H + 2	H – 3	H + 2	H – 3	H + 2	ns
$t_{w(RDH)}$	Pulse duration, $\overline{RD}$ high	H – 4	H + 2	H – 4	H + 2	H – 3	H + 2	ns
$t_{d(RDW)}$	Delay time, $\overline{RD}$ high to $\overline{WE}$ low	2H – 8		2H – 8		2H – 7		ns

† Values derived from characterization data and not tested.

timing requirements over recommended operating conditions @ 5 V [H = 0.5$t_{c(CO)}$]

		'320C2XX-40		'320C2XX-57		'320C2XX-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time, read data from address time		2H – 18		2H – 15		2H – 12	ns
$t_{su(D)RD}$	Setup time, data read before $\overline{RD}$ high	13		13		10		ns
$t_{h(D)RD}$	Hold time, data read from $\overline{RD}$ high	– 2		– 2		– 2		ns
$t_{h(D)A}$	Hold time, read data from address invalid	0		0		0		ms
$t_{su(DCOL)R}$	Setup time, data read before CLKOUT1 low	9		9		8		ns
$t_{h(DCOL)R}$	Hold time, data read from CLKOUT1 low	– 1		– 1		– 1		ns
$t_{a(RD)}$	Access time, read data after $\overline{RD}$ low		H – 12		H – 12		H – 10	ns

ADVANCE INFORMATION

memory and parallel I/O interface read timing (continued)

A15–A0, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, $\overline{RW}$, and $\overline{BR}$ timings are all included in the timings referenced to A15–A0 except when in transition between read and write operations where $\overline{PS}$, $\overline{DS}$, and $\overline{IS}$ pulse high [see $t_{w(NSN)}$].

switching characteristics over recommended operating conditions @ 3 V [H = 0.5$t_{c(CO)}$]

PARAMETER		MIN	MAX	MIN	MAX	UNIT
$t_{su(A)RD}$	Setup time, address valid before $\overline{RD}$ low	H – 7		H – 5		ns
$t_{h(A)RD}$	Hold time, address valid after $\overline{RD}$ high	– 6		– 6		ns
$t_{d(A)CO}$	Delay time, address valid after CLKOUT1 low		8		8	ns
$t_{h(A)CO}$	Hold time, address valid after CLKOUT1 low	– 2		– 2		ns
$t_{d(CO-RD)}$	Delay time, CLKOUT1 high/low to $\overline{RD}$ low/high	– 1	5	– 1	5	ns
$t_{d(CO-S)}$	Delay time, CLKOUT1 low to $\overline{STRB}$ low/high †	1	5	1	5	ns
$t_{w(RDL)}$	Pulse duration, $\overline{RD}$ low (no wait states)	H – 3	H + 2	H – 3	H + 2	ns
$t_{w(RDH)}$	Pulse duration, $\overline{RD}$ high	H – 4	H + 2	H – 4	H + 2	ns
$t_{d(RDW)}$	Delay time, $\overline{RD}$ high to $\overline{WE}$ low	2H – 8		2H – 8		

† Values derived from characterization data and not tested.

timing requirements over recommended operating conditions @ 3 V [H = 0.5$t_{c(CO)}$]

		MIN	MAX	MIN	MAX	UNIT
$t_{a(A)}$	Access time, read data from address time †		2H – 14		2H – 14	ns
$t_{su(D)RD}$	Setup time, data read before $\overline{RD}$ high	13		13		ns
$t_{h(D)RD}$	Hold time, data read from $\overline{RD}$ high	– 2		– 2		ns
$t_{h(D)A}$	Hold time, read data from address invalid	0		0		ms
$t_{su(DCOL)R}$	Setup time, data read before CLKOUT1 low	9		9		ns
$t_{h(DCOL)R}$	Hold time, data read from CLKOUT1 low	– 1		– 1		ns
$t_{a(RD)}$	Access time, read data after $\overline{RD}$ low		H – 12		H – 12	ns

† Values derived from characterization data and not tested.

ADVANCE INFORMATION

memory and parallel I/O interface write timing (continued)

A15–A0, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, $\overline{RW}$, and $\overline{BR}$ timings are all included in the timings referenced to A15–A0 except when in transition between read and write operations where $\overline{PS}$, $\overline{DS}$, and $\overline{IS}$ pulse high [see $t_{w(MSH)}$].

switching characteristics over recommended operating conditions @ 5 V [H = 0.5$t_{c(CO)}$]

PARAMETER		'320C2XX-40		'320C2XX-57		'320C2XX-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{su(A)W}$	Setup time, address valid before $\overline{WE}$ low	H – 7		H – 7		H – 6		ns
$t_{h(A)W}$	Hold time, address valid after $\overline{WE}$ high	H – 10		H – 10		H – 8		ns
$t_{su(A)CO}$	Setup time, address valid before CLKOUT1 low	H – 9		H – 9		H – 8		ns
$t_{h(A)COw}$	Hold time, address valid after CLKOUT1 low	H – 3		H – 3		H – 2		ns
$t_{w(NSN)}$	Pulse duration, $\overline{IS}$, $\overline{DS}$, $\overline{PS}$ inactive high†	H – 9		H – 9		H – 8		ns
$t_{w(WL)}$	Pulse duration, $\overline{WE}$ low (no wait states)	2H – 2	2H + 2	2H – 2	2H + 2	2H – 2	2H + 2	ns
$t_{w(WH)}$	Pulse duration, $\overline{WE}$ high	2H – 2		2H – 2		2H – 2		ns
$t_{d(CO-W)}$	Delay time, CLKOUT1 low to $\overline{WE}$ low/high	0	6	0	6	0	6	ns
$t_{d(WRD)}$	Delay time, $\overline{WE}$ high to $\overline{RD}$ low	3H – 10		3H – 8		3H – 8		ns
$t_{su(D)W}$	Setup time, write data valid before $\overline{WE}$ high	2H – 15	2H†	2H – 15	2H†	2H – 14	2H†	ns
$t_{h(D)W}$	Hold time, write data valid after $\overline{WE}$ high	H – 4	H + 7†	H – 4	H + 7†	H – 3	H + 7†	ns
$t_{su(DCOL)W}$	Setup time, write data valid before CLKOUT1 low	2H – 20	2H†	2H – 20	2H†	2H – 20	2H†	ns
$t_{h(DCOL)W}$	Hold time, write data valid after CLKOUT1 low	H – 4	H + 11†	H – 4	H + 11†	H – 5	H + 11†	ns
$t_{en(D)W}$	Enable time, $\overline{WE}$ to data bus driven †	– 4		– 4		– 3		ns

† Values derived from characterization data and not tested.

switching characteristics over recommended operating conditions @ 3 V [H = 0.5$t_{c(CO)}$]

PARAMETER		'320VC2XX-40 '320VC2XX-57		UNIT
		MIN	MAX	
$t_{su(A)W}$	Setup time, address valid before $\overline{WE}$ low	H – 5		ns
$t_{h(A)W}$	Hold time, address valid after $\overline{WE}$ high	H – 10		ns
$t_{su(A)CO}$	Setup time, address valid before CLKOUT1 low	H – 9		ns
$t_{h(A)COw}$	Hold time, address valid after CLKOUT1 low	H – 3		ns
$t_{w(NSN)}$	Pulse duration, $\overline{IS}$, $\overline{DS}$, $\overline{PS}$ inactive high†	H – 9		ns
$t_{w(WL)}$	Pulse duration, $\overline{WE}$ low (no wait states)	2H – 2	2H + 2	ns
$t_{w(WH)}$	Pulse duration, $\overline{WE}$ high	2H – 2		ns
$t_{d(CO-W)}$	Delay time, CLKOUT1 low to $\overline{WE}$ low/high	0	6	ns
$t_{d(WRD)}$	Delay time, $\overline{WE}$ high to $\overline{RD}$ low	3H – 8		ns
$t_{su(D)W}$	Setup time, write data valid before $\overline{WE}$ high	2H – 15	2H†	ns
$t_{h(D)W}$	Hold time, write data valid after $\overline{WE}$ high	H – 4	H + 7†	ns
$t_{su(DCOL)W}$	Setup time, write data valid before CLKOUT1 low	2H – 20	2H†	ns
$t_{h(DCOL)W}$	Hold time, write data valid after CLKOUT1 low	H – 4	H + 11	ns
$t_{en(D)W}$	Enable time, $\overline{WE}$ to data bus driven†	– 4		ns

† Values derived from characterization data and not tested.

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PARAMETER MEASUREMENT INFORMATION

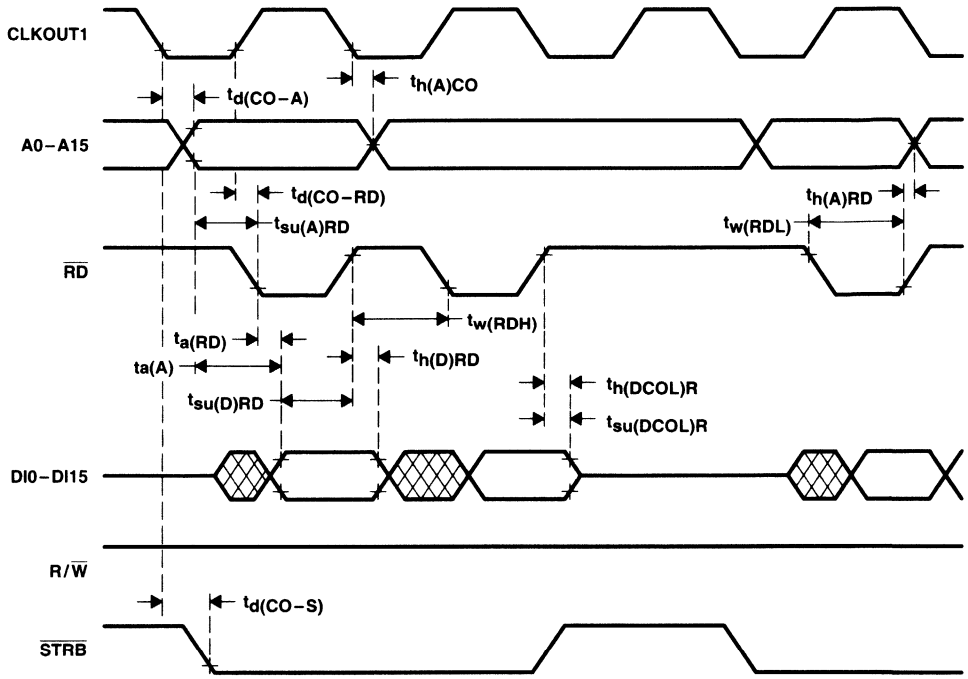


Figure 14. Memory Interface Read Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

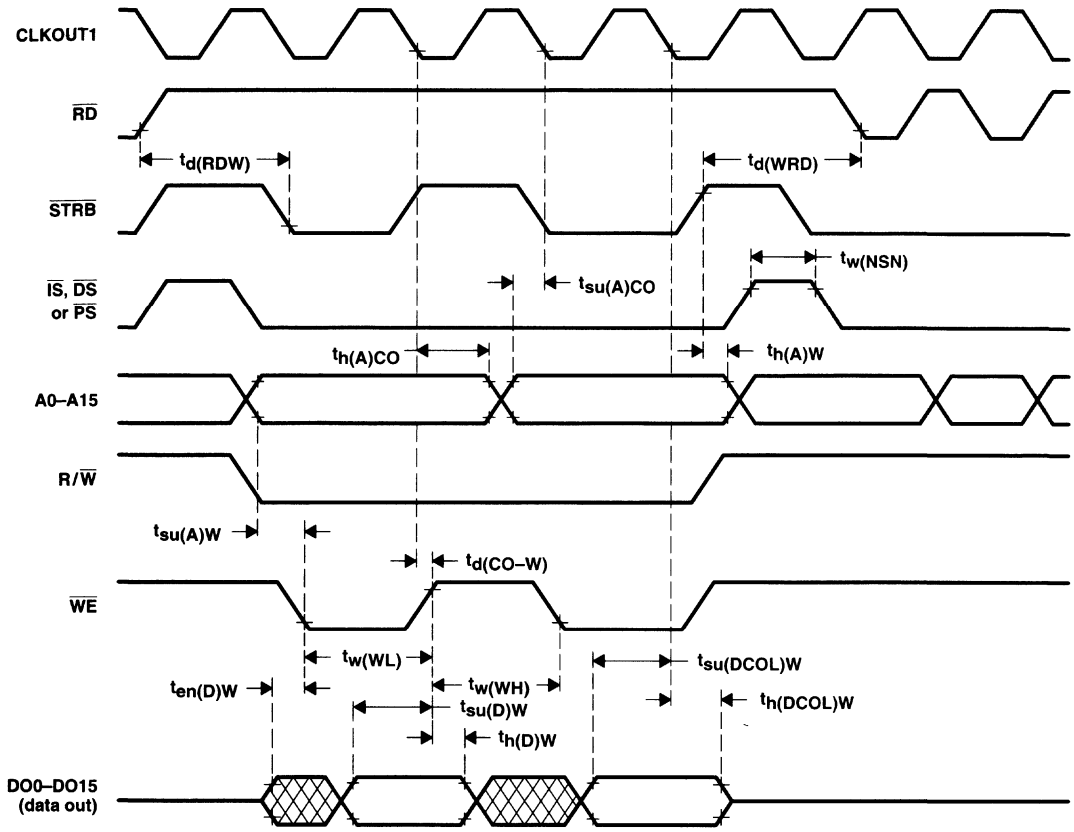


Figure 15. Memory Interface Write Timing

READY timing

timing requirements over recommended operating conditions [H = 0.5$t_{c(CO)}$]

		'320C2XX-40, '320C2XX57, 3/5 V†		'320C2XX-80 5 V		UNIT
		MIN	MAX	MIN	MAX	
$t_{su(R-CO)}$	Setup time, READY before CLKOUT1 rises	11		8		ns
$t_{h(CO-R)}$	Hold time, READY low after CLKOUT1 rises	0		0		ns
$t_{su(R)RD}$	Setup time, READY before $\overline{RD}$ falls	14		11		ns
$t_{h(R)RD}$	Hold time, READY after $\overline{RD}$ falls	4		4		ns
$t_{v(R)W}$	Valid time, READY after $\overline{WE}$ falls	H – 13		H – 10		ns
$t_{h(R)W}$	Hold time, READY after $\overline{WE}$ falls	H + 4		H + 3		ns
$t_{v(R)Ar}$	Valid time, READY after address valid on read	H – 17		H – 15		ns
$t_{v(R)Aw}$	Valid time, READY after address valid on write	2H – 18		2H – 16		ns

† 3-V operation, 'C203 only

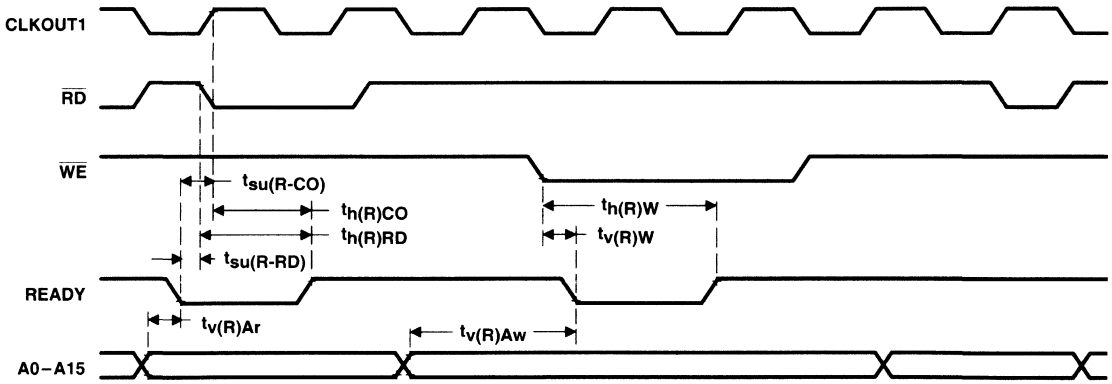


Figure 16. READY Timing

ADVANCE INFORMATION

$\overline{RS}$, $\overline{INT1}$–$\overline{INT3}$, $\overline{NMI}$, $\overline{BIO}$, TOUT, and XF timing

INTN refers to $\overline{BIO}$, $\overline{INT1}$–$\overline{INT3}$, and $\overline{NMI}$.

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$]

		'320C2XX-40, '320C2XX57, 3/5 V†		'320C2XX-80 5 V		UNIT
	PARAMETER	MIN	MAX	MIN	MAX	UNIT
$t_{d(XF)}$	Delay time, XF valid after CLKOUT1	0‡	13	0‡	10	ns
$t_{d(TOUT)}$	Delay time, TOUT high/low after CLKOUT1	0‡	11	0‡	11	ns
$t_{w(TOUT)}$	Pulse duration, TOUT high	2H – 12		2H – 9		ns

† 3-V operation, 'C203 only
‡ Values derived from characterization data and not tested.

timing requirements over recommended operating conditions [H = 0.5$t_{c(CO)}$]

		'320C2XX-40, '320C2XX57, 3/5 V†		'320C2XX-80 5 V		UNIT
		MIN	MAX	MIN	MAX	UNIT
$t_{su(RS)CI}$	Setup time, $\overline{RS}$ no longer high before CLKIN low	11		9		ns
$t_{su(RS)CO}$	Setup time, $\overline{RS}$ no longer low before CLKOUT1 low	14		10		ns
$t_{w(RSL)}$	Pulse duration, $\overline{RS}$ low	12H		12H		ns
$t_{d(EX)}$	Delay time, $\overline{RS}$ high to reset-vector fetch	34H		34H		ns
$t_{su(IN)CO}$	Setup time, $\overline{INTx}$ before CLKOUT1 low (synchronous)	10		10		ns
$t_{h(IN)CO}$	Hold time, $\overline{INTx}$ after CLKOUT1 low (synchronous)	0		0		ns
$t_{w(IN)}$	Pulse duration, $\overline{INTx}$ low/high	2H + 18		2H + 16		ns
$t_{d(IN)}$	Delay time, $\overline{INTx}$ low to interrupt-vector fetch	12H		12H		ns

† 3-V operation, 'C203 only

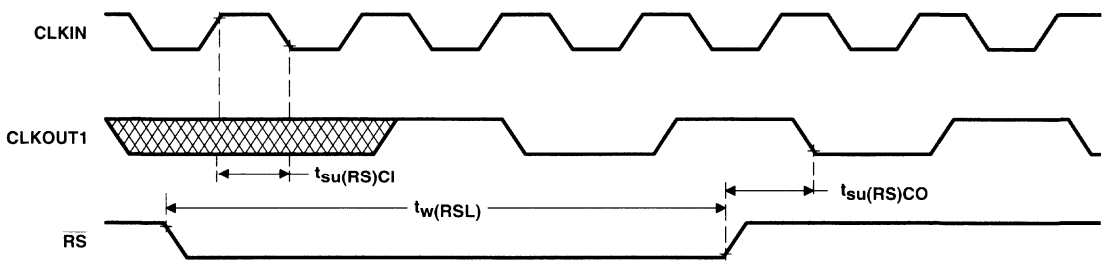


Figure 17. Reset Timing

ADVANCE INFORMATION

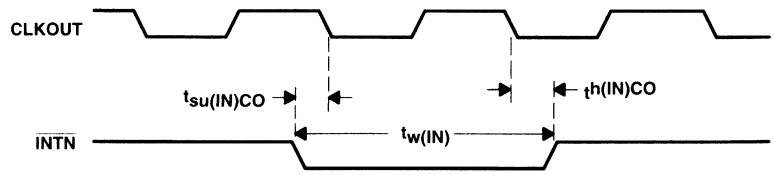


Figure 18. Interrupt and $\overline{BIO}$ Timing

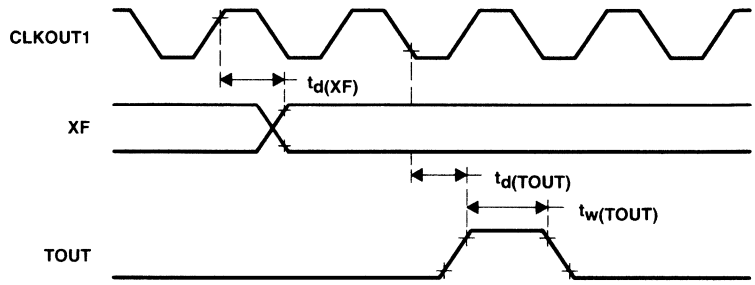


Figure 19. XF and TOUT Timing

external DMA timing

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$]

		'320C2XX-40, '320C2XX57, 3/5 V†		'320C2XX-80 5 V		UNIT
		MIN	MAX	MIN	MAX	UNIT
$t_{d(H-HA)}$	Delay time, $\overline{HOLD}$ low to $\overline{HOLDA}$ low	4H		4H		ns
$t_{d(HH-HA)}$	Delay time, $\overline{HOLD}$ high before $\overline{HOLDA}$ high	2H		2H		ns
$t_{z(M-HA)}$	Address high impedance before $\overline{HOLDA}$ low (see Note 3)	H – 15		H – 10		ns
$t_{en(HA-M)}$	Enable time, $\overline{HOLDA}$ high to address driven	H – 5		H – 4		ns

† 3-V operation, 'C203 only
NOTE 3: This parameter includes all memory control lines.

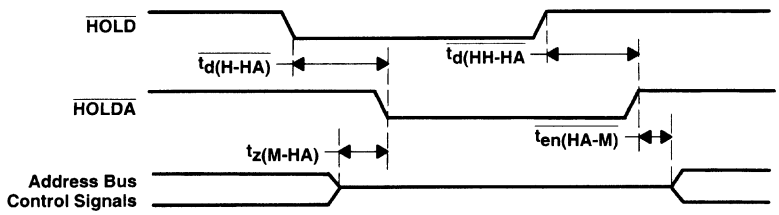


Figure 20. External DMA Timing

ADVANCE INFORMATION

$\overline{\text{IACK}}$ timing

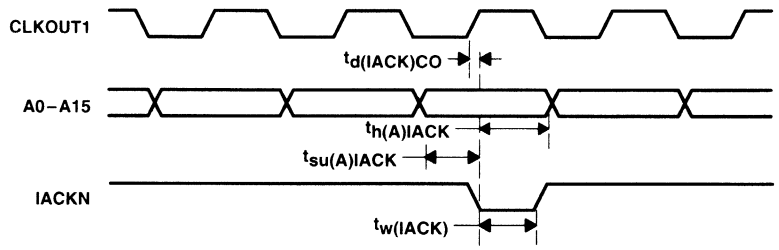
$\overline{\text{IACK}}$ goes low during the fetch of the first word of the interrupt vector. It goes low only on the first cycle of the read when wait states are used. Address pins A1–A4 can be decoded at the falling edge to identify the interrupt being acknowledged.

switching characteristics over recommended operating conditions [H = 0.5 $t_{c(CO)}$]

		'320C2XX-40, '320C2XX57, 5 V†		UNIT
NAME	PARAMETER	MIN	MAX	UNIT
$t_{su(A)IACK}$	Setup time, address valid before $\overline{\text{IACK}}$ low	H – 9		ns
$t_{h(A)IACK}$	Hold time, address valid after $\overline{\text{IACK}}$ high	H – 7		ns
$t_{w(IACK)}$	Pulse duration, $\overline{\text{IACK}}$ low	H – 7		ns
$t_{d(IACK)CO}$	Delay time, CLKOUT1 to $\overline{\text{IACK}}$ low	– 1‡	3	ns

† C209 only

‡ Values derived from characterization data and not tested.



NOTE A: $\overline{\text{IACK}}$ are not affected by wait states.

Figure 21. $\overline{\text{IACK}}$ Timing

ADVANCE INFORMATION

serial-port receive timing

timing requirements over recommended ranges of supply voltage and operating free-air temperature [H = $0.5t_{c(CO)}$]

		'320C2XX-40, '320C2XX57, 3/5 V†		'320C2XX-80 5 V		UNIT
		MIN	MAX	MIN	MAX	UNIT
$t_{c(SCK)}$	Cycle time, serial port clock	4H		4H		ns
$t_{f(SCK)}$	Fall time, serial port clock		8		6	ns
$t_{r(SCK)}$	Rise time, serial port clock		8		6	ns
$t_{w(SCK)}$	Pulse duration, serial port clock low/high	2H		2H		ns
$t_{su(FS)}$	Setup time, FSR before CLKR falling edge	10		7		ns
$t_{su(DR)}$	Setup time, DR before CLKR falling edge	10		7		ns
$t_{h(FS)}$	Hold time, FSR after CLKR falling edge	10		7		ns
$t_{h(DR)}$	Hold time, DR after CLKR falling edge	10		7		ns

† 3-V operation, 'C203 only

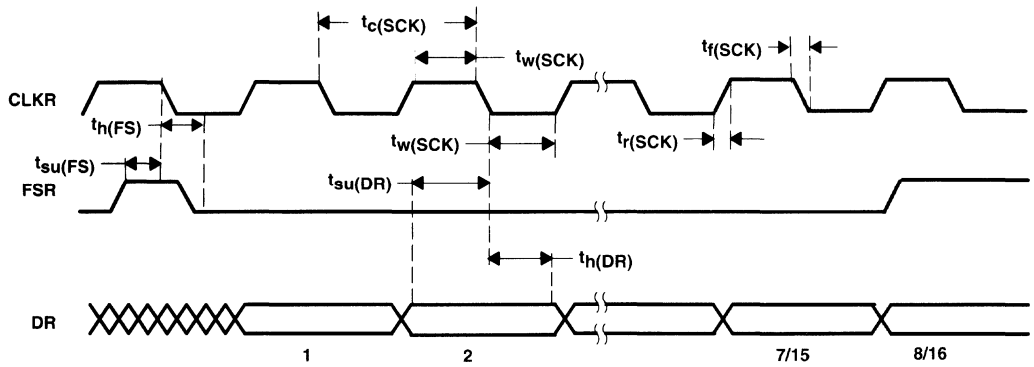


Figure 22. Serial-Port Receive Timing

serial port transmit, external clocks, and external frames

switching characteristics over recommended operating conditions

PARAMETER		MIN	MAX	UNIT
$t_{d(DX)}$	Delay time, DX valid after CLKX high		25	ns
$t_{dis(DX)}$	Disable time, DX after CLKX high		40	ns
$t_{h(DX)}$	Hold time, valid after CLKX high	– 5		ns

serial port transmit, external clocks, and external frames (continued)

timing requirements over recommended ranges of supply voltage and operating free-air temperature [H = 0.5$t_{c(CO)}$]

		'320C2XX-40, '320C2XX57, 3/5 V†		'320C2XX-80 5 V		UNIT
		MIN	MAX	MIN	MAX	UNIT
$t_{c(SCK)}$	Cycle time, serial port clock	4H		4H		ns
$t_{f(SCK)}$	Fall time, serial port clock		8		6	ns
$t_{r(SCK)}$	Rise time, serial port clock		8		6	ns
$t_{w(SCK)}$	Pulse duration, serial port clock low/high	2H		2H		ns
$t_{d(FS)}$	Delay time, FSX after CLKX rising edge high		2H – 8		2H – 8	ns
$t_{h(FS)}$	Hold time, FSX after CLKX falling edge low	10		7		ns
$t_{h(FS)H}$	Hold time, FSX after CLKX rising edge high		2H – 8		2H – 8	ns

† 3-V operation, 'C203 only

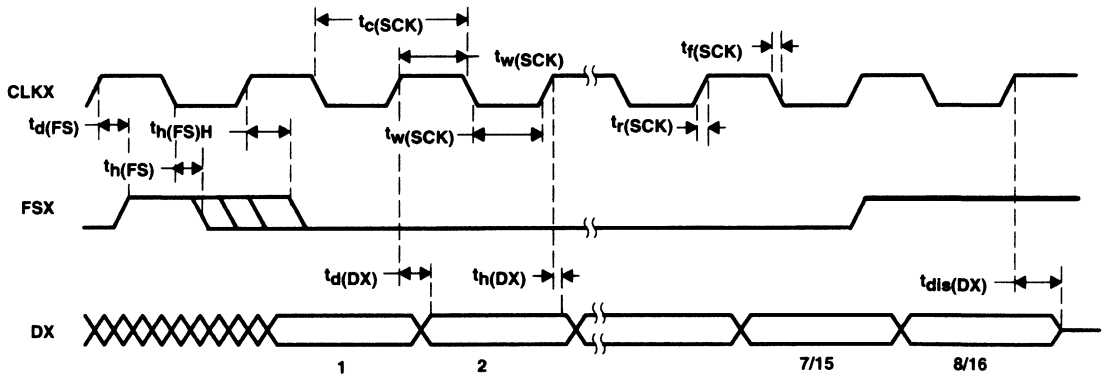


Figure 23. Serial-Port Transmit Timing of External Clocks and External Frames

ADVANCE INFORMATION

serial port transmit, internal clocks, and internal frames

switching characteristics over recommended operating conditions, H = 0.5$t_{c(CO)}$

PARAMETER		'320C2XX-40, '320C2XX57, 3/5 V†			'320C2XX-80 5 V			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$t_{d(FS)}$	Delay time, CLKX rising to FSX	– 5		25	– 4		18	ns
$t_{d(DX)}$	Delay time, CLKX to DX			25			18	ns
$t_{dis(DX)}$	Disable time, CLKX rising to DX			40			29	ns
$t_{c(SCK)}$	Cycle time, serial port clock		4H			4H		ns
$t_{f(SCK)}$	Fall time, serial port clock		5			4		ns
$t_{r(SCK)}$	Rise time, serial port clock		5			4		ns
$t_{w(SCK)}$	Pulse duration, serial port clock low/high	2H – 20			2H – 16			ns
$t_{h(DX)}$	Hold time, DX valid after CLKX rising high	– 5			– 4			ns

† 3-V operation, 'C203 only

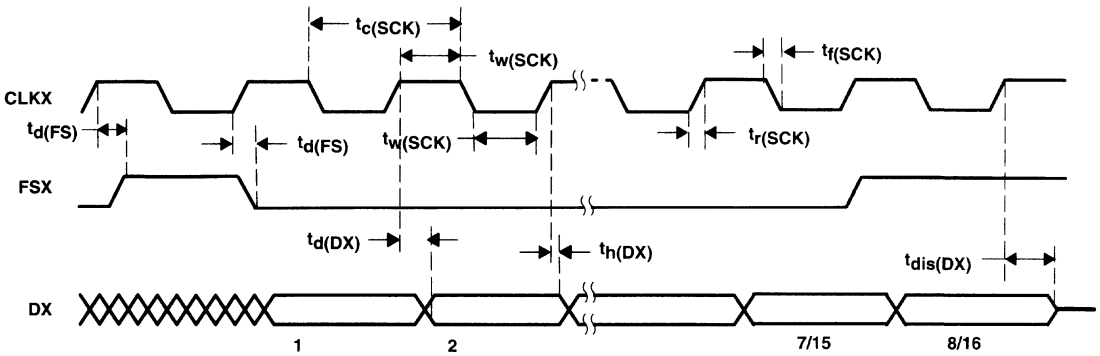


Figure 24. Serial Port Transmit Timing of Internal Clocks and Internal Frames

- Powerful 16-Bit TMS320C5x CPU
- 20-, 25-, 35-, and 50-ns Single-Cycle Instruction Execution Time for 5-V Operation
- 25-, 40-, and 50-ns Single-Cycle Instruction Execution Time for 3-V Operation
- Single-Cycle 16 × 16-Bit Multiply/Add
- 224K × 16-Bit Maximum Addressable External Memory Space (64K Program, 64K Data, 64K I/O, and 32K Global)
- 2K, 4K, 8K, 16K, 32K × 16-Bit Single-Access On-Chip Program ROM
- 1K, 3K, 6K, 9K × 16-Bit Single-Access On-Chip Program/Data RAM (SARAM)
- 1K Dual-Access On-Chip Program/Data RAM (DARAM)
- Full-Duplex Synchronous Serial Port for Coder/Decoder Interface
- Time-Division-Multiplexed (TDM) Serial Port
- Hardware or Software Wait-State Generation Capability
- On-Chip Timer for Control Operations
- Repeat Instructions for Efficient Use of Program Space
- Buffered Serial Port
- Host Port Interface
- Multiple Phase-Locked Loop (PLL) Clocking Options (×1, ×2, ×3, ×4, ×5, ×9 Depending on Device)
- Block Moves for Data/Program Management
- On-Chip Scan-Based Emulation Logic
- Boundary Scan
- Five Packaging Options
  - 100-Pin Quad Flat Package (PJ Suffix)
  - 100-Pin Thin Quad Flat Package (PZ Suffix)
  - 128-Pin Thin Quad Flat Package (PBK Suffix)
  - 132-Pin Quad Flat Package (PQ Suffix)
  - 144-Pin Thin Quad Flat Package (PGE Suffix)
- Low Power Dissipation and Power-Down Modes:
  - 47 mA (2.35 mA/MIP) at 5 V, 40-MHz Clock (Average)
  - 23 mA (1.15 mA/MIP) at 3 V, 40-MHz Clock (Average)
  - 10 mA at 5 V, 40-MHz Clock (IDLE1 Mode)
  - 3 mA at 5 V, 40-MHz Clock (IDLE2 Mode)
  - 5 μA at 5 V, Clocks Off (IDLE2 Mode)
- High-Performance Static CMOS Technology
- IEEE Standard 1149.1† Test-Access Port (JTAG)

description

The TMS320C5x generation of the Texas Instruments (TI™) TMS320 digital signal processors (DSPs) is fabricated with static CMOS integrated circuit technology; the architectural design is based upon that of an earlier TI DSP, the TMS320C25. The combination of advanced Harvard architecture, on-chip peripherals, on-chip memory, and a highly specialized instruction set is the basis of the operational flexibility and speed of the 'C5x‡ devices. They execute up to 50 million instructions per second (MIPS).

The 'C5x devices offer these advantages:

- Enhanced TMS320 architectural design for increased performance and versatility
- Modular architectural design for fast development of spin-off devices
- Advanced integrated-circuit processing technology for increased performance
- Upward-compatible source code (source code for 'C1x and 'C2x DSPs is upward compatible with 'C5x DSPs.)
- Enhanced TMS320 instruction set for faster algorithms and for optimized high-level language operation
- New static-design techniques for minimizing power consumption and maximizing radiation tolerance

TI is a trademark of Texas Instruments Incorporated.
† IEEE Standard 1149.1–1990, IEEE Standard Test-Access Port and Boundary-Scan Architecture
‡ References to 'C5x in this document include both TMS320C5x and TMS320LC5x devices unless specified otherwise.

description (continued)

Table 1 provides a comparison of the devices in the 'C5x generation. It shows the capacity of on-chip RAM and ROM memories, number of serial and parallel I/O ports, execution time of one machine cycle, and type of package with total pin count.

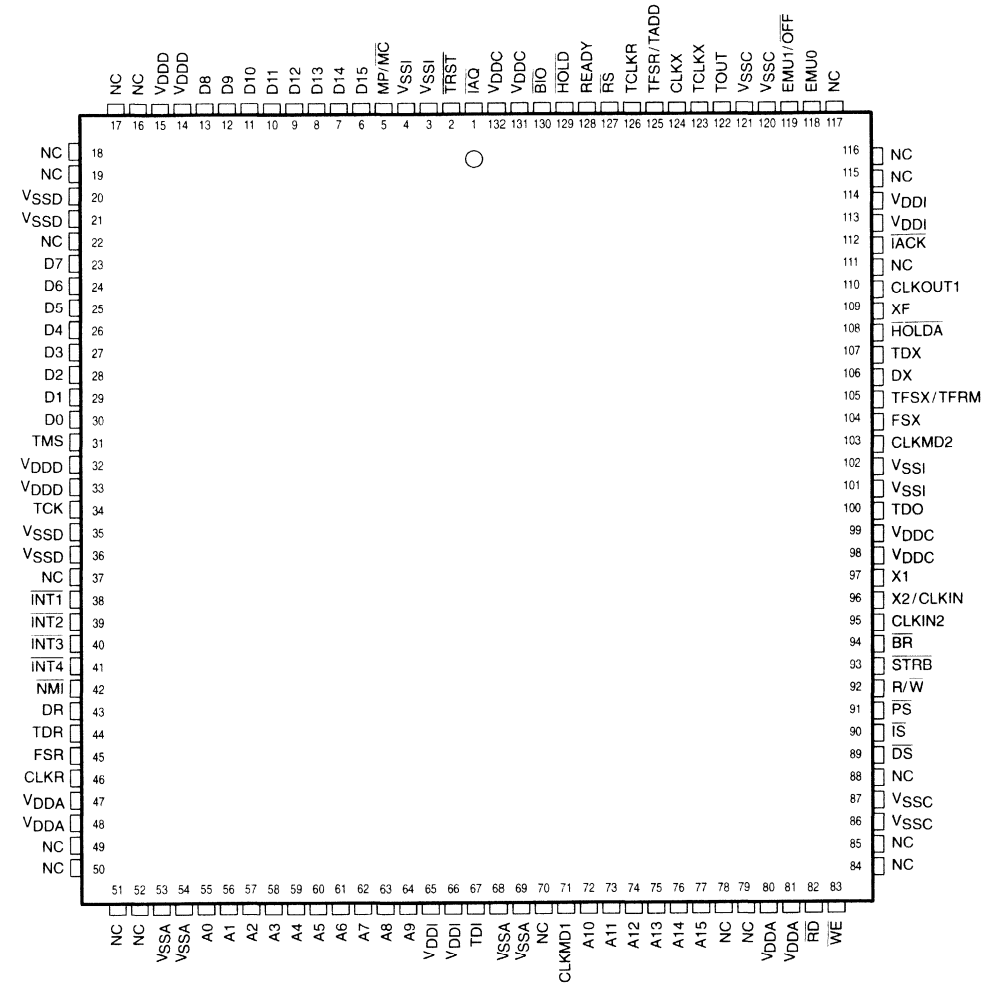
Table 1. Characteristics of the 'C5x Processors

TMS320 DEVICES	ON-CHIP MEMORY (16-BIT WORDS)				I/O PORTS		POWER SUPPLY (V)	CYCLE TIME (ns)	PACKAGE TYPE QFP‡
	DARAM		SARAM	ROM					
	DATA	DATA + PROG	DATA + PROG	PROG	SERIAL	PARALLEL†			
TMS320C50	544	512	9K	2K§	2	64K	5	50/35/25	132 pin
TMS320LC50	544	512	9K	2K§	2	64K	3.3	50/40/25	132 pin
TMS320C51	544	512	1K	8K§	2	64K	5	50/35/25/20	100/132 pin
TMS320LC51	544	512	1K	8K§	2	64K	3.3	50/40/25	100/132 pin
TMS320C52	544	512	–	4K§	1¶	64K	5	50/35/25/20	100 pin
TMS320LC52	544	512	–	4K§	1¶	64K	3.3	50/40/25	100 pin
TMS320C53	544	512	3K	16K§	2	64K	5	50/35/25	132 pin
TMS320LC53	544	512	3K	16K§	2	64K	3.3	50/40/25	132 pin
TMS320C53S	544	512	3K	16K§	2¶	64K	5	50/35/25	100 pin
TMS320LC53S	544	512	3K	16K§	2¶	64K	3.3	50/40/25	100 pin
TMS320LC56	544	512	6K	32K	2 #	64K	3.3	35/25	100 pin
TMS320LC57	544	512	6K	32K	2 #	64K + HPI‖	3.3	35/25	128 pin
TMS320C57S	544	512	6K	2K§	2 #	64K + HPI‖	5	50/35/25	144 pin
TMS320LC57S	544	512	6K	2K§	2 #	64K + HPI‖	3.3	50/35	144 pin

† Sixteen of the 64K parallel I/O ports are memory mapped.
‡ QFP = Quad flatpack
§ ROM boot loader available
¶ TDM serial port not available
# Includes auto-buffered serial port (BSP) but TDM serial port not available
‖ HPI = Host port interface

Pinouts for each package are device-specific.

TMS320C50, TMS320LC50, TMS320LC51, TMS320LC53, TMS320LC53
PQ PACKAGE
(TOP VIEW)



NOTE: NC = No connect (These pins are reserved.)

Pin Functions for Devices in the PQ Package

SIGNAL	TYPE	DESCRIPTION
PARALLEL INTERFACE BUS		
A0–A15	I/O/Z	16-bit external address bus (MSB: A15, LSB: A0)
D0–D15	I/O/Z	16-bit external data bus (MSB: D15, LSB: D0)
$\overline{PS}$, $\overline{DS}$, $\overline{IS}$	O/Z	Program, data, and I/O space select outputs, respectively
$\overline{STRB}$	I/O/Z	Timing strobe for external cycles and external DMA
R/$\overline{W}$	I/O/Z	Read/write select for external cycles and external DMA
$\overline{RD}$, $\overline{WE}$	O/Z	Read and write strobes, respectively, for external cycles
READY	I	External bus ready/wait-state control input
$\overline{BR}$	I/O/Z	Bus request. Arbitrates global memory and external DMA
SYSTEM INTERFACE/CONTROL SIGNALS		
$\overline{RS}$	I	Reset. Initializes device and sets PC to zero
MP/$\overline{MC}$	I	Microprocessor/microcomputer mode select. Enables internal ROM
$\overline{HOLD}$	I	Puts parallel I/F bus in high-impedance state after current cycle
$\overline{HOLDA}$	O/Z	Hold acknowledge. Indicates external bus in hold state
XF	O/Z	External flag output. Set/cleared through software
$\overline{BIO}$	I	I/O branch input. Implements conditional branches
TOUT	O/Z	Timer output signal. Indicates output of internal timer
$\overline{IAQ}$	O/Z	Instruction acquisition signal
$\overline{IACK}$	O/Z	Interrupt acknowledge signal
$\overline{INT1}$–$\overline{INT4}$	I	External interrupt inputs
$\overline{NMI}$	I	Nonmaskable external interrupt
SERIAL PORT INTERFACE (SPI)		
DR	I	Serial receive-data input
DX	O/Z	Serial transmit-data output. In high-impedance state when not transmitting
CLKR	I	Serial receive-data clock input
CLKX	I/O/Z	Serial transmit-data clock. Internal or external source
FSR	I	Serial receive-frame-synchronization input
FSX	I/O/Z	Serial transmit-frame-synchronization signal. Internal or external source
TDM SERIAL-PORT INTERFACE		
TDR	I	TDM serial receive-data input
TDX	O/Z	TDM serial transmit-data output. In high-impedance state when not transmitting
TCLKR	I	TDM serial receive-data clock input
TCLKX	I/O/Z	TDM serial transmit-data clock. Internal or external source
TFSR / TADD	I/O/Z	TDM serial receive-frame-synchronization input. In the TDM mode, TFSR/TADD is used to output/input the address of the port.
TFSX/TFRM	I	TDM serial transmit-frame-synchronization signal. Internal or external source. In the TDM mode, TFSX/TFRM becomes TFRM, the TDM frame synchronization.

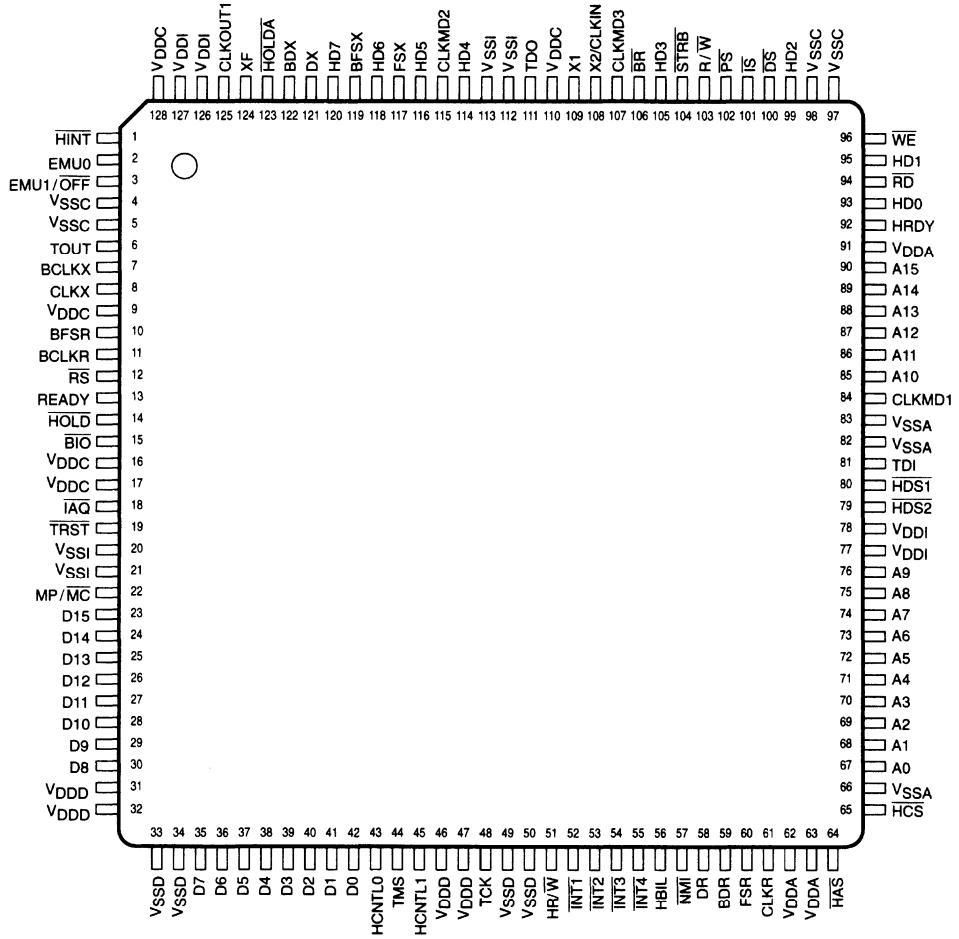
LEGEND:
I = Input
O = Output
Z = High impedance

Pin Functions for Devices in the PQ Package (Continued)

EMULATION/IEEE STANDARD 1149.1 TEST ACCESS PORT (TAP)		
TDI	I	TAP scan data input
TDO	O/Z	TAP scan data output
TMS	I	TAP mode select input
TCK	I	TAP clock input
$\overline{TRST}$	I	TAP reset (with pulldown resistor). Disables TAP when low
EMU0	I/O/Z	Emulation control 0. Reserved for emulation use
EMU1/$\overline{OFF}$	I/O/Z	Emulation control 1. Puts outputs in high-impedance state when low
CLOCK GENERATION AND CONTROL		
X1	O	Oscillator output
X2/CLKIN	I	Clock/oscillator input
CLKIN2	I	Clock input
CLKMD1, CLKMD2	I	Clock-mode select inputs
CLKOUT1	O/Z	Device system-clock output
POWER SUPPLY CONNECTIONS		
V_{DDA}	S	Supply connection, address-bus output
V_{DDD}	S	Supply connection, data-bus output
V_{DDC}	S	Supply connection, control output
V_{DDI}	S	Supply connection, internal logic
V_{SSA}	S	Supply connection, address-bus output
V_{SSD}	S	Supply connection, data-bus output
V_{SSC}	S	Supply connection, control output
V_{SSI}	S	Supply connection, internal logic

LEGEND:
I = Input
O = Output
S = Supply
Z = High impedance

TMS320LC57
PBK PACKAGE
(TOP VIEW)



Pin Functions for the TMS320LC57 in the PBK Package

SIGNAL	TYPE	DESCRIPTION
		PARALLEL INTERFACE BUS
A0–A15	I/O/Z	16-bit external address bus (MSB: A15, LSB: A0)
D0–D15	I/O/Z	16-bit external data bus (MSB: D15, LSB: D0)
$\overline{PS}$, $\overline{DS}$, $\overline{IS}$	O/Z	Program, data, and I/O space select outputs, respectively
$\overline{STRB}$	I/O/Z	Timing strobe for external cycles and external DMA
R/$\overline{W}$	I/O/Z	Read/write select for external cycles and external DMA
$\overline{RD}$, $\overline{WE}$	O/Z	Read and write strobes, respectively, for external cycles
READY	I	External bus ready/wait-state control input
$\overline{BR}$	I/O/Z	Bus request. Arbitrates global memory and external DMA
		SYSTEM INTERFACE/CONTROL SIGNALS
$\overline{RS}$	I	Reset. Initializes device and sets PC to zero
MP/$\overline{MC}$	I	Microprocessor/microcomputer mode select. Enables internal ROM
$\overline{HOLD}$	I	Puts parallel I/F bus in high-impedance state after current cycle
$\overline{HOLDA}$	O/Z	Hold acknowledge. Indicates external bus in hold state
XF	O/Z	External flag output. Set/cleared through software
$\overline{BIO}$	I	I/O branch input. Implements conditional branches
TOUT	O/Z	Timer output signal. Indicates output of internal timer
$\overline{IAQ}$	O/Z	Instruction acquisition signal
$\overline{INT1}$–$\overline{INT4}$	I	External interrupt inputs
$\overline{NMI}$	I	Nonmaskable external interrupt
		SERIAL PORT INTERFACE
DR	I	Serial receive-data input
DX	O/Z	Serial transmit-data output. In high-impedance state when not transmitting
CLKR	I	Serial receive-data clock input
CLKX	I/O/Z	Serial transmit-data clock. Internal or external source
FSR	I	Serial receive-frame-synchronization input
FSX	I/O/Z	Serial transmit-frame-synchronization signal. Internal or external source
		HOST PORT INTERFACE (HPI)
HCNTL0	I	HPI mode control 1
HCNTL1	I	HPI mode control 2
$\overline{HINT}$	O/Z	Host interrupt
$\overline{HDS1}$	I	HPI data strobe 1
$\overline{HDS2}$	I	HPI data strobe 2
HR/$\overline{W}$	I	HPI read/write strobe
$\overline{HAS}$	I	HPI address strobe
HRDY	O/Z	HPI ready signal
$\overline{HCS}$	I	HPI chip select
HBIL	I	HPI byte identification input
HD0–HD7	I/O/Z	HPI data bus

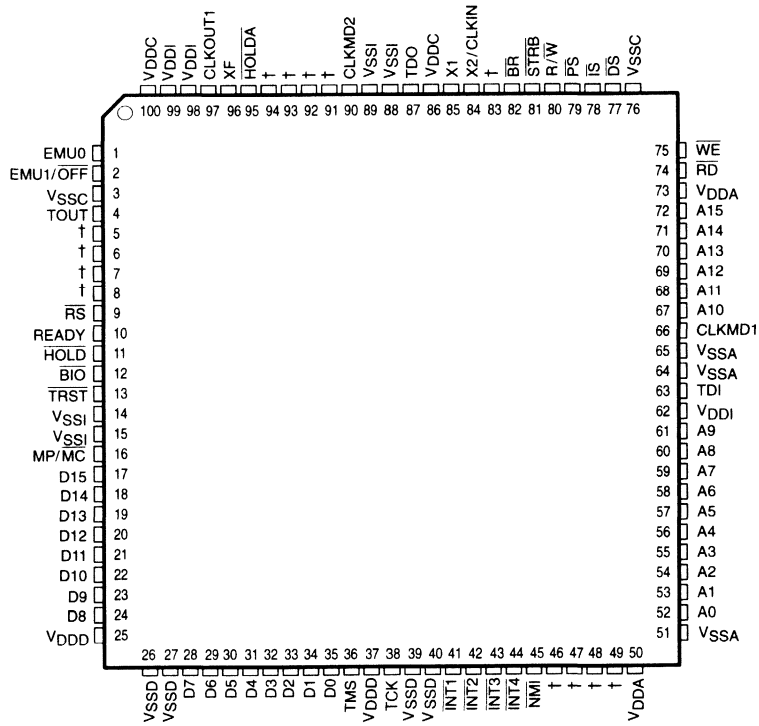
LEGEND:
I = Input
O = Output
Z = High impedance

Pin Functions for the TMS320LC57 in the PBK Package (Continued)

SIGNAL	TYPE	DESCRIPTION
		BUFFERED SERIAL PORT
BDR	I	BSP receive data input
BDX	O/Z	BSP transmit data output; in high-impedance state when not transmitting
BCLKR	I	BSP receive-data clock input
BCLKX	I/O/Z	BSP transmit-data clock; internal or external source
BFSR	I	BSP receive frame-synchronization input
BFSX	I/O/Z	BSP transmit frame-synchronization signal; internal or external source
		EMULATION/JTAG INTERFACE
TDI	I	JTAG-test-port scan data input
TDO	O/Z	JTAG-test-port scan data output
TMS	I	JTAG-test-port mode select input
TCK	I	JTAG-port clock input
$\overline{TRST}$	I	JTAG-port reset (with pull-down resistor). Disables JTAG when low
EMU0	I/O/Z	Emulation control 0. Reserved for emulation use
EMU1/$\overline{OFF}$	I/O/Z	Emulation control 1. Puts outputs in high-impedance state when low
		CLOCK GENERATION AND CONTROL
X1	O	Oscillator output
X2/CLKIN	I	Clock input
CLKMD1, CLKMD2, CLKMD3	I	Clock-mode select inputs
CLKOUT1	O/Z	Device system-clock output
		POWER SUPPLY CONNECTIONS
V_{DDA}	S	Supply connection, address-bus output
V_{DDD}	S	Supply connection, data-bus output
V_{DDC}	S	Supply connection, control output
V_{DDI}	S	Supply connection, internal logic
V_{SSA}	S	Supply connection, address-bus output
V_{SSD}	S	Supply connection, data-bus output
V_{SSC}	S	Supply connection, control output
V_{SSI}	S	Supply connection, internal logic

LEGEND:
I = Input
O = Output
S = Supply
Z = High impedance

TMS320C51, TMS320LC51, TMS320C52, TMS320LC52, TMS320C53S, TMS320LC53S, TMS320LC56
PZ PACKAGE
(TOP VIEW)



NOTE: NC = No connect (These pins are reserved.)
† See Table 2 for device-specific pinouts.

Table 2. Device-Specific Pinouts for the PZ Package

PIN	'C51, 'LC51	'C52, 'LC52	'C53S, 'LC53S	'LC56‡
5	TCLKX	V_{SSI}	CLKX2	BCLKX
6§	CLKX	CLKX	CLKX1	CLKX
7	TFSR/TADD	V_{SSI}	FSR2	BFSR
8	TCLKR	V_{SSI}	CLKR2	BCLKR
46§	DR	DR	DR1	DR
47	TDR	V_{SSI}	DR2	BDR
48§	FSR	FSR	FSR1	FSR
49§	CLKR	CLKR	CLKR1	CLKR
83	CLKIN2	CLKIN2	CLKIN2	CLKMD3
91§	FSX	FSX	FSX1	FSX
92	TFSX/TFRM	V_{SSI}	FSX2	BFSX
93§	DX	DX	DX1	DX
94	TDX	NC	DX2	BDX

‡ Pin names beginning with "B" indicate signals on the buffered serial port (BSP).
§ No functional change

Pin Functions for Devices in the PZ Package

SIGNAL	TYPE	DESCRIPTION
PARALLEL INTERFACE BUS		
A0–A15	I/O/Z	16-bit external address bus (MSB: A15, LSB: A0)
D0–D15	I/O/Z	16-bit external data bus (MSB: D15, LSB: D0)
$\overline{PS}$, $\overline{DS}$, $\overline{IS}$	O/Z	Program, data, and I/O space select outputs, respectively
$\overline{STRB}$	I/O/Z	Timing strobe for external cycles and external DMA
R/$\overline{W}$	I/O/Z	Read/write select for external cycles and external DMA
$\overline{RD}$, $\overline{WE}$	O/Z	Read and write strobes, respectively, for external cycles
READY	I	External bus ready/wait-state control input
$\overline{BR}$	I/O/Z	Bus request. Arbitrates global memory and external DMA
SYSTEM INTERFACE/CONTROL SIGNALS		
$\overline{RS}$	I	Reset. Initializes device and sets PC to zero
MP/$\overline{MC}$	I	Microprocessor/microcomputer mode select. Enables internal ROM
$\overline{HOLD}$	I	Puts parallel I/F bus in high-impedance state after current cycle
$\overline{HOLDA}$	O/Z	Hold acknowledge. Indicates external bus in hold state
XF	O/Z	External flag output. Set/cleared through software
$\overline{BIO}$	I	I/O branch input. Implements conditional branches
TOUT	O/Z	Timer output signal. Indicates output of internal timer
$\overline{INT1}$–$\overline{INT4}$	I	External interrupt inputs
$\overline{NMI}$	I	Nonmaskable external interrupt
SERIAL PORT INTERFACE		
DR, DR1, DR2	I	Serial receive-data input
DX, DX1, DX2	O/Z	Serial transmit-data output. In high-impedance state when not transmitting
CLKR, CLKR1, CLKR2	I	Serial receive-data clock input
CLKX, CLKX1, CLKX2	I/O/Z	Serial transmit-data clock. Internal or external source
FSR, FSR1, FSR2	I	Serial receive-frame-synchronization input
FSX, FSX1, FSX2	I/O/Z	Serial transmit-frame-synchronization signal. Internal or external source
BUFFERED SERIAL PORT (BSP) (SEE NOTE 1)		
BDR	I	BSP receive data input
BDX	O/Z	BSP transmit data output; in high-impedance state when not transmitting
BCLKR	I	BSP receive-data clock input
BCLKX	I/O/Z	BSP transmit-data clock; internal or external source
BFSR	I	BSP receive frame-synchronization input
BFSX	I/O/Z	BSP transmit frame-synchronization signal; internal or external source

LEGEND:
I = Input
O = Output
Z = High impedance
NOTE 1: 'LC56 devices only

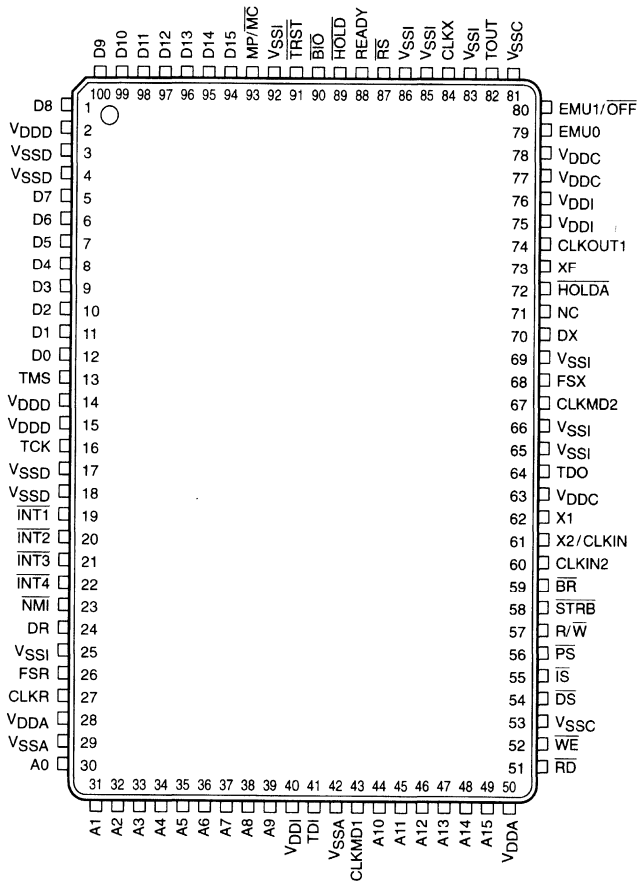
Pin Functions for Devices in the PZ Package (Continued)

SIGNAL	TYPE	DESCRIPTION
TDM SERIAL PORT INTERFACE		
TDR	I	TDM serial receive-data input
TDX	O/Z	TDM serial transmit-data output. In high-impedance state when not transmitting
TCLKR	I	TDM serial receive-data clock input
TCLKX	I/O/Z	TDM serial transmit-data clock. Internal or external source
TFSR / TADD	I/O/Z	TDM serial receive-frame-synchronization input. In the TDM mode, TFSR/TADD is used to output/input the address of the port
TFSX /TFRM	I	TDM serial transmit-frame-synchronization signal. Internal or external source. In the TDM mode, TFSX/TFRM becomes TFRM, the TDM frame sync.
EMULATION/JTAG INTERFACE		
TDI	I	JTAG-test-port scan data input
TDO	O/Z	JTAG-test-port scan data output
TMS	I	JTAG-test-port mode select input
TCK	I	JTAG-port clock input
$\overline{\text{TRST}}$	I	JTAG-port reset (with pull-down resistor). Disables JTAG when low
EMU0	I/O/Z	Emulation control 0. Reserved for emulation use
EMU1/$\overline{\text{OFF}}$	I/O/Z	Emulation control 1. Puts outputs in high-impedance state when low
CLOCK GENERATION AND CONTROL (SEE NOTE 2)		
X1	O	Oscillator output
X2/CLKIN	I	Clock/oscillator input (PLL clock input for 'C56)
CLKIN2	I	Clock input (PLL clock input for 'C50, 'C51, 'C52, 'C53, 'C53S)
CLKMD1, CLKMD2, CLKMD3	I	Clock-mode select inputs
CLKOUT1	O/Z	Device system-clock output
POWER SUPPLY CONNECTIONS		
V_{DDA}	S	Supply connection, address-bus output
V_{DDD}	S	Supply connection, data-bus output
V_{DDC}	S	Supply connection, control output
V_{DDI}	S	Supply connection, internal logic
V_{SSA}	S	Supply connection, address-bus output
V_{SSD}	S	Supply connection, data-bus output
V_{SSC}	S	Supply connection, control output
V_{SSI}	S	Supply connection, internal logic

LEGEND:
I = Input
O = Output
S = Supply
Z = High impedance

NOTE 2: CLKIN2 pin is replaced by CLKMD3 pin on 'LC56 devices.

TMS320C52, TMS320LC52
PJ PACKAGE
(TOP VIEW)



NOTE: NC = No connect (These pins are reserved.)

Pin Functions for the TMS320C52, TMS320LC52 in the PJ Package

SIGNAL	TYPE	DESCRIPTION
		PARALLEL INTERFACE BUS
A0–A15	I/O/Z	16-bit external address bus (MSB: A15, LSB: A0)
D0–D15	I/O/Z	16-bit external data bus (MSB: D15, LSB: D0)
$\overline{PS}$, $\overline{DS}$, $\overline{IS}$	O/Z	Program, data, and I/O space select outputs, respectively
$\overline{STRB}$	I/O/Z	Timing strobe for external cycles and external DMA
R/$\overline{W}$	I/O/Z	Read/write select for external cycles and external DMA
$\overline{RD}$, $\overline{WE}$	O/Z	Read and write strobes, respectively, for external cycles
READY	I	External bus ready/wait-state control input
$\overline{BR}$	I/O/Z	Bus request. Arbitrates global memory and external DMA
		SYSTEM INTERFACE/CONTROL SIGNALS
RS	I	Reset. Initializes device and sets PC to zero
MP/$\overline{MC}$	I	Microprocessor/microcomputer mode select. Enables internal ROM
$\overline{HOLD}$	I	Puts parallel I/F bus in high-impedance state after current cycle
$\overline{HOLDA}$	O/Z	Hold acknowledge. Indicates external bus in hold state
XF	O/Z	External flag output. Set/cleared through software
$\overline{BIO}$	I	I/O branch input. Implements conditional branches
TOUT	O/Z	Timer output signal. Indicates output of internal timer
$\overline{INT1}$–$\overline{INT4}$	I	External interrupt inputs
$\overline{NMI}$	I	Nonmaskable external interrupt
		SERIAL PORT INTERFACE
DR	I	Serial receive-data input
DX	O/Z	Serial transmit-data output. In high-impedance state when not transmitting
CLKR	I	Serial receive-data clock input
CLKX	I/O/Z	Serial transmit-data clock. Internal or external source
FSR	I	Serial receive-frame-synchronization input
FSX	I/O/Z	Serial transmit-frame-synchronization signal. Internal or external source
		EMULATION/JTAG INTERFACE
TDI	I	JTAG-test-port scan data input
TDO	O/Z	JTAG-test-port scan data output
TMS	I	JTAG-test-port mode select input
TCK	I	JTAG-port clock input
$\overline{TRST}$	I	JTAG-port reset (with pulldown resistor). Disables JTAG when low
EMU0	I/O/Z	Emulation control 0. Reserved for emulation use
EMU1/$\overline{OFF}$	I/O/Z	Emulation control 1. Puts outputs in high-impedance state when low

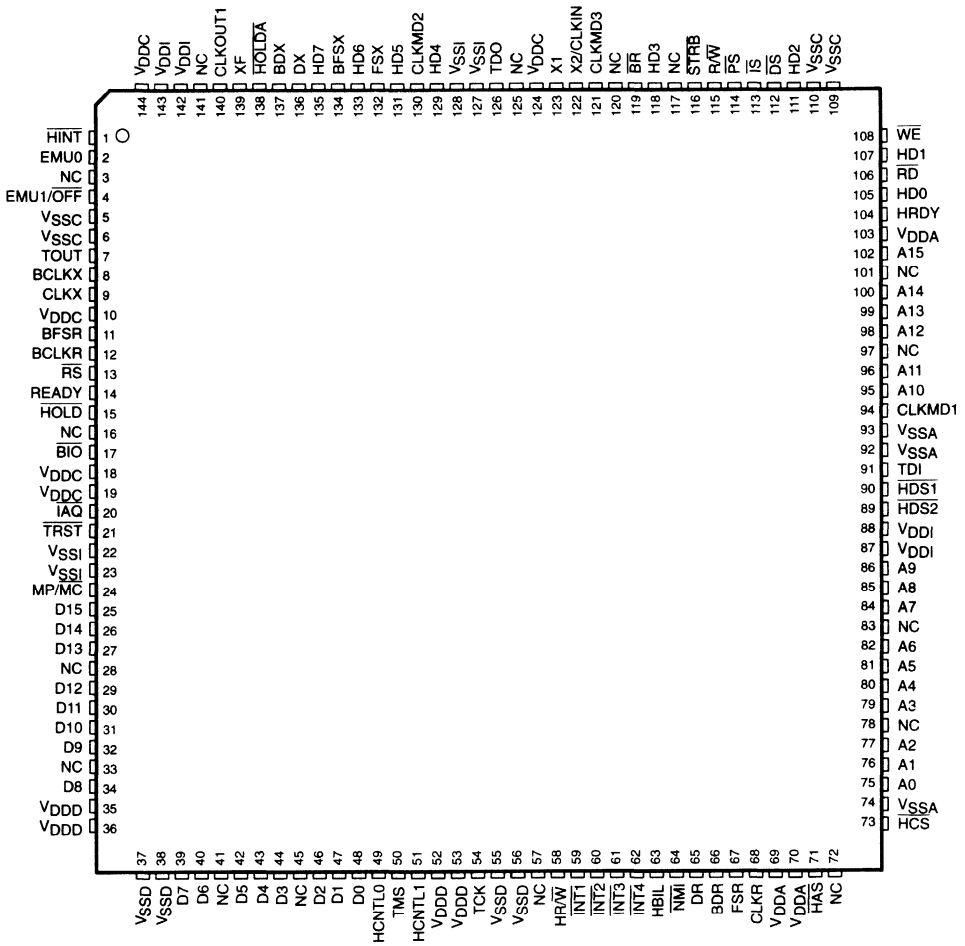
LEGEND:
I = Input
O = Output
Z = High impedance

Pin Functions for the TMS320C52, TMS320LC52 in the PJ Package (Continued)

SIGNAL	TYPE	DESCRIPTION
		CLOCK GENERATION AND CONTROL
X1	O	Oscillator output
X2/CLKIN	I	Clock/oscillator input
CLKIN2	I	Clock input (PLL clock input for 'C52, 'LC52)
CLKMD1, CLKMD2	I	Clock-mode select inputs
CLKOUT1	O/Z	Device system-clock output
		POWER SUPPLY CONNECTIONS
V_{DDA}	S	Supply connection, address-bus output
V_{DDD}	S	Supply connection, data-bus output
V_{DDC}	S	Supply connection, control output
V_{DDI}	S	Supply connection, internal logic
V_{SSA}	S	Supply connection, address-bus output
V_{SSD}	S	Supply connection, data-bus output
V_{SSC}	S	Supply connection, control output
V_{SSI}	S	Supply connection, internal logic

LEGEND:
I = Input
O = Output
S = Supply

TMS320C57S, TMS320LC57S
PGE PACKAGE
(TOP VIEW)



NOTE: NC = No connect (These pins are reserved.)

ADVANCE INFORMATION

Pin Functions for the TMS320C57S, TMS320LC57S in the PGE Package

SIGNAL	TYPE	DESCRIPTION
		PARALLEL INTERFACE BUS
A0–A15	I/O/Z	16-bit external address bus (MSB: A15, LSB: A0)
D0–D15	I/O/Z	16-bit external data bus (MSB: D15, LSB: D0)
$\overline{PS}$, $\overline{DS}$, $\overline{IS}$	O/Z	Program, data, and I/O space select outputs, respectively
$\overline{STRB}$	I/O/Z	Timing strobe for external cycles and external DMA
R/$\overline{W}$	I/O/Z	Read/write select for external cycles and external DMA
$\overline{RD}$, $\overline{WE}$	O/Z	Read and write strobes, respectively, for external cycles
READY	I	External bus ready/wait-state control input
$\overline{BR}$	I/O/Z	Bus request. Arbitrates global memory and external DMA
		SYSTEM INTERFACE/CONTROL SIGNALS
$\overline{RS}$	I	Reset. Initializes device and sets PC to zero
MP/$\overline{MC}$	I	Microprocessor/microcomputer mode select. Enables internal ROM
$\overline{HOLD}$	I	Puts parallel I/F bus in high-impedance state after current cycle
$\overline{HOLDA}$	O/Z	Hold acknowledge. Indicates external bus in hold state
XF	O/Z	External flag output. Set/cleared through software
$\overline{BIO}$	I	I/O branch input. Implements conditional branches
TOUT	O/Z	Timer output signal. Indicates output of internal timer
$\overline{IAQ}$	O/Z	Instruction acquisition signal
$\overline{INT1}$–$\overline{INT4}$	I	External interrupt inputs
$\overline{NMI}$	I	Nonmaskable external interrupt
		SERIAL PORT INTERFACE (SPI)
DR	I	Serial receive-data input
DX	O/Z	Serial transmit-data output. In high-impedance state when not transmitting
CLKR	I	Serial receive-data clock input
CLKX	I/O/Z	Serial transmit-data clock. Internal or external source
FSR	I	Serial receive-frame-synchronization input
FSX	I/O/Z	Serial transmit-frame-synchronization signal. Internal or external source
		HOST PORT INTERFACE (HPI)
HCNTL0	I	HPI mode control 1
HCNTL1	I	HPI mode control 2
$\overline{HINT}$	O/Z	Host interrupt
$\overline{HDS1}$	I	HPI data strobe 1
$\overline{HDS2}$	I	HPI data strobe 2
HR/$\overline{W}$	I	HPI read/write strobe
$\overline{HAS}$	I	HPI address strobe
HRDY	O/Z	HPI ready signal
$\overline{HCS}$	I	HPI chip select
HBIL	I	HPI byte identification input
HD0–HD7	I/O/Z	HPI data bus

LEGEND:
I = Input
O = Output
Z = High impedance

Pin Functions for the TMS320C57S, TMS320LC57S in the PGE Package (Continued)

SIGNAL	TYPE	DESCRIPTION
		BUFFERED SERIAL PORT
BDR	I	BSP receive data input
BDX	O/Z	BSP transmit data output; in high-impedance state when not transmitting
BCLKR	I	BSP receive-data clock input
BCLKX	I/O/Z	BSP transmit-data clock; internal or external source
BFSR	I	BSP receive frame-synchronization input
BFSX	I/O/Z	BSP transmit frame-synchronization signal; internal or external source
		EMULATION/JTAG INTERFACE
TDI	I	JTAG-test-port scan data input
TDO	O/Z	JTAG-test-port scan data output
TMS	I	JTAG-test-port mode select input
TCK	I	JTAG-port clock input
$\overline{\text{TRST}}$	I	JTAG-port reset (with pulldown resistor). Disables JTAG when low
EMU0	I/O/Z	Emulation control 0. Reserved for emulation use
EMU1/$\overline{\text{OFF}}$	I/O/Z	Emulation control 1. Puts outputs in high-impedance state when low
		CLOCK GENERATION AND CONTROL
X1	O	Oscillator output
X2/CLKIN	I	PLL clock input
CLKMD1, CLKMD2, CLKMD3	I	Clock-mode select inputs
CLKOUT1	O/Z	Device system-clock output
		POWER SUPPLY CONNECTIONS
V_{DDA}	S	Supply connection, address-bus output
V_{DDD}	S	Supply connection, data-bus output
V_{DDC}	S	Supply connection, control output
V_{DDI}	S	Supply connection, internal logic
V_{SSA}	S	Supply connection, address-bus output
V_{SSD}	S	Supply connection, data-bus output
V_{SSC}	S	Supply connection, control output
V_{SSI}	S	Supply connection, internal logic

LEGEND:
I = Input
O = Output
S = Supply
Z = High impedance

architecture

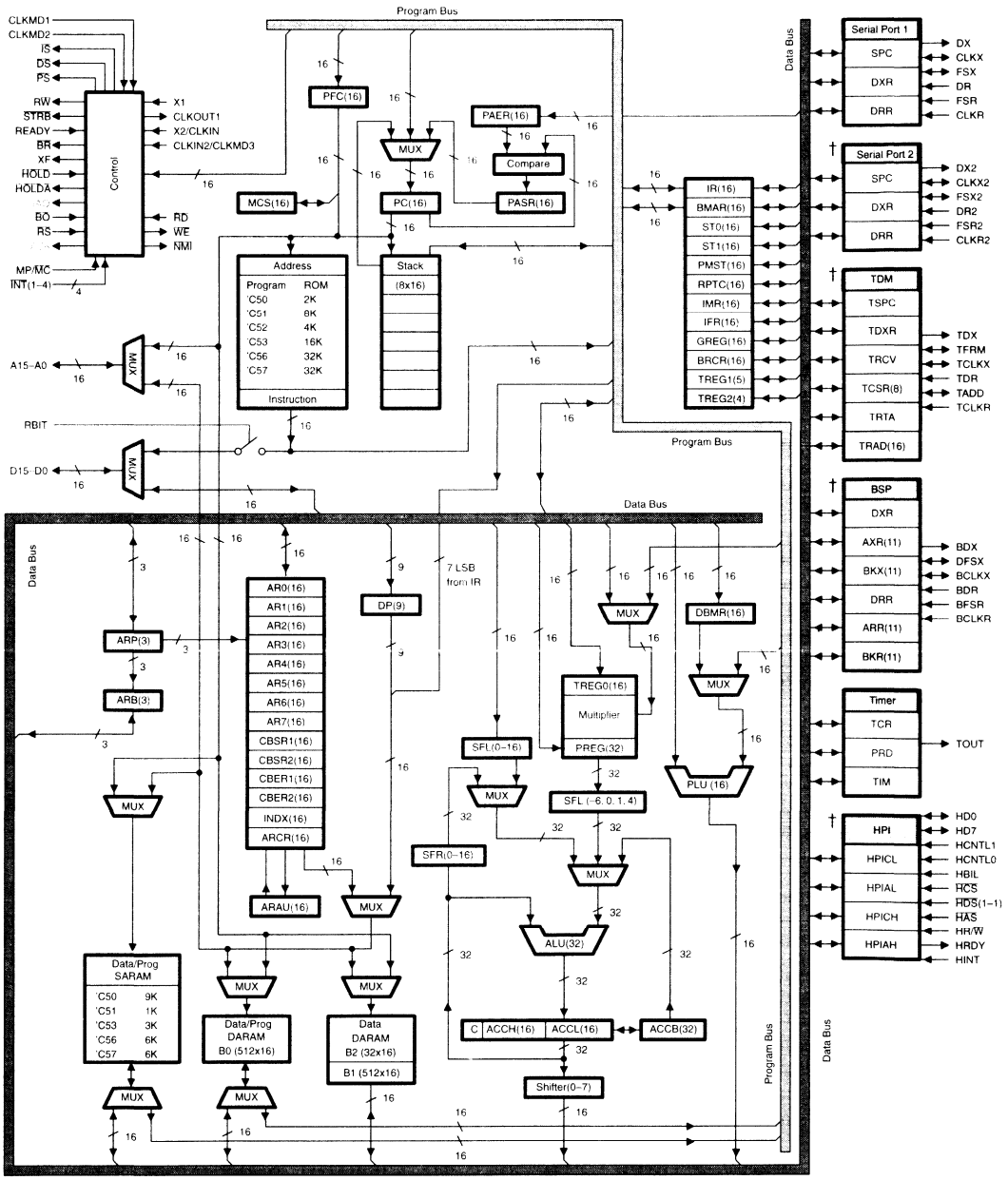
The 'C5x's advanced Harvard-type architecture maximizes the processing power by maintaining two separate memory bus structures, program and data, for full-speed execution. Instructions support data transfers between the two spaces. This architecture permits coefficients stored in program memory to be read into the RAM, eliminating the need for a separate coefficient ROM. The 'C5x architecture also makes available immediate instructions and subroutines based on computed values. Increased throughput on the 'C5x for many DSP applications is accomplished using single-cycle multiply/accumulate instructions with a data-move option, up to eight auxiliary registers with a dedicated arithmetic unit, a parallel logic unit, and faster I/O necessary for data-intensive signal processing. The architectural design emphasizes overall speed, communication, and flexibility in processor configuration. Control signals and instructions provide floating-point support, block-memory transfers, communication to slower off-chip devices, and multiprocessing implementations as shown in the functional block diagram.

Table 3 explains the symbols that are used in the functional block diagram.

Table 3. Symbols Used in Functional Block Diagram

SYMBOL	DESCRIPTION	SYMBOL	DESCRIPTION
ABU	Auto-buffering unit	IFR	Interrupt-flag register
ACCB	Accumulator buffer	IMR	Interrupt-mask register
ACCH	Accumulator high	INDX	Indirect-addressing-index register
ACCL	Accumulator low	IR	Instruction register
ALU	Arithmetic logic unit	MCS	Microcall stack
ARAU	Auxiliary-register arithmetic unit	MUX	Multiplexer
ARB	Auxiliary-register pointer buffer	PAER	Block-repeat-address end register
ARCR	Auxiliary-register compare register	PASR	Block-repeat-address start register
ARP	Auxiliary-register pointer	PC	Program counter
ARR	Address-receive register (ABU)	PFC	Prefetch counter
AR0–AR7	Auxiliary registers	PLU	Parallel logic unit
AXR	Address-transmit register (ABU)	PMST	Processor-mode-status register
BKR	Receive-buffer-size register (ABU)	PRD	Timer-period register
BKX	Transmit-buffer-size register (ABU)	PREG	Product register
BMAR	Block-move-address register	RPTC	Repeat-counter register
BRCR	Block-repeat-counter register	SARAM	Single-access RAM
BSP	Buffered serial port	SFL	Left shifter
C	Carry bit	SFR	Right shifter
CBER1	Circular buffer 1 end address	SPC	Serial-port interface-control register
CBER2	Circular buffer 2 end address	ST0,ST1	Status registers
CBSR1	Circular buffer 1 start address	TCSR	TDM channel-select register
CBSR2	Circular buffer 2 start address	TCR	Timer-control register
DARAM	Dual-access RAM	TDM	Time-division-multiplexed serial port
DBMR	Dynamic bit manipulation register	TDXR	TDM data transmit register
DP	Data memory page pointer	TIM	Timer-count register
DRR	Serial-port data receive register	TRAD	TDM received-address register
DXR	Serial-port data transmit register	TRCV	TDM data-receive register
GREG	Global memory allocation register	TREG0	Temporary register for multiplication
HPI	Host port interface	TREG1	Temporary register for dynamic shift count
HPIAH	HPI-address register (high bytes)	TREG2	Temporary register used as bit pointer in dynamic-bit test
HPIAL	HPI-address register (low bytes)	TRTA	TDM receive-/transmit-address register
HPICH	HPI-control register (high bytes)	TSPC	TDM serial-port-control register
HPICL	HPI-control register (low bytes)		

functional block diagram



† Not available on all devices (see Table 1).

NOTES: A. Signals in shaded text are not available on 100-pin QFP packages.

B. Symbol descriptions appear in Table 3.

32-bit ALU/accumulator

The 32-bit ALU and accumulator implement a wide range of arithmetic and logical functions, the majority of which execute in a single cycle. The ALU is a general-purpose arithmetic/logic unit that operates on 16-bit words taken from data memory or derived from immediate instructions. In addition to the usual arithmetic instructions, the ALU can perform Boolean operations, facilitating the bit manipulation ability required of a high-speed controller. One input to the ALU always is supplied by the accumulator, and the other input can be furnished from the product register (PREG) of the multiplier, the accumulator buffer (ACCB), or the output of the scaling shifter [which has been read from data memory or from the accumulator (ACC)]. After the ALU performs the arithmetic or logical operation, the result is stored in the ACC where additional operations, such as shifting, can be performed. Data input to the ALU can be scaled by the scaling shifter. The 32-bit ACC is split into two 16-bit segments for storage in data memory. Shifters at the output of the ACC provide a left shift of 0 to 7 places. This shift is performed while the data is being transferred to the data bus for storage. The contents of the ACC remain unchanged. When the postscaling shifter is used on the high word of the ACC (bits 31–16), the most significant bits (MSBs) are lost and the least significant bits (LSBs) are filled with bits shifted in from the low word (bits 15–0). When the postscaling shifter is used on the low word, the LSBs are filled with zeros.

The 'C5x supports floating-point operations for applications requiring a large dynamic range. By performing left shifts, the normalization instruction (NORM) is used to normalize fixed-point numbers contained in the ACC. The four bits of the TREG1 define a variable shift through the scaling shifter for the ADDT/LACT/SUBT instructions (add to/load to/subtract from ACC with shift specified by TREG1). These instructions are useful in denormalizing a number (converting from floating point to fixed point). They are also useful for executing an automatic gain control (AGC) going into a filter.

The single-cycle 1-bit to 16-bit right shift of the ACC efficiently aligns the ACC's contents. This, coupled with the 32-bit temporary buffer on the ACC, enhances the effectiveness of the ALU in extended-precision arithmetic. The ACCB provides a temporary storage place for a fast save of the ACC. The ACCB also can be used as an input to the ALU. The minimum or maximum value in a string of numbers is found by comparing the contents of the ACCB with the contents of the ACC. The minimum or maximum value is placed in both registers, and, if the condition is met, the carry bit (C) is set to 1. The minimum and maximum functions are executed by the CRLT and CRGT instructions, respectively.

scaling shifters

The 'C5x provides a scaling shifter that has a 16-bit input connected to the data bus and a 32-bit output connected to the ALU. This scaling shifter produces a left shift of 0 to 16 bits on the input data. The shift count is specified by a constant embedded in the instruction word or by the value in TREG1. The LSBs of the output are filled with zeros; the MSBs may be either filled with zeros or sign extended, depending upon the value of the sign-extension mode (SXM) bit of status register ST1.

The 'C5x also contains several other shifters that allow it to perform numerical scaling, bit extraction, extended-precision arithmetic, and overflow prevention. These shifters are connected to the output of the product register and the ACC.

parallel logic unit

The parallel logic unit (PLU) is a second logic unit, additional to the main ALU, that executes logic operations on data without affecting the contents of the ACC. The PLU provides the bit-manipulation ability required of a high-speed controller and simplifies control/status register operations. The PLU provides a direct logic operation path to data memory space and can set, clear, test, or toggle multiple bits directly in a data memory location, a control/status register, or any register that is mapped into data memory space.

16 × 16-bit parallel multiplier

The 'C5x uses a 16 × 16-bit hardware multiplier that is capable of computing a signed or an unsigned 32-bit product in a single machine cycle. All multiply instructions, except the MPYU (multiply unsigned) instruction, perform a signed multiply operation in the multiplier. That is, two numbers being multiplied are treated as 2s-complement numbers, and the result is a 32-bit 2s-complement number.

There are two registers associated with the multiplier: TREG0, a 16-bit temporary register that holds one of the operands for the multiplier, and PREG, the 32-bit product register that holds the product. Four product shift modes (PM) are available at the PREG's output. These shift modes are useful for performing multiply/accumulate operations, performing fractional arithmetic, or justifying fractional products. The PM field of status register ST1 specifies the PM shift mode.

The product can be shifted one bit to compensate for the extra sign bit gained in multiplying two 16-bit 2s-complement numbers (MPY). A 4-bit shift is used in conjunction with the MPY instruction with a short immediate value (13 bits or less) to eliminate the four extra sign bits gained in multiplying a 16-bit number by a 13-bit number. Finally, the output of PREG can, instead, be right-shifted 6 bits to enable the execution of up to 128 consecutive multiply/accumulates without the possibility of overflow.

The load-TREG0 (LT) instruction normally loads TREG0 to provide one operand (from the data bus), and the MPY instruction provides the second operand (also from the data bus). A multiplication also can be performed with a short or long immediate operand by using tne MPY instruction with an immediate operand. A product is obtained every two cycles except when a long immediate operand is used.

Four multiply/accumulate instructions (MAC, MACD, MADD, and MADS as defined in Table 7) fully utilize the computational bandwidth of the multiplier, allowing both operands to be processed simultaneously. The data for these operations is transferred to the multiplier during each cycle through the program and data buses. This facilitates single-cycle multiply/accumulates when used with repeat (RPT and RPTZ) instructions. In these instructions, the coefficient addresses are generated by the PC, while the data addresses are generated by the ARAU. This allows the repeated instruction to access the values sequentially from the coefficient table and step through the data in any of the indirect addressing modes. The RPTZ instruction also clears the accumulator and the product register to initialize the multiply/accumulate operation.

The MACD and MADD instructions, when repeated, support filter constructs (weighted running averages) so that as the sum-of-products is executed, the sample data is shifted in memory to make room for the next sample and to eliminate the oldest sample. Circular addressing with MAC and MADS instructions also can be used to support filter implementation.

auxiliary registers and auxiliary-register arithmetic unit (ARAU)

The 'C5x provides a register file containing eight auxiliary registers (AR0–AR7). The auxiliary registers are used for indirect addressing of the data memory or for temporary data storage. Indirect auxiliary-register addressing allows placement of the data memory address of an instruction operand into one of the auxiliary registers. These registers are referenced with a 3-bit auxiliary register pointer (ARP) that is loaded with a value from 0 through 7, designated AR0 through AR7, respectively. The auxiliary registers and the ARP can be loaded from data memory, the ACC, the product register, or by an immediate operand defined in the instruction. The contents of these registers can be stored in data memory or used as inputs to the central arithmetic logic unit (CALU). These registers are accessible as memory-mapped locations within the 'C5x data-memory space.

The auxiliary register file (AR0–AR7) is connected to the auxiliary register arithmetic unit (ARAU). The ARAU can autoindex the current auxiliary register while the data memory location is being addressed. Indexing can be performed either by ±1 or by the contents of the INDX register. As a result, accessing tables of information does not require the CALU for address manipulation; thus, the CALU is free for other operations in parallel.

memory

The 'C5x implements three separate address spaces for program memory, data memory, and I/O. Each space accommodates a total of 64K 16-bit words (see Figures 1 through 7). Within the 64K words of data space, the 256 to 32K words at the top of the address range can be defined to be external global memory in increments of powers of two, as specified by the contents of the global memory allocation register (GREG). Access to global memory is arbitrated using the global memory bus request ($\overline{BR}$) signal.

The 'C5x devices include a considerable amount of on-chip memory to aid in system performance and integration including ROM, single-access RAM (SARAM), and dual-access RAM (DARAM). The amount and types of memory available on each device are shown in Table 1.

On the 'C5x, the first 96 (0–5Fh) data-memory locations are allocated for memory-mapped registers. This memory-mapped register space contains various control and status registers including those for the CPU, serial port, timer, and software wait-state generators. Additionally, the first 16 I/O port locations are mapped into this data-memory space, allowing them to be accessed either as data memory using single-word instructions or as I/O locations with two-word instructions. Two-word instructions allow access to the full 64K words of I/O space.

The mask-programmable ROM is located in program memory space. Customers can arrange to have this ROM programmed with contents unique to to any particular application. The ROM is enabled or disabled by the state of the MP/$\overline{MC}$ control input upon resetting the device or by manipulating the MP/$\overline{MC}$ bit in the PMST status register after reset. The ROM occupies the lowest block of program memory when enabled. When disabled, these addresses are located in the device's external program-memory space.

The 'C5x also has a mask-programmable option that provides security protection for the contents of on-chip ROM. When this internal option bit is programmed, no externally-originating instruction can access the on-chip ROM. This feature can be used to provide security for proprietary algorithms.

An optional boot loader is available in the device's on-chip ROM. This boot loader can be used to transfer a program automatically from data memory or the serial port to anywhere in program memory. In data memory, the program can be located on any 1K-word boundary and can be in either byte-wide or 16-bit word format. Once the code is transferred, the boot loader releases control to the program for execution.

The 'C5x devices provide two types of RAM: single-access RAM (SARAM) and dual-access RAM (DARAM). The single-access RAM requires a full machine cycle to perform a read or a write; however, this is not one large RAM block in which only one access per cycle is allowed. It is made up of 2K-word size-independent RAM blocks and each one allows one CPU access per cycle. The CPU can read or write one block while accessing another block at the same time. All 'C5x processors support multiple accesses to its SARAM in one cycle as long as they go to different RAM blocks. If the total SARAM size is not a multiple of two, one block is made smaller than 2K words. With an understanding of this structure, programmers can arrange code and data appropriately to improve code performance. Table 4 shows the sizes of available SARAM on the applicable 'C5x devices.

Table 4. SARAM Block Sizes

DEVICE	NUMBER OF SARAM BLOCKS
'C50/'LC50	Four 2K blocks and one 1K block
'C51/'LC51	One 1K block
'C53/'C53S/'LC53	One 2K block and one 1K block
'LC56	Three 2K blocks
'C57S/'LC57/'LC57S	Three 2K blocks

memory (continued)

The 'C5x dual-access RAM (DARAM) allows writes to, and reads from, the RAM in the same cycle without the address restrictions of the SARAM. The dual-access RAM is configured in three blocks: block 0 (B0), block 1 (B1), and block 2 (B2). Block 1 is 512 words in data memory and block 2 is 32 words in data memory. Block 0 is a 512-word block which can be configured as data or program memory. The CLRC CNF (configure B0 as data memory) and SETC CNF (configure B0 as program memory) instructions allow dynamic configuration of the memory maps through software. When using block 0 as program memory, instructions can be downloaded from external program memory into on-chip RAM and then executed.

When using on-chip RAM, ROM, or high-speed external memory, the 'C5x runs at full speed with no wait states. The ability of the DARAM to allow two accesses to be performed in one cycle, coupled with the parallel nature of the 'C5x architecture, enables the device to perform three concurrent memory accesses in any given machine cycle. Externally, the READY line can be used to interface the 'C5x to slower, less expensive external memory. Downloading programs from slow off-chip memory to on-chip RAM can speed processing while cutting system costs.

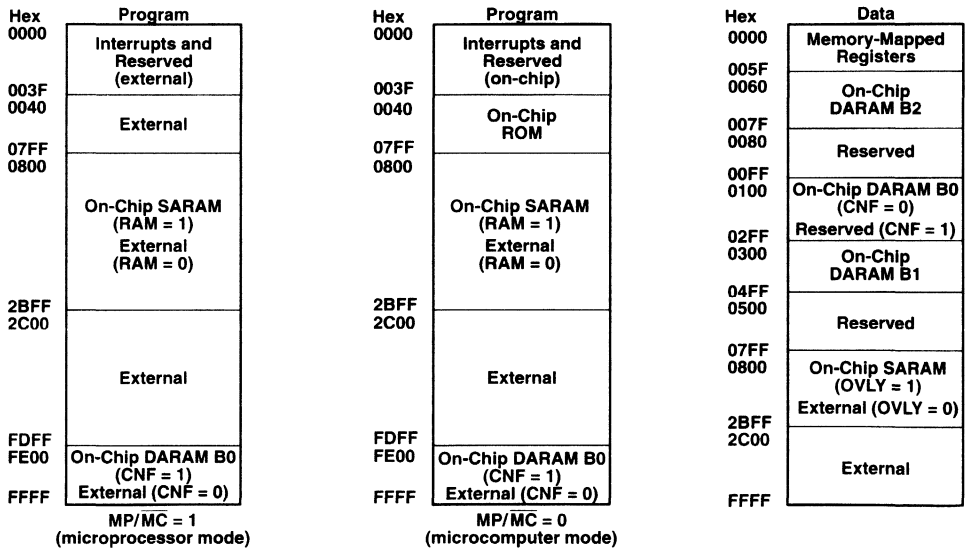


Figure 1. TMS320C50 and TMS320LC50 Memory Map

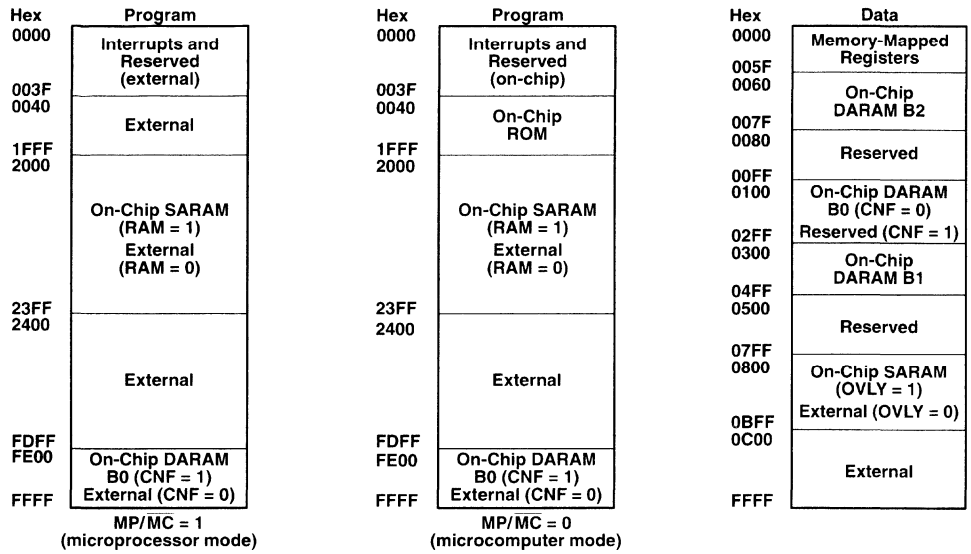


Figure 2. TMS320C51 and TMS320LC51 Memory Map

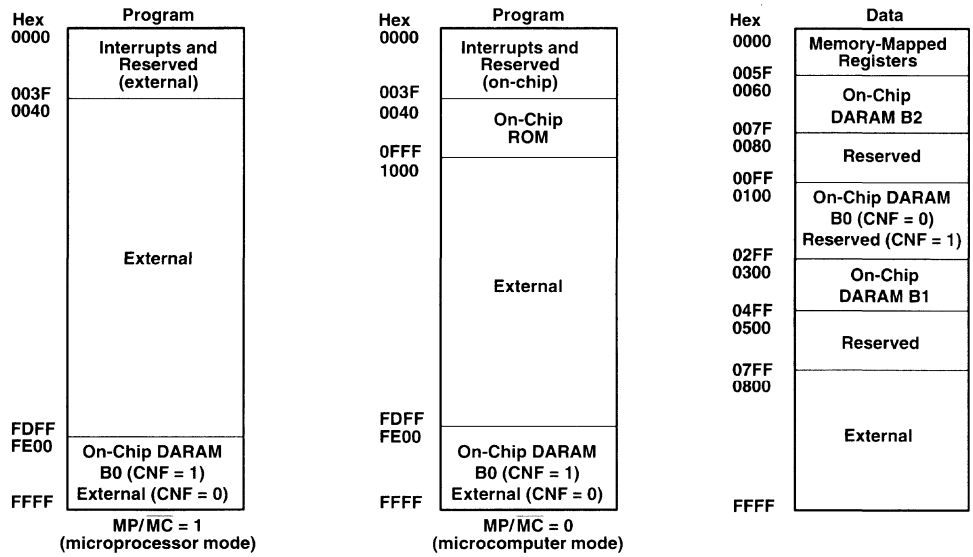


Figure 3. TMS320C52 and TMS320LC52 Memory Map

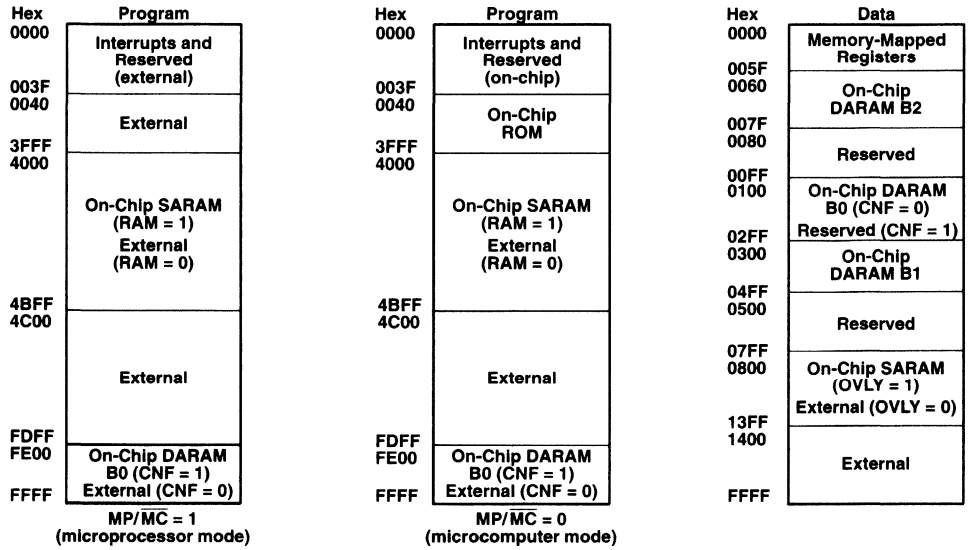


Figure 4. TMS320C53, TMS320C53S, TMS320LC53, and TMS320LC53S Memory Map

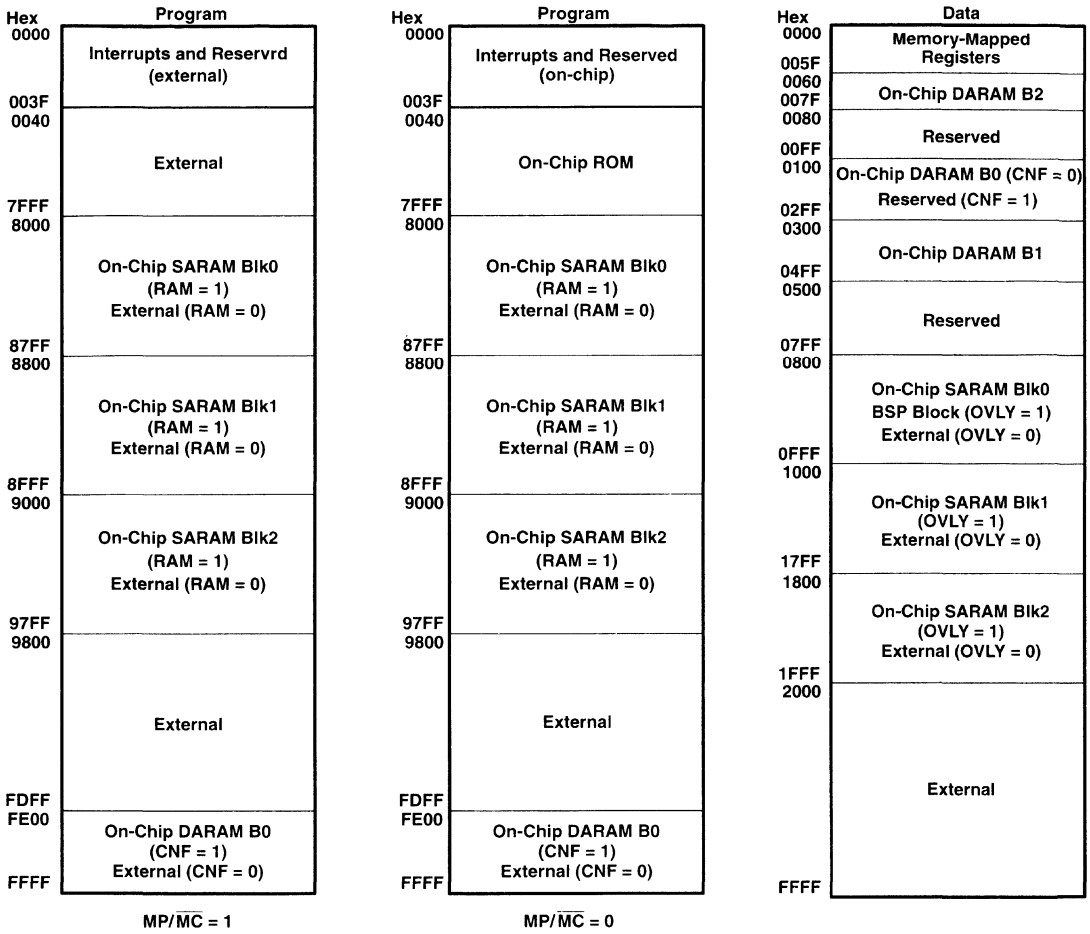


Figure 5. TMS320LC56 Memory Map

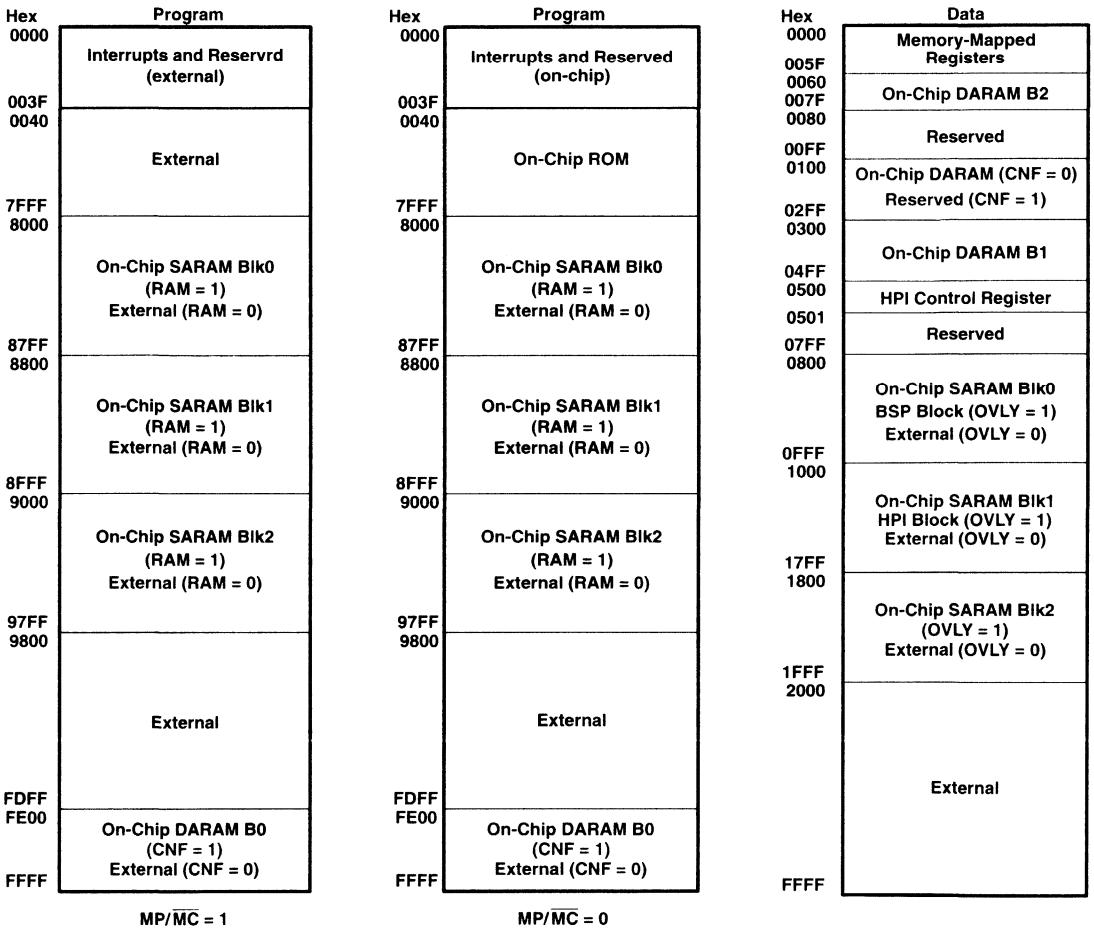


Figure 6. TMS320LC57 Memory Map

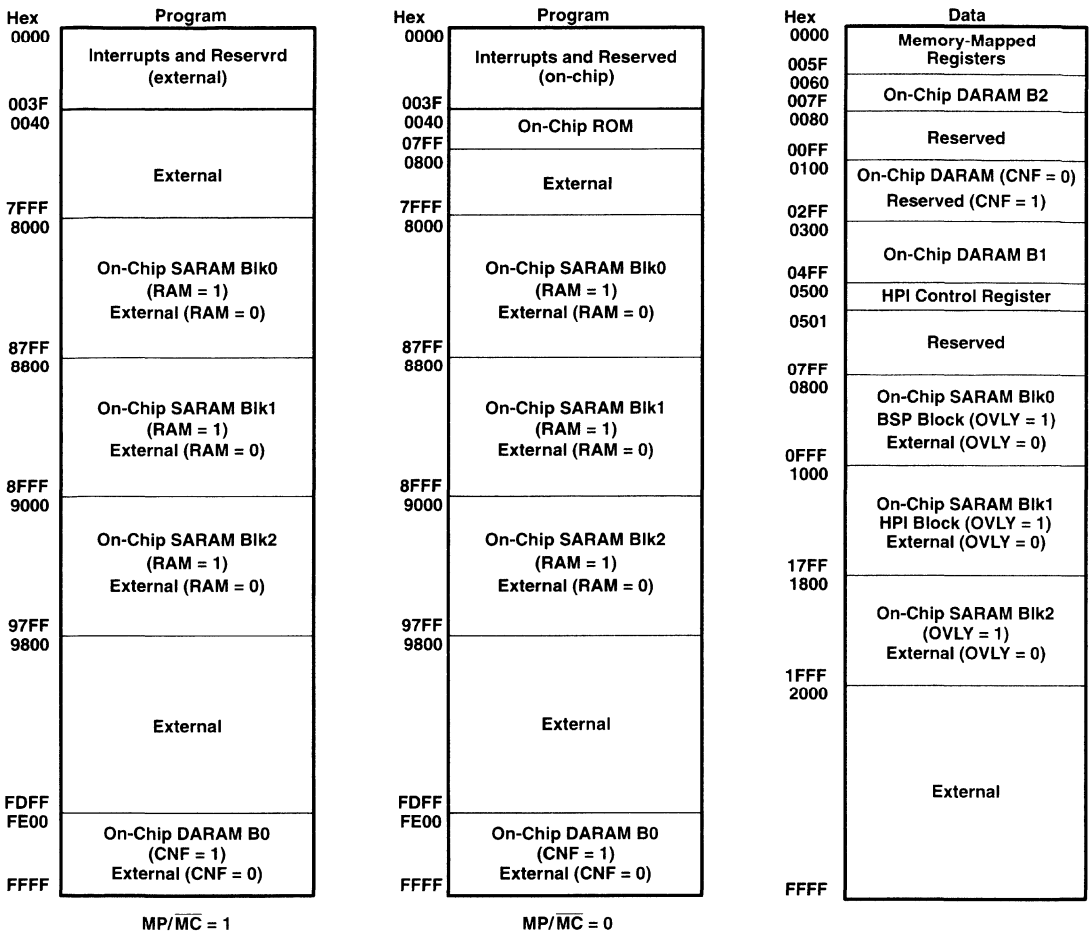


Figure 7. TMS320C57S Memory Map

interrupts and subroutines

The 'C5x implements four general-purpose interrupts, $\overline{INT4}$–$\overline{INT1}$, along with reset ($\overline{RS}$) and the nonmaskable interrupt ($\overline{NMI}$) which are available for external devices to request the attention of the processor. Internal interrupts are generated by the serial port (RINT and XINT), by the timer (TINT), and by the software-interrupt (TRAP, INTR, and NMI) instructions. Interrupts are prioritized with $\overline{RS}$ having the highest priority, followed by $\overline{NMI}$, and $\overline{INT4}$ having the lowest priority. Additionally, any interrupt except $\overline{RS}$ and $\overline{NMI}$ can be masked individually with a dedicated bit in the interrupt mask register (IMR) and can be cleared, set, or tested using its own dedicated bit in the interrupt flag register (IFR). The reset and NMI functions are not maskable.

All interrupt vector locations are on two-word boundaries so that branch instructions can be accommodated in those locations. While normally located at program memory address 0, the interrupt vectors can be remapped to the beginning of any 2K-word page in program memory by modifying the contents of the interrupt vector pointer (IPTR) located in the PMST status register.

A built-in mechanism protects multicycle instructions from interrupts. If an interrupt occurs during a multicycle instruction, the interrupt is not processed until the instruction completes execution. This mechanism applies to instructions that are repeated (using the RPT instruction) and to instructions that become multicycle because of wait states.

Each time an interrupt is serviced or a subroutine is entered, the PC is pushed onto an internal hardware stack, providing a mechanism for returning to the previous context. The stack contains eight locations, allowing interrupts or subroutines to be nested up to eight levels deep.

In addition to the eight-level hardware PC stack, eleven key CPU registers are equipped with an associated single-level stack or shadow register into which the registers' contents are saved upon servicing an interrupt. The contents are restored into their particular CPU registers once a return-from-interrupt instruction (RETE or RETI) is executed. The registers that have the shadow-register feature include the ACC and buffer, product register, status registers, and several other key CPU registers. The shadow-register feature allows sophisticated context save and restore operations to be handled automatically in cases where nested interrupts are not required or if interrupt servicing is performed serially.

power-down modes

The 'C5x implements several power-down modes in which the 'C5x core enters a dormant state and dissipates considerably less power. A power-down mode is invoked either by executing the IDLE/IDLE2 instructions or by driving the $\overline{HOLD}$ input low. When the $\overline{HOLD}$ signal initiates the power-down mode, on-chip peripherals continue to operate; this power-down mode is terminated when $\overline{HOLD}$ goes inactive.

While the 'C5x is in a power-down mode, all internal contents are maintained; this allows operation to continue unaltered when the power-down mode is terminated. All CPU activities are halted when the IDLE instruction is executed, but the CLKOUT1 pin remains active. The peripheral circuits continue to operate, allowing peripherals such as serial ports and timers to take the CPU out of its powered-down state. A power-down mode, when initiated by an IDLE instruction, is terminated upon receipt of an interrupt.

The IDLE2 instruction is used for a complete shutdown of the core CPU as well as all on-chip peripherals. In IDLE2, the power is reduced significantly because the entire device is stopped. The power-down mode is terminated by activating any of the external interrupt pins ($\overline{RS}$, $\overline{NMI}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, and $\overline{INT4}$) for at least five machine cycles.

bus-keeper circuitry (TMS320LC56/'C57S/'LC57)

The TMS320LC56/'C57S/'LC57 devices provide built-in bus keeper circuitry which holds the last state driven on the data bus by either the DSP or an external device after the bus is no longer being driven. This capability prevents excess power consumption caused by a floating bus, thus allowing optimization of power consumption without the need for external pullup resistors.

external interface

The 'C5x supports a wide range of system interfacing requirements. Program, data, and I/O address spaces provide interface to memory and I/O, maximizing system throughput. The full 16-bit address and data bus, along with the $\overline{PS}$, $\overline{DS}$, and $\overline{IS}$ space select signals, allow addressing of 64K 16-bit words in each of the three spaces.

I/O design is simplified by having I/O treated the same way as memory. I/O devices are mapped into the I/O address space using the processor's external address and data buses in the same manner as memory-mapped devices.

The 'C5x external parallel interface provides various control signals to facilitate interfacing to the device. The R/$\overline{W}$ output signal is provided to indicate whether the current cycle is a read or a write. The $\overline{STRB}$ output signal provides a timing reference for all external cycles. For convenience, the device also provides the $\overline{RD}$ and the $\overline{WE}$ output signals, which indicate a read and a write cycle, respectively, along with timing information for those cycles. The availability of these signals minimizes external gating necessary for interfacing external devices to the 'C5x.

Interface to memory and I/O devices of varying speeds is accomplished by using the READY line. When transactions are made with slower devices, the 'C5x processor waits until the other device completes its function and signals the processor via the READY line. Once a ready indication is provided back to the 'C5x from the external device, execution continues.

The bus request ($\overline{BR}$) signal is used in conjunction with the other 'C5x interface signals to arbitrate external global-memory accesses. Global memory is external data-memory space in which the $\overline{BR}$ signal is asserted at the beginning of the access. When an external global-memory device receives the the bus request, the external device responds by asserting the READY signal after the global memory access is arbitrated and the global access is completed.

external direct-memory access (DMA) capability

All 'C5x devices with single-access RAM offer a unique feature allowing another processor to read and write to the 'C5x internal memory. To initiate a read or write operation to the 'C5x single-access RAM, the host or master processor requests a hold state on the DSP's external bus. When acknowledged with $\overline{HOLDA}$, the host can request access to the internal bus by pulling the $\overline{BR}$ signal low. Unlike the hold mode, which allows the current operation to complete and allows CPU operation to continue (if status bit HM=0), a $\overline{BR}$-requested DMA always halts the operation currently being executed by the CPU. Access to the internal bus always is granted on the third clock cycle after the $\overline{BR}$ signal is received. In the PQ package, the $\overline{IAQ}$ pin also indicates when bus access has been granted. In the PZ package, this pin is not present so the host is required to wait two clock cycles after driving the bus request low before beginning DMA transfer.

host port interface (HPI) (TMS320C57S, TMS320LC57, TMS320LC57S only)

The HPI is an 8-bit parallel port used to interface a host processor to the 'C57S/'LC57. The host port is connected to a 2k word on-chip buffer through a dedicated internal bus. The dedicated bus allows the CPU to work uninterrupted while the host processor accesses the host port. The HPI memory buffer is a single-access RAM block which is accessible by both the CPU and the host. The HPI memory also can be used as general-purpose data or program memory. Both the CPU and the host have access to the HPI control register (HPIC) and the host can address the HPI memory through the HPI address register (HPIA).

Data transfers of 16-bit words occur as two consecutive bytes with a dedicated pin, HBIL, indicating whether the high or low byte is being transmitted. Two control pins, HCNTL1 and HCNTL0, control host access to the HPIA, HPI data (with an optional automatic address increment), or the HPIC. The host can interrupt the 'C57S/'LC57 by writing to HPIC. The 'C57S/'LC57 can interrupt the host with a dedicated $\overline{HINT}$ pin that the host acknowledges and clears.

host port interface (continued)

The HPI has two modes of operation, shared-access mode (SAM) and host-only mode (HOM). In SAM, the normal mode of operation, both the 'C57S/'LC57 and the host can access HPI memory. In this mode, asynchronous host accesses are resynchronized internally and, in case of conflict, the host has access priority and the 'C57S/'LC57S waits one cycle. Host and CPU accesses to the HPI memory can be resychronized through polling of a command word or through interrupts to prevent stalling the CPU for one cycle. The HOM capability allows the host to access HPI memory while the 'C57S/'LC57 is in IDLE2 mode (all internal clocks stopped) or in reset mode. The external 'C57S/'LC57S clock even can be stopped. The host can, therefore, access the HPI RAM while the 'C57S/'LC57 is in its optimum configuration in terms of power consumption.

The HPI control register has two data strobes, $\overline{\text{HDS1}}$ and $\overline{\text{HDS2}}$, a read/write strobe HR/$\overline{\text{W}}$, and an address strobe $\overline{\text{HAS}}$, to enable a glueless interface to a variety of industry-standard host devices. The HPI is easily interfaced to hosts with multiplexed address/data bus, separate address and data buses, one data strobe, and a read/write strobe, or two separate strobes for read and write. An HPI-ready pin, HRDY, is provided to specify wait states for hosts that support an asynchronous input. When the 'C57S/'LC57 operating frequency is variable, or when the host is capable of accessing at a faster rate than the maximum shared-access mode access rate, the HRDY pin provides a convenient way to adjust the host access rate automatically (no software handshake needed) to a change in the 'C57S/'LC57 clock rate or an HPI-mode switch.

The HPI supports high-speed back-to-back accesses. In the shared-access mode, the HPI can handle one byte every five 'C57S/'LC57 periods (that is, 64 Mb/s with a 40-MHz 'C57S/'LC57). The HPI is designed so that the host can take advantage of this high bandwidth and run at frequencies up to $(f \times n) \div 5$, where n is the number of host cycles for an external access and f is the 'C57S/'LC57 frequency. In host-only mode, the HPI supports even higher speed back-to-back host accesses: 1 byte every 50 ns (that is, 160 Mb/s) independently of the 'C57S/'LC57 clock rate.

serial ports

The 'C5x provides high-speed full-duplex serial ports that allow direct interface to other 'C5x devices, codecs, and other devices in a system. There is a general-purpose serial port, a time-division-multiplexed (TDM) serial port, and an auto-buffered serial port (BSP).

The general-purpose serial port uses two memory-mapped registers for data transfer: the data-transmit register (DXR) and the data-receive register (DRR). Both registers can be accessed in the same manner as any other memory location. The transmit and receive sections of the serial port each have associated clocks, frame-synchronization pulses, and serial shift registers, and serial data can be transferred either in bytes or in 16-bit words. Serial port receive and transmit operations can generate their own maskable transmit and receive interrupts (XINT and RINT), allowing serial port transfers to be managed by way of software. The 'C5x serial ports are double-buffered and fully static.

The TDM port allows the device to communicate through time-division multiplexing with up to seven other 'C5x devices with TDM ports. Time-division multiplexing is the division of time intervals into a number of subintervals with each subinterval representing a prespecified communications channel. The TDM port serially transmits 16-bit words on a single data line (TDAT) and destination addresses on a single address line (TADD). Each device can transmit data on a single channel and receive data from one or more of the eight channels providing a simple and efficient interface for multiprocessing applications. A frame synchronization pulse occurs once every 128 clock cycles corresponding to transmission of one 16-bit word on each of the eight channels. Like the general-purpose serial port, the TDM port is double-buffered on both input and output data. The TDM port also can be configured in software to operate as a general-purpose serial port as described above. Both types of ports are capable of operating at up to one-fourth the machine cycle rate (CLKOUT1).

The buffered serial port (BSP) consists of a full-duplex double-buffered serial port interface (SPI) and an auto-buffering unit (ABU). The SPI block of the BSP is an enhanced version of the general-purpose serial port. The auto-buffering unit allows the SPI to read/write directly to 'C5x internal memory using a dedicated bus independently of the CPU. This results in minimum overhead for SPI transactions and faster data rates.

serial ports (continued)

When auto-buffering capability is disabled (standard mode), transfers with SPI are performed under software control through interrupts. In this mode, the ABU is transparent and the word-based interrupts (WXINT and WRINT) provided by the SPI are sent to the CPU as transmit interrupt (XINT) and receive interrupt (RINT). When auto buffering is enabled, word transfers are done directly between the SPI and the 'C5x internal memory, using ABU-embedded address generators.

The ABU has its own set of circular addressing registers with corresponding address-generation units. Memory for the buffers resides in 2K words of 'C5x internal memory. The length and starting addresses of the buffers are user-programmable. A buffer-empty/-full interrupt can be posted to the CPU. Buffering is halted easily because of an auto-disabling capability. Auto-buffering capability can be enabled separately for transmit and receive sections. When auto-buffering is disabled, operation is similar to the general-purpose serial port.

The SPI allows transfer of 8-, 10-, 12-, or 16-bit data packets. In burst mode, data packets are directed by a frame-synchronization pulse for every packet. In continuous mode, the frame-synchronization pulse occurs when the data transmission is initiated and no further pulses occur. The frame and clock strobes are frequency and polarity programmable. The SPI is fully static and operates at arbitrarily low clock frequencies. The maximum operating frequency is CLKOUT1 (28.6 Mb/s at 35 ns, 40 Mb/s at 25 ns). The SPI transmit section also includes a pulse-coded modulation (PCM) mode that allows easy interface with a PCM line.

Most 'C5x devices provide one general-purpose serial port and one TDM port. The 'C52 provides one general-purpose serial port and no TDM port. The 'C53SX provides two general-purpose serial ports and no TDM port. The 'LC56, 'C57S, and 'LC57 devices provide one general-purpose serial port and one buffered serial port.

software wait-state generators

Software wait-state generation is incorporated in the 'C5x without any external hardware for interfacing with slower off-chip memory and I/O devices. The circuitry consists of 16 wait-state generating circuits and is user-programmable to operate with 0, 1, 2, 3, or 7 wait states. For off-chip memory accesses, these wait-state generators are mapped on 16K-word boundaries in program memory, data memory, and the I/O ports.

The 'C53S/'C57S and 'LC56/57 devices have software-programmable wait-state generators that are controlled by one 16-bit wait-state register PDWSR at address 0x28. The programmed number of wait states (0 through 7) applies to all external addresses at the corresponding address space (program, data, I/O) regardless of address value.

timer

The 'C5x features a 16-bit timing circuit with a 4-bit prescaler. This timer clocks between one-half and one thirty-second the machine rate of the device itself, depending on the programmable timer's divide-down ratio. This timer can be stopped, restarted, reset, or disabled by specific status bits.

The timer can be used to generate CPU interrupts periodically. The timer is decremented by one at every CLKOUT1 cycle. A timer interrupt (TINT) and a pulse equal to the duration of a CLKOUT1 cycle on the external TOUT pin are generated each time the counter decrements to zero. The timer provides a convenient means of performing periodic I/O or other functions. When the timer is stopped, the internal clocks to the timer are shut off, allowing the device to run in a low-power mode of operation.

IEEE 1149.1 boundary scan interface

The IEEE 1149.1 boundary-scan interface is used for emulation and test purposes. The IEEE 1149.1 scanning logic provides the boundary-scan path to and from the interfacing devices. Also, it can be used to test pin-to-pin continuity as well as to perform operational tests on those peripheral devices that surround the 'C5x. On 'C5x devices which do not provide boundary-scan capability, the IEEE 1149.1 interface is used for emulation purposes only. It is interfaced to other internal scanning logic circuitry, which has access to all of the on-chip resources. Thus, the 'C5x can perform on-board emulation by means of IEEE 1149.1 serial pins and the emulation-dedicated pins (see IEEE Standard 1149.1 for more details). Table 5 shows IEEE 1149.1 and boundary-scan functions supported by the 'C5x family of devices.

Table 5. IEEE 1149.1 Interface/Boundary Scan/On-Chip Analysis Block Configurations on the 'C5x/'LC5x Device Family

DEVICE TYPE	IEEE 1149.1 INTERFACE	BOUNDARY-SCAN CAPABILITY	ON-CHIP ANALYSIS BLOCK
'C50/'LC50	Yes	Yes	Full
'C51/'LC51	Yes	Yes	Full
'C52/'LC52	Yes	No	Full
'C53/'LC53	Yes	Yes	Full
'C53S/'LC53S	Yes	No	Reduced
'LC56	Yes	No	Full
'C57S	Yes	Yes	Full
'LC57	Yes	No	Full

on-chip analysis block

The on-chip analysis block, in conjunction with the 'C5x EVM, provides the capability to perform a variety of debugging and performance evaluation functions in a target system. The full analysis block provides capability for message passing by a combination of monitor mode and scan, flexible breakpoint setup based on events, counting of events, and a PC discontinuity trace buffer. Breakpoints can be triggered based on the following events: program fetches/reads/writes, EMU0/1 pin activity (used in multiprocessing), data reads/writes, CPU events (calls, returns, interrupts/traps, branches, pipeline clock), and event-counter overflow. The event counter is a 16-bit counter which can be used for performance analysis. The event counter can be incremented based on the occurrence of the following events: CPU clocks (performance monitoring), pipeline advances, instruction fetches (used to count instructions for an algorithm), branches, calls, returns, interrupts/traps, program reads/writes, or data reads/writes. The PC discontinuity-trace buffer provides a method to monitor program counter flow.

These analysis functions are available on all 'C5x devices except the 'C53S and 'LC53S which have a reduced analysis block (see Table 5). The reduced analysis block provides capability for message passing and breakpoints based on program fetches/reads/writes and EMU0/1 pin activity.

multiprocessing

The flexibility of the 'C5x allows configurations to satisfy a wide range of system requirements; the device can be used in a variety of system configurations, including, but not limited to, the following:

- A standalone processor
- A multiprocessor with devices in parallel
- A slave/host multiprocessor with global-memory space
- A peripheral processor interfaced via processor-controlled signals to another device

multiprocessing (continued)

For multiprocessing applications, the 'C5x is capable of allocating global-memory space and communicating with that space via the $\overline{BR}$ and ready control signals. Global memory is data memory shared by more than one device. Global memory access must be arbitrated. The 8-bit memory-mapped global memory allocation register (GREG) specifies part of the 'C5x's data memory as global external memory. The contents of the register determine the size of the global memory space. If the current instruction addresses an operand within that space, $\overline{BR}$ is asserted to request control of the bus. The length of the memory cycle is controlled by the READY line.

The 'C5x supports direct memory access (DMA) to its external program, data, and I/O spaces using the $\overline{HOLD}$ and $\overline{HOLDA}$ signals. Another device can take complete control of the 'C5x's external memory interface by asserting $\overline{HOLD}$ low. This causes the 'C5x to to place its address, data, and control lines in the high-impedance state and assert $\overline{HOLDA}$. While external memory is being accessed, program execution from on-chip memory can proceed concurrently when the device is in hold mode.

Multiple 'C5x devices can be interconnected through their serial ports. This form of interconnection allows information to be transferred at high speed while using a minimum number of signal connections. A complete full-duplex serial-port interconnection between multiple processors can be accomplished with as few as four signal lines.

instruction set

The 'C5x microprocessor implements a comprehensive instruction set that supports both numeric-intensive signal processing operations and general-purpose applications, such as multiprocessing and high-speed control. Source code for the 'C1x and 'C2x DSPs is upward compatible with the 'C5x.

For maximum throughput, the next instruction is prefetched while the current one is being executed. Because the same data lines are used to communicate to external data, program, or I/O space, the number of cycles an instruction requires to execute varies, depending on whether the next data operand fetch is from internal or external memory. Highest throughput is achieved by maintaining data memory on chip and using either internal or fast external program memory.

addressing modes

The 'C5x instruction set provides six basic memory-addressing modes: direct, indirect, immediate, register, memory mapped, and circular addressing.

In direct addressing, the instruction word contains the lowest seven bits of the data-memory address. This field is concatenated with the nine bits of the data-memory page pointer (DP) to form the 16-bit data-memory address. Therefore, in the direct-addressing mode, data memory is paged effectively with a total of 512 pages, each of which contains 128 words.

Indirect addressing accesses data memory through the auxiliary registers. In indirect addressing mode, the address of the instruction operand is contained in the currently selected auxiliary register. Eight auxiliary registers (AR0–AR7) provide flexible and powerful indirect addressing. To select a specific auxiliary register, the auxiliary register pointer (ARP) is loaded with a value from 0 to 7 for AR0 through AR7, respectively.

There are seven types of indirect addressing: autoincrement or autodecrement, postindexing by either adding or subtracting the contents of AR0, single-indirect addressing with no increment or decrement, and bit-reversed addressing (used in FFTs) with increment or decrement. All operations are performed on the current auxiliary register in the same cycle as the original instruction, following which the current auxiliary register and ARP can be modified.

addressing modes (continued)

In immediate addressing, the actual operand data is provided in a portion of the instruction word or words. There are two types of immediate addressing: long and short. In short-immediate addressing, the data is contained in a portion of the bits in a single-word instruction. In long-immediate addressing, the data is contained in the second word of a two-word instruction. The immediate-addressing mode is useful for data that does not need to be stored or used more than once during the course of program execution, such as initialization values, constants, etc.

The register-addressing mode uses operands in CPU registers either explicitly, such as with a direct reference to a specific register, or implicitly, with instructions that intrinsically reference certain registers. In either case, operand reference is simplified because 16-bit values can be used without specifying a full 16-bit operand address or immediate value.

Memory-mapped addressing provides the convenience of easy access to memory-mapped registers located on page zero of data memory. The flexibility of memory-mapped addressing results because accesses are made independently of actual DP value and without having to provide a complete address of the memory location being accessed. Commonly used on-board registers can be accessed with a simplified addressing scheme.

Circular addressing is the most sophisticated 'C5x addressing mode. This addressing mode allows specified buffers in memory to be accessed sequentially with a pointer that automatically wraps around to the beginning of the buffer when the last location is accessed. A total of two independent circular buffers can be allocated at any given time.

Five dedicated registers are allocated for implementation of circular addressing: a beginning-of-buffer and an end-of-buffer register for each of the two independent circular buffers and a control register. Additionally, one of the auxiliary registers is used as the pointer into the circular buffer. All registers used in circular addressing must be initialized properly prior to performing any circular buffer access.

The circular-addressing mode allows implementation of circular buffers, which facilitate data structures used in FIR filters, convolution and correlation algorithms, and waveform generators. Having the capability to access circular buffers automatically with no overhead allows these types of data structures to be implemented most efficiently.

repeat feature

The repeat function can be used with instructions such as multiply/accumulates (MAC and MACD), block moves (BLDD and BLPD), I/O transfers (IN/OUT), and table read/writes (TBLR/TBLW). These instructions, although normally multicycle, are pipelined when the repeat feature is used, and they effectively become single-cycle instructions. For example, the table-read instruction may take three or more cycles to execute, but when the instruction is repeated, a table location can be read every cycle.

The repeat counter (RPTC) is a 16-bit register that, when loaded with a number N, causes the next single instruction to be executed N + 1 times. The RPTC register is loaded by either the RPT or the RPTZ instruction, resulting in a maximum of 65,536 executions of a given instruction. RPTC is cleared by reset. The RPTZ instruction clears both ACC and PREG before the next instruction starts repeating. Once a repeat instruction (RPT or RPTZ) is decoded, all interrupts including $\overline{\text{NMI}}$ (except reset) are masked until the completion of the repeat loop. However, the device responds to the $\overline{\text{HOLD}}$ signal while executing an RPT/RPTZ loop.

repeat feature (continued)

The 'C5x implements a block-repeat feature that provides zero-overhead looping for implementation of FOR and DO loops. The function is controlled by three registers (PASR, PAER, and BRCR) and the BRAF bit in the PMST register. The block-repeat counter register (BRCR) is loaded with a loop count of 0 to 65,535. Then, execution of the RPTB (repeat block) instruction loads the program-address-start register (PASR) with the address of the instruction following the RPTB instruction and loads the program-address-end register (PAER) with its long-immediate operand. The long-immediate operand is the address of the instruction following the last instruction in the loop minus one. (The repeat block must contain at least three instruction words.) Execution of the RPTB instruction automatically sets active the BRAF bit. With each PC update, the PAER contents are compared to the PC. If they are equal, the BRCR contents are compared to zero. If the BRCR contents are greater than zero, BRCR is decremented and the PASR is loaded into the PC, repeating the loop. If not, the BRAF bit is set low and the processor resumes execution past the end of the code's loop.

The equivalent of a WHILE loop can be implemented by setting the BRAF bit to zero if the exit condition is met. The program then completes the current pass through the loop but does not go back to the top. To exit, the bit must be reset at least four instruction words before the end of the loop. It is possible to exit block-repeat loops and return to them without stopping and restarting the loop. Branches, calls, and interrupts do not necessarily affect the loop. When program control is returned to the loop, loop execution is resumed.

instruction set summary

This section summarizes the operational codes (opcodes) of the instruction set for the 'C5x digital signal processors. The instruction set is a super set of the 'C1x and 'C2x instruction sets. The instructions are arranged according to function and are alphabetized by mnemonic within each category. The symbols in Table 6 are used in the instruction set opcode table (Table 7). The Texas Instruments 'C5x assembler accepts 'C2x instructions as well as 'C5x instructions.

The number of words that an instruction occupies in program memory is specified in column 4 of Table 7. In these cases, different forms of the instruction occupy a different number of words. For example, the ADD instruction occupies one word when the operand is a short immediate value or two words if the operand is a long immediate value.

The number of cycles that an instruction requires to execute is listed in column 5 of Table 7. All instructions are assumed to be executed from internal program memory and internal data dual-access memory. The cycle timings are for single-instruction execution, not for repeat mode.

A read or write access to any peripheral memory-mapped register in data memory locations 20h–4Fh adds one cycle to the cycle time shown because all peripherals perform these accesses over the internal peripheral bus.

instruction set summary (continued)

Table 6. Opcode Symbols

SYMBOL	DESCRIPTION
A	Address
ACC	Accumulator
ACCB	Accumulator buffer
ARX	Auxiliary register value (0–7)
BITX	4-bit field specifies which bit to test for the BIT instruction
BMAR	Block-move address register
DBMR	Dynamic bit-manipulation register
I	Addressing-mode bit
II...II	Immediate operand value
INTM	Interrupt-mode flag bit
INTR#	Interrupt vector number
N	Field for the XC instruction, indicating the number of instructions (one or two) to execute conditionally
PREG	Product register
PROG	Program memory
RPTC	Repeat counter
SHF, SHFT	3/4 bit shift value
TC	Test-control bit
T P	Two bits used by the conditional execution instructions to represent the conditions TC, NTC, and $\overline{BIO}$ T P Meaning 0 0 $\overline{BIO}$ low 0 1 TC = 1 1 0 TC = 0 1 1 None of the above conditions
TREGn	Temporary register n (n = 0, 1, or 2)
Z L V C	4-bit field representing the following conditions: Z: ACC = 0 L: ACC < 0 V: Overflow C: Carry A conditional instruction contains two of these 4-bit fields. The 4-LSB field of the instruction is a 4-bit mask field. A 1 in the corresponding mask bit indicates that the condition is being tested. The second 4-bit field (bits 4–7) indicates the state of the conditions designated by the mask bits as being tested. For example, to test for ACC ≥ 0, the Z and L fields are set while the V and C fields are not set. The next 4-bit field contains the state of the conditions to test. The Z field is set to indicate testing the condition ACC = 0, and the L field is reset to indicate testing the condition ACC ≥ 0. The conditions possible with these 8 bits are shown in the BCND, CC, and XC instructions. To determine if the conditions are met, the 4-LSB bit mask is ANDed with the conditions. If any bits are set, the conditions are met.

instruction set summary (continued)

Table 7. TMS320C5x Instruction Set Opcodes

ACCUMULATOR MEMORY REFERENCE INSTRUCTIONS				
INSTRUCTION	**MNEMONIC**	**OPCODE**	**WORDS**	**CYCLES**
Absolute value of ACC	ABS	1011 1110 0000 0000	1	1
Add ACCB to ACC with carry	ADCB	1011 1110 0001 0001	1	1
Add to ACC with shift	ADD	0010 SHFT IAAA AAAA	1	1
Add to low ACC short immediate	ADD	1011 1000 IIII IIII	1	1
Add to ACC long immediate with shift	ADD	1011 1111 1001 SHFT	2	2
Add to ACC with shift of 16	ADD	0110 0001 IAAA AAAA	1	1
Add ACCB to ACC	ADDB	1011 1110 0001 0000	1	1
Add to ACC with carry	ADDC	0110 0000 IAAA AAAA	1	1
Add to low ACC with sign extension suppressed	ADDS	0110 0010 IAAA AAAA	1	1
Add to ACC with shift specified by TREG1 [3–0]	ADDT	0110 0011 IAAA AAAA	1	1
AND ACC with data value	AND	0110 1110 IAAA AAAA	1	1
AND with ACC long immediate with shift	AND	1011 1111 1011 SHFT	2	2
AND with ACC long immediate with shift of 16	AND	1011 1110 1000 0001	2	2
AND ACCB with ACC	ANDB	1011 1110 0001 0010	1	1
Barrel shift ACC right	BSAR	1011 1111 1110 SHFT	1	1
Complement ACC	CMPL	1011 1110 0000 0001	1	1
Store ACC in ACCB if ACC > ACCB	CRGT	1011 1110 0001 1011	1	1
Store ACC in ACCB if ACC< ACCB	CRLT	1011 1110 0001 1100	1	1
Exchange ACCB with ACC	EXAR	1011 1110 0001 1101	1	1
Load ACC with ACCB	LACB	1011 1110 0001 1111	1	1
Load ACC with shift	LACC	0001 SHFT IAAA AAAA	1	1
Load ACC long immediate with shift	LACC	1011 1111 1000 SHFT	2	2
Load ACC with shift of 16	LACC	0110 1010 IAAA AAAA	1	1
Load low word of ACC with immediate	LACL	1011 1001 IIII IIII	1	1
Load low word of ACC	LACL	0110 1001 IAAA AAAA	1	1
Load ACC with shift specified by TREG1 [3–0]	LACT	0110 1011 IAAA AAAA	1	1
Load ACCL with memory-mapped register	LAMM	0000 1000 IAAA AAAA	1	1 or 2
Negate ACC	NEG	1011 1110 0000 0010	1	1
Normalize ACC	NORM	1010 0000 IAAA AAAA	1	1
OR ACC with data value	OR	0110 1101 IAAA AAAA	1	1
OR with ACC long immediate with shift	OR	1011 1111 1100 SHFT	2	2
OR with ACC long immediate with shift of 16	OR	1011 1110 1000 0010	2	2
OR ACCB with ACC	ORB	1011 1110 0001 0011	1	1
Rotate ACC 1 bit left	ROL	1011 1110 0000 1100	1	1
Rotate ACCB and ACC left	ROLB	1011 1110 0001 0100	1	1
Rotate ACC 1 bit right	ROR	1011 1110 0000 1101	1	1
Rotate ACCB and ACC right	RORB	1011 1110 0001 0101	1	1
Store ACC in ACCB	SACB	1011 1110 0001 1110	1	1
Store high ACC with shift	SACH	1001 1SHF IAAA AAAA	1	1
Store low ACC with shift	SACL	1001 0SHF IAAA AAAA	1	1
Store ACCL to memory-mapped register	SAMM	1000 1000 IAAA AAAA	1	1 or 2
Shift ACC 16 bits right if TREG1 [4] = 0	SATH	1011 1110 0101 1010	1	1
Shift ACC0–ACC15 right as specified by TREG1 [3–0]	SATL	1011 1110 0101 1011	1	1
Subtract ACCB from ACC	SBB	1011 1110 0001 1000	1	1
Subtract ACCB from ACC with borrow	SBBB	1011 1110 0001 1001	1	1
Shift ACC 1 bit left	SFL	1011 1110 0000 1001	1	1
Shift ACCB and ACC left	SFLB	1011 1110 0001 0110	1	1
Shift ACC 1 bit right	SFR	1011 1110 0000 1010	1	1
Shift ACCB and ACC right	SFRB	1011 1110 0001 0111	1	1
Subtract from ACC with shift	SUB	0011 SHFT IAAA AAAA	1	1
Subtract from ACC with shift of 16	SUB	0110 0101 IAAA AAAA	1	1
Subtract from ACC short immediate	SUB	1011 1010 IIII IIII	1	1
Subtract from ACC long immediate with shift	SUB	1011 1111 1010 SHFT	2	2

instruction set summary (continued)

Table 7. TMS320C5x Instruction Set Opcodes (Continued)

ACCUMULATOR MEMORY REFERENCE INSTRUCTIONS (CONTINUED)				
INSTRUCTION	**MNEMONIC**	**OPCODE**	**WORDS**	**CYCLES**
Subtract from ACC with borrow	SUBB	0110 0100 IAAA AAAA	1	1
Conditional subtract	SUBC	0000 1010 IAAA AAAA	1	1
Subtract from ACC with sign extension suppressed	SUBS	0110 0110 IAAA AAAA	1	1
Subtract from ACC, shift specified by TREG1 [3–0]	SUBT	0110 0111 IAAA AAAA	1	1
XOR ACC with data value	XOR	0110 1100 IAAA AAAA	1	1
XOR with ACC long immediate with shift	XOR	1011 1111 1101 SHFT	2	2
XOR with ACC long immediate with shift of 16	XOR	1011 1110 1000 0011	2	2
XOR ACCB with ACC	XORB	1011 1110 0001 1010	1	1
Zero ACC, load high ACC with rounding	ZALR	0110 1000 IAAA AAAA	1	1
Zero ACC and product register	ZAP	1011 1110 0101 1001	1	1
AUXILIARY REGISTERS AND DATA PAGE POINTER INSTRUCTIONS				
INSTRUCTION	**MNEMONIC**	**OPCODE**	**WORDS**	**CYCLES**
Add to AR short immediate	ADRK	0111 1000 IIII IIII	1	1
Compare AR with CMPR	CMPR	1011 1111 0100 01CM	1	1
Load AR from addressed data	LAR	0000 0ARX IAAA AAAA	1	1
Load AR short immediate	LAR	1011 0ARX IIII IIII	1	1
Load AR long immediate	LAR	1011 1111 0000 1ARX	2	2
Load data page pointer with addressed data	LDP	0000 1101 IAAA AAAA	1	2
Load data page immediate	LDP	1011 110I IIII IIII	1	2
Modify auxiliary register	MAR	1000 1011 IAAA AAAA	1	1
Store AR to addressed data	SAR	1000 0ARX IAAA AAAA	1	1
Subtract from AR short immediate	SBRK	0111 1100 IIII IIII	1	1
BRANCH INSTRUCTIONS				
INSTRUCTION	**MNEMONIC**	**OPCODE**	**WORDS**	**CYCLES**
Branch unconditional with AR update	B	0111 1001 1AAA AAAA	2	4
Branch addressed by ACC	BACC	1011 1110 0010 0000	1	4
Branch addressed by ACC delayed	BACCD	1011 1110 0010 0001	1	2
Branch AR ≠ 0 with AR update	BANZ	0111 1011 1AAA AAAA	2	2 or 4
Branch AR ≠ 0 with AR update delayed	BANZD	0111 1111 1AAA AAAA	2	2
Branch conditional	BCND	1110 00TP ZLVC ZLVC	2	2 or 4
Branch conditional delayed	BCNDD	1111 00TP ZLVC ZLVC	2	2
Branch unconditional with AR update delayed	BD	0111 1101 1AAA AAAA	2	2
Call subroutine addressed by ACC	CALA	1011 1110 0011 0000	1	4
Call subroutine addressed by ACC delayed	CALAD	1011 1110 0011 1101	1	2
Call unconditional with AR update	CALL	0111 1010 1AAA AAAA	2	4
Call unconditional with AR update delayed	CALLD	0111 1110 1AAA AAAA	2	2
Call conditional	CC	1110 10TP ZLVC ZLVC	2	2 or 4
Call conditional delayed	CCD	1111 10TP ZLVC ZLVC	2	2
Software interrupt	INTR	1011 1110 011I NTR#	1	4
Nonmaskable interrupt	NMI	1011 1110 0101 0010	1	4
Return	RET	1110 1111 0000 0000	1	4
Return conditional	RETC	1110 11TP ZLVC ZLVC	1	2 or 4
Return conditionally, delayed	RETCD	1111 11TP ZLVC ZLVC	1	2
Return, delayed	RETD	1111 1111 0000 0000	1	2
Return from interrupt with enable	RETE	1011 1110 0011 1010	1	4
Return from interrupt	RETI	1011 1110 0011 1000	1	4
Trap	TRAP	1011 1110 0101 0001	1	4
Execute next one or two INST on condition	XC	111N 01TP ZLVC ZLVC	1	1

instruction set summary (continued)

Table 7. TMS320C5x Instruction Set Opcodes (Continued)

I/O AND DATA MEMORY OPERATIONS				
INSTRUCTION	**MNEMONIC**	**OPCODE**	**WORDS**	**CYCLES**
Block move from data to data memory	BLDD	1010 1000 IAAA AAAA	2	3
Block move data to data DEST long immediate	BLDD	1010 1001 IAAA AAAA	2	3
Block move data to data with source in BMAR	BLDD	1010 1100 IAAA AAAA	1	2
Block move data to data with DEST in BMAR	BLDD	1010 1101 IAAA AAAA	1	2
Block move data to PROG with DEST in BMAR	BLDP	0101 0111 IAAA AAAA	1	2
Block move from program to data memory	BLPD	1010 0101 IAAA AAAA	2	3
Block move PROG to data with source in BMAR	BLPD	1010 0100 IAAA AAAA	1	2
Data move in data memory	DMOV	0111 0111 IAAA AAAA	1	1
Input external access	IN	1010 1111 IAAA AAAA	2	2
Load memory-mapped register	LMMR	1000 1001 IAAA AAAA	2	2 or 3
Out external access	OUT	0000 1100 IAAA AAAA	2	3
Store memory-mapped register	SMMR	0000 1001 IAAA AAAA	2	2 or 3
Table read	TBLR	1010 0110 IAAA AAAA	1	3
Table write	TBLW	1010 0111 IAAA AAAA	1	3
PARALLEL LOGIC UNIT INSTRUCTIONS				
INSTRUCTION	**MNEMONIC**	**OPCODE**	**WORDS**	**CYCLES**
AND DBMR with data value	APL	0101 1010 IAAA AAAA	1	1
AND long immediate with data value	APL	0101 1110 IAAA AAAA	2	2
Compare DBMR to data value	CPL	0101 1011 IAAA AAAA	1	1
Compare data with long immediate	CPL	0101 1111 IAAA AAAA	2	2
OR DBMR to data value	OPL	0101 1001 IAAA AAAA	1	1
OR long immediate with data value	OPL	0101 1101 IAAA AAAA	2	2
Store long immediate to data	SPLK	1010 1110 IAAA AAAA	2	2
XOR DBMR to data value	XPL	0101 1000 IAAA AAAA	1	1
XOR long immediate with data value	XPL	0101 1100 IAAA AAAA	2	2
T REGISTER, P REGISTER, AND MULTIPLY INSTRUCTIONS				
INSTRUCTION	**MNEMONIC**	**OPCODE**	**WORDS**	**CYCLES**
Add PREG to ACC	APAC	1011 1110 0000 0100	1	1
Load high PREG	LPH	0111 0101 IAAA AAAA	1	1
Load TREG0	LT	0111 0011 IAAA AAAA	1	1
Load TREG0 and accumulate previous product	LTA	0111 0000 IAAA AAAA	1	1
Load TREG0, accumulate previous product, and move data	LTD	0111 0010 IAAA AAAA	1 1	1 1
Load TREG0 and load ACC with PREG	LTP	0111 0001 IAAA AAAA	1	1
Load TREG0 and subtract previous product	LTS	0111 0100 IAAA AAAA	1	1
Multiply/accumulate	MAC	1010 0010 IAAA AAAA	2	3
Multiply/accumulate with data shift	MACD	1010 0011 IAAA AAAA	2	3
Mult/ACC w/source ADRS in BMAR and DMOV	MADD	1010 1011 IAAA AAAA	1	3
Mult/ACC with source address in BMAR	MADS	1010 1010 IAAA AAAA	1	3
Multiply data value times TREG0	MPY	0101 0100 IAAA AAAA	1	1
Multiply TREG0 by 13-bit immediate	MPY	110I IIII IIII IIII	1	1
Multiply TREG0 by long immediate	MPY	1011 1110 1000 0000	2	2
Multiply TREG0 by data, add previous product	MPYA	0101 0000 IAAA AAAA	1	1
Multiply TREG0 by data, ACC – PREG	MPYS	0101 0001 IAAA AAAA	1	1
Multiply unsigned data value times TREG0	MPYU	0101 0101 IAAA AAAA	1	1
Load ACC with product register	PAC	1011 1110 0000 0011	1	1
Subtract product from ACC	SPAC	1011 1110 0000 0101	1	1
Store high product register	SPH	1000 1101 IAAA AAAA	1	1
Store low product register	SPL	1000 1100 IAAA AAAA	1	1
Set PREG shift count	SPM	1011 1111 0000 00PM	1	1
Data to TREG0, square it, add PREG to ACC	SQRA	0101 0010 IAAA AAAA	1	1
Data to TREG0, square it, ACC – PREG	SQRS	0101 0011 IAAA AAAA	1	1
Zero product register	ZPR	1011 1110 0101 1000	1	1

instruction set summary (continued)

Table 7. TMS320C5x Instruction Set Opcodes (Continued)

CONTROL INSTRUCTIONS				
INSTRUCTION	**MNEMONIC**	**OPCODE**	**WORDS**	**CYCLES**
Test bit specified immediate	BIT	0100 BITX IAAA AAAA	1	1
Test bit in data value as specified by TREG2 [3–0]	BITT	0110 1111 IAAA AAAA	1	1
Reset overflow mode	CLRC	1011 1110 0100 0010	1	1
Reset sign extension mode	CLRC	1011 1110 0100 0110	1	1
Reset hold mode	CLRC	1011 1110 0100 1000	1	1
Reset TC bit	CLRC	1011 1110 0100 1010	1	1
Reset carry	CLRC	1011 1110 0100 1110	1	1
Reset CNF bit	CLRC	1011 1110 0100 0100	1	1
Reset INTM bit	CLRC	1011 1110 0100 0000	1	1
Reset XF pin	CLRC	1011 1110 0100 1100	1	1
Idle	IDLE	1011 1110 0010 0010	1	1
Idle until interrupt — low-power mode	IDLE2	1011 1110 0010 0011	1	1
Load status register 0	LST	0000 1110 IAAA AAAA	1	2
Load status register 1	LST	0000 1111 IAAA AAAA	1	2
No operation	NOP	1000 1011 0000 0000	1	1
Pop PC stack to low ACC	POP	1011 1110 0011 0010	1	1
Pop stack to data memory	POPD	1000 1010 IAAA AAAA	1	1
Push data memory value onto PC stack	PSHD	0111 0110 IAAA AAAA	1	1
Push low ACC to PC stack	PUSH	1011 1110 0011 1100	1	1
Repeat instruction as specified by data	RPT	0000 1011 IAAA AAAA	1	2
Repeat next INST specified by long immediate	RPT	1011 1110 1100 0100	2	2
Repeat INST specified by short immediate	RPT	1011 1011 IIII IIII	1	2
Block repeat	RPTB	1011 1110 1100 0110	2	2
Clear ACC/PREG and repeat next INST long immediate	RPTZ	1011 1110 1100 0101	2	2
Set overflow mode	SETC	1011 1110 0100 0011	1	1
Set sign extension mode	SETC	1011 1110 0100 0111	1	1
Set hold mode	SETC	1011 1110 0100 1001	1	1
Set TC bit	SETC	1011 1110 0100 1011	1	1
Set carry	SETC	1011 1110 0100 1111	1	1
Set XF pin high	SETC	1011 1110 0100 1101	1	1
Set CNF bit	SETC	1011 1110 0100 0101	1	1
Set INTM bit	SETC	1011 1110 0100 0001	1	1
Store status register 0	SST	1000 1110 IAAA AAAA	1	1
Store status register 1	SST	1000 1111 IAAA AAAA	1	1

development support

Texas Instruments offers an extensive line of development tools for the 'C5x generation of DSPs, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of 'C5x-based applications:

Software Development Tools:
Assembler/Linker
Simulator
Optimizing ANSI C compiler
Application algorithms
C/Assembly debugger and code profiler

development support (continued)

Hardware Development Tools:
Extended development set (XDS™) emulator (supports 'C5x multiprocessor system debug)
'C5x EVM (Evaluation Module)
'C5x DSK (DSP Starter Kit)

The *TMS320 Family Development Support Reference Guide* (SPRU011) contains information about development support products for all TMS320 family member devices, including documentation. Refer to this document for further information about TMS320 documentation or any other TMS320 support products from Texas Instruments. There is an additional document, the *TMS320 Third Party Support Reference Guide* (SPRU052), which contains information about TMS320-related products from other companies in the industry. To receive copies of TMS320 literature, contact the Literature Response Center at 800/477-8924.

See Table 8 for complete listings of development support tools for the 'C5x. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

Table 8. TMS320C5x, TMS320LC5x Development Support Tools

DEVELOPMENT TOOL	PLATFORM	PART NUMBER
Software		
Compiler/Assembler/Linker	PC-DOS™, OS/2™	TMDS3242855-02
Compiler/Assembler/Linker	SPARC™, HP™	TMDS3242555-08
Assembler/Linker	PC-DOS, OS/2™	TMDS3242850-02
Simulator	PC-DOS, WIN™	TMDS3245851-02
Simulator	SPARC	TMDS3245551-09
Digital Filter Design Package	PC-DOS	DFDP
Debugger/Emulation Software	PC-DOS, OS/2, WIN	TMDS3240150
Debugger/Emulation Software	SPARC™	TMDS3240650
Hardware		
XDS-510 XL Emulator	PC-DOS, OS/2	TMD000510
XDS-510 WS Emulator	SPARC	TMDS000510WS
EVM Evaluation Module	PC-DOS, WIN	TMDS3260050
DSK DSP Starter Kit	PC-DOS	TMDS3200051

device and development support tool nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320 devices and support tools. Each TMS320 member has one of three prefixes: TMX, TMP, or TMS. Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS). This development flow is defined below.

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

PC-DOS and OS/2 are trademarks of International Business Machines Corp.
SPARC is a trademark of SPARC International, Inc.
WIN is a trademark of Microsoft Corporation.
HP is a trademark of Hewlett-Packard Company.
XDS is a trademark of Texas Instruments Incorporated.

device and development support tool nomenclature (continued)

TMS Fully-qualified production device

Support tool development evolutionary flow:

TMDX Development support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully qualified development support product

TMX and TMP devices and TMDX development support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development support tools have been characterized fully, and the quality and reliability of the device has been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, N, FN, or GB) and temperature range (for example, L). Figure 8 provides a legend for reading the complete device name for any TMS320 family member.

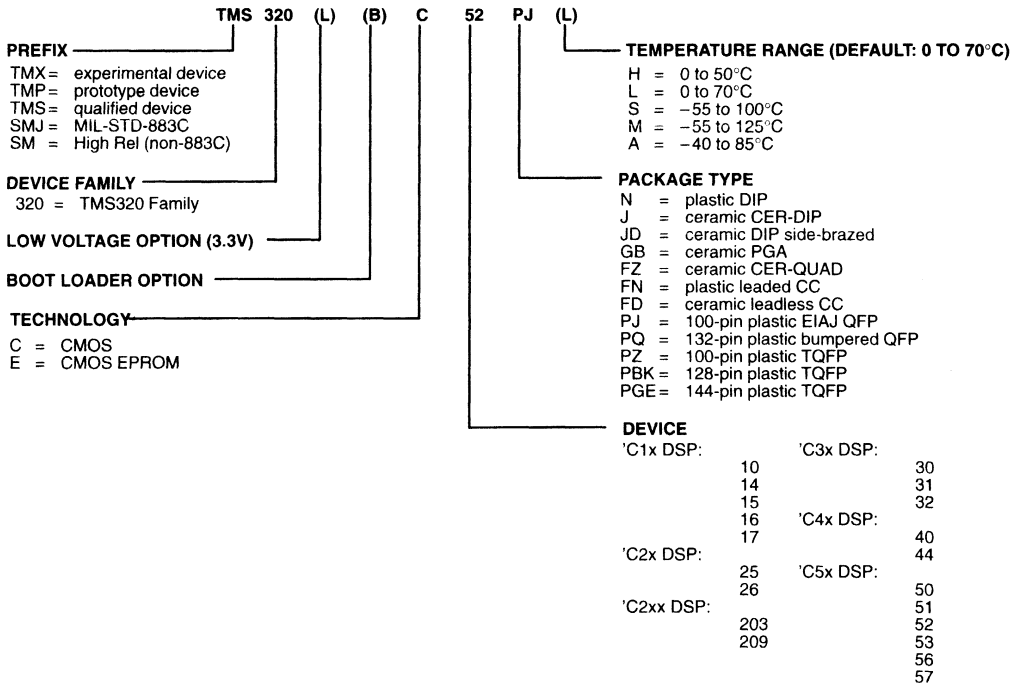


Figure 8. TMS320 Device Nomenclature

documentation support

Extensive documentation supports all TMS320 family generations of devices from product announcement through applications development. The types of documentation available include data sheets, such as this document, with design specifications, complete user's guides for all devices, development support tools, and three volumes of the publication *Digital Signal Processing Applications with the TMS320 Family* (literature numbers SPRA012, SPRA016, and SPRA017).

The application book series describes hardware and software applications, including algorithms, for fixed and floating point TMS320 family devices. The *TMS320C5x User's Guide* (literature number SPRU056), which describes in detail the fifth-generation TMS320 products, is currently available.

A series of DSP textbooks is published by Prentice-Hall and John Wiley & Sons to support digital signal processing research and education. The TMS320 newsletter, *Details on Signal Processing*, is published quarterly and distributed to update TMS320 customers on product information. The TMS320 DSP bulletin board service (BBS) provides access to information pertaining to the TMS320 family, including documentation, source code and object code for many DSP algorithms and utilities. The BBS can be reached at 713/274-2323.

Information regarding TI DSP products is also available on the Worldwide Web at http:/www.ti.com uniform resource locator (URL).

absolute maximum ratings over operating ambient-air temperature range (unless otherwise noted) ('320C5x only)†

Supply voltage range, V_{DD} (see Note 3) . . . . . – 0.3 V to 7 V
Input voltage range, V_I . . . . . – 0.3 V to 7 V
Output voltage range, V_O . . . . . – 0.3 V to 7 V
Operating ambient temperature range, T_A . . . . . –40°C to 85°C
Operating case temperature, T_C . . . . . 0°C to 85°C
Storage temperature range, T_{stg} . . . . . – 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 3: All voltage values are with respect to V_{SS}.

recommended operating conditions ('320C5x only)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.75	5	5.25	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	X2/CLKIN, CLKIN2	3		$V_{DD}+0.3$	V
		CLKX, CLKR, TCLKX, TCLKR	2.5		$V_{DD}+0.3$	
		All other inputs	2		$V_{DD}+0.3$	
V_{IL}	Low-level input voltage	X2/CLKIN, CLKIN2, CLKX, CLKR, TCLKX, TCLKR	– 0.3		0.7	V
		All other inputs	– 0.3		0.8	
I_{OH}	High-level output current (see Note 4)				– 300‡	µA
I_{OL}	Low-level output current				2	mA
T_C	Operating case temperature		0		85	°C
T_A	Operating ambient temperature		–40		85	°C

‡ This I_{OH} can be exceeded when using a 1-kΩ pulldown resistor on the TDM serial port TADD output; however, this output still meets V_{OH} specifications under these conditions.

NOTE 4: Figure 9 shows the test load circuit and Figure 10 and Figure 11 show the voltage reference levels.

electrical characteristics over recommended ranges of supply voltage and operating ambient-air temperature (unless otherwise noted) ('320C5x only)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{OH}	High-level output voltage (see Note 4)	I_{OH} = 300 µA	2.4	3		V
V_{OL}	Low-level output voltage (see Note 4)	I_{OL} = 2 mA		0.3	0.6	V
I_{OZ}	High-impedance output current (V_{DD} = 5.25 V)	$\overline{BR}$ (with internal pullup)	– 500		20	µA
		All other 3-state outputs	– 20		20	
I_I	Input current (V_I = V_{SS} to V_{DD})	$\overline{TRST}$ (with internal pulldown)	– 10		800	µA
		TMS, TCK, TDI (with internal pullups)	– 500		10	
		X2/CLKIN	– 50		50	
		All other inputs	– 10		10	
$I_{DD(core)}$	Supply current, core CPU	f_x = 40 MHz, V_{DD} = 5.25 V		60		mA
		f_x = 57 MHz, V_{DD} = 5.25 V		67		
		f_x = 80 MHz, V_{DD} = 5.25 V		94		
		f_x = 100 MHz, V_{DD} = 5.25 V		110		
$I_{DD(pins)}$	Supply current, pins	f_x = 40 MHz, V_{DD} = 5.25 V		40		mA
		f_x = 57 MHz, V_{DD} = 5.25 V		45		
		f_x = 80 MHz, V_{DD} = 5.25 V		63		
		f_x = 100 MHz, V_{DD} = 5.25 V		75		
$I_{DD(standby)}$	Supply current, standby	IDLE2, divide-by-two clock mode, clocks shut off		5		µA
C_i	Input capacitance			15		pF
C_o	Output capacitance			15		pF

† Typical values are at V_{DD} = 5 V, T_A = 25°C, unless otherwise specified.
NOTE 4: Figure 9 shows the test load circuit and Figure 10 and Figure 11 show the voltage reference levels.

absolute maximum ratings over specified temperature range (unless otherwise noted) ('320LC5x only)†

Supply voltage range, V_{DD} (see Note 3) . . . . . −0.3 V to 5 V
Input voltage range, V_I . . . . . −0.3 V to 5 V
Output voltage range, V_O . . . . . −0.3 V to 5 V
Operating ambient temperature range, T_A . . . . . −40° to 85°C
Operating case temperature, T_C . . . . . 0°C to 85°C
Storage temperature range, T_{stg} . . . . . −55° to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 3: All voltage values are with respect to V_{SS}.

recommended operating conditions ('320LC5x only)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		3.13	3.3	3.47	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	X2/CLKIN, CLKIN2	2.5		V_{DD} + 0.3	V
		CLKX, CLKR, TCLKX, TCLKR	2.0		V_{DD} + 0.3	
		All other inputs	1.8		V_{DD} + 0.3	
V_{IL}	Low-level input voltage	X2/CLKIN, CLKIN2, CLKX, CLKR, TCLKX, TCLKR	−0.3		0.5	V
		All other inputs	−0.3		0.6	V
I_{OH}	High-level output current				− 300‡	μA
I_{OL}	Low-level output current				2	mA
T_C	Operating case temperature		0		85	°C
T_A	Operating ambient temperature		−40		85	°C

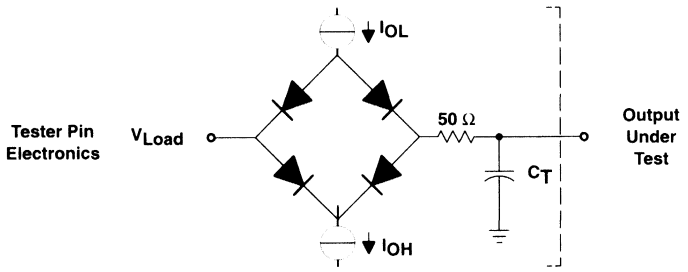
‡ This I_{OH} may be exceeded when using a 1-kΩ pulldown resistor on the TDM serial port TADD output; however, this output still meets V_{OH} specifications under these conditions.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) ('320LC5x only)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (see Note 4)	I_{OH} = 300 µA	2.0			V
		I_{OH} = 20 µA		V_{DD} – 0.3‡		
V_{OL}	Low-level output voltage (see Note 4)	I_{OL} = 2 mA			0.4	V
		I_{OL} = 20 µA		0.3‡		
I_{OZ}	High-impedance output current (V_{DD} = 3.47 V)	$\overline{BR}$ (with internal pullup)	–500		20	µA
		All other 3-state outputs	–20		20	
I_I	Input current (V_I = V_{SS} to V_{DD})	$\overline{TRST}$(with internal pulldown)	–10		800	µA
		TMS, TCK, TDI pins (with internal pullups)	–500		10	
		X2/CLKIN (oscillator enabled)	–50		50	
		X2/CLKIN (oscillator disabled)	–10		10	
		All other inputs	–10		10	
$I_{DD(core)}$	Supply current, core CPU	f_x = 40 MHz, V_{DD} = 3.47 V		26		mA
		f_x = 50 MHz, V_{DD} = 3.47 V		33		
		f_x = 80 MHz, V_{DD} = 3.47 V		53		
$I_{DD(pins)}$	Supply current, pins	f_x = 40 MHz, V_{DD} = 3.47 V		18		mA
		f_x = 50 MHz, V_{DD} = 3.47 V		22		
		f_x = 80 MHz, V_{DD} = 3.47 V		35		
$I_{DD(standby)}$	Supply current, standby	IDLE2, divide-by-two clock mode, clocks shut off		5		µA
C_i	Input capacitance			15		pF
C_o	Output capacitance			15		pF

† All typical values are at V_{DD} = 3.3 V, T_A = 25°C.
‡ Values derived from characterization data and not tested
NOTE 4: Figure 9 shows the test load circuit and Figure 10 and Figure 11 show the voltage reference levels.

PARAMETER MEASUREMENT INFORMATION



Where:

I_{OL}	=	2 mA (all outputs) minimum
I_{OH}	=	300 μA (all outputs) minimum
V_{LOAD}	=	1.5 V
C_T	=	80-pF typical load circuit capacitance

Figure 9. Test Load Circuit

signal transition levels

The data in this section is shown for both the 5-V version ('C5x) and the 3.3-V version ('LC5x). In each case, the 5-V data is shown followed by the 3.3-V data in parentheses. TTL-output levels are driven to a minimum logic-high level of 2.4 V (2 V) and to a maximum logic-low level of 0.6 V (0.4 V). Figure 10 shows the TTL-level outputs.

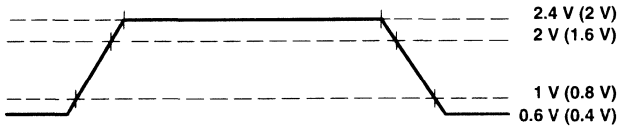


Figure 10. TTL-Level Outputs

TTL-output transition times are specified as follows:

- For a *high-to-low transition*, the level at which the output is said to be no longer high is 2 V (1.6 V), and the level at which the output is said to be low is 1 V (0.8 V).
- For a *low-to-high transition*, the level at which the output is said to be no longer low is 1 V (0.8 V), and the level at which the output is said to be high is 2 V (1.6 V).

Figure 11 shows the TTL-level inputs.

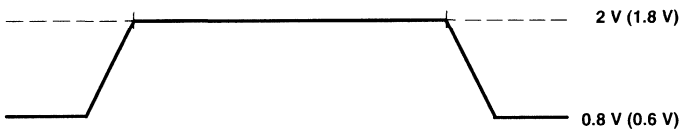


Figure 11. TTL-Level Inputs

TTL-compatible input transition times are specified as follows:

- For a *high-to-low transition* on an input signal, the level at which the input is said to be no longer high is 2 V (1.8 V), and the level at which the input is said to be low is 0.8 V (0.6 V).
- For a *low-to-high transition* on an input signal, the level at which the input is said to be no longer low is 0.8 V (0.6 V), and the level at which the input is said to be high is 2 V (1.8 V).

PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols used are created in accordance with JEDEC Standard 100-A. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

Lowercase subscripts and their meanings:	
a	access time
c	cycle time (period)
d	delay time
dis	disable time
en	enable time
f	fall time
h	hold time
r	rise time
su	setup time
t	transition time
v	valid time
w	pulse duration (width)
X	Unknown, changing, or don't care level

Letters and symbols and their meanings:	
H	High
L	Low
V	Valid
Z	High impedance

CLOCK CHARACTERISTICS AND TIMING

The 'C5x can use either its internal oscillator or an external frequency source for a clock. The clock mode is determined by the clock mode pins (CLKMD1, CLKMD2, and CLKMD3). Table 9 shows the standard clock options available on the 'C50, 'LC50, 'C51, 'LC51, 'C52, 'LC52, 'C53, 'LC53, 'C53S, and 'LC53S. For these devices, the CLKIN2 pin functions as the external frequency input when using the PLL options. An expanded set of clock options is shown in Table 10 and is available on the 'LC56, 'C57S, and 'LC57 devices. For these devices, X2/CLKIN functions as the external frequency input when using the PLL options.

Table 9. Standard Clock Options

CLKMD1	CLKMD2	CLOCK SOURCE
1	0	PLL clock generator option†
0	1	Reserved for test purposes
1	1	External divide-by-two option or internal divide-by-two clock option with an external crystal
0	0	External divide-by-two option with the internal oscillator disabled

† PLL multiply-by-one option on 'C50, 'C51, 'C53, 'C53S devices, PLL multiply-by-two option on 'C52 device

Table 10. PLL Clock Option for 'LC56, 'C57S, and 'LC57

CLKMD1	CLKMD2	CLKMD3	CLOCK SOURCE
0	0	0	PLL multiply-by-three
0	1	0	PLL multiply-by-four
1	0	0	PLL multiply-by-five
1	1	0	PLL multiply-by-nine
0	0	1	External divide-by-two option with oscillator disabled
0	1	1	PLL multiply-by-two
1	0	1	PLL multiply-by-one
1	1	1	External/Internal divide-by-two with oscillator enabled

internal divide-by-two clock option with external crystal

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN. The frequency of CLKOUT1 is one-half of the crystal's oscillating frequency. The crystal should be in either fundamental or overtone operation and parallel resonant, with an effective series resistance of 30 Ω and a power dissipation of 1 mW; it should be specified at a load capacitance of 20 pF. Overtone crystals require an additional tuned-LC circuit. Figure 12 shows an external crystal (fundamental frequency) connected to the on-chip oscillator.

recommended operating conditions for internal divide-by-two clock option

		MIN	NOM	MAX	UNIT
f_{clk} Input clock frequency	TMS320C5x-40	0†		40.96	MHz
	TMS320C5x-57	0†		57.14	
	TMS320C5x-80	0†		80	
	TMS320C5x-100‡	0†		100	
	TMS320LC5x-40	0†		40	MHz
	TMS320LC5x-50	0†		50	
	TMS320LC5x-80	0†		80	
C1, C2 Load capacitance			10		pF

† This device utilizes a fully static design and, therefore, can operate with input clock cycle time ($t_{c(CI)}$) approaching ∞. The device is characterized at frequencies approaching 0 Hz, but is tested at f_{clk} = 6.7 MHz to meet device test time requirements.
‡ '320C51, '320C52 currently available at this clock speed

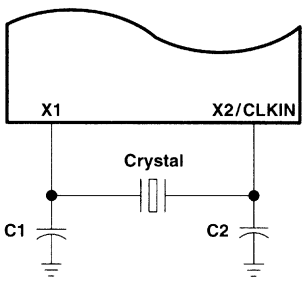


Figure 12. Internal Clock Option

external divide-by-two clock option

An external frequency source can be used by injecting the frequency directly into X2/CLKIN with X1 left unconnected. Refer to Table 9 and Table 10 for appropriate configuration of the CLKMD1, CLKMD2 and CLKMD3 pins to generate the external divide-by-2 clock option. The external frequency injected must conform to the specifications listed in the timing requirements table.

switching characteristics over recommended operating conditions [H = 0.5 $t_{c(CO)}$] ('320C5x only) (see Figure 13)

PARAMETER		'320C5x-40			'320C5x-57			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(CO)}$	Cycle time, CLKOUT1	48.8	$2t_{c(CI)}$	†	35	$2t_{c(CI)}$	†	ns
$t_{d(CIH-COH/L)}$	Delay time, X2/CLKIN high to CLKOUT1 high/low	3	11	20	3	11	20	ns
$t_{f(CO)}$	Fall time, CLKOUT1		5			5		ns
$t_{r(CO)}$	Rise time, CLKOUT1		5			5		ns
$t_{w(COL)}$	Pulse duration, CLKOUT1 low	H – 3	H	H + 2	H – 3	H	H + 2	ns
$t_{w(COH)}$	Pulse duration, CLKOUT1 high	H – 3	H	H + 2	H – 3	H	H + 2	ns

PARAMETER		'320C5x-80			'320C5x-100			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(CO)}$	Cycle time, CLKOUT1	25	$2t_{c(CI)}$	†	20	$2t_{c(CI)}$	†	ns
$t_{d(CIH-COH/L)}$	Delay time, X2/CLKIN high to CLKOUT1 high/low	1	9	18	1	9	18	ns
$t_{f(CO)}$	Fall time, CLKOUT1		4			4		ns
$t_{r(CO)}$	Rise time, CLKOUT1		4			4		ns
$t_{w(COL)}$	Pulse duration, CLKOUT1 low	H – 3	H	H + 2	H – 3	H	H + 2	ns
$t_{w(COH)}$	Pulse duration, CLKOUT1 high	H – 3	H	H + 2	H – 3	H	H + 2	ns

switching characteristics over recommended operating conditions [H = 0.5 $t_{c(CO)}$] ('320LC5x only) (see Figure 13)

PARAMETER		'320LC5x-40			'320LC5x-50			'320LC5x-80			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
$t_{c(CO)}$	Cycle time, CLKOUT1	50	$2t_{c(CI)}$	†	40	$2t_{c(CI)}$	†	25	$2t_{c(CI)}$	†	ns
$t_{d(CIH-COH/L)}$	Delay time, X2/CLKIN high to CLKOUT1 high/low	3	11	20	3	11	20	1	9	18	ns
$t_{f(CO)}$	Fall time, CLKOUT1		5			5			4		ns
$t_{r(CO)}$	Rise time, CLKOUT1		5			5			4		ns
$t_{w(COL)}$	Pulse duration, CLKOUT1 low	H – 3	H	H + 2	H – 3	H	H + 2	H – 3	H	H + 2	ns
$t_{w(COH)}$	Pulse duration, CLKOUT1 high	H – 3	H	H + 2	H – 3	H	H + 2	H – 3	H	H + 2	ns

† This device utilizes a fully static design and, therefore, can operate with $t_{c(CI)}$ approaching infinity. The device is characterized at frequencies approaching 0 Hz but is tested at $t_{c(CO)}$ = 300 ns to meet device test time requirements.

timing requirements over recommended ranges of supply voltage and operating ambient-air temperature ('320C5x only) (see Figure 13)

		'320C5x-40		'320C5x-57		'320C5x-80		'320C5x-100		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(CI)}$	Cycle time, X2/CLKIN	24.4	†	17.5	†	12.5	†	10	†	ns
$t_{f(CI)}$	Fall time, X2/CLKIN‡		5		5		4		4	ns
$t_{r(CI)}$	Rise time, X2/CLKIN‡		5		5		4		4	ns
$t_{w(CIL)}$	Pulse duration, X2/CLKIN low	11	†	8	†	5	†	5	†	ns
$t_{w(CIH)}$	Pulse duration, X2/CLKIN high	11	†	8	†	5	†	5	†	ns

timing requirements over recommended ranges of supply voltage and operating ambient-air temperature ('320LC5x only) (see Figure 13)

		'320LC5x-40		'320LC5x-50		'320LC5x-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(CI)}$	Cycle time, X2/CLKIN	25	†	20	†	12.5	†	ns
$t_{f(CI)}$	Fall time, X2/CLKIN‡		5		5		4	ns
$t_{r(CI)}$	Rise time, X2/CLKIN‡		5		5		4	ns
$t_{w(CIL)}$	Pulse duration, X2/CLKIN low	11	†	9	†	5	†	ns
$t_{w(CIH)}$	Pulse duration, X2/CLKIN high	11	†	9	†	5	†	ns

† This device utilizes a fully static design and, therefore, can operate with $t_{c(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz, but is tested at a minimum of $t_{c(CI)}$ = 150 ns to meet device test time requirements.
‡ Values derived from characterization data and not tested

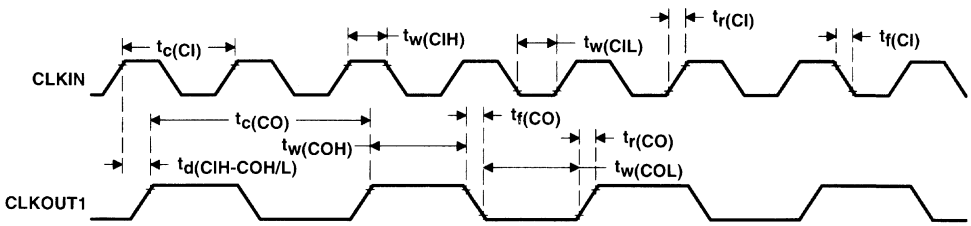


Figure 13. External Divide-by-Two Clock Timing

PLL clock generator option

An external frequency source can be used by injecting the frequency directly into CLKIN2† with X1 left unconnected and X2 connected to V_{DD}. This external frequency is multiplied by the factors shown in Table 9 and Table 10 to generate the internal machine cycle. The multiply-by-one option is available on the 'C50, 'LC50, 'C51, 'LC51, 'C53, 'LC53, 'C53S and 'LC53S. The multiply-by-two option is available on the 'C52 and 'LC52. Multiplication factors of 1, 2, 3, 4, 5, and 9 are available on the 'LC56, 'LC57, 'C57S and 'LC57S. Refer to Table 9 and Table 10 for appropriate configuration of the CLKMD1, CLKMD2 and CLKMD3 pins to generate the desired PLL multiplication factor. The external frequency injected must conform to the specifications listed in the timing requirements table.

switching characteristics over recommended operating conditions [H = 0.5 $t_{c(CO)}$] ('320C5x only) (see Figure 14)

PARAMETER		'320C5x-40			'320C5x-57			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(CO)}$	Cycle time, CLKOUT1	48.8		75	35		75	ns
$t_{f(CO)}$	Fall time, CLKOUT1		5			5		ns
$t_{r(CO)}$	Rise time, CLKOUT1		5			5		ns
$t_{w(COL)}$	Pulse duration, CLKOUT1 low	H – 3†	H	H + 2†	H – 3†	H	H + 2†	ns
$t_{w(COH)}$	Pulse duration, CLKOUT1 high	H – 3†	H	H + 2†	H – 3†	H	H + 2†	ns
$t_{d(C2H-COH)}$	Delay time, CLKIN2 high to CLKOUT1 high	2	9	16	2	9	16	ns
$t_{d(TP)}$	Delay time, transitory phase—PLL synchronized after CLKIN2 supplied†			$1000t_{c(C2)}$‡			$1000t_{c(C2)}$‡	ns

PARAMETER		'320C5x-80			'320C5x-100			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(CO)}$	Cycle time, CLKOUT1	25		55	20		45	ns
$t_{f(CO)}$	Fall time, CLKOUT1		4			4		ns
$t_{r(CO)}$	Rise time, CLKOUT1		4			4		ns
$t_{w(COL)}$	Pulse duration, CLKOUT1 low	H – 3†	H	H + 2†	H – 3†	H	H + 2†	ns
$t_{w(COH)}$	Pulse duration, CLKOUT1 high	H – 3†	H	H + 2†	H – 3†	H	H + 2†	ns
$t_{d(C2H-COH)}$	Delay time, CLKIN2 high to CLKOUT1 high	1	8	15	1	8	15	ns
$t_{d(TP)}$	Delay time, transitory phase—PLL synchronized after CLKIN2 supplied†			$1000t_{c(C2)}$‡			$1000t_{c(C2)}$‡	ns

† Values assured by design and not tested
‡ On the TMS320C57S devices, CLKIN2 functions as the PLL clock input.

switching characteristics over recommended operating conditions [H = 0.5 $t_{c(CO)}$] ('320LC5x only) (see Figure 14)

PARAMETER		'320LC5x-40			'320LC5x-50			'320LC5x-80			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(CO)}$	Cycle time, CLKOUT1	50		75†	40		75†	25		55†	ns
$t_{d(C2H-COH)}$	Delay time, CLKIN2 high to CLKOUT1 high	2	9	16	2	9	16	1	8	15	ns
$t_{f(CO)}$	Fall time, CLKOUT1		5			5			4		ns
$t_{r(CO)}$	Rise time, CLKOUT1		5			5			4		ns
$t_{w(COL)}$	Pulse duration, CLKOUT1 low	H – 3‡	H	H + 2‡	H – 3‡	H	H + 2‡	H – 3‡	H	H + 2‡	ns
$t_{w(COH)}$	Pulse duration, CLKOUT1 high	H – 3‡	H	H + 2‡	H – 3‡	H	H + 2‡	H – 3‡	H	H + 2‡	ns
$t_{d(TP)}$	Delay time, transitory phase—PLL synchronized after CLKIN2 supplied			$1000t_{c(C2)}$			$1000t_{c(C2)}$			$1000t_{c(C2)}$	ns

† Clocks can only be stopped while executing IDLE2 when using the PLL clock generator option.
‡ Values assured by design and not tested
§ On the 'LC56, 'LC57, and 'LC57S devices, CLKIN2 functions as the PLL clock input.

timing requirements over recommended ranges of supply voltage and operating ambient-air temperature ('320C5x only) (see Figure 14)

			'320C5x-40		'320C5x-57		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(C2)}$	Cycle time, CLKIN2	Multiply-by-one†	48.8	75‡	35	75‡	ns
		Multiply-by-two§	97.6	150‡	70	150‡	ns
$t_{f(C2)}$	Fall time, CLKIN2¶			5		5	ns
$t_{r(C2)}$	Rise time, CLKIN2¶			5		5	ns
$t_{w(C2L)}$	Pulse duration, CLKIN2 low		15	$t_{c(C2)}-15$	11	$t_{c(C2)}-11$	ns
$t_{w(C2H)}$	Pulse duration, CLKIN2 high		15	$t_{c(C2)}-15$	11	$t_{c(C2)}-11$	ns

			'320C5x-80		'320C5x-100		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(C2)}$	Cycle time, CLKIN2	Multiply-by-one†	25	75‡	20	75‡	ns
		Multiply-by-two§	50	150‡	40	110‡	ns
$t_{f(C2)}$	Fall time, CLKIN2¶			4		4	ns
$t_{r(C2)}$	Rise time, CLKIN2¶			4		4	ns
$t_{w(C2L)}$	Pulse duration, CLKIN2 low		8	$t_{c(C2)}-8$	7	$t_{c(C2)}-7$	ns
$t_{w(C2H)}$	Pulse duration, CLKIN2 high		8	$t_{c(C2)}-8$	7	$t_{c(C2)}-7$	ns

timing requirements over recommended ranges of supply voltage and operating ambient-air temperature ('320LC5x only) (see Figure 14)

			'320LC5x-40		'320LC5x-50		'320LC5x-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(C2)}$	Cycle time, CLKIN2	Multiply-by-one†	50	75‡	40	75‡	25	37.5‡	ns
		Multiply-by-two§	100	150‡	80	150‡	50	110‡	ns
$t_{f(C2)}$	Fall time, CLKIN2¶			5		5		4	ns
$t_{r(C2)}$	Rise time, CLKIN2¶			5		5		4	ns
$t_{w(C2L)}$	Pulse duration, CLKIN2 low		15	$t_{c(C2)}-15$	13	$t_{c(C2)}-13$	8	$t_{c(C2)}-8$	ns
$t_{w(C2H)}$	Pulse duration, CLKIN2 high		15	$t_{c(C2)}-15$	13	$t_{c(C2)}-13$	8	$t_{c(C2)}-8$	ns

† Not available on 'C52, 'LC52

‡ Clocks can be stopped only while executing IDLE2 when using the PLL clock generator option. The $t_{d(TP)}$ (the transitory phase) occurs when restarting clock from IDLE2 in this mode.

§ Available on 'C52, 'LC52, 'LC56, 'C57S, 'LC57, and 'LC57S

¶ Values derived from characterization data and not tested

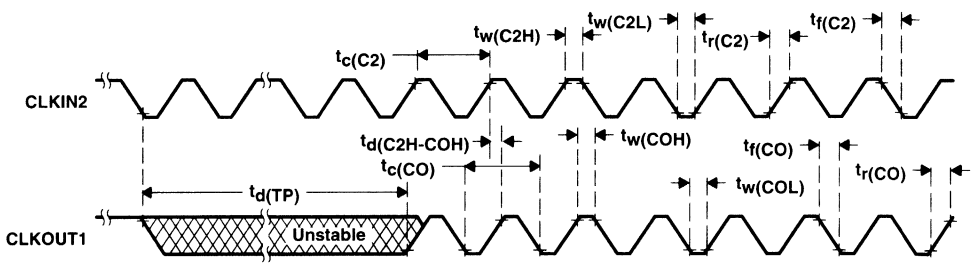


Figure 14. PLL Clock Generator Timing

MEMORY AND PARALLEL I/O INTERFACE READ

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] ('320C5x only) (see Figure 15)

PARAMETER		'320C5x-40		'320C5x-57		'320C5x-80		'320C5x-100		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{su(AV-RDL)}$	Setup time, address valid before $\overline{RD}$ low†	H – 10‡		H – 10‡		H – 7‡		H – 6‡		ns
$t_{h(RDH-AV)}$	Hold time, address valid after $\overline{RD}$ high†	0‡		0‡		0‡		0‡		ns
$t_{w(RDL)}$	Pulse duration, $\overline{RD}$ low§¶#	H – 2	H + 2	H – 2	H + 2	H – 2	H + 2	H – 2	H + 2	ns
$t_{w(RDH)}$	Pulse duration, $\overline{RD}$ high§¶#	H – 2		H – 2		H – 2		H – 2		ns
$t_{d(CO-ST)}$	Delay time, CLKOUT1 to $\overline{STRB}$ rising or falling edge§¶	– 1	3	– 2	2	– 2	2	– 2	2	ns
$t_{d(CO-RD)}$	Delay time, CLKOUT1 to $\overline{RD}$ rising or falling edge§¶	– 3	1	– 3	1	– 3	1	– 3	1	ns
$t_{d(RDH-WEL)}$	Delay time, $\overline{RD}$ high to $\overline{WE}$ low	2H – 5		2H – 5		2H – 4		2H – 4		ns

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] ('320LC5x only) (see Figure 15)

PARAMETER		'320LC5x-40 '320LC5x-50		'320LC5x-80		UNIT
		MIN	MAX	MIN	MAX	
$t_{su(AV-RDL)}$	Setup time, address valid before $\overline{RD}$ low†	H – 10‡		H – 7‡		ns
$t_{h(RDH-AV)}$	Hold time, address valid after $\overline{RD}$ high†	0‡		0‡		ns
$t_{w(RDL)}$	Pulse duration, $\overline{RD}$ low§¶#	H – 2	H + 2	H – 2	H + 2	ns
$t_{w(RDH)}$	Pulse duration, $\overline{RD}$ high§¶#	H – 2		H – 2		ns
$t_{d(RDH-WEL)}$	Delay time, $\overline{RD}$ high to $\overline{WE}$ low	2H – 5		2H – 4		ns
$t_{d(CO-RD)}$	Delay time, CLKOUT1 to $\overline{RD}$ rising or falling edge§¶	– 2	2	– 3	1	ns
$t_{d(CO-ST)}$	Delay time, CLKOUT1 to $\overline{STRB}$ rising or falling edge§¶	0	4	– 2	2	ns

† A0–A15, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, R/$\overline{W}$, and $\overline{BR}$ timings all are included in timings referenced as address.
‡ See Figure 16 for address bus timing variation with load capacitance.
§ These timings are for the cycles following the first cycle after reset, which is always seven wait states.
¶ Values are derived from characterization data and not tested.
# Timings are valid for zero wait-state cycles only.

timing requirements over recommended ranges of supply voltage and operating ambient-air temperature [H = 0.5$t_{c(CO)}$] ('320C5x only) (see Figure 15)

		'320C5x-40		'320C5x-57		'320C5x-80		'320C5x-100		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(RDAV)}$	Access time, read data from address valid		2H – 18†		2H – 15†		2H – 10†		2H – 10†	ns
$t_{a(RDL-RD)}$	Access time, read data after $\overline{RD}$ low		H – 10		H – 10		H – 7		H – 6	ns
$t_{su(RD-RDH)}$	Setup time, read data before $\overline{RD}$ high	10		10		7		6		ns
$t_{h(RDH-RD)}$	Hold time, read data after $\overline{RD}$ high	0		0		0		0		ns

timing requirements over recommended ranges of supply voltage and operating ambient-air temperature [H = 0.5$t_{c(CO)}$] ('320LC5x only) (see Figure 15)

		'320LC5x-40 '320LC5x-50		'320LC5x-80		UNIT
		MIN	MAX	MIN	MAX	
$t_{a(RDAV)}$	Access time, read data from address valid		2H – 17†		2H – 10†	ns
$t_{su(RD-RDH)}$	Setup time, read data before $\overline{RD}$ high	10		7		ns
$t_{h(RDH-RD)}$	Hold time, read data after $\overline{RD}$ high	0		0		ns
$t_{a(RDL-RD)}$	Access time, read data after $\overline{RD}$ low		H – 10		H – 7	ns

† See Figure 16 for address bus timing variation with load capacitance.

MEMORY AND PARALLEL I/O INTERFACE WRITE

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] ('320C5x only) (see Figure 15)

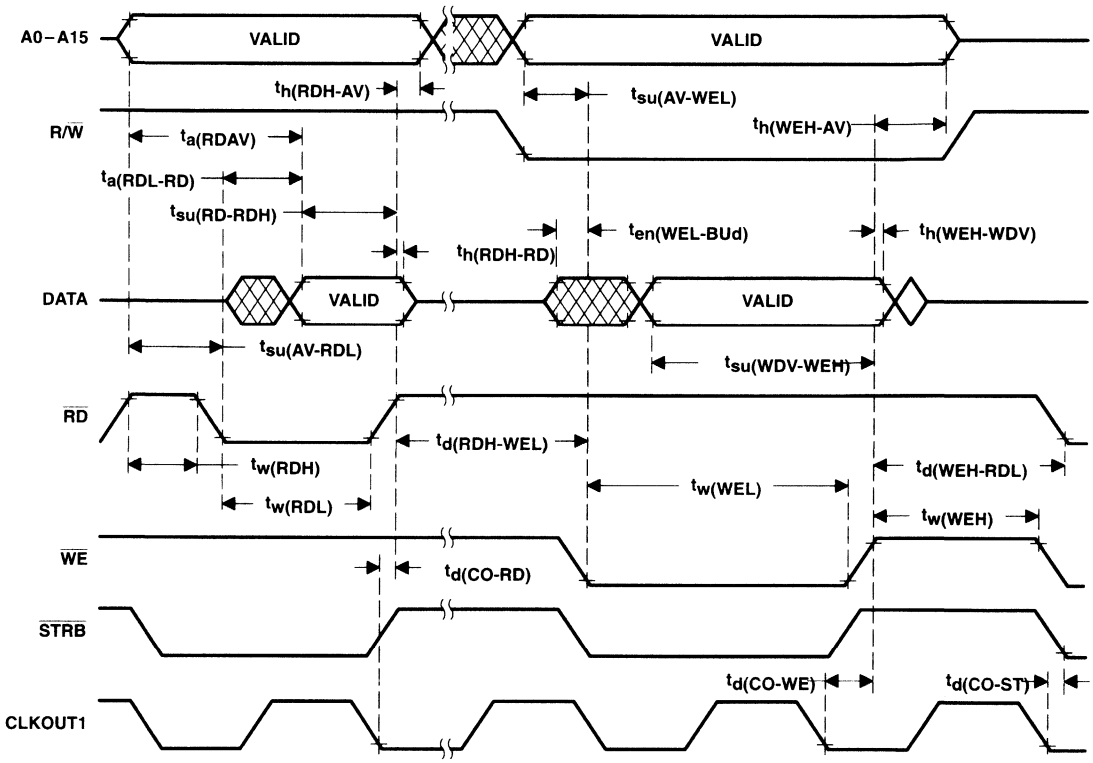
PARAMETER		'320C5x-40		'320C5x-57		'320C5x-80		'320C5x-100		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{su(AV-WEL)}$	Setup time, address valid before $\overline{WE}$ low†	H – 5‡		H – 5‡		H – 4‡		H – 3‡		ns
$t_{su(WDV-WEH)}$	Setup time, write data valid before $\overline{WE}$ high	2H – 20	2H§¶	2H – 20	2H§¶	2H – 14	2H§¶	2H – 14	2H§¶	ns
$t_{h(WEH-AV)}$	Hold time, address valid after $\overline{WE}$ high†	H – 10‡		H – 10‡		H – 7‡		H – 7‡		ns
$t_{h(WEH-WDV)}$	Hold time, write data valid after $\overline{WE}$ high	H – 5	H + 10§	H – 5	H + 10§	H – 4	H + 7§	H – 4	H + 7§	ns
$t_{w(WEL)}$	Pulse duration, $\overline{WE}$ low§¶	2H – 2	2H + 2§	2H – 2	2H + 2§	2H – 2	2H + 2	2H – 2	2H + 2	ns
$t_{w(WEH)}$	Pulse duration, $\overline{WE}$ high§	2H – 2		2H – 2		2H – 2		2H – 2		ns
$t_{d(CO-ST)}$	Delay time, CLKOUT1 to $\overline{STRB}$ rising or falling edge§	– 1	3	– 2	2	– 2	2	– 2	2	ns
$t_{d(CO-WE)}$	Delay time, CLKOUT1 to $\overline{WE}$ rising or falling edge§	0	4	– 1	3	– 1	3	– 1	3	ns
$t_{d(WEH-RDL)}$	Delay time, $\overline{WE}$ high to $\overline{RD}$ low	3H – 10		3H – 10		3H – 7		3H – 7		ns
$t_{en(WEL-BUd)}$	Enable time, $\overline{WE}$ low to data bus driven	– 5§		– 5§		– 4§		– 4§		ns

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] ('320LC5x only) (see Figure 15)

PARAMETER		'320LC5x-40 '320LC5x-50		'320LC5x-80		UNIT
		MIN	MAX	MIN	MAX	
$t_{su(AV-WEL)}$	Setup time, address valid before $\overline{WE}$ low†	H – 7‡		H – 4‡		ns
$t_{su(WDV-WEH)}$	Setup time, write data valid before $\overline{WE}$ high#	2H – 20	2H§¶	2H – 14	2H§¶	ns
$t_{h(WEH-AV)}$	Hold time, address valid after $\overline{WE}$ high†	H – 10‡		H – 7‡		ns
$t_{h(WEH-WDV)}$	Hold time, write data valid after $\overline{WE}$ high	H – 5	H + 10§	H – 4	H + 7§	ns
$t_{w(WEL)}$	Pulse duration, $\overline{WE}$ low¶§	2H – 4	2H + 2	2H – 4	2H + 2	ns
$t_{w(WEH)}$	Pulse duration, $\overline{WE}$ high¶	2H – 2		2H – 2		ns
$t_{d(WEH-RDL)}$	Delay time, $\overline{WE}$ high to $\overline{RD}$ low	3H – 10		3H – 7		ns
$t_{d(CO-ST)}$	Delay time, CLKOUT1 to $\overline{STRB}$ rising or falling edge¶	0	4	– 2	2	ns
$t_{d(CO-WE)}$	Delay time, CLKOUT1 to $\overline{WE}$ rising or falling edge¶	0	4	– 1	3	ns
$t_{en(WE-BUd)}$	Enable time, $\overline{WE}$ to data bus driven	– 5§		– 4§		ns

† A0–A15, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, R/$\overline{W}$, and $\overline{BR}$ timings are all included in timings referenced as address.
‡ See Figure 16 for address bus timing variation with load capacitance.
§ Values derived from characterization data and not tested
¶ This value holds true for zero wait states or one software wait state only.
# $\overline{STRB}$ and $\overline{WE}$ edges are 0–4 ns from CLKOUT1 edges on writes. Rising and falling edges of these signals track each other; tolerance of resulting pulsewidths is ±2 ns, not ±4 ns.

MEMORY AND PARALLEL I/O INTERFACE WRITE (CONTINUED)



NOTES: A. All timings are for 0 wait states. However, external writes always require two cycles to prevent external bus conflicts. The diagram illustrates a one-cycle read and a two-cycle write and is not drawn to scale. All external writes immediately preceded by an external read or immediately followed by an external read require three machine cycles.

B. Refer to Appendix B of *TMS320C5x User's Guide* (literature number SPRU056) for logical timings of external interface.

Figure 15. Memory and Parallel I/O Interface Read and Write Timing

MEMORY AND PARALLEL I/O INTERFACE WRITE (CONTINUED)

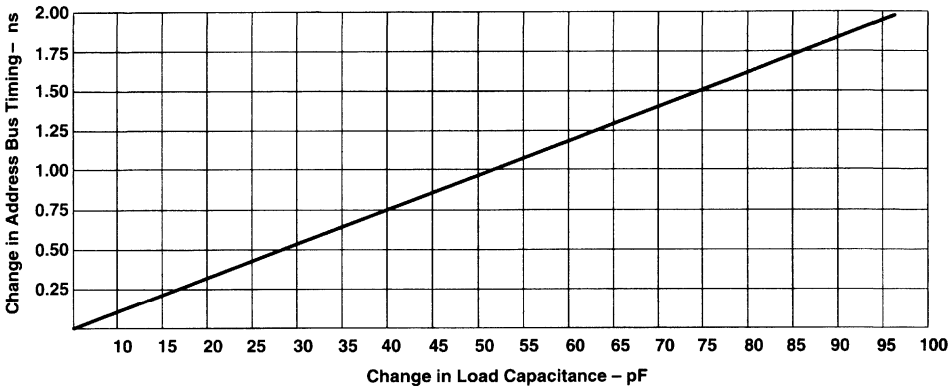


Figure 16. Address Bus Timing Variation With Load Capacitance

READY TIMING FOR EXTERNALLY-GENERATED WAIT STATES

timing requirements over recommended ranges of supply voltage and operating ambient-air temperature (see Note 5) (see Figure 17 and Figure 18)

		'320C5x-40 '320C5x-57 '320LC5x-40 '320LC5x-50		'320C5x-80 '320LC5x-80		'320C5x-100		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{su(RY-COH)}$	Setup time, READY before CLKOUT1 rising edge	10		7		6		ns
$t_{su(RY-RDL)}$	Setup time, READY before $\overline{RD}$ falling edge	10		7		6		ns
$t_{h(COH-RYH)}$	Hold time, READY after CLKOUT1 rising edge	0		0		0		ns
$t_{h(RDL-RY)}$	Hold time, READY after $\overline{RD}$ falling edge	0		0		0		ns
$t_{h(WEL-RY)}$	Hold time, READY after $\overline{WE}$ falling edge	H + 5		H + 4		H + 3		ns
$t_{v(WEL-RY)}$	Valid time, READY after $\overline{WE}$ falling edge		H – 15		H – 10		H – 8	ns

NOTE 5: The external READY input is sampled only after the internal software wait states are completed.

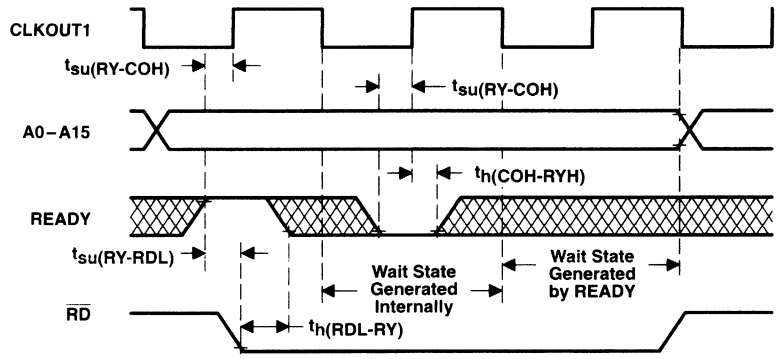


Figure 17. Ready Timing for Externally-Generated Wait States During an External Read Cycle

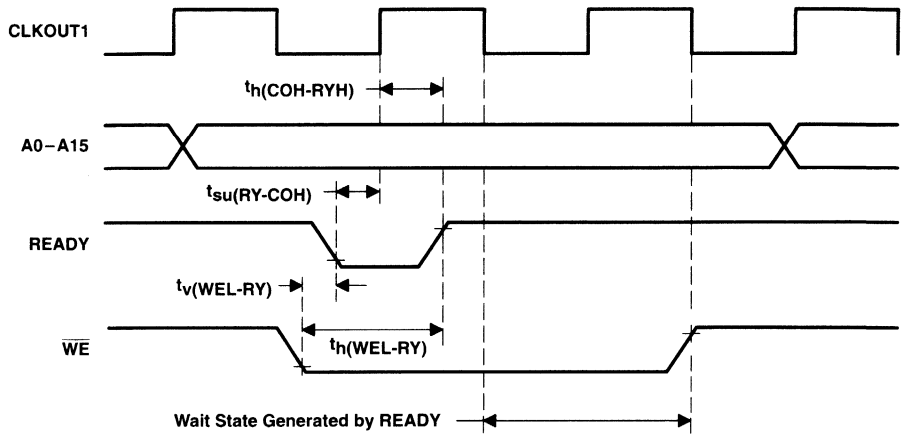


Figure 18. Ready Timing for Externally-Generated Wait States During an External Write Cycle

RESET, INTERRUPT, AND $\overline{BIO}$

timing requirements over recommended ranges of supply voltage and operating ambient-air temperature [H = $0.5t_{c(CO)}$] (see Figure 19)

		'320C5x-40 '320C5x-57 '320LC5x-40 '320LC5x-50		'320C5x-80 '320C5x-100 '320LC5x-80		UNIT
		MIN	MAX	MIN	MAX	
$t_{su(IN-COL)}$	Setup time, $\overline{INT1}$–$\overline{INT4}$, $\overline{NMI}$ before CLKOUT1 low†	15		10		ns
$t_{su(RS-COL)}$	Setup time, $\overline{RS}$ before CLKOUT1 low	15	2H – 5‡	10	2H – 5‡	ns
$t_{su(RS-CIL)}$	Setup time, $\overline{RS}$ before X2/CLKIN low	10		7		ns
$t_{su(BI-COL)}$	Setup time, $\overline{BIO}$ before CLKOUT1 low	15		10		ns
$t_{h(COL-IN)}$	Hold time, $\overline{INT1}$–$\overline{INT4}$, $\overline{NMI}$ after CLKOUT1 low†	0		0		ns
$t_{h(COL-BI)}$	Hold time, $\overline{BIO}$ after CLKOUT1 low	0		0		ns
$t_{w(INL)SYN}$	Pulse duration, $\overline{INT1}$–$\overline{INT4}$, $\overline{NMI}$ low, synchronous	4H + 15§		4H + 10§		ns
$t_{w(INH)SYN}$	Pulse duration, $\overline{INT1}$–$\overline{INT4}$, $\overline{NMI}$ high, synchronous	2H + 15§		2H + 10§		ns
$t_{w(INL)ASY}$	Pulse duration, $\overline{INT1}$–$\overline{INT4}$, $\overline{NMI}$ low, asynchronous‡	6H + 15§		6H + 10§		ns
$t_{w(INH)ASY}$	Pulse duration, $\overline{INT1}$–$\overline{INT4}$, $\overline{NMI}$ high, asynchronous‡	4H + 15§		4H + 10§		ns
$t_{w(RSL)}$	Pulse duration, $\overline{RS}$ low	12H		12H		ns
$t_{w(BIL)SYN}$	Pulse duration, $\overline{BIO}$ low, synchronous	15		10		ns
$t_{w(BIL)ASY}$	Pulse duration, $\overline{BIO}$ low, asynchronous‡	H + 15		H + 10		ns
$t_{d(RSH)}$	Delay time, $\overline{RS}$ high to reset vector fetch	34H		34H		ns

† These parameters must be met to use the synchronous timings. Both reset and the interrupts can operate asynchronously. The pulse durations require an extra half-cycle to ensure internal synchronization.
‡ Values derived from characterization data and not tested
§ If in IDLE2, add 4H to these timings.

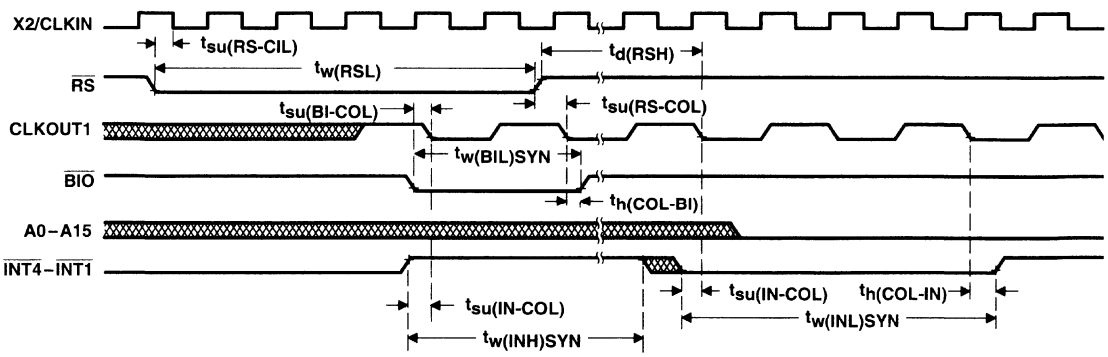


Figure 19. Reset, Interrupt, and $\overline{BIO}$ Timings

INSTRUCTION ACQUISITION (IAQ), INTERRUPT ACKNOWLEDGE (IACK), EXTERNAL FLAG (XF), AND TOUT (SEE NOTE 6)

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] (see Figure 20)

PARAMETER		'320C5x-40 '320C5x-57 '320LC5x-40 '320LC5x-50		'320C5x-80 '320C5x-100 '320LC5x-80		UNIT
		MIN	MAX	MIN	MAX	
$t_{su(AV-IQL)}$	Setup time, address valid before $\overline{IAQ}$ low†	H – 12‡		H – 9‡		ns
$t_{h(IQL-AV)}$	Hold time, address valid after $\overline{IAQ}$ low	H – 10‡		H – 7‡		ns
$t_{w(IQL)}$	Pulse duration, $\overline{IAQ}$ low	H – 10‡		H – 7‡		ns
$t_{d(CO-TU)}$	Delay time, CLKOUT1 falling edge to TOUT	– 6	6	– 6	6	ns
$t_{su(AV-IKL)}$	Setup time, address valid before $\overline{IACK}$ low§	H – 12‡		H – 9‡		ns
$t_{h(IKL-AV)}$	Hold time, address valid after $\overline{IACK}$ low	H – 10‡		H – 7‡		ns
$t_{w(IKL)}$	Pulse duration, $\overline{IACK}$ low	H – 10‡		H – 7‡		ns
$t_{w(TUH)}$	Pulse duration, TOUT high	2H – 12		2H – 9		ns
$t_{d(CO-XFV)}$	Delay time, XF valid after CLKOUT1	0	12	0	9	ns

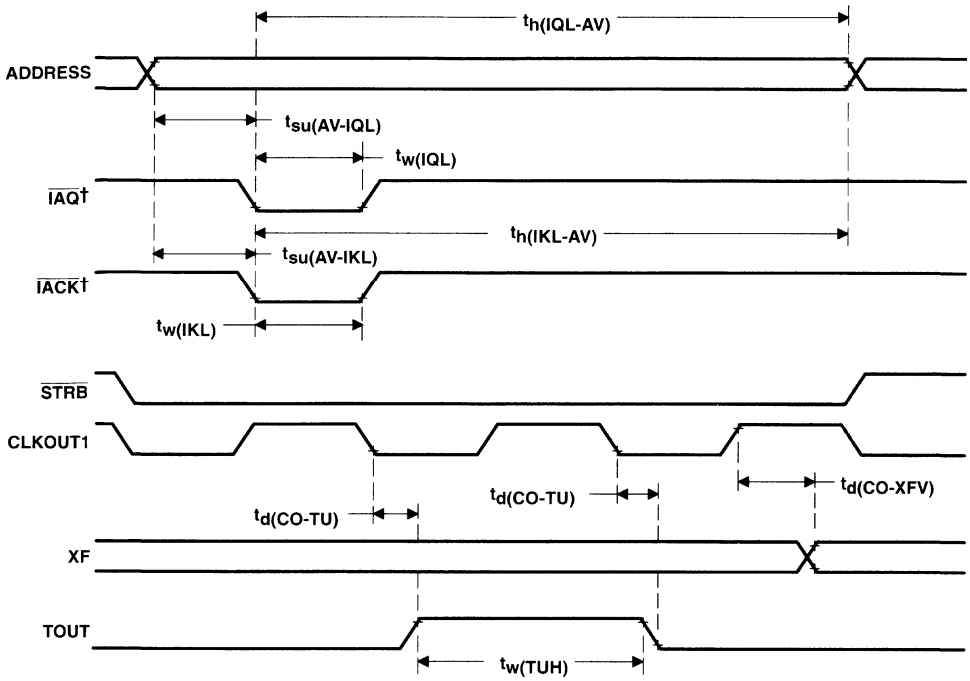
† $\overline{IAQ}$ goes low during an instruction acquisition. It goes low only on the first cycle of the read when wait states are used. The falling edge should be used to latch the valid address. The AVIS bit in the PMST register must be set to zero for the address to be valid when the instruction being addressed resides in on-chip memory.

‡ Valid only if the external address reflects the current instruction activity (that is, code is executing on chip with no external bus cycles and AVIS is on or code is executing off chip)

§ $\overline{IACK}$ goes low during the fetch of the first word of the interrupt vector. It goes low only on the first cycle of the read when wait states are used. Address pins A1 – A4 can be decoded at the falling edge to identify the interrupt being acknowledged. The AVIS bit in the PMST register must be set to zero for the address to be valid when the vectors reside in on-chip memory.

NOTE 6: $\overline{IAQ}$ pin is not present on 100-pin packages.
$\overline{IACK}$ pin is not present on 100-pin and 128-pin packages.

INSTRUCTION ACQUISITION (IAQ), INTERRUPT ACKNOWLEDGE (IACK), EXTERNAL FLAG (XF), AND TOUT (SEE NOTE 6) (CONTINUED)



† $\overline{IAQ}$ and $\overline{IACK}$ are not affected by wait states.

Figure 20. $\overline{IAQ}$, $\overline{IACK}$, and XF Timings Example With Two External Wait States

EXTERNAL DMA

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] (see Note 7) (see Figure 21)

PARAMETER		'320C5x-40 '320C5x-57 '320LC5x-40 '320LC5x-50		'320C5x-80 '320LC5x-80		'320C5x-100		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{d(HOL-HAL)}$	Delay time, $\overline{HOLD}$ low to $\overline{HOLDA}$ low	4H	†	4H	†	4H	†	ns
$t_{d(HOH-HAH)}$	Delay time, $\overline{HOLD}$ high before $\overline{HOLDA}$ high	2H		2H		2H		ns
$t_{h(AZ-HAL)}$	Address high-impedance before $\overline{HOLDA}$ low‡	H – 15§		H – 10§		H – 8§		ns
$t_{en(HAH-Ad)}$	Enable time, $\overline{HOLDA}$ high to address driven	H – 5§		H – 4§		H – 3§		ns
$t_{d(XBL-IQL)}$	Delay time, $\overline{XBR}$ low to $\overline{IAQ}$ low	4H§	6H§	4H§	6H§	4H§	6H§	ns
$t_{d(XBH-IQH)}$	Delay time, $\overline{XBR}$ high to $\overline{IAQ}$ high	2H§	4H§	2H§	4H§	2H§	4H§	ns
$t_{d(XSL-RDV)}$	Delay time, read data valid after $\overline{XSTRB}$ low		40		29		25	ns
$t_{h(XSH-RD)}$	Hold time, read data valid after $\overline{XSTRB}$ high	0		0		0		ns
$t_{en(IQL-RDd)}$	Enable time, $\overline{IAQ}$ low to read data driven¶	0§	2H§	0§	2H§	0§	2H§	ns
$t_{h(XRL-DZ)}$	Hold time, XR/$\overline{W}$ low to data high impedance	0§	15§	0§	10§	0§	8	ns
$t_{h(IQH-DZ)}$	Hold time, $\overline{IAQ}$ high to data high impedance		H§		H§		H§	ns
$t_{en(D-XRH)}$	Enable time, data from XR/$\overline{W}$ going high		4§		3§		2§	ns

† $\overline{HOLD}$ is not acknowledged until current external access request is complete.
‡ This parameter includes all memory control lines.
§ Values derived from characterization data and not tested
¶ This parameter refers to the delay between the time the condition ($\overline{IAQ}$ = 0 and XR/$\overline{W}$ = 1) is satisfied and the time that the 'C5x data lines become valid.
NOTE 7: X preceding a name refers to external drive of the signal.

timing requirements over recommended ranges of supply voltage and operating ambient-air temperature (see Note 7) (see Figure 21)

		'320C5x-40 '320C5x-57 '320LC5x-40 '320LC5x-50		'320C5x-80 '320LC5x-80		'320C5x-100		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{d(HAL-XBL)}$	Delay time, $\overline{HOLDA}$ low to $\overline{XBR}$ low#	0§		0§		0§		ns
$t_{d(IQL-XSL)}$	Delay time, $\overline{IAQ}$ low to $\overline{XSTRB}$ low#	0§		0§		0§		ns
$t_{su(AV-XSL)}$	Setup time, Xaddress valid before $\overline{XSTRB}$ low	15		12		10		ns
$t_{su(DV-XSL)}$	Setup time, Xdata valid before $\overline{XSTRB}$ low	15		12		10		ns
$t_{h(XSL-D)}$	Hold time, Xdata hold after $\overline{XSTRB}$ low	15		12		10		ns
$t_{h(XSL-WA)}$	Hold time, write Xaddress hold after $\overline{XSTRB}$ low	15		12		10		ns
$t_{w(XSL)}$	Pulse duration, $\overline{XSTRB}$ low	45		40		35		ns
$t_{w(XSH)}$	Pulse duration, $\overline{XSTRB}$ high	45		40		35		ns
$t_{su(RW-XSL)}$	Setup time, R/$\overline{W}$ valid before $\overline{XSTRB}$ low	20		20		18		ns
$t_{h(XSH-RA)}$	Hold time, read Xaddress after $\overline{XSTRB}$ high	0		0		0		ns

§ Values derived from characterization data and not tested
# $\overline{XBR}$, XR/$\overline{W}$, and $\overline{XSTRB}$ lines must be pulled up with a 10-kΩ resistor to be certain that they are in an inactive high state during the transition period between the 'C5x driving them and the external circuit driving them.
NOTE 7: X preceding a name refers to external drive of the signal.

EXTERNAL DMA (CONTINUED)

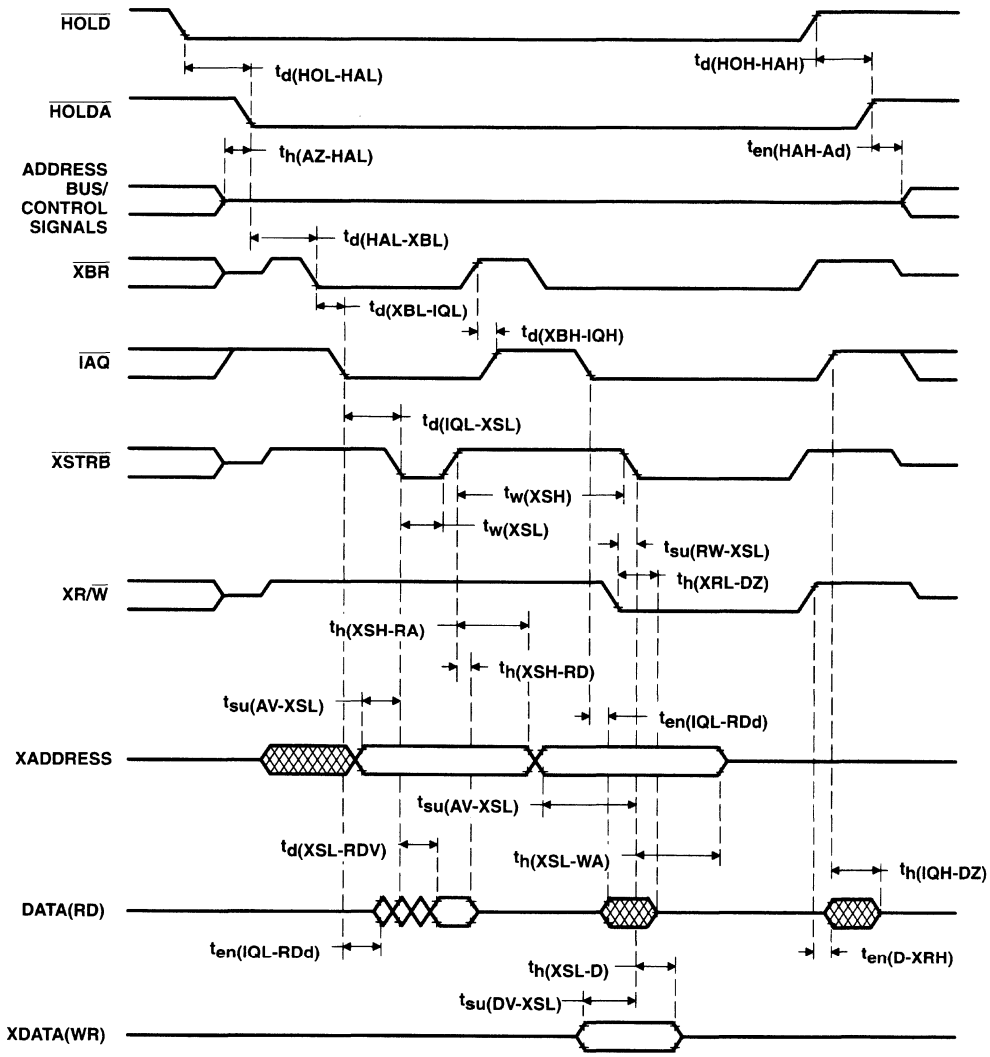


Figure 21. External DMA Timing

SERIAL-PORT RECEIVE TIMING

timing requirements over recommended ranges of supply voltage and operating ambient-air temperature [H = 0.5$t_{c(CO)}$] (see Figure 22)

		'320C5x-40 '320C5x-57 '320LC5x-40 '320LC5x-50		'320C5x-80 '320LC5x-80		'320C5x-100		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(SCK)}$	Cycle time, serial-port clock	5.2H†	‡	5.2H†	‡	5.2H†	‡	ns
$t_{f(SCK)}$	Fall time, serial-port clock		8§		6§		6§	ns
$t_{r(SCK)}$	Rise time, serial-port clock		8§		6§		6§	ns
$t_{w(SCK)}$	Pulse duration, serial-port clock low/high	2.1H†		2.1H†		2.1H†		ns
$t_{su(FS-CK)}$	Setup time, FSR before CLKR falling edge	10		7		6		ns
$t_{su(DR-CK)}$	Setup time, DR before CLKR falling edge	10		7		6		ns
$t_{h(CK-FS)}$	Hold time, FSR after CLKR falling edge	10		7		6		ns
$t_{h(CK-DR)}$	Hold time, DR valid after CLKR falling edge	10		7		6		ns

† Values ensured by design but not tested

‡ The serial-port design is fully static and, therefore, can operate with $t_{c(SCK)}$ approaching ∞. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.

§ Values derived from characterization data and not tested

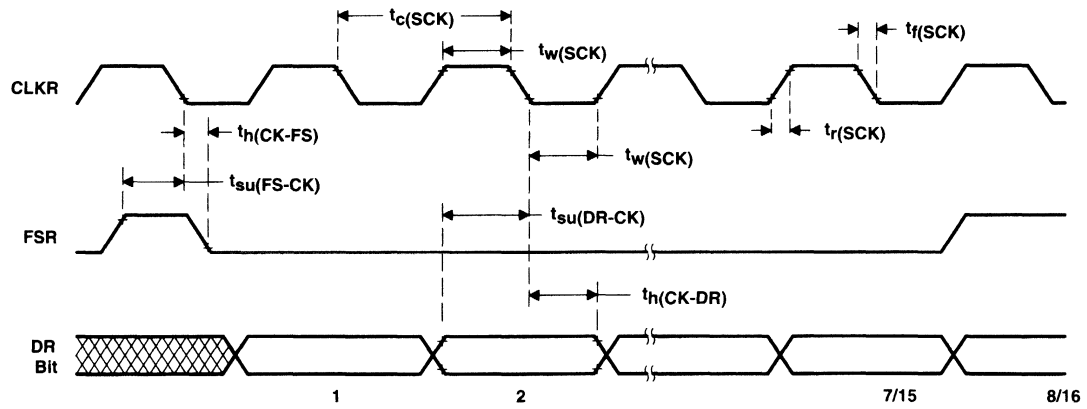


Figure 22. Serial-Port Receive Timing

SERIAL-PORT TRANSMIT TIMING, EXTERNAL CLOCKS, AND EXTERNAL FRAMES

switching characteristics over recommended operating conditions (see Note 8) (see Figure 23)

PARAMETER		MIN	MAX	UNIT
$t_{d(CXH-DXV)}$	Delay time, DX valid after CLKX high		25	ns
$t_{dis(CXH-DX)}$	Disable time, DX invalid after CLKX high		40†	ns
$t_{h(CXH-DXV)}$	Hold time, DX valid after CLKX high	– 5		ns

timing requirements over recommended ranges of supply voltage and operating ambient-air temperature [H = $0.5t_{c(CO)}$] (see Note 8) (see Figure 23)

		'320C5x-40 '320C5x-57 '320LC5x-40 '320LC5x-50		'320C5x-80 '320LC5x-80		'320C5x-100		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(SCK)}$	Cycle time, serial-port clock	5.2H‡	§	5.2H‡	§	5.2H‡	§	ns
$t_{f(SCK)}$	Fall time, serial-port clock		8†		6†		6†	ns
$t_{r(SCK)}$	Rise time, serial-port clock		8†		6†		6†	ns
$t_{w(SCK)}$	Pulse duration, serial-port clock low/high	2.1H‡		2.1H‡		2.1H‡		ns
$t_{d(CXH-FXH)}$	Delay time, FSX high after CLKX high		2H – 8		2H – 8		2H – 5	ns
$t_{h(CXL-FXL)}$	Hold time, FSX low after CLKX low	10		7		6		ns
$t_{h(CXH-FXL)}$	Hold time, FSX low after CLKX high		2H – 8¶		2H – 8¶		2H – 5¶	ns

† Values derived from characterization data and not tested

‡ Values ensured by design but not tested

§ The serial-port design is fully static and, therefore, can operate with $t_{c(SCK)}$ approaching ∞. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.

¶ If the FSX pulse does not meet this specification, the first bit of serial data is driven on the DX pin until the falling edge of FSX. After the falling edge of FSX, data is shifted out on the DX pin. The transmit buffer empty interrupt is generated when the $t_{h(CXL-FXL)}$ and $t_{h(CXH-FXL)}$ specification is met.

NOTE 8: Internal clock with external FSX and vice versa are also allowable. However, FSX timings to CLKX always are defined depending on the source of FSX, and CLKX timings always are dependent on the source of CLKX. Specifically, the relationship of FSX to CLKX is independent of the source of CLKX.

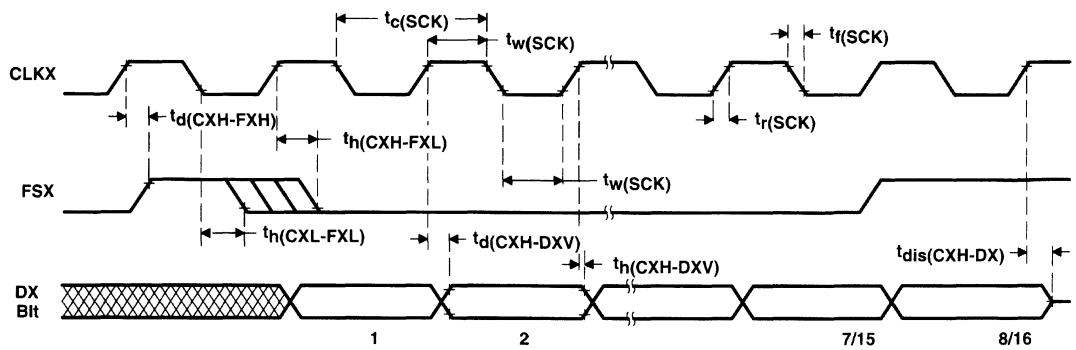


Figure 23. Serial-Port Transmit Timing of External Clocks and External Frames

SERIAL-PORT TRANSMIT TIMING, INTERNAL CLOCKS, AND INTERNAL FRAMES (SEE NOTE 8)

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] (see Figure 24)

PARAMETER		'320C5x-40 '320C5x-57 '320LC5x-40 '320LC5x-50			'320C5x-80 '320C5x-100 '320LC5x-80			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$t_{d(CX-FX)}$	Delay time, CLKX rising edge to FSX	– 5		25	– 4		18	ns
$t_{d(CX-DX)}$	Delay time, CLKX rising edge to DX			25			18	ns
$t_{dis(CX-DX)}$	Disable time, CLKX rising edge to DX			40†			29†	ns
$t_{c(SCK)}$	Cycle time, serial-port clock		8H			8H		ns
$t_{f(SCK)}$	Fall time, serial-port clock		5			4		ns
$t_{r(SCK)}$	Rise time, serial-port clock		5			4		ns
$t_{w(SCK)}$	Pulse duration, serial-port clock low/high	4H – 20			4H – 14			ns
$t_{h(CXH-DXV)}$	Hold time, DX valid after CLKX high	– 5			– 4			ns

† Values derived from characterization data and not tested

NOTE 8: Internal clock with external FSX and vice versa are also allowable. However, FSX timings to CLKX always are defined depending on the source of FSX, and CLKX timings always are dependent on the source of CLKX. Specifically, the relationship of FSX to CLKX is independent of the source of CLKX.

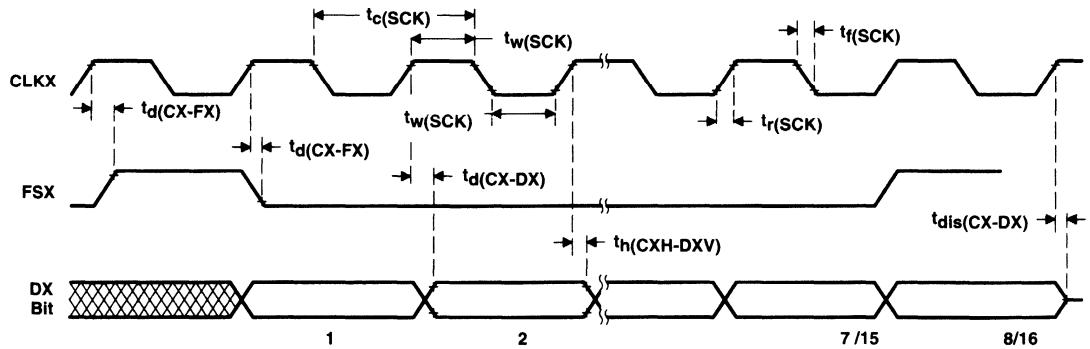


Figure 24. Serial-Port Transmit Timing of Internal Clocks and Internal Frames

SERIAL-PORT RECEIVE TIMING IN TDM MODE

timing requirements over recommended ranges of supply voltage and operating ambient-air temperature [H = 0.5$t_{c(CO)}$] (see Figure 25)

		'320C5x-40 '320C5x-57 '320LC5x-40 '320LC5x-50		'320C5x-80 '320LC5x-80		'320C5x-100		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(SCK)}$	Cycle time, serial-port clock	5.2H†	‡	5.2H†	‡	5.2H§	‡	ns
$t_{f(SCK)}$	Fall time, serial-port clock		8¶		8¶		8¶	ns
$t_{r(SCK)}$	Rise time, serial-port clock		8¶		8¶		8¶	ns
$t_{w(SCK)}$	Pulse duration, serial-port clock low/high	2.1H†		2.1H†		2.1H†		ns
$t_{su(TD-TCH)}$	Setup time, TDAT before TCLK rising edge	30		21		18		ns
$t_{h(TCH-TD)}$	Hold time, TDAT after TCLK rising edge	– 3		– 2		– 2		ns
$t_{su(TA-TCH)}$	Setup time, TADD before TCLK rising edge#	20		12		10		ns
$t_{h(TCH-TA)}$	Hold time, TADD after TCLK rising edge#	– 3		– 2		– 2		ns
$t_{su(TF-TCH)}$	Setup time, TFRM before TCLK rising edge§	10		10		10		ns
$t_{h(TCH-TF)}$	Hold time, TFRM after TCLK rising edge§	10		10		10		ns

† Values ensured by design and are not tested
‡ The serial-port design is fully static and, therefore, can operate with $t_{c(SCK)}$ approaching ∞. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.
§ TFRM timing and waveforms shown in Figure 25 are for external TFRM. TFRM also can be configured as internal. The TFRM internal case is illustrated in the transmit timing diagram in Figure 26.
¶ Values derived from characterization data and not tested
# These parameters apply only to the first bits in the serial bit string.

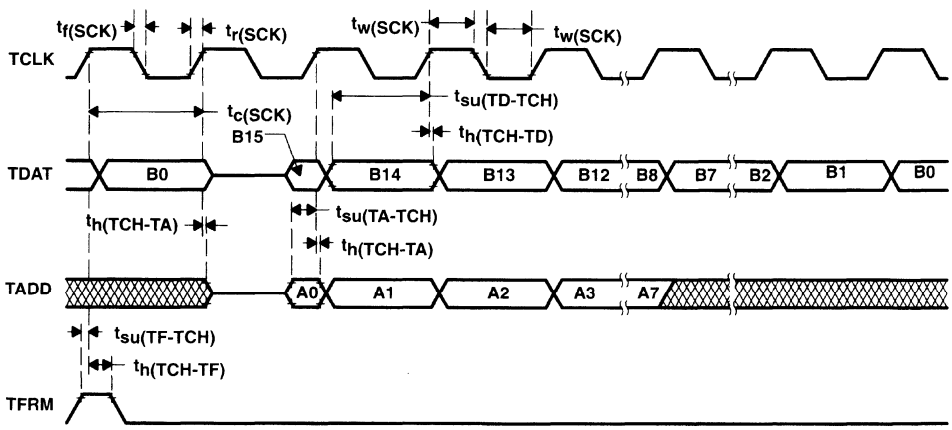


Figure 25. Serial-Port Receive Timing in TDM Mode

SERIAL-PORT TRANSMIT TIMING IN TDM MODE

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] (see Figure 26)

PARAMETER		'320C5x-40 '320C5x-57 '320LC5x-40 '320LC5x-50		'320C5x-80 '320LC5x-80		'320C5x-100		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{h(TCH-TDV)}$	Hold time, TDAT/TADD valid after TCLK rising edge	0		0		0		ns
$t_{d(TCH-TFV)}$	Delay time, TFRM valid after TCLK rising edge†	H	3H + 10	H	3H + 7		3H + 5	ns
$t_{d(TC-TDV)}$	Delay time, TCLK to valid TDAT/TADD		20		15		12	ns

† TFRM timing and waveforms shown in Figure 28 are for internal TFRM. TFRM can also be configured as external. The TFRM external case is illustrated in the receive timing diagram in Figure 27.

timing requirements over recommended ranges of supply voltage and operating ambient-air temperature [H = 0.5$t_{c(CO)}$] (see Figure 26)

		'320C5x-40 '320C5x-57 '320LC5x-40 '320LC5x-50			'320C5x-80 '320LC5x-80			'320C5x-100			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(SCK)}$	Cycle time, serial-port clock	5.2H‡	8H§	¶	5.2H‡	8H§	¶	5.2H‡	8H§	¶	ns
$t_{f(SCK)}$	Fall time, serial-port clock			8#			6#			5#	ns
$t_{r(SCK)}$	Rise time, serial-port clock			8#			6#			5#	ns
$t_{w(SCK)}$	Pulse duration, serial-port clock low/high	2.1H‡			2.1H‡			2.1H‡			ns

‡ Values ensured by design and are not tested
§ When SCK is generated internally
¶ The serial-port design is fully static and, therefore, can operate with $t_{c(SCK)}$ approaching ∞. It is characterized approaching an input frequency of 0 Hz but tested as a much higher frequency to minimize test time.
# Values derived from characterization data and not tested

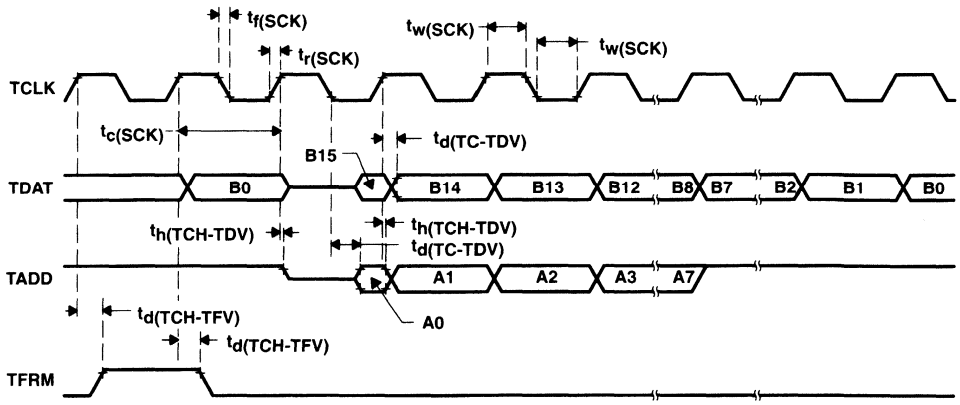


Figure 26. Serial-Port Transmit Timing in TDM Mode

BUFFERED SERIAL-PORT RECEIVE TIMING

timing requirements over recommended ranges of supply voltage and operating ambient-air temperature [H = $0.5t_{c(CO)}$] (see Figure 27)

		MIN	MAX	UNIT
$t_{c(SCK)}$	Cycle time, serial-port clock	25	†	ns
$t_{f(SCK)}$	Fall time, serial-port clock		6‡	ns
$t_{r(SCK)}$	Rise time, serial-port clock		6‡	ns
$t_{w(SCK)}$	Pulse duration, serial-port clock low/high	12		ns
$t_{su(FS-CK)}$	Setup time, FSR before CLKR falling edge	2		ns
$t_{su(DR-CK)}$	Setup time, DR before CLKR falling edge	0		ns
$t_{h(CK-FS)}$	Hold time, FSR after CLKR falling edge	12	$t_{c(SCK)}$§	ns
$t_{h(CK-DR)}$	Hold time, DR after CLKR falling edge	15		ns

† The serial-port design is fully static and, therefore, can operate with $t_{c(SCK)}$ approaching ∞. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.
‡ Values derived from characterization data and not tested
§ First bit is read when FSR is sampled low by CLKR clock.

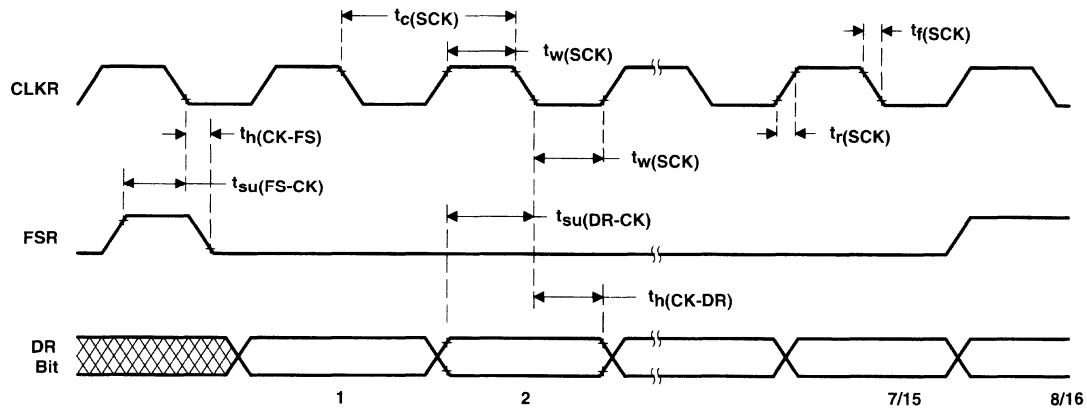


Figure 27. Buffered Serial-Port Receive Timing

BUFFERED SERIAL-PORT TRANSMIT TIMING OF EXTERNAL FRAMES (SEE NOTES 9 AND 10)

switching characteristics over recommended operating conditions (see Figure 28)

PARAMETER		MIN	MAX	UNIT
$t_{d(CXH-DXV)}$	Delay time, DX valid after CLKX rising edge	5	21	ns
$t_{dis(CXH-DX)}$	Disable time, DX invalid after CLKX rising edge	5	15	ns
$t_{dis(CXH-DX)PCM}$	Disable time in PCM mode, DX invalid after CLKX rising edge		15	ns
$t_{en(CXH-DX)PCM}$	Enable time in PCM mode, DX valid after CLKX rising edge	21		ns
$t_{h(CXH-DXV)}$	Hold time, DX valid after CLKX rising edge	5	20	ns

timing requirements over recommended operating conditions (see Figure 28)

		MIN	MAX	UNIT
$t_{c(SCK)}$	Cycle time, serial-port clock	25	†	ns
$t_{f(SCK)}$	Fall time, serial-port clock		4‡	ns
$t_{r(SCK)}$	Rise time, serial-port clock		4‡	ns
$t_{w(SCK)}$	Pulse duration, serial-port clock low/high	8.5		ns
$t_{su(FX-CXL)}$	Setup time, FSX before CLKX falling edge	5		ns
$t_{h(CXL-FX)}$	Hold time, FSX after CLKX falling edge	5	$t_{c(SCK)}-5$§	ns

† The serial-port design is fully static and, therefore, can operate with $t_{c(SCK)}$ approaching ∞. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.

‡ Values derived from characterization data and not tested

§ If the FSX pulse does not meet this specification, the first bit of the serial data is driven on the DX pin until FSX goes low (sampled on falling edge of CLKX). After falling edge of the FSX, data is shifted out on the DX pin.

NOTE 9: Internal clock with external FSX and vice versa are also allowable. However, FSX timings to CLKX always are defined depending on the source of FSX, and CLKX timings always are dependent upon the source of CLKX. Specifically, the relationship of FSX to CLKX is independent of the source of CLKX. External FSX timings are obtained from the "timing requirements over recommended operating conditions" table listed in the "Buffered Serial-Port Transmit Timing of External Frames" section and internal FSX timings are obtained from the "switching characteristics over recommended operating conditions" table listed under the "Buffered Serial-Port Transmit Timing of Internal Frame and Internal Clock" section. Internal CLKX timings are obtained from the "switching characteristics over recommended operating conditions" table listed under the "Buffered Serial-Port Transmit Timing of Internal Frame and Internal Clock" section and external CLKX timings are obtained from the "timing requirements over recommended operating conditions" table in the "Buffered Serial-Port Transmit Timing of External Frames" section.

NOTE 10: Timings for CLKX and FSX are given with polarity bits (CLKP and FSP) set to 0

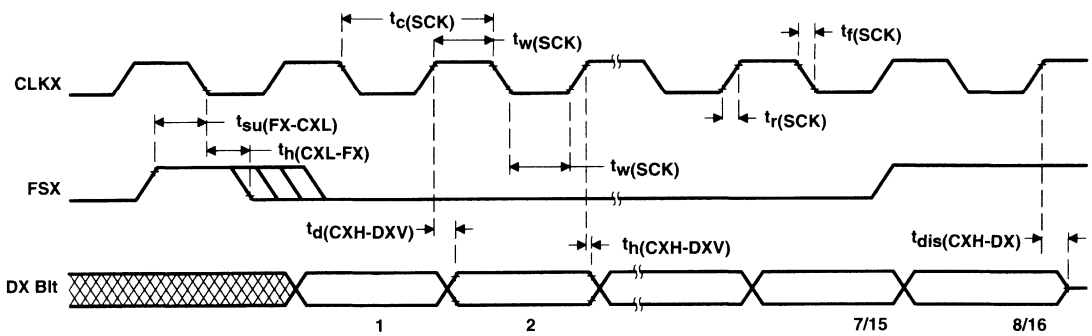


Figure 28. Buffered Serial-Port Transmit Timing of External Clocks and External Frames

BUFFERED SERIAL-PORT TRANSMIT TIMING OF INTERNAL FRAME AND INTERNAL CLOCK (SEE NOTES 9 AND 10)

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] (see Figure 29)

	PARAMETER	MIN	MAX	UNIT
$t_{d(CXH-FXH)}$	Delay time, FSX high after CLKX rising edge		10	ns
$t_{d(CXH-FXL)}$	Delay time, FSX low after CLKX rising edge		10	ns
$t_{d(CXH-DXV)}$	Delay time, DX valid after CLKX rising edge	5	10	ns
$t_{dis(CXH-DX)}$	Disable time, DX invalid after CLKX rising edge	4	8	ns
$t_{dis(CXH-DX)PCM}$	Disable time in PCM mode, DX invalid after CLKX rising edge		10	ns
$t_{en(CXH-DX)PCM}$	Enable time in PCM mode, DX valid after CLKX rising edge	16		ns
$t_{c(SCK)}$	Cycle time, serial-port clock	2H	62H	ns
$t_{f(SCK)}$	Fall time, serial-port clock		4†	ns
$t_{r(SCK)}$	Rise time, serial-port clock		4†	ns
$t_{w(SCK)}$	Pulse duration, serial-port clock low/high	H–4		ns
$t_{h(CXH-DXV)}$	Hold time, DX valid after CLKX rising edge	4	8	ns

† Values derived from characterization data and not tested

NOTES: 9. Internal clock with external FSX and vice versa are also allowable. However, FSX timings to CLKX always are defined depending on the source of FSX, and CLKX timings always are dependent upon the source of CLKX. Specifically, the relationship of FSX to CLKX is independent of the source of CLKX. External FSX timings are obtained from the "timing requirements over recommended operating conditions" table listed in the "Buffered Serial-Port Transmit Timing of External Frames" section and internal FSX timings are obtained from the "switching characteristics over recommended operating conditions" table listed under the "Buffered Serial-Port Transmit Timing of Internal Frame and Internal Clock" section. Internal CLKX timings are obtained from the "switching characteristics over recommended operating conditions" table listed under the "Buffered Serial-Port Transmit Timing of Internal Frame and Internal Clock" section and external CLKX timings are obtained from the "timing requirements over recommended operating conditions" table in the "Buffered Serial-Port Transmit Timing of External Frames" section.

10. Timings for CLKX and FSX are given with polarity bits (CLKP and FSP) set to 0.

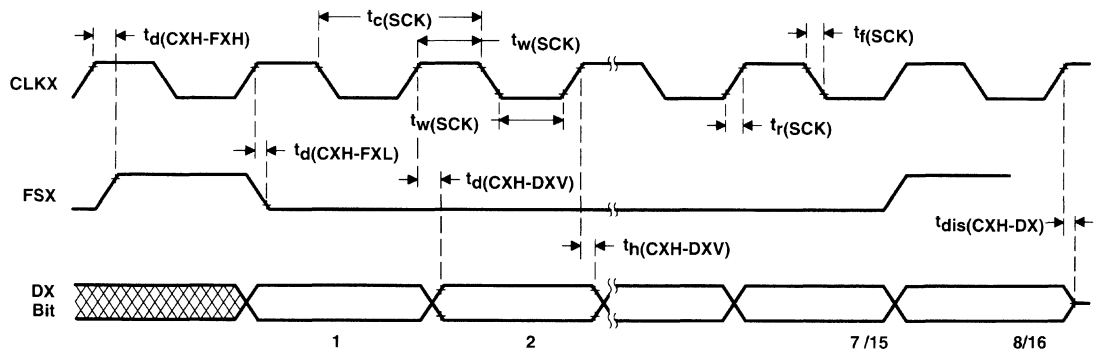


Figure 29. Buffered Serial-Port Transmit Timing of Internal Clocks and Internal Frames

HOST PORT INTERFACE (TMS320C57S, TMS320LC57 ONLY)

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] (See Notes 11 and 12) (see Figure 30 through Figure 33)

	PARAMETER	MIN	MAX	UNIT
$t_{d(DSL-HDV)}$	Delay time, $\overline{DS}$ low to HD valid	5		ns
$t_{d(HEL-HDV1)}$	Delay time, $\overline{HDS}$ falling to HD valid for first byte of a subsequent read: Case 1: Shared-access mode if $t_{w(\overline{HDS})h}$ < 7H † ‡ Case 2: Shared-access mode if $t_{w(\overline{HDS})h}$ > 7H Case 3: Host-only mode if $t_{w(\overline{HDS})h}$ < 7H Case 4: Host-only mode if $t_{w(\overline{HDS})h}$ > 7H		7H+20–$t_{w(DSH)}$ 20 40–$t_{w(DSH)}$ 20	ns
$t_{d(DSL-HDV2)}$	Delay time, $\overline{DS}$ low to HD valid, second byte		20	ns
$t_{d(DSH-HYH)}$	Delay time, $\overline{DS}$ high to HRDY high			ns
$t_{su(HDV-HYH)}$	Setup time, HD valid before HRDY rising edge	3H–10		ns
$t_{h(DSH-HDV)}$	Hold time, HD valid after $\overline{DS}$ rising edge	0	12§	ns
$t_{d(COH-HYH)}$	Delay time, CLKOUT rising edge to HRDY high		10	ns
$t_{d(DSH-HYL)}$	Delay time, $\overline{HDS}$ or $\overline{HCS}$ high to HRDY low		12	ns
$t_{d(COH-HTX)}$	Delay time, CLKOUT rising edge to $\overline{HINT}$ change		10	ns

† Host-only mode timings apply for read accesses to HPIC or HPIA, write accesses to BOB, and resetting DSPINT or HINT to 0 in shared-access mode. HRDY does not go low for these accesses.
‡ Shared-access mode timings are met automatically if HRDY is used.
§ HD release
NOTES: 11. SAM = shared-access mode, HOM = host-only mode
HAD stands for HCNTRL0, HCNTRL1, and HR/$\overline{W}$.
$\overline{HDS}$ refers to either $\overline{HDS1}$ or $\overline{HDS2}$.
$\overline{DS}$ refers to the logical OR of $\overline{HCS}$ and $\overline{HDS}$.
12. On host-read accesses to the HPI, the setup time of HD before $\overline{DS}$ rising edge depends on the host waveforms and cannot be specified here.

timing requirements over recommended operating conditions [H = 0.5$t_{c(CO)}$] (See Note 11) (see Figure 30 through Figure 33)

		MIN	MAX	UNIT
$t_{su(HBV-DSL)}$	Setup time, HAD/HBIL valid before $\overline{HAS}$ or $\overline{DS}$ falling edge#	10		ns
$t_{h(DSL-HBV)}$	Hold time, HAD/HBIL valid after $\overline{HAS}$ or $\overline{DS}$ falling edge#	10		ns
$t_{su(HSL-DSL)}$	Setup time, $\overline{HAS}$ low before $\overline{DS}$ falling edge	10		ns
$t_{w(DSL)}$	Pulse duration, $\overline{DS}$ low	25		ns
$t_{w(DSH)}$	Pulse duration, $\overline{DS}$ high	10		ns
$t_{c(DSH-DSH)}$	Cycle time, $\overline{DS}$ rising edge to next $\overline{DS}$ rising edge: Case 1: When using HRDY (see Figure 32) Case 2a: SAM accesses and HOM active writes to DSPINT or HINT without using HRDY (see Figure 30 and Figure 31) Case 2b: When not using HRDY for other HOM accesses	 50 10H¶ 50		ns
$t_{su(HDV-DSH)}$	Setup time, HD valid before $\overline{DS}$ rising edge	10		ns
$t_{h(DSH-HDV)}$	Hold time, HD valid after $\overline{DS}$ rising edge	0		ns

¶ A host not using HRDY must meet the 10 H requirement all the time unless a software handshake is used to change the access rate according to the HPI mode.
# When $\overline{HAS}$ is tied to V_{DD}, timing is referenced to $\overline{DS}$.
NOTE 11: SAM = shared-access mode, HOM = host-only mode
HAD stands for HCNTRL0, HCNTRL1, and HR/$\overline{W}$.
$\overline{HDS}$ refers to either $\overline{HDS1}$ or $\overline{HDS2}$.
$\overline{DS}$ refers to the logical OR of $\overline{HCS}$ and $\overline{HDS}$.

HOST PORT INTERFACE (TMS320C57S, TMS320LC57 ONLY) (CONTINUED)

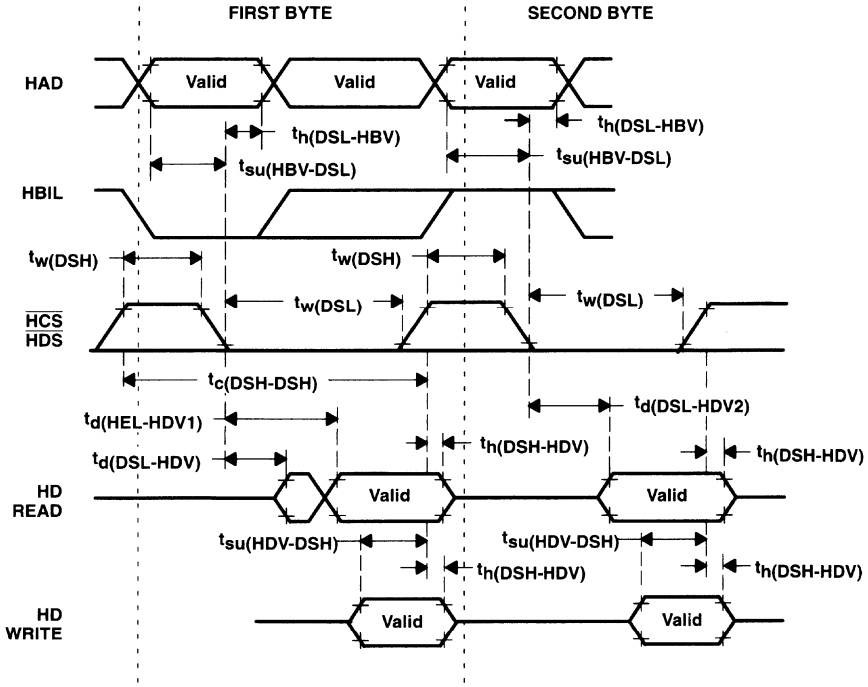


Figure 30. Read/Write Access Timings Without HRDY or $\overline{HAS}$

HOST PORT INTERFACE (TMS320C57S, TMS320LC57 ONLY) (CONTINUED)

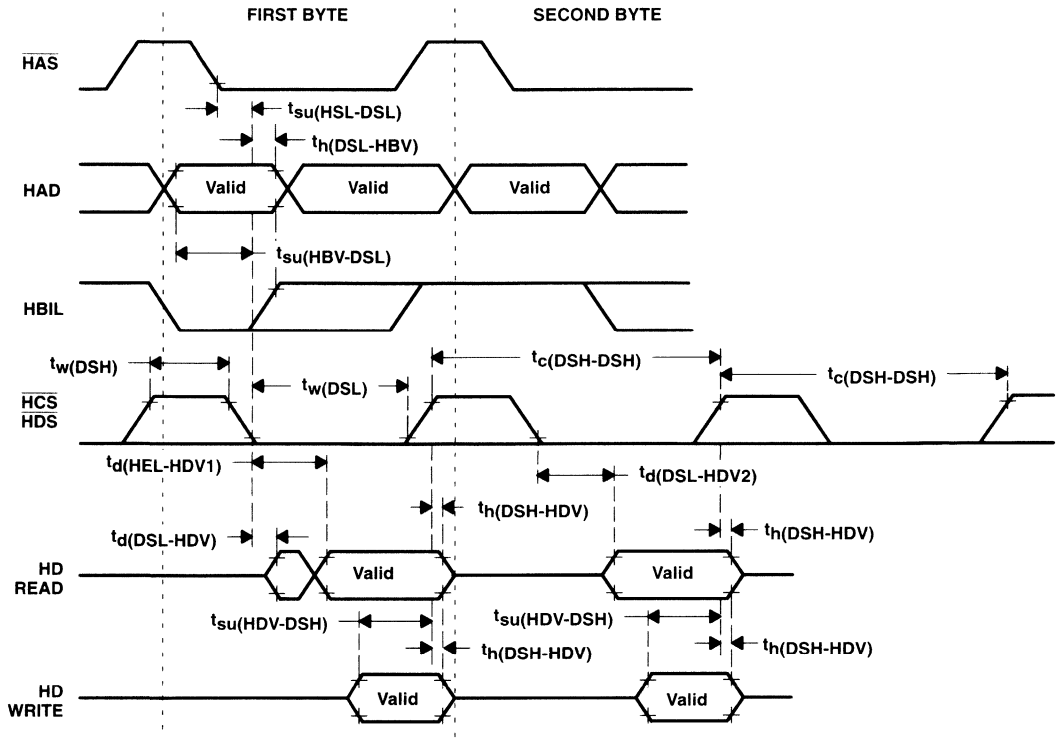
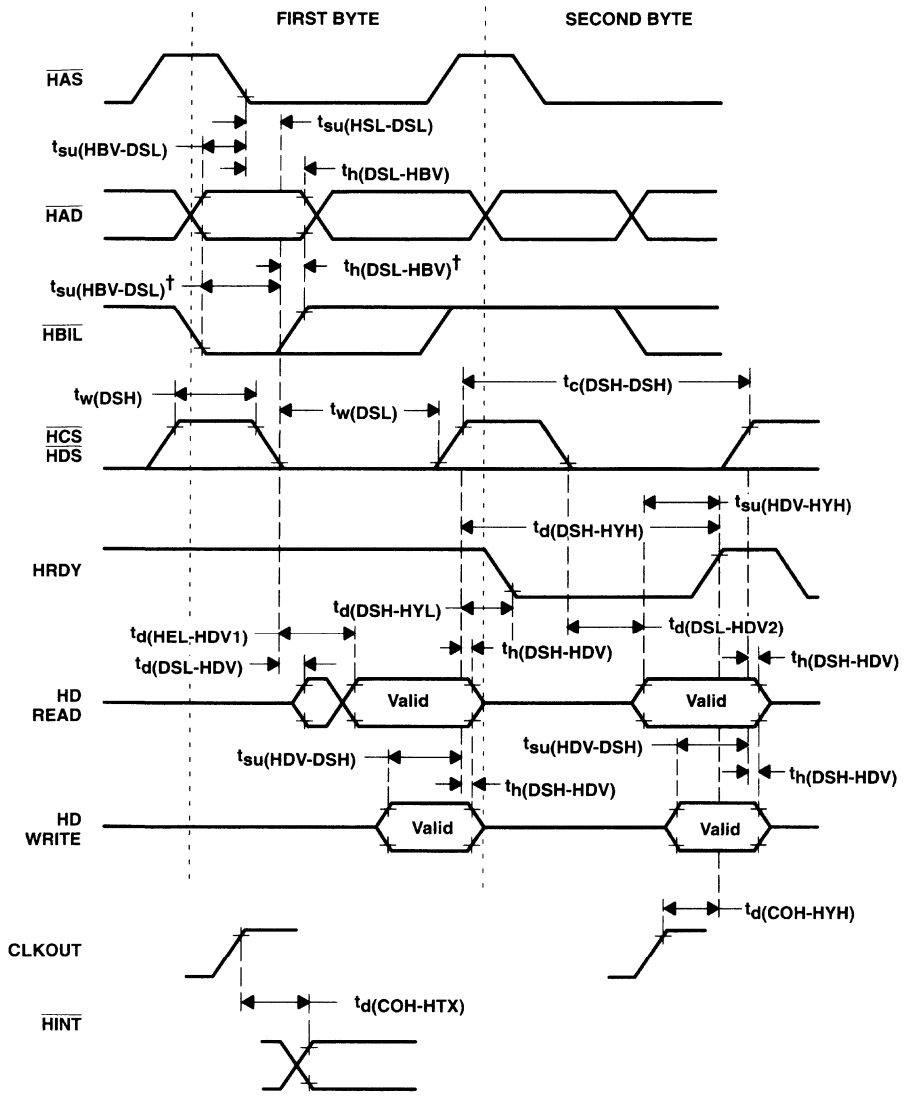


Figure 31. Read/Write Access Timings Using $\overline{\text{HAS}}$ Without HRDY

HOST PORT INTERFACE (TMS320C57S, TMS320LC57 ONLY) (CONTINUED)



† When $\overline{HAS}$ is tied to V_{DD}

Figure 32. Read/Write Access Timing With HRDY

HOST PORT INTERFACE (TMS320C57S, TMS320LC57 ONLY) (CONTINUED)

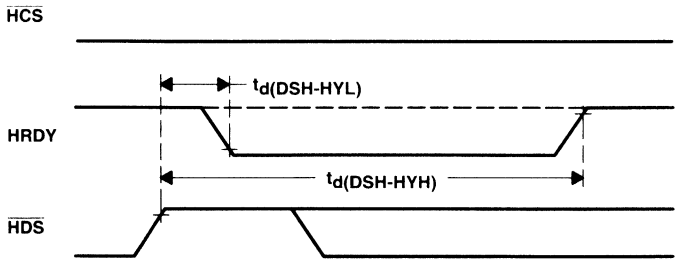


Figure 33. HRDY Signal When $\overline{HCS}$ Is Always Low

- Advanced Multibus Architecture With Three Separate 16-Bit Data Memory Buses and One Program Memory Bus
- 40-Bit Arithmetic Logic Unit (ALU) Including a 40-Bit Barrel Shifter and Two Independent 40-Bit Accumulators
- 17- × 17-Bit Parallel Multiplier Coupled to a 40-Bit Dedicated Adder for Non-Pipelined Single-Cycle Multiply/Accumulate (MAC) Operation
- Compare Select Store Unit (CSSU) for the Add/Compare Selection of the Viterbi Operator
- Exponent Encoder to Compute an Exponent Value of a 40-Bit Accumulator Value in a Single Cycle
- Two Address Generators With Eight Auxiliary Registers and Two Auxiliary Register Arithmetic Units
- Data Bus With a Bus Holder Feature
- 192K × 16-Bit Maximum Addressable Memory Space (64K Words Program, 64K Words Data, and 64K Words I/O)
- On-Chip ROM with Some Configurable to Program/Data Memory
- Dual-Access On-Chip RAM
- Single-Instruction Repeat and Block Repeat Operations for Program Code
- Block Memory Move Instructions for Better Program and Data Management
- Instructions With a 32-Bit Long Word Operand
- Instructions With Two- or Three-Operand Reads
- Arithmetic Instructions With Parallel Store and Parallel Load
- Conditional Store Instructions
- Fast Return From Interrupt
- On-Chip Peripherals
  - Software-Programmable Wait-State Generator and Programmable Bank Switching
  - On-Chip Phase-Locked Loop (PLL) Clock Generator With Internal Oscillator or External Clock Source
  - Full-Duplexed Serial Port to Support 8- or 16-Bit Transfers ('C541, 'LC541, 'VC541, 'LC544, 'VC544, 'LC545, 'VC545, 'LC546, and 'VC546 Only)
  - Time-Division Multiplexed (TDM) Serial Port ('C542, 'LC542, 'VC542, 'LC543 and 'VC543 Only)
  - Buffered Serial Port (BSP) ('C542, 'LC542 'VC542, 'LC543, 'VC543, 'LC545, 'VC545, 'LC546, and 'VC546 Only)
  - 8-Bit Parallel Host Port Interface (HPI) ('C542, 'LC542, 'VC542, 'LC545, and 'VC545 Only)
  - One 16-Bit Timer
  - External-Input/Output (XIO) Off Control to Disable the External Data Bus, Address Bus and Control Signals
- Power Consumption Control With IDLE1, IDLE2, and IDLE3 Instructions With Power-Down Modes
- CLKOUT Off Control to Disable the CLKOUT
- On-Chip Scan-Based Emulation Logic, IEEE Std 1149.1† (JTAG) Boundary Scan Logic
- 25-ns Single-Cycle Fixed-Point Instruction Execution Time [40 million instructions per second (MIPS)] for 5-V Power Supply ('C541 and 'C542 Only)
- 20-ns and 25-ns Single-Cycle Fixed-Point Instruction Execution Time (50 MIPS and 40 MIPS) for 3-V Power Supply ('LC54x and 'VC54x)

ADVANCE INFORMATION

† IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.

ADVANCE INFORMATION

description

The TMS320C54x, TMS320LC54x and TMS320VC54x fixed-point, digital signal processor (DSP) families are fabricated with a combination of an advanced modified Harvard architecture which has one program memory bus and three data memory buses. These processors also provide a central arithmetic logic unit (CALU) which has a high-degree of parallelism and application-specific hardware logic, on-chip memory, additional on-chip peripherals. These DSP families also provide a highly specialized instruction set which is the basis of the operational flexibility and speed of these DSPs.

Separate program and data spaces allow simultaneous access to program instructions and data, providing the high degree of parallelism. Two reads and one write operation can be performed in a single cycle. Instructions with parallel store and application-specific instructions can fully utilize this architecture. In addition, data can be transferred between data and program spaces. Such parallelism supports a powerful set of arithmetic, logic, and bit-manipulation operations that all can be performed in a single machine cycle. In addition, the 'C54x, 'LC54x and 'VC54x versions include the control mechanisms to manage interrupts, repeated operations, and function calling.

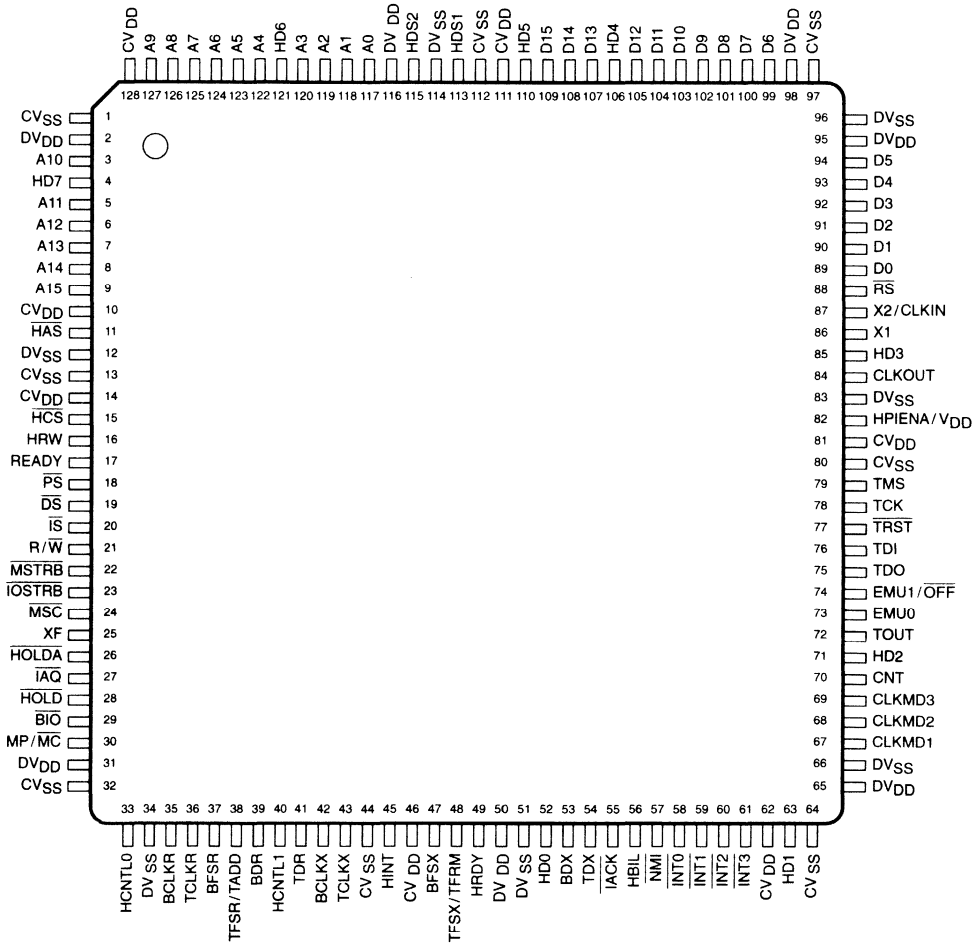
Table 1 provides an overview of the 'C54x/'LC54x/'VC54x generation of DSPs. The table shows the capacity of on-chip RAM and ROM memories, the peripherals, the execution time of one machine cycle, and the type of package with its total pin count. Use the information in Table 1 to select the best processor for each application.

Table 1. Characteristics of the 'C54x/'LC54x/'VC54x Processors

DSP TYPE	NOMINAL VOLTAGE (V)	ON-CHIP MEMORY		PERIPHERALS			CYCLE TIME (ns)	PACKAGE TYPE
		RAM†	ROM	SERIAL PORT	TIMER	HPI		
TMS320C541	5.0	5K	28K‡	2	1	No	25	100 pin (TQFP)
TMS320LC541	3.3	5K	28K‡	2	1	No	20/25	100 pin (TQFP)
TMS320VC541	3.0	5K	28K‡	2	1	No	20/25	100 pin (TQFP)
TMS320C542	5.0	10K	2K	2§	1	Yes	25	144 pin (TQFP)
TMS320LC542	3.3	10K	2K	2§	1	Yes	20/25	128 pin (TQFP)/144 pin (TQFP)
TMS320VC542	3.0	10K	2K	2§	1	Yes	20/25	128 pin (TQFP)/144 pin (TQFP)
TMS320LC543	3.3	10K	2K	2§	1	No	20/25	100 pin (TQFP)
TMS320VC543	3.0	10K	2K	2§	1	No	20/25	100 pin (TQFP)
TMS320LC544	3.3	4K	24K‡	2	1	No	20/25	80 pin (TQFP)
TMS320VC544	3.0	4K	24K‡	2	1	No	20/25	80 pin (TQFP)
TMS320LC545	3.3	6K	48K¶	2#	1	Yes	20/25	128 pin (TQFP)
TMS320VC545	3.0	6K	48K¶	2#	1	Yes	20/25	128 pin (TQFP)
TMS320LC546	3.3	6K	48K¶	2#	1	No	20/25	100 pin (TQFP)
TMS320VC546	3.0	6K	48K¶	2#	1	No	20/25	100 pin (TQFP)

Legend:
TQFP = Thin Quad Flat Pack
† The dual-access RAM can be configured as data memory or program and data memory.
‡ For 'C541/'LC541/'VC541/'LC544/'VC544, 8K words of ROM can be configured as program memory or program/data memory.
§ TDM and buffered serial ports
¶ For 'LC545/'VC545/'LC546/'VC546, 16K words of ROM can be configured as program memory or program/data memory.
# Standard and buffered serial ports

TMS320LC542, TMS320VC542
PBK PACKAGE†
(TOP VIEW)



† DV_{SS} and DV_{DD} are power supplies for I/O pins while CV_{SS} and CV_{DD} are power supplies for core CPU.

The pin function table on the following pages lists each pin number, signal, function, and operating mode(s) for the TMS320LC542PBK/'VC542PBK (128-pin) packages.

ADVANCE INFORMATION

Pin Functions for the TMS320LC542PBK/'VC542PBK (128-Pin TQFP Package)

PIN NAME	PIN NO	FUNCTION†	DESCRIPTION
CV_{SS}	1	Supply	Ground
DV_{DD}	2	Supply	$+V_{DD}$
A10	3	O/Z	Parallel port address bus
HD7	4	I/O/Z	Parallel bi-directional data bus (HPI)
A11–A15	5–9	O/Z	Parallel port address bus
CV_{DD}	10	Supply	$+V_{DD}$
$\overline{HAS}$	11	I	Address data strobe (HPI)
DV_{SS}	12	Supply	Ground
CV_{SS}	13	Supply	Ground
CV_{DD}	14	Supply	$+V_{DD}$
$\overline{HCS}$	15	I	Chip select input (HPI)
HRW	16	I	Read/write (HPI)
READY	17	I	External access ready to complete
$\overline{PS}$	18	O/Z	Program space select
$\overline{DS}$	19	O/Z	Data space select
$\overline{IS}$	20	O/Z	I/O select
$R/\overline{W}$	21	O/Z	Read/write
$\overline{MSTRB}$	22	O/Z	External memory access strobe
$\overline{IOSTRB}$	23	O/Z	External I/O access strobe
$\overline{MSC}$	24	O/Z	Microstate complete
XF	25	O/Z	External flag
$\overline{HOLDA}$	26	O/Z	Hold acknowledge
$\overline{IAQ}$	27	O/Z	Instruction acquisition
$\overline{HOLD}$	28	I	Request access of local memory
$\overline{BIO}$	29	I	Bit I/O pin
$MP/\overline{MC}$	30	I	Microprocessor/microcomputer
DV_{DD}	31	Supply	$+V_{DD}$
CV_{SS}	32	Supply	Ground
HCNTL0	33	I	Control inputs (HPI)
DV_{SS}	34	Supply	Ground
BCLKR	35	I	Receive clock input (BSP)
TCLKR	36	I	Receive clock input (TDM)
BFSR	37	I	Frame synchronization pulse for receive (BSP)
TFSR/TADD	38	I/O	Receive frame synchronization (TDM)
BDR	39	I	Serial data receive input (BSP)
HCNTL1	40	I	Control inputs (HPI)
TDR	41	I	Serial data receive input (TDM)
BCLKX	42	I/O/Z	Serial port 0 transmit clock (BSP)
TCLKX	43	I/O/Z	Serial port 0 transmit clock (TDM)

† I = Input, O = Output, Z = High impedance

Pin Functions for the TMS320LC542PBK/'VC542PBK (128-Pin TQFP Package) (Continued)

PIN NAME	PIN NO	FUNCTION†	DESCRIPTION
CV_{SS}	44	Supply	Ground
HINT	45	O/Z	Interrupt output (HPI)
CV_{DD}	46	Supply	$+V_{DD}$
BFSX	47	I/O/Z	Frame synchronization pulse for transmit (BSP)
TFSX/TFRM	48	I/O/Z	Transmit frame synchronization (TDM)
HRDY	49	O/Z	Ready output (HPI)
DV_{DD}	50	Supply	$+V_{DD}$
DV_{SS}	51	Supply	Ground
HD0	52	I/O/Z	Parallel bi-directional data bus (HPI)
BDX	53	O/Z	Serial data transmit output (BSP)
TDX	54	O/Z	Serial data transmit output (TDM)
$\overline{IACK}$	55	O/Z	Interrupt acknowledge
HBIL	56	I	Byte indentification input (HPI)
$\overline{NMI}$	57	I	Nonmaskable interrupt
$\overline{INT0}$–$\overline{INT3}$	58–61	I	Interrupt 0 through Interrupt 3
CV_{DD}	62	Supply	$+V_{DD}$
HD1	63	I/O/Z	Parallel bi-directional data bus (HPI)
CV_{SS}	64	Supply	Ground
DV_{DD}	65	Supply	$+V_{DD}$
DV_{SS}	66	Supply	Ground
CLKMD1	67	I	Clock mode pin 1
CLKMD2	68	I	Clock mode pin 2
CLKMD3	69	I	Clock mode pin 3
CNT	70	I	I/O level select
HD2	71	I/O/Z	Parallel bi-directional data bus (HPI)
TOUT	72	O/Z	Timer output
EMU0	73	I/O/Z	Emulator interrupt 0
EMU1/$\overline{OFF}$	74	I/O/Z	Emulator interrupt 1/shutoff
TDO	75	O/Z	Test data output (IEEE standard 1149.1)
TDI	76	I	Test data input (IEEE standard 1149.1)
$\overline{TRST}$	77	I	Test reset (IEEE standard 1149.1)
TCK	78	I	Test clock (IEEE standard 1149.1)
TMS	79	I	Test mode select (IEEE standard 1149.1)
CV_{SS}	80	Supply	Ground
CV_{DD}	81	Supply	$+V_{DD}$
HPIENA/V_{DD}	82	I	HPI module select input
DV_{SS}	83	Supply	Ground
CLKOUT	84	O/Z	Machine clock output

† I = Input, O = Output, Z = High impedance

ADVANCE INFORMATION

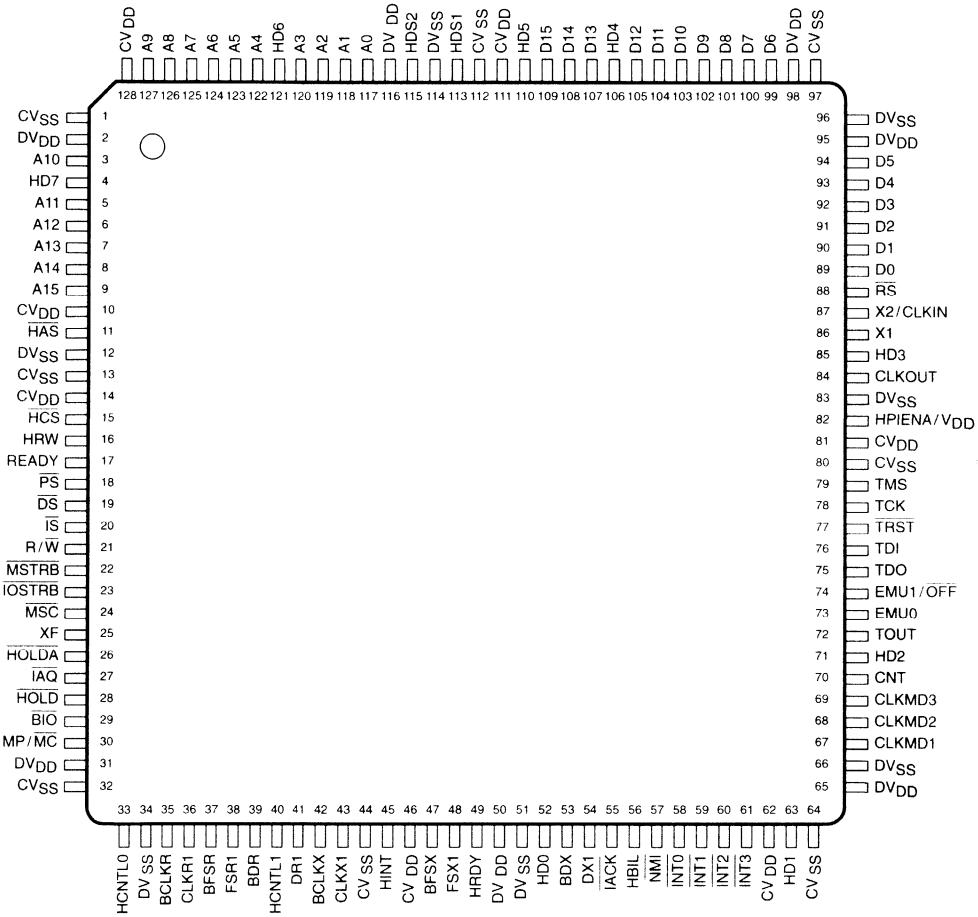
Pin Functions for the TMS320LC542PBK/'VC542PBK (128-Pin TQFP Package) (Continued)

PIN NAME	PIN NO	FUNCTION†	DESCRIPTION
HD3	85	I/O/Z	Parallel bi-directional data bus (HPI)
X1	86	O	Oscillator output
X2/CLKIN	87	I	Oscillator/external clock input
$\overline{RS}$	88	I	Device reset
D0–D5	89–94	I/O/Z	Parallel data port
DV_{DD}	95	Supply	$+V_{DD}$
DV_{SS}	96	Supply	Ground
CV_{SS}	97	Supply	Ground
DV_{DD}	98	Supply	$+V_{DD}$
D6–D12	99–105	I/O/Z	Parallel data port
HD4	106	I/O/Z	Parallel bi-directional data bus (HPI)
D13–D15	107–109	I/O/Z	Parallel data port
HD5	110	I/O/Z	Parallel bi-directional data bus (HPI)
CV_{DD}	111	Supply	$+V_{DD}$
CV_{SS}	112	Supply	Ground
HDS1	113	I	Data strobe input (HPI)
DV_{SS}	114	Supply	Ground
HDS2	115	I	Data strobe input (HPI)
DV_{DD}	116	Supply	$+V_{DD}$
A0–A3	117–120	O/Z	Parallel port address bus
HD6	121	I/O/Z	Parallel bi-directional data bus (HPI)
A4–A9	122–127	O/Z	Parallel port address bus
CV_{DD}	128	Supply	$+V_{DD}$

† I = Input, O = Output, Z = High impedance

ADVANCE INFORMATION

TMS320LC545, TMS320VC545
PBK PACKAGE†
(TOP VIEW)



† DV_{SS} and DV_{DD} are power supplies for I/O pins while CV_{SS} and CV_{DD} are power supplies for core CPU.

The pin function table on the following pages lists each pin number, signal, function, and operating mode(s) for the TMS320LC545PBK/'VC545PBK (128-pin) packages.

ADVANCE INFORMATION

Pin Functions for the TMS320LC545PBK/'VC545PBK (128-Pin TQFP Package)

PIN NAME	PIN NO	FUNCTION†	DESCRIPTION
CV_{SS}	1	Supply	Ground
DV_{DD}	2	Supply	$+V_{DD}$
A10	3	O/Z	Parallel port address bus
HD7	4	I/O/Z	Parallel bi-directional data bus (HPI)
A11–A15	5–9	O/Z	Parallel port address bus
CV_{DD}	10	Supply	$+V_{DD}$
$\overline{HAS}$	11	I	Address data strobe (HPI)
DV_{SS}	12	Supply	Ground
CV_{SS}	13	Supply	Ground
CV_{DD}	14	Supply	$+V_{DD}$
$\overline{HCS}$	15	I	Chip select input (HPI)
HRW	16	I	Read/write (HPI)
READY	17	I	External access ready to complete
$\overline{PS}$	18	O/Z	Program space select
$\overline{DS}$	19	O/Z	Data space select
$\overline{IS}$	20	O/Z	I/O select
R/$\overline{W}$	21	O/Z	Read/write
$\overline{MSTRB}$	22	O/Z	External memory access strobe
$\overline{IOSTRB}$	23	O/Z	External I/O access strobe
$\overline{MSC}$	24	O/Z	Microstate complete
XF	25	O/Z	External flag
$\overline{HOLDA}$	26	O/Z	Hold acknowledge
$\overline{IAQ}$	27	O/Z	Instruction acquisition
$\overline{HOLD}$	28	I	Request access of local memory
$\overline{BIO}$	29	I	Bit I/O pin
MP/$\overline{MC}$	30	I	Microprocessor/microcomputer
DV_{DD}	31	Supply	$+V_{DD}$
CV_{SS}	32	Supply	Ground
HCNTL0	33	I	Control inputs (HPI)
DV_{SS}	34	Supply	Ground
BCLKR	35	I	Receive clock input (BSP)
CLKR1	36	I	Receive clock input
BFSR	37	I	Frame synchronization pulse for receive (BSP)
FSR1	38	I/O	Receive frame synchronization
BDR	39	I	Serial data receive input (BSP)
HCNTL1	40	I	Control inputs (HPI)
DR1	41	I	Serial data receive input
BCLKX	42	I/O/Z	Serial port transmit clock (BSP)
CLKX1	43	I/O/Z	Serial port transmit clock

† I = Input, O = Output, Z = High impedance

ADVANCE INFORMATION

Pin Functions for the TMS320LC545PBK/'VC545PBK (128-Pin TQFP Package) (Continued)

PIN NAME	PIN NO	FUNCTION†	DESCRIPTION
CV_{SS}	44	Supply	Ground
HINT	45	O/Z	Interrupt output (HPI)
CV_{DD}	46	Supply	$+V_{DD}$
BFSX	47	I/O/Z	Frame synchronization pulse for transmit (BSP)
FSX1	48	I/O/Z	Transmit frame synchronization
HRDY	49	O/Z	Ready output (HPI)
DV_{DD}	50	Supply	$+V_{DD}$
DV_{SS}	51	Supply	Ground
HD0	52	I/O/Z	Parallel bi-directional data bus (HPI)
BDX	53	O/Z	Serial data transmit output (BSP)
DX1	54	O/Z	Serial data transmit output
$\overline{IACK}$	55	O/Z	Interrupt acknowledge
HBIL	56	I	Byte indentification input (HPI)
$\overline{NMI}$	57	I	Nonmaskable interrupt
$\overline{INT0}$–$\overline{INT3}$	58–61	I	Interrupt 0 through Interrupt 3
CV_{DD}	62	Supply	$+V_{DD}$
HD1	63	I/O/Z	Parallel bi-directional data bus (HPI)
CV_{SS}	64	Supply	Ground
DV_{DD}	65	Supply	$+V_{DD}$
DV_{SS}	66	Supply	Ground
CLKMD1	67	I	Clock mode pin 1
CLKMD2	68	I	Clock mode pin 2
CLKMD3	69	I	Clock mode pin 3
CNT	70	I	I/O level select
HD2	71	I/O/Z	Parallel bi-directional data bus (HPI)
TOUT	72	O/Z	Timer output
EMU0	73	I/O/Z	Emulator interrupt 0
EMU1/$\overline{OFF}$	74	I/O/Z	Emulator interrupt 1/shutoff
TDO	75	O/Z	Test data output (IEEE standard 1149.1)
TDI	76	I	Test data input (IEEE standard 1149.1)
$\overline{TRST}$	77	I	Test reset (IEEE standard 1149.1)
TCK	78	I	Test clock (IEEE standard 1149.1)
TMS	79	I	Test mode select (IEEE standard 1149.1)
CV_{SS}	80	Supply	Ground
CV_{DD}	81	Supply	$+V_{DD}$
HPIENA/V_{DD}	82	I	HPI module select input
DV_{SS}	83	Supply	Ground
CLKOUT	84	O/Z	Machine clock output

† I = Input, O = Output, Z = High impedance

ADVANCE INFORMATION

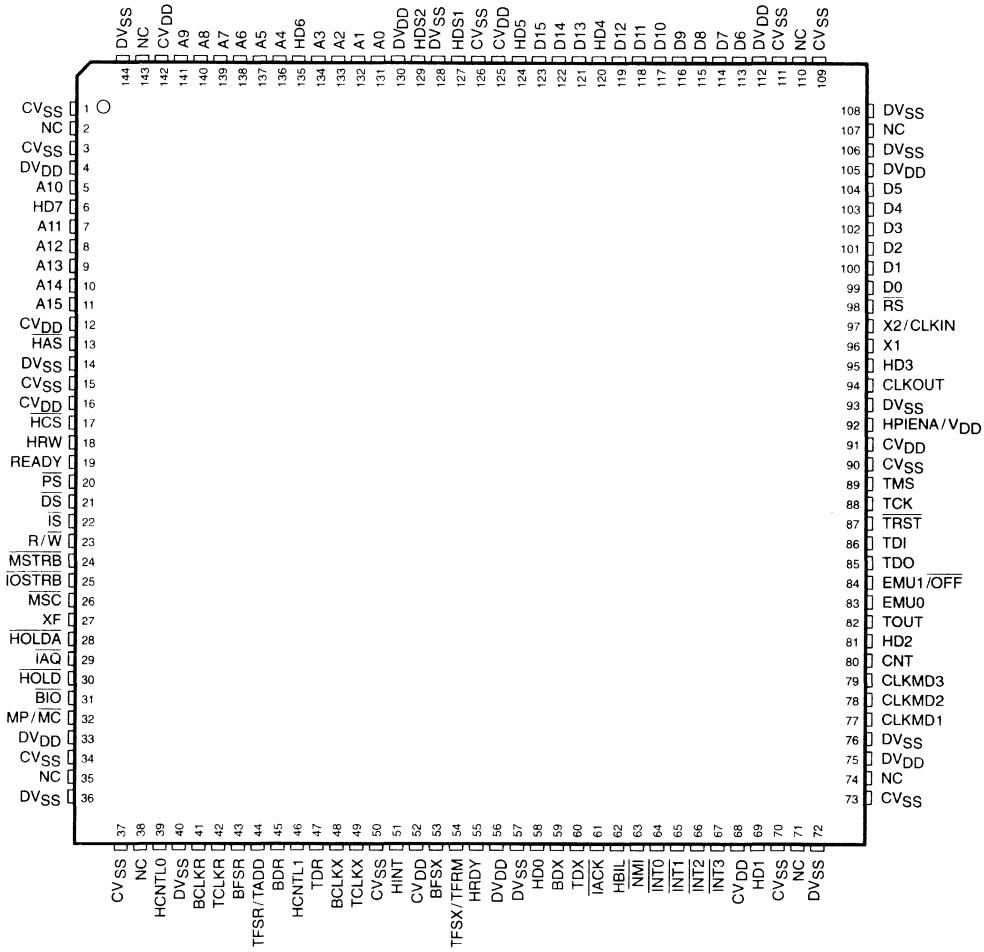
Pin Functions for the TMS320LC545PBK/'VC545PBK (128-Pin TQFP Package) (Continued)

PIN NAME	PIN NO	FUNCTION†	DESCRIPTION
HD3	85	I/O/Z	Parallel bi-directional data bus (HPI)
X1	86	O	Oscillator output
X2/CLKIN	87	I	Oscillator/external clock input
$\overline{RS}$	88	I	Device reset
D0–D5	89–94	I/O/Z	Parallel data port
DV_{DD}	95	Supply	$+V_{DD}$
DV_{SS}	96	Supply	Ground
CV_{SS}	97	Supply	Ground
DV_{DD}	98	Supply	$+V_{DD}$
D6–D12	99–105	I/O/Z	Parallel data port
HD4	106	I/O/Z	Parallel bi-directional data bus (HPI)
D13–D15	107–109	I/O/Z	Parallel data port
HD5	110	I/O/Z	Parallel bi-directional data bus (HPI)
CV_{DD}	111	Supply	$+V_{DD}$
CV_{SS}	112	Supply	Ground
HDS1	113	I	Data strobe input (HPI)
DV_{SS}	114	Supply	Ground
HDS2	115	I	Data strobe input (HPI)
DV_{DD}	116	Supply	$+V_{DD}$
A0–A3	117–120	O/Z	Parallel port address bus
HD6	121	I/O/Z	Parallel bi-directional data bus (HPI)
A4–A9	122–127	O/Z	Parallel port address bus
CV_{DD}	128	Supply	$+V_{DD}$

† I = Input, O = Output, Z = High impedance

ADVANCE INFORMATION

TMS320C542/TMS320LC542/TMS320VC542
PGE PACKAGE†‡
(TOP VIEW)



† NC = No connection
‡ DV_{SS} and DV_{DD} are power supplies for I/O pins while CV_{SS} and CV_{DD} are power supplies for core CPU.

The pin function table on the following pages lists each pin number, signal, function, and operating mode(s) for the TMS320C542PGE/'LC542PGE/'VC542PGE (144-pin) packages.

ADVANCE INFORMATION

Pin Functions for the TMS320C542PGE/'LC542PGE/'VC542PGE (144-Pin TQFP Package)

PIN NAME	PIN NO	FUNCTION†	DESCRIPTION
CV_{SS}	1	Supply	Ground
NC	2	N/A	No connection
CV_{SS}	3	Supply	Ground
DV_{DD}	4	Supply	$+V_{DD}$
A10	5	O/Z	Parallel port address bus
HD7	6	I/O/Z	Parallel bi-directional data bus (HPI)
A11–A15	7–11	O/Z	Parallel port address bus
CV_{DD}	12	Supply	$+V_{DD}$
$\overline{HAS}$	13	I	Address data strobe (HPI)
DV_{SS}	14	Supply	Ground
CV_{SS}	15	Supply	Ground
CV_{DD}	16	Supply	$+V_{DD}$
$\overline{HCS}$	17	I	Chip select input (HPI)
HRW	18	I	Read/write (HPI)
READY	19	I	External access ready to complete
$\overline{PS}$	20	O/Z	Program space select
$\overline{DS}$	21	O/Z	Data space select
$\overline{IS}$	22	O/Z	I/O select
R/$\overline{W}$	23	O/Z	Read/write
$\overline{MSTRB}$	24	O/Z	External memory access strobe
$\overline{IOSTRB}$	25	O/Z	External I/O access strobe
$\overline{MSC}$	26	O/Z	Microstate complete
XF	27	O/Z	External flag
$\overline{HOLDA}$	28	O/Z	Hold acknowledge
$\overline{IAQ}$	29	O/Z	Instruction acquisition
$\overline{HOLD}$	30	I	Request access of local memory
$\overline{BIO}$	31	I	Bit I/O pin
MP/$\overline{MC}$	32	I	Microprocessor/microcomputer
DV_{DD}	33	Supply	$+V_{DD}$
CV_{SS}	34	Supply	Ground
NC	35	N/A	No connection
DV_{SS}	36	Supply	Ground
CV_{SS}	37	Supply	Ground
NC	38	N/A	No connection
HCNTL0	39	I	Control inputs (HPI)
DV_{SS}	40	Supply	Ground
BCLKR	41	I	Receive clock input (BSP)
TCLKR	42	I	Receive clock input (TDM)
BFSR	43	I	Frame synchronization pulse for receive (BSP)
TFSR/TADD	44	I/O	Receive frame synchronization (TDM)

† I = Input, O = Output, Z = High impedance

ADVANCE INFORMATION

Pin Functions for the TMS320C542PGE/'LC542PGE/'VC542PGE (144-Pin TQFP Package) (Continued)

PIN NAME	PIN NO	FUNCTION†	DESCRIPTION
BDR	45	I	Serial data receive input (BSP)
HCNTL1	46	I	Control inputs (HPI)
TDR	47	I	Serial data receive input (TDM)
BCLKX	48	I/O/Z	Serial port transmit clock (BSP)
TCLKX	49	I/O/Z	Serial port transmit clock (TDM)
CV_{SS}	50	Supply	Ground
HINT	51	O/Z	Interrupt output (HPI)
CV_{DD}	52	Supply	$+V_{DD}$
BFSX	53	I/O/Z	Frame synchronization pulse for transmit (BSP)
TFSX/TFRM	54	I/O/Z	Transmit frame synchronization (TDM)
HRDY	55	O/Z	Ready output (HPI)
DV_{DD}	56	Supply	$+V_{DD}$
DV_{SS}	57	Supply	Ground
HD0	58	I/O/Z	Parallel bi-directional data bus (HPI)
BDX	59	O/Z	Serial data transmit output (BSP)
TDX	60	O/Z	Serial data transmit output (TDM)
$\overline{IACK}$	61	O/Z	Interrupt acknowledge
HBIL	62	I	Byte identification input (HPI)
$\overline{NMI}$	63	I	Nonmaskable interrupt
$\overline{INT0}$–$\overline{INT3}$	64–67	I	Interrupt 0 through Interrupt 3
CV_{DD}	68	Supply	$+V_{DD}$
HD1	69	I/O/Z	Parallel bi-directional data bus (HPI)
CV_{SS}	70	Supply	Ground
NC	71	N/A	No connection
DV_{SS}	72	Supply	Ground
CV_{SS}	73	Supply	Ground
NC	74	NA	No connection
DV_{DD}	75	Supply	$+V_{DD}$
DV_{SS}	76	Supply	Ground
CLKMD1	77	I	Clock mode pin 1
CLKMD2	78	I	Clock mode pin 2
CLKMD3	79	I	Clock mode pin 3
CNT	80	I	I/O level select
HD2	81	I/O/Z	Parallel bi-directional data bus (HPI)
TOUT	82	O/Z	Timer output
EMU0	83	I/O/Z	Emulator interrupt 0
EMU1/$\overline{OFF}$	84	I/O/Z	Emulator interrupt 1/shut off
TDO	85	O/Z	Test data output (IEEE standard 1149.1)

† I = Input, O = Output, Z = High impedance

ADVANCE INFORMATION

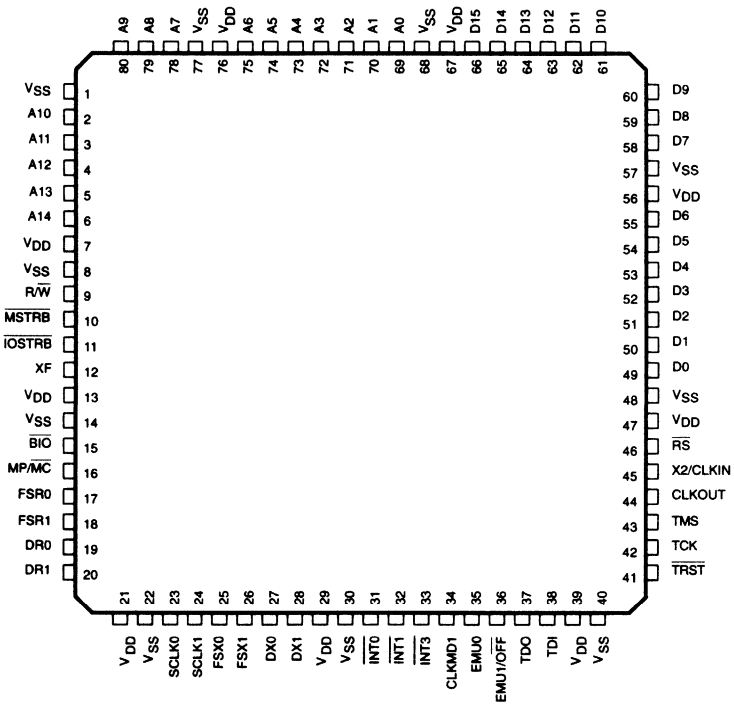
Pin Functions for the TMS320C542PGE/'LC542PGE/'VC542PGE (144-Pin TQFP Package) (Continued)

PIN NAME	PIN NO	FUNCTION†	DESCRIPTION
TDI	86	I	Test data input (IEEE standard 1149.1)
$\overline{TRST}$	87	I	Test reset (IEEE standard 1149.1)
TCK	88	I	Test clock (IEEE standard 1149.1)
TMS	89	I	Test mode select (IEEE standard 1149.1)
CV_{SS}	90	Supply	Ground
CV_{DD}	91	Supply	$+V_{DD}$
HPIENA/V_{DD}	92	I	HPI module select input
DV_{SS}	93	Supply	Ground
CLKOUT	94	O/Z	Machine clock output
HD3	95	I/O/Z	Parallel bi-directional data bus (HPI)
X1	96	O	Oscillator output
X2/CLKIN	97	I	Oscillator/external clock input
$\overline{RS}$	98	I	Device reset
D0–D5	99–104	I/O/Z	Parallel data port
DV_{DD}	105	Supply	$+V_{DD}$
DV_{SS}	106	Supply	Ground
NC	107	N/A	No connection
DV_{SS}	108	Supply	Ground
CV_{SS}	109	Supply	Ground
NC	110	N/A	No connection
CV_{SS}	111	Supply	Ground
DV_{DD}	112	Supply	$+V_{DD}$
D6–D12	113–119	I/O/Z	Parallel data port
HD4	120	I/O/Z	Parallel bi-directional data bus (HPI)
D13–D15	121–123	I/O/Z	Parallel data port
HD5	124	I/O/Z	Parallel bi-directional data bus (HPI)
CV_{DD}	125	Supply	$+V_{DD}$
CV_{SS}	126	Supply	Ground
HDS1	127	I	Data strobe input (HPI)
DV_{SS}	128	Supply	Ground
HDS2	129	I	Data strobe input (HPI)
DV_{DD}	130	Supply	$+V_{DD}$
A0–A3	131–134	O/Z	Parallel port address bus
HD6	135	I/O/Z	Parallel bi-directional data bus (HPI)
A4–A9	136–141	O/Z	Parallel port address bus
CV_{DD}	142	Supply	$+V_{DD}$
NC	143		
DV_{SS}	144	Supply	$+V_{DD}$

† I = Input, O = Output, Z = High impedance

ADVANCE INFORMATION

TMS320LC544, TMS320VC544
PN PACKAGE
(TOP VIEW)



The pin function table on the following pages lists each pin number, signal, function, and operating mode(s) for the TMS320LC544PN/TMS320VC544PN (80-pin) packages.

ADVANCE INFORMATION

Pin Functions for the TMS320LC544PN/TMS320VC544PN (80-Pin TQFP Package)

PIN NAME	PIN NO	FUNCTION†	DESCRIPTION
V_{SS}	1	Supply	Ground
A10–A14	2–6	O/Z	Parallel port address bus
V_{DD}	7	Supply	+V_{DD}
V_{SS}	8	Supply	Ground
R/$\overline{W}$	9	O/Z	Read/Write
$\overline{MSTRB}$	10	O/Z	External memory access strobe
$\overline{IOSTRB}$	11	O/Z	External I/O access strobe
XF	12	O/Z	External flag
V_{DD}	13	Supply	+V_{DD}
V_{SS}	14	Supply	Ground
$\overline{BIO}$	15	I	Bit I/O pin
MP/$\overline{MC}$	16	I	Microprocessor/microcomputer
FSR0	17	I	Serial port 0 receive frame synchronization
FSR1	18	I	Serial port 1 receive frame synchronization
DR0	19	I	Serial port 0 data receive
DR1	20	I	Serial port 1 data receive
V_{DD}	21	Supply	+V_{DD}
V_{SS}	22	Supply	Ground
SCLK0	23	I/O/Z	Serial port 0 clock
SCLK1	24	I/O/Z	Serial port 1 clock
FSX0	25	I/O/Z	Serial port 0 transmit frame synchronization
FSX1	26	I/O/Z	Serial port 1 transmit frame synchronization
DX0	27	O/Z	Serial port 0 transmit output
DX1	28	O/Z	Serial port 1 transmit output

† I = Input, O = Output, Z = High impedance

ADVANCE INFORMATION

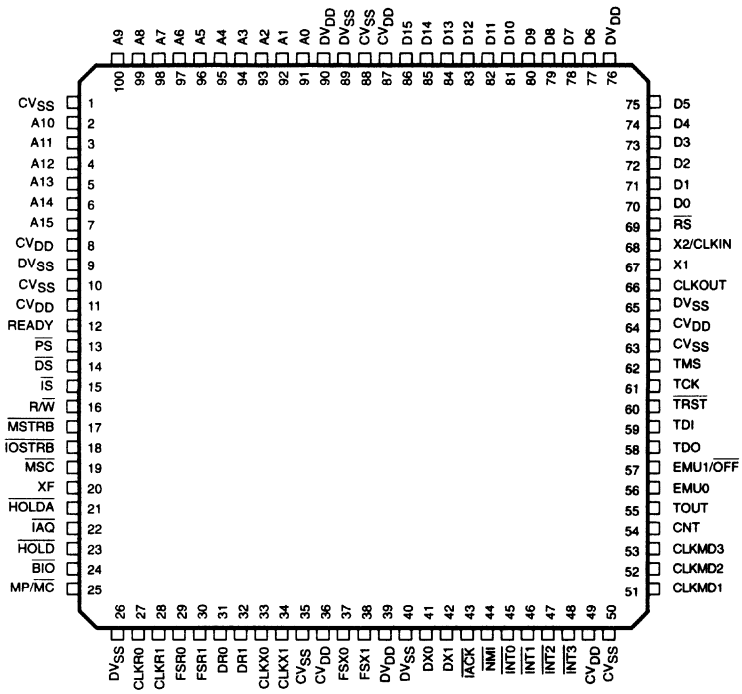
Pin Functions for the TMS320LC544PN/TMS320VC544PN (80-Pin TQFP Package) (Continued)

PIN NAME	PIN NO	FUNCTION†	DESCRIPTION
V_{DD}	29	Supply	$+V_{DD}$
V_{SS}	30	Supply	Ground
$\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$	31–33	I	Interrupt 0, 1, 3
CLKMD1	34	I	Clock mode pin 1
EMU0	35	I/O/Z	Emulator interrupt 0
EMU1/$\overline{OFF}$	36	I/O/Z	Emulator interrupt 1/shut off
TDO	37	O/Z	Test data output (IEEE standard 1149.1)
TDI	38	I	Test data input (IEEE standard 1149.1)
V_{DD}	39	Supply	$+V_{DD}$
V_{SS}	40	Supply	Ground
$\overline{TRST}$	41	I	Test reset (IEEE standard 1149.1)
TCK	42	I	Test clock (IEEE standard 1149.1)
TMS	43	I	Test mode select (IEEE standard 1149.1)
CLKOUT	44	O/Z	Machine clock output
X2/CLKIN	45	I	External clock input
$\overline{RS}$	46	I	Device reset
V_{DD}	47	Supply	$+V_{DD}$
V_{SS}	48	Supply	Ground
D0–D6	49–55	I/O/Z	Parallel data port
V_{DD}	56	Supply	$+V_{DD}$
V_{SS}	57	Supply	Ground
D7–D15	58–66	I/O/Z	Parallel data port
V_{DD}	67	Supply	$+V_{DD}$
V_{SS}	68	Supply	Ground
A0–A6	69–75	O/Z	Parallel port address bus
V_{DD}	76	Supply	$+V_{DD}$
V_{SS}	77	Supply	Ground
A7–A9	78–80	O/Z	Parallel port address bus

† I = Input, O = Output, Z = High impedance

ADVANCE INFORMATION

TMS320C541, TMS320LC541, TMS320VC541
PZ PACKAGE†
(TOP VIEW)



† DV_{SS} and DV_{DD} are power supplies for I/O pins while CV_{SS} and CV_{DD} are power supplies for core CPU.

The pin function table on the following pages lists each pin number, signal, function, and operating mode(s) for the TMS320C541PZ/TMS320LC541PZ/TMS320VC541PZ (100-pin) packages.

ADVANCE INFORMATION

Pin Functions for the TMS320C541PZ/TMS320LC541PZ/TMS320VC541PZ (100-Pin TQFP Package)

PIN NAME	PIN NO	FUNCTION†	DESCRIPTION
CV_{SS}	1	Supply	Ground
A10–A15	2–7	O/Z	Parallel port address bus
CV_{DD}	8	Supply	$+V_{DD}$
DV_{SS}	9	Supply	Ground
CV_{SS}	10	Supply	Ground
CV_{DD}	11	Supply	$+V_{DD}$
READY	12	I	External access ready to complete
$\overline{PS}$	13	O/Z	Program space select
$\overline{DS}$	14	O/Z	Data space select
$\overline{IS}$	15	O/Z	I/O space select
R/$\overline{W}$	16	O/Z	Read/write
$\overline{MSTRB}$	17	O/Z	External memory access strobe
$\overline{IOSTRB}$	18	O/Z	External I/O access strobe
$\overline{MSC}$	19	O/Z	Microstate complete
XF	20	O/Z	External flag
$\overline{HOLDA}$	21	O/Z	Hold acknowledge
$\overline{IAQ}$	22	O/Z	Instruction acquisition
$\overline{HOLD}$	23	I	Request access of local memory
$\overline{BIO}$	24	I	Bit I/O pin
MP/$\overline{MC}$	25	I	Microprocessor/microcomputer
DV_{SS}	26	Supply	Ground
CLKR0	27	I	Serial port 0 receive clock
CLKR1	28	I	Serial port 1 receive clock
FSR0	29	I	Serial port 0 receive frame synchronization
FSR1	30	I	Serial port 1 receive frame synchronization
DR0	31	I	Serial port 0 data receive
DR1	32	I	Serial port 1 data receive
CLKX0	33	I/O/Z	Serial port 0 transmit clock
CLKX1	34	I/O/Z	Serial port 1 transmit clock
CV_{SS}	35	Supply	Ground
CV_{DD}	36	Supply	$+V_{DD}$
FSX0	37	I/O/Z	Serial port 0 transmit frame synchronization
FSX1	38	I/O/Z	Serial port 1 transmit frame synchronization
DV_{DD}	39	Supply	$+V_{DD}$
DV_{SS}	40	Supply	Ground
DX0	41	O/Z	Serial port 0 transmit output
DX1	42	O/Z	Serial port 1 transmit output

† I = Input, O = Output, Z = High impedance

ADVANCE INFORMATION

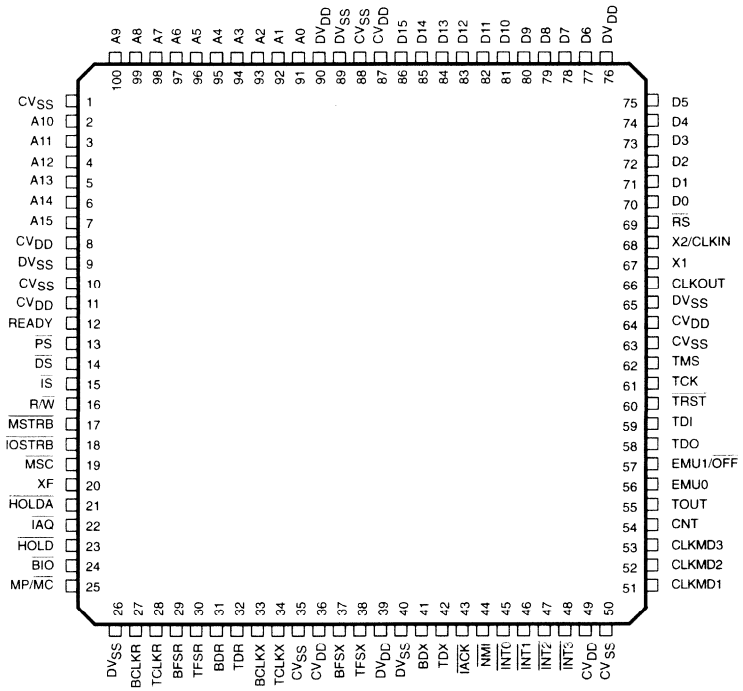
Pin Functions for the TMS320C541PZ/TMS320LC541PZ/TMS320VC541PZ (100-Pin TQFP Package) (Continued)

PIN NAME	PIN NO	FUNCTION†	DESCRIPTION
$\overline{IACK}$	43	O/Z	Interrupt acknowledge
$\overline{NMI}$	44	I	Non-maskable interrupt
$\overline{INT0}$–$\overline{INT3}$	45–48	I	Interrupt 0 through Interrupt 3
CV_{DD}	49	Supply	$+V_{DD}$
CV_{SS}	50	Supply	Ground
CLKMD1	51	I	Clock mode pin 1
CLKMD2	52	I	Clock mode pin 2
CLKMD3	53	I	Clock mode pin 3
CNT	54	I	I/O level select
TOUT	55	O/Z	Timer output
EMU0	56	I/O/Z	Emulator interrupt 0
EMU1/$\overline{OFF}$	57	I/O/Z	Emulator interrupt 1/shut off
TDO	58	O/Z	Test data output (IEEE standard 1149.1)
TDI	59	I	Test data input (IEEE standard 1149.1)
$\overline{TRST}$	60	I	Test reset (IEEE standard 1149.1)
TCK	61	I	Test clock (IEEE standard 1149.1)
TMS	62	I	Test mode select (IEEE standard 1149.1)
CV_{SS}	63	Supply	Ground
CV_{DD}	64	Supply	$+V_{DD}$
DV_{SS}	65	Supply	Ground
CLKOUT	66	O/Z	Machine clock output
X1	67	O	Oscillator output
X2/CLKIN	68	I	Oscillator/external clock input
$\overline{RS}$	69	I	Device reset
D0–D5	70–75	I/O/Z	Parallel data port
DV_{DD}	76	Supply	$+V_{DD}$
D6–D15	77–86	I/O/Z	Parallel data port
CV_{DD}	87	Supply	$+V_{DD}$
CV_{SS}	88	Supply	Ground
DV_{SS}	89	Supply	Ground
DV_{DD}	90	Supply	$+V_{DD}$
A0–A9	91–100	O/Z	Parallel port address bus

† I = Input, O = Output, Z = High impedance

ADVANCE INFORMATION

TMS320LC543, TMS320VC543
PZ PACKAGE†
(TOP VIEW)



† DV_{SS} and DV_{DD} are power supplies for I/O pins while CV_{SS} and CV_{DD} are power supplies for core CPU.

The pin function table on the following pages lists each pin number, signal, function, and operating mode(s) for the TMS320LC543PZ/TMS320VC543PZ (100-pin) packages.

For the 'LC543 and 'VC543, the letter B in front of CLKR, FSR, DR, CLKX, FSX, and DX means buffered serial port (BSP). The letter T in front of CLKR, FSR, DR, CLKX, FSX, and DX means time-division multiplexed (TDM).

ADVANCE INFORMATION

Pin Functions for the TMS320LC543PZ/TMS320VC543PZ (100-Pin TQFP Package)

PIN NAME	PIN NO	FUNCTION†	DESCRIPTION
CV_{SS}	1	Supply	Ground
A10–A15	2–7	O/Z	Parallel port address bus
CV_{DD}	8	Supply	$+V_{DD}$
DV_{SS}	9	Supply	Ground
CV_{SS}	10	Supply	Ground
CV_{DD}	11	Supply	$+V_{DD}$
READY	12	I	External access ready to complete
$\overline{PS}$	13	O/Z	Program space select
$\overline{DS}$	14	O/Z	Data space select
$\overline{IS}$	15	O/Z	I/O space select
R/$\overline{W}$	16	O/Z	Read/write
$\overline{MSTRB}$	17	O/Z	External memory access strobe
$\overline{IOSTRB}$	18	O/Z	External I/O access strobe
$\overline{MSC}$	19	O/Z	Microstate complete
XF	20	O/Z	External flag
$\overline{HOLDA}$	21	O/Z	Hold acknowledge
$\overline{IAQ}$	22	O/Z	Instruction acquisition
$\overline{HOLD}$	23	I	Request access of local memory
$\overline{BIO}$	24	I	Bit I/O pin
MP/$\overline{MC}$	25	I	Microprocessor/microcomputer
DV_{SS}	26	Supply	Ground
BCLKR	27	I	Buffered serial port receive clock
TCLKR	28	I	TDM serial port receive clock
BFSR	29	I	Buffered serial port receive frame synchronization
TFSR	30	I	TDM serial port receive frame synchronization
BDR	31	I	Buffered serial port data receive
TDR	32	I	TDM serial port data receive
BCLKX	33	I/O/Z	Buffered serial port transmit clock
TCLKX	34	I/O/Z	TDM serial port transmit clock
CV_{SS}	35	Supply	Ground
CV_{DD}	36	Supply	$+V_{DD}$
BFSX	37	I/O/Z	Buffered serial port transmit frame synchronization
TFSX	38	I/O/Z	TDM serial port transmit frame synchronization
DV_{DD}	39	Supply	$+V_{DD}$
DV_{SS}	40	Supply	Ground
BDX	41	O/Z	Buffered serial port transmit output
TDX	42	O/Z	TDM serial port transmit output

† I = Input, O = Output, Z = High impedance

ADVANCE INFORMATION

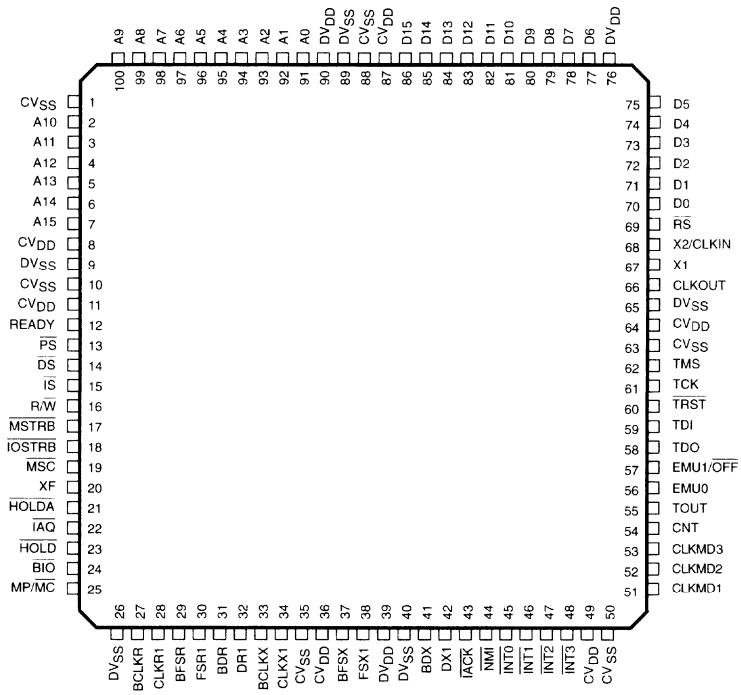
Pin Functions for the TMS320LC543PZ/TMS320VC543PZ (100-Pin TQFP Package) (Continued)

PIN NAME	PIN NO	FUNCTION†	DESCRIPTION
$\overline{IACK}$	43	O/Z	Interrupt acknowledge
$\overline{NMI}$	44	I	Non-maskable interrupt
$\overline{INT0}$–$\overline{INT3}$	45–48	I	Interrupt 0 through Interrupt 3
CV_{DD}	49	Supply	$+V_{DD}$
CV_{SS}	50	Supply	Ground
CLKMD1	51	I	Clock mode pin 1
CLKMD2	52	I	Clock mode pin 2
CLKMD3	53	I	Clock mode pin 3
CNT	54	I	I/O level select
TOUT	55	O/Z	Timer output
EMU0	56	I/O/Z	Emulator interrupt 0
EMU1/$\overline{OFF}$	57	I/O/Z	Emulator interrupt 1/shut off
TDO	58	O/Z	Test data output (IEEE standard 1149.1)
TDI	59	I	Test data input (IEEE standard 1149.1)
$\overline{TRST}$	60	I	Test reset (IEEE standard 1149.1)
TCK	61	I	Test clock (IEEE standard 1149.1)
TMS	62	I	Test mode select (IEEE standard 1149.1)
CV_{SS}	63	Supply	Ground
CV_{DD}	64	Supply	$+V_{DD}$
DV_{SS}	65	Supply	Ground
CLKOUT	66	O/Z	Machine clock output
X1	67	O	Oscillator output
X2/CLKIN	68	I	Oscillator/external clock input
$\overline{RS}$	69	I	Device reset
D0–D5	70–75	I/O/Z	Parallel data port
DV_{DD}	76	Supply	$+V_{DD}$
D6–D15	77–86	I/O/Z	Parallel data port
CV_{DD}	87	Supply	$+V_{DD}$
CV_{SS}	88	Supply	Ground
DV_{SS}	89	Supply	Ground
DV_{DD}	90	Supply	$+V_{DD}$
A0–A9	91–100	O/Z	Parallel port address bus

† I = Input, O = Output, Z = High impedance

ADVANCE INFORMATION

TMS320LC546, TMS320VC546
PZ PACKAGE†
(TOP VIEW)



† DV_{SS} and DV_{DD} are power supplies for I/O pins while CV_{SS} and CV_{DD} are power supplies for core CPU.

The pin function table on the following pages lists each pin number, signal, function, and operating mode(s) for the TMS320LC546PZ/TMS320VC546PZ (100-pin) packages.

For the 'LC546 and 'VC546, the letter B in front of CLKR, FSR, DR, FSX, and DX means BSP.

ADVANCE INFORMATION

Pin Functions for the TMS320LC546PZ/TMS320VC546PZ (100-Pin TQFP Package)

PIN NAME	PIN NO	FUNCTION†	DESCRIPTION
CV_{SS}	1	Supply	Ground
A10–A15	2–7	O/Z	Parallel port address bus
CV_{DD}	8	Supply	$+V_{DD}$
DV_{SS}	9	Supply	Ground
CV_{SS}	10	Supply	Ground
CV_{DD}	11	Supply	$+V_{DD}$
READY	12	I	External access ready to complete
$\overline{PS}$	13	O/Z	Program space select
$\overline{DS}$	14	O/Z	Data space select
$\overline{IS}$	15	O/Z	I/O space select
R/$\overline{W}$	16	O/Z	Read/write
$\overline{MSTRB}$	17	O/Z	External memory access strobe
$\overline{IOSTRB}$	18	O/Z	External I/O access strobe
$\overline{MSC}$	19	O/Z	Microstate complete
XF	20	O/Z	External flag
$\overline{HOLDA}$	21	O/Z	Hold acknowledge
$\overline{IAQ}$	22	O/Z	Instruction acquisition
$\overline{HOLD}$	23	I	Request access of local memory
$\overline{BIO}$	24	I	Bit I/O pin
MP/$\overline{MC}$	25	I	Microprocessor/microcomputer
DV_{SS}	26	Supply	Ground
BCLKR	27	I	Buffered serial port receive clock
CLKR1	28	I	Serial port 1 receive clock
BFSR	29	I	Buffered serial port receive frame synchronization
FSR1	30	I	Serial port 1 receive frame synchronization
BDR	31	I	Buffered serial port data receive
DR1	32	I	Serial port 1 data receive
BCLKX	33	I/O/Z	Buffered serial port transmit clock
CLKX1	34	I/O/Z	Serial port 1 transmit clock
CV_{SS}	35	Supply	Ground
CV_{DD}	36	Supply	$+V_{DD}$
BFSX	37	I/O/Z	Buffered serial port transmit frame synchronization
FSX1	38	I/O/Z	Serial port 1 transmit frame synchronization
DV_{DD}	39	Supply	$+V_{DD}$
DV_{SS}	40	Supply	Ground
BDX	41	O/Z	Buffered serial port transmit output
DX1	42	O/Z	Serial port 1 transmit output

† I = Input, O = Output, Z = High impedance

ADVANCE INFORMATION

Pin Functions for the TMS320LC546PZ/TMS320VC546PZ (100-Pin TQFP Package) (Continued)

PIN NAME	PIN NO	FUNCTION†	DESCRIPTION
$\overline{IACK}$	43	O/Z	Interrupt acknowledge
$\overline{NMI}$	44	I	Non-maskable interrupt
$\overline{INT0}$–$\overline{INT3}$	45–48	I	Interrupt 0 through Interrupt 3
CV_{DD}	49	Supply	$+V_{DD}$
CV_{SS}	50	Supply	Ground
CLKMD1	51	I	Clock mode pin 1
CLKMD2	52	I	Clock mode pin 2
CLKMD3	53	I	Clock mode pin 3
CNT	54	I	I/O level select
TOUT	55	O/Z	Timer output
EMU0	56	I/O/Z	Emulator interrupt 0
EMU1/$\overline{OFF}$	57	I/O/Z	Emulator interrupt 1/shut off
TDO	58	O/Z	Test data output (IEEE standard 1149.1)
TDI	59	I	Test data input (IEEE standard 1149.1)
$\overline{TRST}$	60	I	Test reset (IEEE standard 1149.1)
TCK	61	I	Test clock (IEEE standard 1149.1)
TMS	62	I	Test mode select (IEEE standard 1149.1)
CV_{SS}	63	Supply	Ground
CV_{DD}	64	Supply	$+V_{DD}$
DV_{SS}	65	Supply	Ground
CLKOUT	66	O/Z	Machine clock output
X1	67	O	Oscillator output
X2/CLKIN	68	I	Oscillator/external clock input
$\overline{RS}$	69	I	Device reset
D0–D5	70–75	I/O/Z	Parallel data port
DV_{DD}	76	Supply	$+V_{DD}$
D6–D15	77–86	I/O/Z	Parallel data port
CV_{DD}	87	Supply	$+V_{DD}$
CV_{SS}	88	Supply	Ground
DV_{SS}	89	Supply	Ground
DV_{DD}	90	Supply	$+V_{DD}$
A0–A9	91–100	O/Z	Parallel port address bus

† I = Input, O = Output, Z = High impedance

ADVANCE INFORMATION

The following tables list each signal, function, and operating mode(s) grouped by function.

Signal Descriptions

PIN NAME	PIN TYPE†	DESCRIPTION
DATA SIGNALS		
A15 (MSB) A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 (LSB)	O/Z	Parallel address bus A15 (MSB) through A0 (LSB). A15–A0 are multiplexed to address external data/program memory or I/O. A15–A0 are placed in the high-impedance state in the hold mode. A15–A0 also go into the high-impedance state when $\overline{OFF}$ is low.
D15 (MSB) D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 (LSB)	I/O/Z	Parallel data bus D15 (MSB) through D0 (LSB). D15–D0 are multiplexed to transfer data between the core CPU and external data/program memory or I/O devices. D15–D0 are placed in high-impedance state when not output or when $\overline{RS}$ or $\overline{HOLD}$ is asserted. D15–D0 also go into the high-impedance state when $\overline{OFF}$ is low. The data bus has a feature called bus holder that eliminates passive components and power dissipation associated with it. The bus holder keeps the data bus at the previous logic level when the bus goes into a high-impedance state.
INITIALIZATION, INTERRUPT AND RESET OPERATIONS		
$\overline{IACK}$	O/Z	Interrupt acknowledge signal. $\overline{IACK}$ Indicates receipt of an interrupt and that the program counter is fetching the interrupt vector location designated by A15–0. $\overline{IACK}$ also goes into the high-impedance state when $\overline{OFF}$ is low.
$\overline{INT0}$ $\overline{INT1}$ $\overline{INT2}$ $\overline{INT3}$	I	External user interrupt inputs. $\overline{INT0}$ – $\overline{INT3}$ are prioritized and maskable by the interrupt mask register and interrupt mode bit. $\overline{INT0}$ – $\overline{INT3}$ can be polled and reset by the interrupt flag register.
$\overline{NMI}$	I	Nonmaskable interrupt. $\overline{NMI}$ is an external interrupt that cannot be masked via the INTM or the IMR. When $\overline{NMI}$ is activated, the processor traps to the appropriate vector location.
$\overline{RS}$	I	Reset input. $\overline{RS}$ causes the DSP to terminate execution and forces the program counter to 0FF80h. When $\overline{RS}$ is brought to a high level, execution begins at location 0FF80h of program memory. $\overline{RS}$ affects various registers and status bits.

† I = Input, O = Output, Z = High impedance

ADVANCE INFORMATION

Signal Descriptions (Continued)

PIN NAME	PIN TYPE†	DESCRIPTION
INITIALIZATION, INTERRUPT AND RESET OPERATIONS (CONTINUED)		
MP/$\overline{MC}$	I	Microprocessor/microcomputer mode-select pin. If active low at reset (microcomputer mode), MP / $\overline{MC}$ causes the internal program ROM to be mapped into the upper 28K ('C541,'LC541 and 'VC541) words of program memory space. In the microprocessor mode, off-chip memory and its corresponding addresses instead of internal program ROM are accessed by the DSP.
CNT	I	I/O level select. For 5-V operation, all input and output voltage levels are TTL-compatible when CNT is pulled down to a low level. For 3-V operation with CMOS-compatible I/O interface levels, CNT is pulled to a high level.
MULTIPROCESSING SIGNALS		
$\overline{BIO}$	I	Branch control input. A branch can be conditionally executed when $\overline{BIO}$ is active. If low, the processor executes the conditional instruction. The $\overline{BIO}$ condition is sampled during the decode phase of the pipeline for XC instruction, and all other instructions sample $\overline{BIO}$ during the read phase of the pipeline.
XF	O/Z	External flag output (latched software-programmable signal). XF is set high by the SSBX XF instruction, set low by RSBX XF instruction or by loading ST1. XF is used for signaling other processors in multiprocessor configurations or as a general-purpose output pin. XF goes into the high-impedance state when $\overline{OFF}$ is low, and is set high at reset.
MEMORY CONTROL SIGNALS		
$\overline{DS}$ $\overline{PS}$ $\overline{IS}$	O/Z	Data, program, and I/O space select signals. $\overline{DS}$, $\overline{PS}$, and $\overline{IS}$ are always high unless driven low for communicating to a particular external space. Active period corresponds to valid address information. Placed into a high-impedance state in hold mode. $\overline{DS}$, $\overline{PS}$, and $\overline{IS}$ also go into the high-impedance state when $\overline{OFF}$ is low.
$\overline{MSTRB}$	O/Z	Memory strobe signal. $\overline{MSTRB}$ is always high unless low-level asserted to indicate an external bus access to data or program memory. Placed in high-impedance state in hold mode. $\overline{MSTRB}$ also goes into the high-impedance state when $\overline{OFF}$ is low.
READY	I	Data ready input. READY indicates that an external device is prepared for a bus transaction to be completed. If the device is not ready (READY is low), the processor waits one cycle and checks READY again. Note that the processor performs ready detection if at least two software wait states are programmed. The READY signal is not sampled until the completion of the software wait states.
R/$\overline{W}$	O/Z	Read/write signal. R/$\overline{W}$ indicates transfer direction during communication to an external device and is normally in read mode (high), unless asserted low when the DSP performs a write operation. Placed in the high-impedance state in hold mode, R/$\overline{W}$ also goes into the high-impedance state when $\overline{OFF}$ is low.
$\overline{IOSTRB}$	O/Z	I/O strobe signal. $\overline{IOSTRB}$ is always high unless low level asserted to indicate an external bus access to an I/O device. Placed in high-impedance state in hold mode. $\overline{IOSTRB}$ also goes into the high-impedance state when $\overline{OFF}$ is low.
$\overline{HOLD}$	I	Hold input. $\overline{HOLD}$ is asserted to request control of the address, data, and control lines. When acknowledged by the 'C54x, these lines go into high-impedance state.
$\overline{HOLDA}$	O/Z	Hold acknowledge signal. $\overline{HOLDA}$ indicates to the external circuitry that the processor is in a hold state and that the address, data, and control lines are in a high-impedance state allowing them to be available to the external circuitry. $\overline{HOLDA}$ also goes into the high-impedance state when is $\overline{OFF}$ low.
$\overline{MSC}$	O/Z	Microstate complete signal. $\overline{MSC}$ goes low when the last wait state of two or more internal software wait states programmed are executed. If connected to the READY line, it forces one external wait state after the last internal wait state has been completed. $\overline{MSC}$ also goes into the high-impedance state when $\overline{OFF}$ is low.
$\overline{IAQ}$	O/Z	Instruction acquisition signal. $\overline{IAQ}$ is asserted (active low) when there is an instruction address on the address bus and goes into the high-impedance state when $\overline{OFF}$ is low.

† I = Input, O = Output, Z = High impedance

ADVANCE INFORMATION

Signal Descriptions (Continued)

PIN NAME	PIN TYPE†	DESCRIPTION
OSCILLATOR/TIMER SIGNALS		
CLKOUT	O/Z	Master clock output signal. CLKOUT cycles at the machine-cycle rate of the CPU. The internal machine cycle is bounded by the rising edges of this signal. CLKOUT also goes into the high-impedance state when $\overline{OFF}$ is low.
CLKMD1 CLKMD2 CLKMD3	I	Clock mode external/internal input signals. They allow you to select and configure different clock modes such as crystal, external clock, various PLL factors.
X2/CLKIN	I	Input pin to internal oscillator from the crystal. If the internal (crystal) oscillator is not being used, a clock can become input to the device using this pin. The internal machine cycle time is determined by the clock operating mode pins (CLKMD1, CLKMD2 and CLKMD3).
X1	O	Output pin from the internal oscillator for the crystal. If the internal oscillator is not used, X1 should be left unconnected. X1 does not go into the high-impedance state when $\overline{OFF}$ is low.
TOUT	O	Timer output. TOUT signals a pulse when the on-chip timer counts down past zero. The pulse is a CLKOUT cycle wide. TOUT also goes into the high-impedance state when $\overline{OFF}$ is low.
BUFFERED SERIAL PORT (BSP) SIGNALS		
BCLKR	I	Receive clock input. BCLKR serves as the serial shift clock for the buffered serial port receiver.
BDR	I	Serial data receive input.
BFSR	I	Frame synchronization pulse for receive input. The BFSR pulse initiates the receive data process over BDR.
BCLKX	I/O/Z	Transmit clock. BCLKX serves as the serial shift clock for the buffered serial port transmitter. If $\overline{RS}$ is asserted when BCLKX is configured as output, then BCLKX is turned into input mode by reset operation. BCLKX goes into the high-impedance state when $\overline{OFF}$ is low.
BDX	O/Z	Serial data transmit output. BDX is placed in the high-impedance state when not transmitting, when $\overline{RS}$ is asserted or when $\overline{OFF}$ is low.
BFSX	I/O/Z	Frame synchronization pulse for transmit input/output. The BFSX pulse initiates the transmit data process over BDX. If $\overline{RS}$ is asserted when BFSX is configured as output, then BFSX is turned into input mode by reset operation. BFSX goes into the high-impedance state when $\overline{OFF}$ is low.
SERIAL PORT 0 AND SERIAL PORT 1 SIGNALS		
CLKR0 CLKR1	I	Receive clocks. External clock signal for clocking data from the data receive (DR) pin into the serial port receive shift registers (RSR). Must be present during serial port transfers. If the serial port is not being used, CLKR0 and CLKR1 can be sampled as an input via IN0 bit of the SPC register.
CLKX0 CLKX1	I/O/Z	Transmit clock. Clock signal for clocking data from the serial port transmit shift register (XSR) to the data transmit (DX) pin. CLKX can be an input if MCM in the serial port control register is cleared to 0. It also can be driven by the device at 1/4 CLKOUT frequency when MCM is set to 1. If the serial port is not used, CLKX can be sampled as an input via IN1 of the SPC register. CLKX0 and CLKX1 go into the high-impedance state when $\overline{OFF}$ is low.
DR0 DR1	I	Serial-data-receive input. Serial data is received in the RSR by DR.
DX0 DX1	O/Z	Serial port transmit output. Serial data is transmitted from the XSR via DX. DX0 and DX1 are placed in the high-impedance state when not transmitting and when $\overline{OFF}$ is low.
FSR0 FSR1	I	Frame synchronization pulse for receive input. The falling edge of the FSR pulse initiates the data-receive process, beginning the clocking of the RSR.
FSX0 FSX1	I/O/Z	Frame synchronization pulse for transmit input/output. The falling edge of the FSX pulse initiates the data transmit process, beginning the clocking of the XSR. Following reset, the default operating condition of FSX is an input. FSX0 and FSX1 can be selected by software to be an output when TXM in the serial control register is set to 1. This pin goes into the high-impedance state when $\overline{OFF}$ is low.

† I = Input, O = Output, Z = High impedance

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Signal Descriptions (Continued)

PIN NAME	PIN TYPE†	DESCRIPTION
TDM SERIAL PORT SIGNAL		
TCLKR	I	Receive clock input
TDR	I	Serial data receive input
TFSR/TADD	I/O	Receive frame synchronization or address
TCLKX	I/O/Z	Transmit clock
TDX	O/Z	Serial data transmit output
TFSX/TFRM	I/O/Z	Transmit frame synchronization
MISCELLANEOUS PIN		
NC		No connection
HOST PORT INTERFACE SIGNALS		
HD0–HD7	I/O/Z	Parallel bi-directional data bus. HD0–HD7 are placed in high-impedance state when not outputting data. The signals go into the high-impedance state when $\overline{OFF}$ is low.
HCNTL0 HCNTL1	I	Control inputs
HBIL	I	Byte identification input
$\overline{HCS}$	I	Chip select input
$\overline{HDS1}$ $\overline{HDS2}$	I	Data strobe inputs
$\overline{HAS}$	I	Address strobe input
HRW	I	Read/write input
HRDY	O/Z	Ready output. This signal goes into the high-impedance state when $\overline{OFF}$ is low.
HINT	O/Z	Interrupt output. When the DSP is in reset, this signal is driven high. The signal goes into the high-impedance state when $\overline{OFF}$ is low.
HPIENA/V_{DD}	I	HPI module select input. This signal must be tied to V_{DD} to have HPI selected. If this input is left open or connected to ground, HPI module will not be selected, internal pullup for HPI input pins are enabled and HPI data bus has keepers set.
SUPPLY PNS		
CV_{SS}	Supply	Ground. CV_{SS} is the dedicated power supply for the core CPU.
CV_{DD}	Supply	+VDD. CV_{DD} is the dedicated power supply for the core CPU.
DV_{SS}	Supply	Ground. DV_{SS} is the dedicated power supply for I/O pins.
DV_{DD}	Supply	+V_{DD}. DV_{DD} is the dedicated power supply for I/O pins.
TEST PINS		
TCK	I	IEEE standard 1149.1 test clock. This is normally a free-running clock signal with a 50% duty cycle. The changes on test access port (TAP) of input signals TMS and TDI are clocked into the TAP controller, instruction register, or selected test data register on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK.
TD	I	IEEE standard 1149.1 test data input, pin with internal pullup device. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO	O/Z	IEEE standard 1149.1 test data output. The contents of the selected register (instruction or data) is shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance state except when scanning of data is in progress. TDO also goes into the high-impedance state when $\overline{OFF}$ is low.

† I = Input, O = Output, Z = High impedance

Signal Descriptions (Continued)

PIN NAME	PIN TYPE†	DESCRIPTION
TEST PINS (CONTINUED)		
TMS	I	IEEE standard 1149.1 test mode select. Pin with internal pullup device. This serial control input is clocked into the test access port (TAP) controller on the rising edge of TCK.
$\overline{\text{TRST}}$	I	IEEE standard 1149.1 test reset. $\overline{\text{TRST}}$, when high, gives the IEEE standard 1149.1 scan system control of the operations of the device. If $\overline{\text{TRST}}$ is not connected or driven low, the device operates in its functional mode, and the IEEE standard 1149.1 signals are ignored. Pin with internal pullup device.
EMU0	I/O/Z	Emulator 0 pin. When $\overline{\text{TRST}}$ is driven low, EMU0 must be high for activation of the $\overline{\text{OFF}}$ condition. When $\overline{\text{TRST}}$ is driven high, EMU0 is used as an interrupt to or from the emulator system and is defined as input/output via IEEE standard 1149.1 scan system.
EMU1/$\overline{\text{OFF}}$	I/O/Z	Emulator 1 pin/disable all outputs. When $\overline{\text{TRST}}$ is driven high, EMU1/$\overline{\text{OFF}}$ is used as an interrupt to or from the emulator system and is defined as input/output via IEEE standard 1149.1 scan system. When $\overline{\text{TRST}}$ is driven low, EMU1/$\overline{\text{OFF}}$ is configured as $\overline{\text{OFF}}$. The EMU1/$\overline{\text{OFF}}$ signal, when active low, puts all output drivers into the high-impedance state. Note that $\overline{\text{OFF}}$ is used exclusively for testing and emulation purposes (not for multiprocessing applications). Thus, for $\overline{\text{OFF}}$ condition, the following conditions apply: $\overline{\text{TRST}}$ = low, EMU0 = high EMU1/$\overline{\text{OFF}}$ = low

† I = Input, O = Output, Z = High impedance

architecture

The 'C54x/'LC54x/'VC54x DSPs use an advanced, modified Harvard architecture that maximizes processing power by maintaining three separate bus structures for data memory and one for program memory. Separate program and data spaces allow simultaneous access to program instructions and data, providing a high degree of parallelism. For example, two reads and one write operation can be performed in a single cycle. Instructions with parallel store and application-specific instructions fully utilize this architecture. In addition, data can be transferred between data and program spaces. Such parallelism supports a powerful set of arithmetic, logic, and bit-manipulation operations that all can be performed in a single machine cycle. In addition, the 'C54x/'LC54x/'VC54x include the control mechanisms to manage interrupts, repeated operations, and function calling.

The functional block diagram includes the principal blocks and bus structure in the 'C54x/'LC54x/'VC54x devices.

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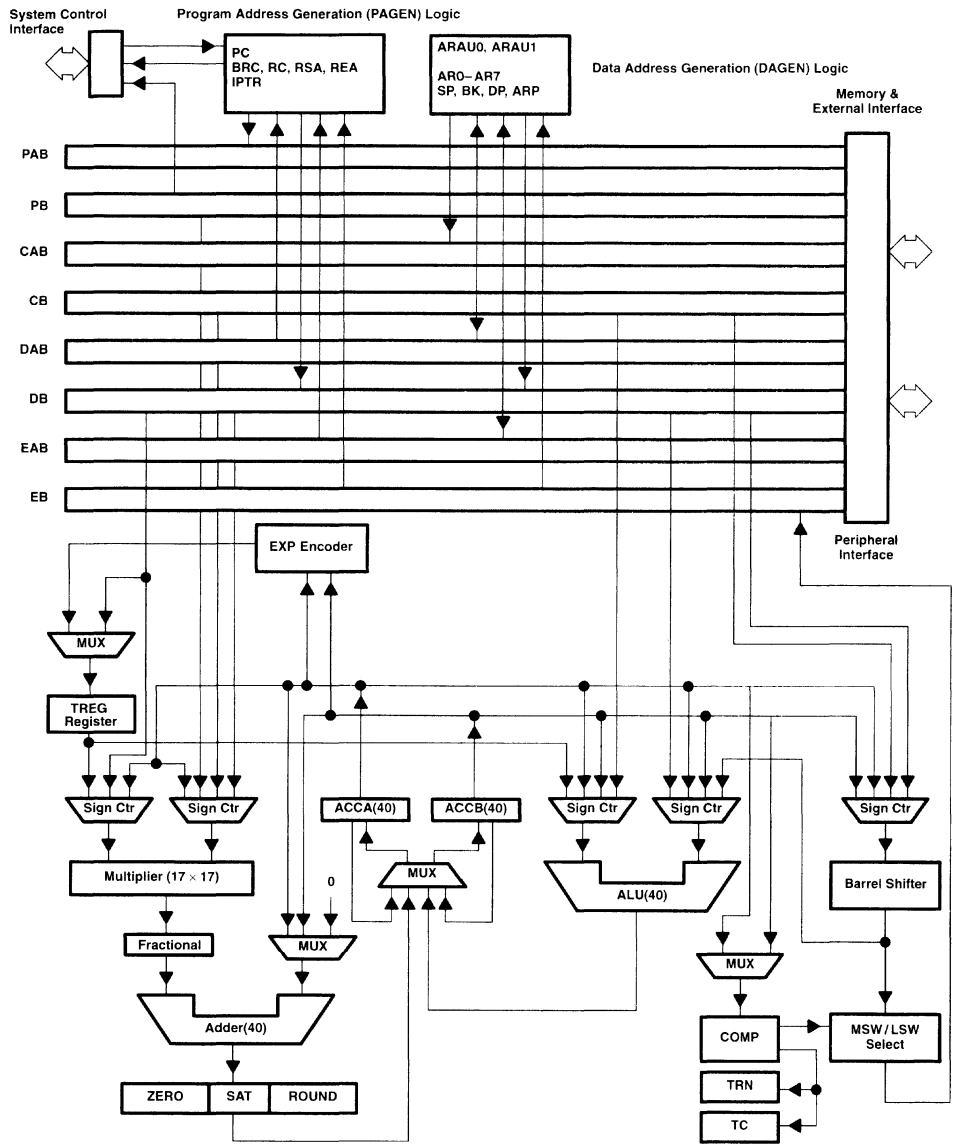
functional block diagram of the 'C54x/'LC54x/'VC54x internal hardware



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bus structure

The 'C54x/'LC54x/'VC54x device architecture is built around eight major 16-bit buses:

- One program bus (P bus), which carries the instruction code and immediate operands from program memory
- Three data buses (CB, DB, and EB), which interconnect to various elements, such as the CPU, data-address generation logic, program-address generation logic, on-chip peripherals, and data memory
  - The CB and DB carry the operands read from data memory.
  - The EB carries the data to be written to memory.
- Four address buses (PAB, CAB, DAB, and EAB), which carry the addresses needed for instruction execution

The 'C54x/'LC54x/'VC54x devices have the capability to generate up to two data memory addresses per cycle, which are stored into two auxiliary register arithmetic units (ARAU0 and ARAU1).

The program bus (PB) can carry data operands stored in program space (for instance, a coefficient table) to the multiplier for multiply/accumulate operations or to a destination in data space for the data move instruction. This capability allows implementation of single-cycle three-operand instructions such as FIRS.

The 'C54x/'LC54x/'VC54x devices also have an on-chip bi-directional bus for accessing on-chip peripherals; this bus is connected to DB and EB through the bus exchanger in the CPU interface. Accesses using this bus can require more than two cycles for reads and writes depending on the peripheral's structure.

The 'C54x/'LC54x/'VC54x devices can have bus keepers connected to the data bus. Bus keepers ensure that the data bus does not float. When bus keepers are enabled, the data bus maintains its previous level. Setting bit 1 of the bank switching control register (BSCR) enables bus keepers and clearing bit 1 disables the bus keepers. Resets automatically disable the bus keepers.

Table 2 summarizes the buses used by various types of accesses.

Table 2. Bus Usage for Accesses

ACCESS TYPE	ADDRESS BUS				DATA BUS			
	PAB	CAB	DAB	EAB	PB	CB	DB	EB
Program read	√				√			
Program write	√							√
Data single read			√				√	
Data dual read		√	√			√	√	
Data long (32-bit) read		√(hw)	√(lw)			√(hw)	√(lw)	
Data single write				√				√
Data read/data write			√	√			√	√
Dual read/coefficient read	√	√	√		√	√	√	
Peripheral read			√				√	
Peripheral write				√				√

Legend:
hw = high 16-bit word
lw = low 16-bit word

central processing unit (CPU)

The CPU of the 'C54x,/'LC54x/'VC54x devices contains:

- A 40-bit arithmetic logic unit (ALU)
- Two 40-bit accumulators
- A barrel shifter
- A 17 × 17-bit multiplier
- A compare select and store unit (CSSU)

arithmetic logic unit (ALU)

The 'C54x/'LC54x/'VC54x perform 2s-complement arithmetic using: a 40-bit arithmetic logic unit (ALU) and two 40-bit accumulators (ACCA and ACCB). The ALU also can perform Boolean operations.

The ALU can function as two 16-bit ALUs and perform two 16-bit operations simultaneously when the C16 bit in status register 1 (ST1) is set.

accumulators

The accumulators, ACCA and ACCB, store the output from the ALU or the multiplier / adder block; the accumulators can also provide a second input to the ALU or the multiplier / adder. The accumulators are divided into three parts:

- Guard bits (bits 32–39)
- A high-order word (bits 16–31)
- A low-order word (bits 0–15)

Instructions are provided for storing the guard bits, the high- and the low-order accumulator words in data memory, and for manipulating 32-bit accumulator words in or out of data memory. Also, any of the accumulators can be used as temporary storage for the other.

barrel shifter

The 'C54x/'LC54x/'VC54x's barrel shifter has a 40-bit input connected to the accumulator, or data memory (C, D bus) and a 40-bit output connected to the ALU, or data memory (E bus). The barrel shifter produces a left shift of 0 to 31 bits and a right shift of 0 to 16 bits on the input data. The shift requirements are defined in the shift count field (ASM) of ST1 or defined in the temporary register (TREG), which is designated as a shift count register. This shifter and the exponent detector normalize the values in an accumulator in a single cycle. The LSBs of the output are filled with 0s and the MSBs can be either zero-filled or sign-extended, depending on the state of the sign-extended mode bit (SXM) of ST1. Additional shift capabilities enable the processor to perform numerical scaling, bit extraction, extended arithmetic, and overflow prevention operations.

multiplier/adder

The multiplier / adder performs 17 × 17-bit 2s-complement multiplication with a 40-bit accumulation in a single instruction cycle. The multiplier / adder block consists of several elements: a multiplier, adder, signed / unsigned input control, fractional control, a zero detector, a rounder (2s-complement), overflow / saturation logic, and TREG. The multiplier has two inputs: one input is selected from either TREG, data memory operand, or an accumulator; the other is selected from either program memory, data memory, an accumulator, or an immediate value. The fast on-chip multiplier allows the 'C54x to efficiently perform operations such as convolution, correlation, and filtering.

In addition, the multiplier and ALU together execute multiply/accumulate (MAC) computations and ALU operations in parallel in a single instruction cycle. This function is used in determining the Euclid distance, and implementing symmetrical and LMS filters, which are required for complex DSP algorithms.

compare, select and store unit (CSSU)

The compare, select, and store unit (CSSU) performs maximum comparisons between the accumulator's high and low word, allows test/control (TC) flag bit of status control register 0 (ST0) and transition (TRN) register to keep their transition histories, and selects larger word in accumulator to be stored into data memory. The CSSU also accelerates Viterbi-type butterfly computation with optimized on-chip hardware.

program control

Program control is provided by several hardware and software mechanisms:

- The program controller decodes instructions, manages the pipeline, stores the status of operations, and decodes conditional operations. Some of the hardware elements included in the program controller are the program counter, the status and control register, the stack, and the address-generation logic.
- Some of the software mechanisms used for program control include branches, calls, conditional instructions, a repeat instruction, reset, and interrupts.

power-down modes

There are three power-down modes, activated by the IDLE1, IDLE2, and IDLE3 instructions. In these modes, the 'C54x/'LC54x/'VC54x enters a dormant state and dissipates considerably less power than in normal operation. The IDLE1 instruction is used to shut down the CPU. The IDLE2 instruction is used to shut down the CPU and on-chip peripherals. The IDLE3 instruction is used to completely shut down the 'C54x/'LC54x/'√C54x processor. This instruction stops the PLL circuitry as well as the CPU and peripherals.

memory

The total memory address range of the 'C54x/'LC54x/'VC54x devices is 192K 16-bit words. The memory space is divided into three specific memory segments: 64K word program, 64K-word data, and 64K-word I/O. The program memory space contains the instructions to be executed as well as tables used in execution. The data memory space stores data used by the instructions. The I/O memory space interfaces to external memory-mapped peripherals and can also serve as extra data storage space.

The parallel nature of the architecture of these DSPs allows them to perform four concurrent memory operations in any given machine cycle: fetching an instruction, reading two operands, and writing an operand. The four parallel buses are the program-read bus (PB), the write-data bus (EB) and two read-data buses (CB and DB). Each bus accesses different memory spaces for different aspects of the DSPs operation. Additionally, this architecture allows dual-operand reads, 32-bit-long word accesses, and a single read with a parallel store.

The 'C54x/'LC54x/'VC54x DSPs include on-chip memory to aid in system performance and integration.

on-chip ROM

The 'C541, 'LC541 and 'VC541 all feature a 28K-word × 16-bit on-chip maskable ROM. 8K words of the 'C541, 'LC541 and 'VC541 ROM can be mapped into program and data memory space if the data ROM (DROM) bit in the processor mode status (PMST) register is set. This allows an instruction to use data stored in the ROM as an operand.

The 'LC544 and 'VC544 both feature a 24K-word × 16-bit on-chip maskable ROM. 8K words of the 'LC544 and 'VC544 ROM can be mapped into program and data memory space if the DROM bit in the PMST register is set.

The 'LC545/'VC545/'LC546/'VC546 all feature a 48K-word × 16-bit on-chip maskable ROM. 16K words of the ROM on these devices can be mapped into program and data memory space if the DROM bit in the PMST register is set.

The 'C542/'LC542/'VC542/'LC543/'VC543 all feature 2K-word × 16-bit on-chip ROM.

Customers can arrange to have the ROM of the 'C54x/'LC54x/'VC54x programmed with contents unique to any particular application.

on-chip ROM (continued)

A boot loader is available in the standard 'C54x/'LC54x/'VC54x on-chip ROM. This boot loader can be used to transfer user code from an external source to anywhere in the program memory at power up automatically. If MP/$\overline{MC}$ of the device is sampled low during a hardware reset, execution begins at location FF80h of the on-chip ROM. This location contains a branch instruction to the start of the boot loader program. The standard 'C54x/'LC54x/'VC54x devices provide different ways to download the code to accommodate various system requirements:

- Parallel from 8-bit of 16-bit wide EPROM
- Parallel from I/O space 8-bit of 16-bit mode
- Serial boot from serial ports 8-bit of 16-bit mode
- Host port interface boot ('C542, 'LC542, 'VC542, 'LC545, 'VC545 devices only)
- Warm boot

on-chip dual-access RAM

The 'C541, 'LC541 and 'VC541 devices have a 5K-word × 16-bit on-chip dual-access RAM (DARAM) (5 blocks of 1K-word each).

The 'C542, 'LC542, 'VC542, 'LC543 and 'VC543 have a 10K-word × 16-bit on-chip DARAM (5 blocks of 2K-word each).

The 'LC544 and 'VC544 have a 4K-word × 16-bit on-chip DARAM (2 blocks of 2K-word each).

The 'LC545, 'VC545, 'LC546 and 'VC546 have a 6K-word × 16-bit on-chip DARAM (3 blocks of 2K-word each).

Each of these RAM blocks can be accessed twice per machine cycle. This memory is intended primarily to store data values; however, it can be used to store program as well. At reset, the DARAM is mapped into data memory space. DARAM can be mapped into program/data memory space by setting the OVLY bit in the PMST register.

on-chip memory security

The 'C54x/'LC54x/'VC54x devices have a maskable option to protect the contents of on-chip memories. When the related bit is set, no externally originating instruction can access the on-chip memory spaces.

on-chip memory security (continued)

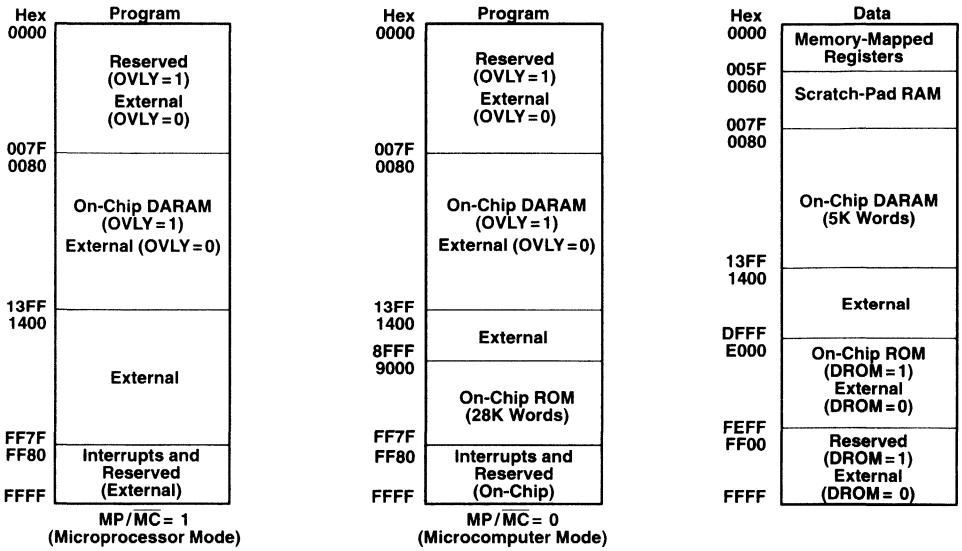


Figure 1. Memory Map ('C541, 'LC541, 'VC541)

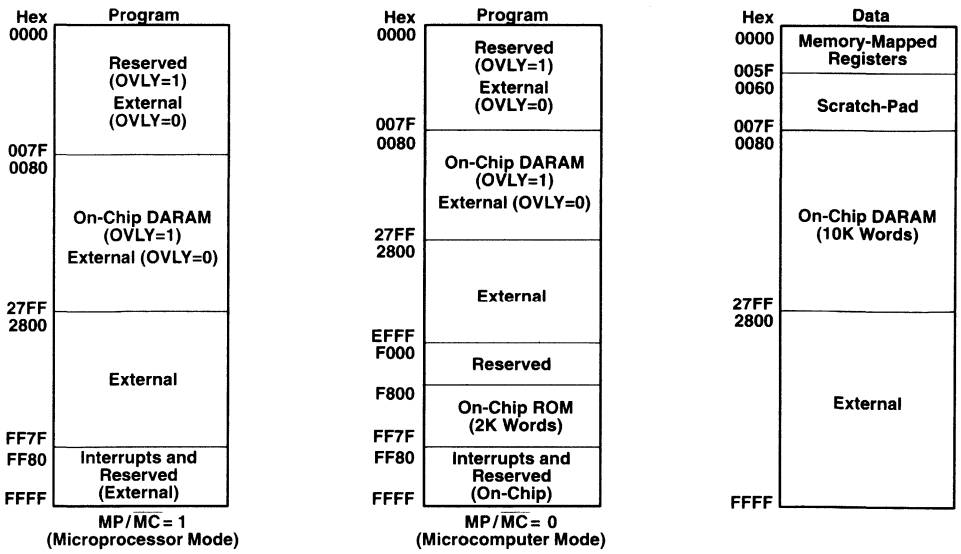


Figure 2. Memory Map ('C542, 'LC542, 'VC542, 'LC543 and 'VC543)

ADVANCE INFORMATION

on-chip memory security (continued)

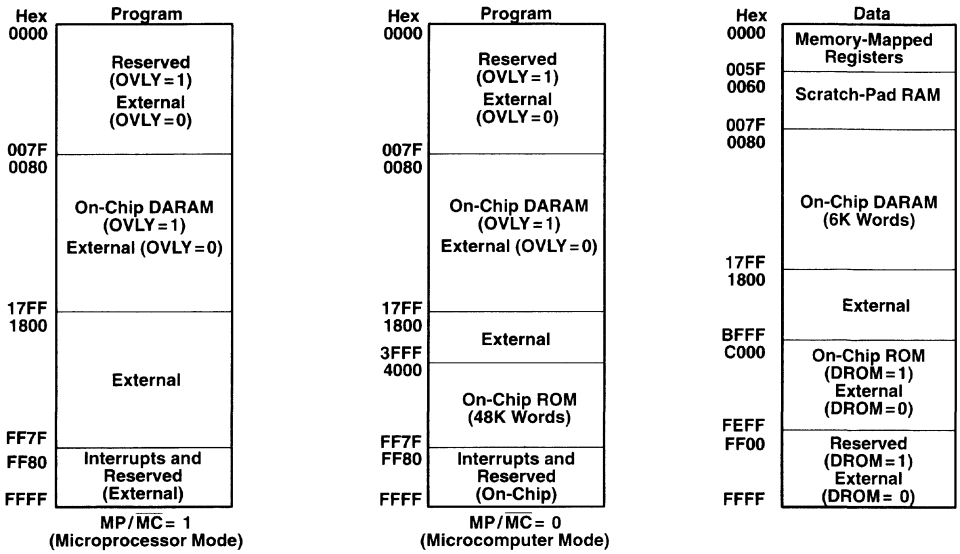
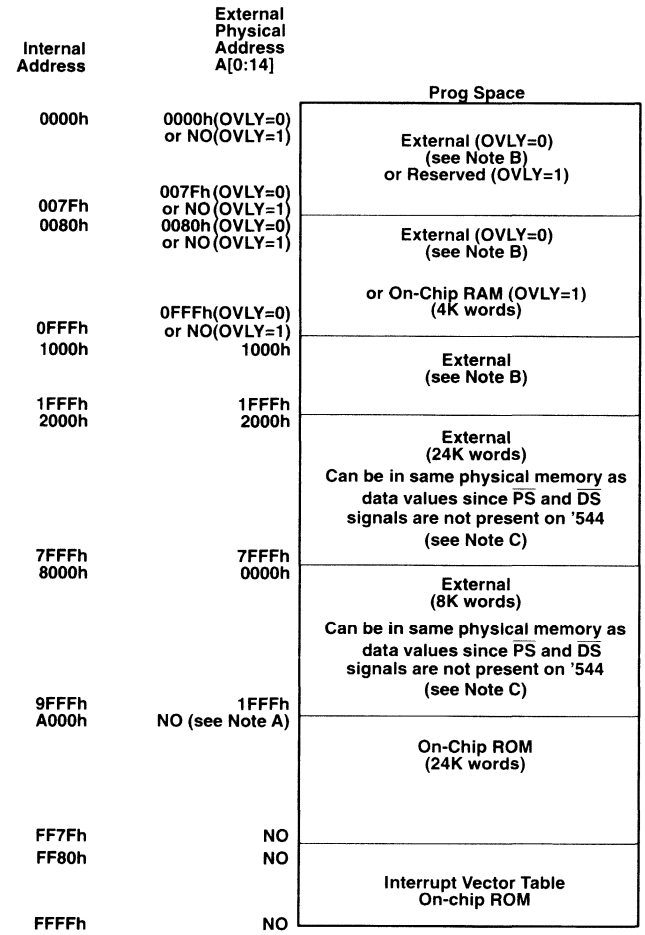


Figure 3. Memory Map ('LC545, 'VC545, 'LC546, and 'VC546)

ADVANCE INFORMATION

'LC544/'VC544 memory maps



NOTES: A. This space is on-chip only. NO means no external access.

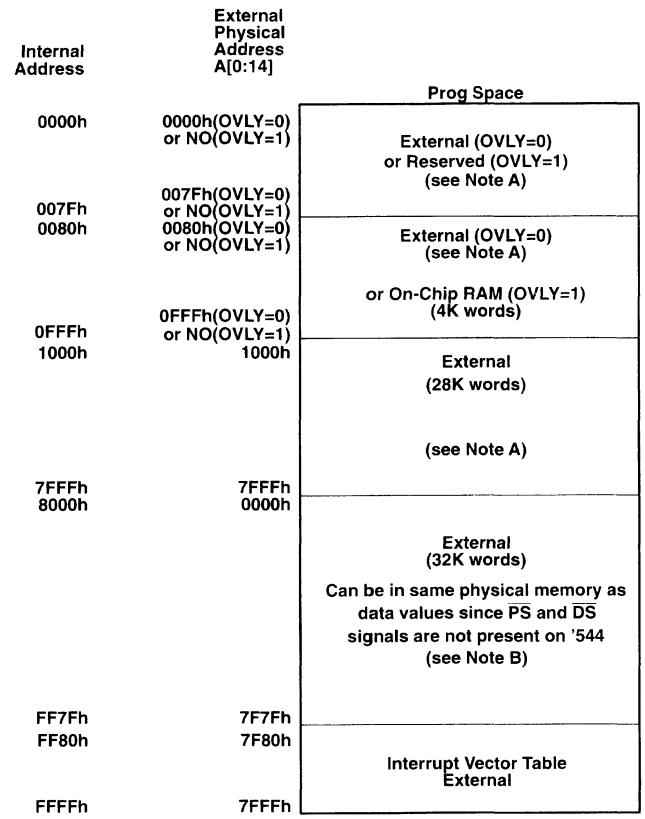
B. The space placed between 0000h and 1FFFh (when OVLY is off) or between 1000h and 1FFFh (when OVLY is on) addresses requires special attention. An access at this space is the same as an access at the image address in the 8000h–9FFFh (internal address) space. For example, access at 1000h is an access at internal 9000h (or in other words external 1000h).

C. It is the user's responsibility to make sure that data and program do not overlay in the same external physical addresses.

Figure 4. Memory Map – Program Space With MP/$\overline{MC}$=0 ('LC544 and 'VC544)

ADVANCE INFORMATION

'LC544/'VC544 memory maps (continued)



NOTES: A. The space placed between 0000h and 7FFFh (when OVLY is off) or between 1000h and 7FFFh (when OVLY is on) addresses requires special attention. An access at this space is the same as an access at the image address in the 8000h–FFFFh (internal address) space.

B. For example, access at 1000h the same as an access at internal 9000h (or, in other words, external 1000h).

Figure 5. Memory Map – Program Space With MP/$\overline{MC}$=1 ('LC544 and 'VC544)

'LC544/'VC544 memory maps (continued)

Internal Address	External Physical Address A[0:14]	Data Space
0000h	NO (see Note D)	Memory-Mapped Registers
005Fh	NO	
0060h	NO	Scratch-Pad
007Fh	NO	
0080h	NO	On-Chip DARAM (4K words)
0FFFh	NO	
1000h	1000h	External (28K words) Can be in same physical memory as program values since PS and DS signals are not present on '544 (see Note B)
7FFFh	7FFFh	
8000h	0000h	External (4K words) Can be in same physical memory as program values since PS and DS signals are not present on '544 (see Note B)
8FFFh	0FFFh	
9000h	1000h	External (see Note C)
DFFFh	5FFFh	
E000h	6000h(DROM=0) or NO(DROM=1)	External (DROM=0) (see Note D) or On-Chip DROM (DROM=1)
FEFFh		
FF00h	7F00h(DROM=0) or NO(DROM=1)	External (DROM=0) (see Note D) or Reserved (DROM=1)
FFFFh		

NOTES: A. This space is on-chip only. NO means no external access.
B. It is the user's responsibility to make sure that data and program do not overlay in the same external physical addresses.
C. The 20K words of space placed between 9000h and DFFFh internal addresses requires special attention. An access at this space is the same as an access at the image address in the 1000h–5FFFh space. For example, access at B000h (internal address) is an access at external 3000h.
D. When DROM=0, the 8K words of space placed between E000h and FFFFh internal addresses requires special attention. An access at this space is the same as an access at the image address in the 6000h–7FFFh space.

Figure 6. Memory Map – Data Space ('LC544 and 'VC544)

The external memory space on the 'LC544 and 'VC544 device addresses up to 32K of 16-bit words through its external 15 line address bus A[0:14]. Since A15 line still is present in internal address buses, the internal address reach is 64K for both data and program spaces. Two types of addresses are defined in Figure 4, Figure 5, and Figure 6.

–> internal address which appears on internal buses (PAB, CAB, DAB, EAB).
–> external physical address which appears on the external A[0:14] bus.

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program memory

The external program memory space on the 'C54x/'LC54x/'VC54x devices addresses up to 64K 16-bit words. Software can configure their memory cells to reside inside or outside of the program address map. When the cells are mapped into program space, the device automatically accesses them when their addresses are within bounds. When the program-address generation (PAGEN) logic generates an address outside its bounds, the device automatically generates an external access. The advantages of operating from on-chip memory are as follows:

- Higher performance because no wait states are required
- Lower cost than external memory
- Lower power than external memory

The advantage of operating from off-chip memory is the ability to access a larger address space.

program memory address map

The reset, interrupt, and trap vectors are addressed in program space. These vectors are soft — meaning that the processor, when taking the trap, loads the program counter (PC) with the trap address and executes the code at the vector location. Four words are reserved at each vector location to accommodate a delayed branch instruction, and either two 1-word instructions or one 2-word instruction, which allows branching to the appropriate interrupt service routine without the overhead.

At device reset, the reset, interrupt, and trap vectors are mapped to address FF80h in program space. However, these vectors can be remapped to the beginning of any 128-word page in program space after device reset. This is done by loading the interrupt vector pointer (IPTR) bits in the PMST register with the appropriate 128-word page boundary address. After loading IPTR, any user interrupt or trap vector is mapped to the new 128-word page. For example:

```
STM    #05800h,PMST     ;Remapped vectors to start at 5800h.
```

This example moves the interrupt vectors to off-chip program space at address 05800h. Any subsequent interrupt (except for a device reset) fetches its interrupt vector from that new location. For example, if, after loading the IPTR, an $\overline{\text{INT2}}$ occurs, the interrupt service routine vector is fetched from location 5848h in program space as opposed to location FFC8h. This feature facilitates moving the desired vectors out of the boot ROM and then removing the ROM from the memory map. Once the system code is booted into the system from the boot-loader code resident in ROM, the application reloads the IPTR with a value pointing to the new vectors. In the previous example, the STM instruction is used to modify the PMST. Note that the STM instruction modifies not only the IPTR but other status/control bits in the PMST register.

NOTE: The hardware reset ($\overline{\text{RS}}$) vector can not be remapped, because the hardware reset loads the IPTR with 1s. Therefore, the reset vector is always fetched at location FF80h in program space. In addition, for the 'C54x/'LC54x/'VC54x, 128 words are reserved in the on-chip ROM for device-testing purposes. Application code written to be implemented in on-chip ROM must reserve these 128 words at addresses FF00h–FF7Fh in program space.

data memory

The data memory space on the 'C54x/'LC54x/'VC54x device addresses contains up to 64K of 16-bit words. The 'C54x/'LC54x/'VC54x devices automatically access the on-chip RAM when addressing within its bounds. When an address is generated outside the RAM bounds, the device automatically generates an external access.

The advantages of operating from on-chip memory are as follows:

- Higher performance because no wait states are required
- Higher performance because of better flow within the pipeline of the CALU
- Lower cost than external memory
- Lower power than external memory

The advantage of operating from off-chip memory is the ability to access a larger address space.

on-chip peripherals

All the 'C54x/'LC54x/'VC54x devices have the same CPU structure; however, they have different on-chip peripherals connected to their CPUs. The on-chip peripheral options provided are:

- Software-programmable wait-state generator
- Programmable bank switching
- Parallel I/O ports
- Serial ports
- A hardware timer
- A clock generator

software-programmable wait-state generator

Software-programmable wait-state generators can be used to extend external bus cycles up to seven machine cycles to interface with slower off-chip memory and I/O devices. The software wait-state generators are incorporated without any external hardware. For off-chip memory access, a number of wait states can be specified for every 32K-word block of program and data memory space, and for one 64K-word block of I/O space within the software wait-state (SWWSR) register.

programmable bank switching

Programmable bank switching can be used to insert one cycle automatically when crossing memory-bank boundaries inside program memory or data memory space. One cycle also can be inserted when crossing from program-memory space to data-memory space. This extra cycle allows memory devices to release the bus before other devices start driving the bus; thus avoiding bus contention. The size of memory bank for the bank switching is defined by the bank switching control register (BSCR).

parallel I/O ports

Each 'C54x/'LC54x/'VC54x device has a total of 64K-I/O ports. These ports can be addressed by the PORTR instruction or the PORTW instruction. The $\overline{IS}$ signal indicates a read/write operation through an I/O port. The 'C54x/'LC54x/'VC54x devices can interface easily with external devices through the I/O ports while requiring minimal off-chip address decoding circuits.

host-port interface ('C542, 'LC542, 'VC542, 'LC545, and 'VC545 only)

The host-port interface is an 8-bit parallel port used to interface a host processor to the DSP device. Information is exchanged between the DSP device and the host processor through on-chip memory that is accessible by both the host and the DSP device. The DSP devices have access to the HPI control (HPIC) register and the host can address the HPI memory through the HPI address register (HPIA). HPI memory is a 2K 16-bit DARAM block which can also be used as general-purpose on-chip data or program DARAM.

Data transfers of 16-bit words occur as two consecutive bytes with a dedicated pin (HBIL) indicating whether the high or low byte is being transmitted. Two control pins, HCNTL1 and HCNTL0, control host access to the HPIA, HPI data (with an optional automatic address increment), or the HPIC. The host can interrupt the DSP device by writing to HPIC. The DSP device can interrupt the host with a dedicated $\overline{HINT}$ pin that the host can acknowledge and clear.

The HPI has two modes of operation, shared-access mode (SAM) and host-only mode (HOM). In SAM, the normal mode of operation, both the DSP device and the host can access HPI memory. In this mode, asynchronous host accesses are resynchronized internally and, in case of conflict, the host has access priority and the DSP device waits one cycle. The HOM capability allows the host to access HPI memory while the DSP device is in IDLE2 (all internal clocks stopped) or in reset mode. The host can therefore access the HPI RAM while the DSP device is in its optimal configuration in terms of power consumption.

host port interface ('C542, 'LC542, 'VC542, 'LC545, and 'VC545 only) (continued)

The HPI control register has two data strobes, $\overline{\text{HDS1}}$ and $\overline{\text{HDS2}}$, a read/write strobe HR/$\overline{\text{W}}$, and an address strobe $\overline{\text{HAS}}$, to enable a glueless interface to a variety of industry-standard host devices. The HPI is interfaced easily to hosts with multiplexed address/data bus, separate address and data buses, one data strobe, and a read/write strobe, or two separate strobes for read and write.

The HPI supports high-speed back-to-back accesses. In the shared-access mode, it can handle one byte every five DSP device periods, that is, 64 Mb/s with a 40-MIPS DSP. The HPI is designed so that the host can take advantage of this high bandwidth and run at frequencies up to $(f \times n) \div 5$, where n is the number of host cycles for an external access and f is the DSP device frequency. In host-only mode, the HPI supports even higher speed back-to-back host accesses: 1 byte every 50 ns, that is, 160 Mb/s, independently of the DSP device-clock rate.

serial ports

The 'C54x/'LC54x/'VC54x devices provide high-speed full-duplex serial ports that allow direct interface to other 'C54x/'LC54x/'VC54x devices, codecs, and other devices in a system. There is a general-purpose serial port, a time-division-multiplexed (TDM) serial port, and an auto-buffered serial port (BSP).

The general-purpose serial port utilizes two memory-mapped registers for data transfer: the data transmit register (DXR) and the data receive register (DRR). Both of these registers can be accessed in the same manner as any other memory location. The transmit and receive sections of the serial port each have associated clocks, frame-synchronization pulses, and serial-shift registers, and serial data can be transferred either in bytes or in 16-bit words. Serial port receive and transmit operations can generate their own maskable transmit and receive interrupts (XINT and RINT), allowing serial-port transfers to be managed through software. The 'C54x/'LC54x/'VC54x serial ports are double buffered and fully static.

The TDM port allows the device to communicate through time-division multiplexing with up to seven other 'C54x/'LC54x/'VC54x devices with TDM ports. Time-division multiplexing is the division of time intervals into a number of subintervals with each subinterval representing a prespecified communications channel. The TDM port serially transmits 16-bit words on a single data line (TDAT) and destination addresses on a single address line (TADD). Each device can transmit data on a single channel and receive data from one or more of the eight channels providing a simple and efficient interface for multiprocessing applications. A frame synchronization pulse occurs once every 128 clock cycles corresponding to transmission of one 16-bit word on each of the eight channels. Like the general-purpose serial port, the TDM port is double buffered on both input and output data. The TDM port can also be configured in software to operate as a general-purpose serial port as described above. Both types of ports described above are capable of operating at up to one-fourth the machine cycle rate (CLKOUT).

The buffered-serial port (BSP) consists of a full-duplex double-buffered serial-port interface (SPI) and an auto-buffering unit (ABU). The SPI block of the BSP is an enhanced version of the general-purpose serial port. The auto-buffering unit allows the SPI to read/write directly to 'C54x/'LC54x/'VC54x internal memory using a dedicated bus independently of the CPU. This results in minimal overhead for SPI transactions and faster data rates.

When auto-buffering capability is disabled (standard mode), transfers with SPI are performed under software control through interrupts. In this mode, the ABU is transparent and the word-based interrupts (WXINT and WRINT) provided by the SPI are sent to the CPU as transmit interrupt (XINT) and receive interrupt (RINT). When auto buffering is enabled, word transfers are done directly between the SPI and the 'C54x/'LC54x/'VC54x internal memory using ABU-embedded address generators.

serial ports (continued)

The ABU has its own set of circular-addressing registers with corresponding address-generation units. Memory for the buffers resides in 2K words of 'C54x/'LC54x/'VC54x internal memory. The length and starting addresses of the buffers are user programmable. A buffer-empty/-full interrupt can be posted to the CPU. Buffering is easily halted by an auto-disabling capability. Auto-buffering capability can be enabled separately for transmit and receive sections. When auto buffering is disabled, operation is similar to the general-purpose serial port.

The SPI allows transfer of 8-, 10-, 12-, or 16-bit data packets. In burst mode, data packets are directed by a frame synchronization pulse for every packet. In continuous mode, the frame synchronization pulse occurs when the data transmission is initiated and no further pulses occur. The frame and clock strobes are frequency and polarity programmable. The SPI is fully static and operates at arbitrarily low clock frequencies. The maximum operating frequency is CLKOUT (40 Mb/s at 25 ns).

Table 3 provides a comparison of the serial ports available in the 'C54x/'LC54x/'VC54x generation.

Table 3. Serial Port Configurations for the 'C54x/'LC54x/'VC54x

DEVICE	GENERAL-PURPOSE SERIAL PORT	BUFFERED SERIAL PORT	TDM SERIAL PORT
TMS320C541	2		
TMS320LC541	2		
TMS320VC541	2		
TMS320C542		1	1
TMS320LC542		1	1
TMS320VC542		1	1
TMS320LC543		1	1
TMS320VC543		1	1
TMS320LC544	2		
TMS320VC544	2		
TMS320LC545	1	1	
TMS320VC545	1	1	
TMS320LC546	1	1	
TMS320VC546	1	1	

hardware timer

The 'C54x/'LC54x/'VC54x devices feature a 16-bit timing circuit with a four-bit prescaler. The timer counter is decremented by one at every CLKOUT cycle. Each time the counter decrements to zero, a timer interrupt is generated. The timer can be stopped, restarted, reset, or disabled by specific status bits.

clock generator

The clock generator consists of an internal oscillator and a phase-locked loop (PLL) circuit. The clock generator can be driven internally by connecting a crystal resonator circuit, or driven by an external clock source. The PLL circuit can generate an internal CPU clock by multiplying the clock source frequency by a specific factor. Therefore, you can use a clock source with a lower frequency than that of the CPU.

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memory-mapped registers

All 'C54x/'LC54x/'VC54x devices have 26 memory-mapped CPU registers, which are mapped in data memory space address 0h to 1Fh. Each of these devices also has a set of memory-mapped registers associated with peripherals. Table 4 gives a list of CPU memory-mapped registers (MMR) common to all 'C54x/'LC54x/'VC54x devices. Table 5 shows additional peripheral MMRs associated with the 'C541/'LC541/'VC541/'LC544/'VC544 devices. Table 6 shows additional peripheral MMRs associated with the 'LC545/'VC545/'LC546/'VC546 devices. Table 7 shows additional peripheral MMRs associated with the 'C542/'LC542/'VC542/'LC543/'VC543 devices.

Table 4. Core Processor Memory-Mapped Registers

NAME	ADDRESS		DESCRIPTION
	Dec	Hex	
IMR	0	0	Interrupt mask register
IFR	1	1	Interrupt flag register
–	2–5	2–5	Reserved for testing
ST0	6	6	Status register 0
ST1	7	7	Status register 1
AL	8	8	Accumulator A low word (15–0)
AH	9	9	Accumulator A high word (31–16)
AG	10	A	Accumulator A guard bits (39–32)
BL	11	B	Accumulator B low word (15–0)
BH	12	C	Accumulator B high word (31–16)
BG	13	D	Accumulator B guard bits (39–32)
TREG	14	E	Temporary register
TRN	15	F	Transition register
AR0	16	10	Auxiliary register 0
AR1	17	11	Auxiliary register 1
AR2	18	12	Auxiliary register 2
AR3	19	13	Auxiliary register 3
AR4	20	14	Auxiliary register 4
AR5	21	15	Auxiliary register 5
AR6	22	16	Auxiliary register 6
AR7	23	17	Auxiliary register 7
SP	24	18	Stack pointer register
BK	25	19	Circular buffer size register
BRC	26	1A	Block repeat Counter
RSA	27	1B	Block repeat start address
REA	28	1C	Block repeat end address
PMST	29	1D	Processor mode status (PMST) register
–	30–31	1E–1F	Reserved

Table 5. Peripheral Memory-Mapped Registers ('C541, 'LC541, 'VC541, 'LC544 and 'VC544 Only)

NAME	ADDRESS		DESCRIPTION
	Dec	Hex	
DRR0	32	20	Serial port 0 data receive register
DXR0	33	21	Serial port 0 data transmit register
SPC0	34	22	Serial port 0 control register
—	35	23	Reserved
TIM	36	24	Timer register
PRD	37	25	Timer period register
TCR	38	26	Timer control register
—	39	27	Reserved
SWWSR	40	28	S/W wait-state register
BSCR	41	29	Bank switching control register
—	42–47	2A–2F	Reserved
DRR1	48	30	Serial port 1 data receive register
DXR1	49	31	Serial port 1 transmit register
SPC1	50	32	Serial port 1 control register
—	51	33	Reserved
—	52–95	34–5F	Reserved

Table 6. Peripheral Memory-Mapped Registers ('LC545, 'VC545, 'LC546 and 'VC546 Only)

NAME	ADDRESS		DESCRIPTION	TYPE
	Dec	Hex		
DRR	32	20	Data receive register	BSP
DXR	33	21	Data transmit register	BSP
SPC	34	22	Serial port control register	BSP
SPCE	35	23	BSP control extension register	BSP
TIM	36	24	Timer register	Timer
PRD	37	25	Timer period counter	Timer
TCR	38	26	Timer control register	Timer
—	39	27	Reserved	
SWWSR	40	28	S/W wait-state register	External bus
BSCR	41	29	Bank switching control register	External bus
—	42 – 43	2A – 2B	Reserved	
HPIC	44	2C	HPI control register	HPI†
—	45 – 47	2D – 2F	Reserved	
DRR1	48	30	Data receive register	Serial port
DXR1	49	31	Transmit register	Serial port
SPC1	50	32	Serial port control register	Serial port
—	51 – 55	33 – 37	Reserved	
AXR	56	38	ABU‡ transmit address register	BSP
BKX	57	39	ABU‡ transmit buffer size register	BSP
ARR	58	3A	ABU‡ receive address register	BSP
BKR	59	3B	ABU‡ receive buffer size register	BSP

† Host port interface (HPI) on 'LC545, 'VC545, only
‡ Auto-buffering unit (ABU)

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Table 7. Peripheral Memory-Mapped Registers ('C542, 'LC542, 'VC542, 'LC543 and 'VC543 Only)

NAME	ADDRESS		DESCRIPTION	TYPE
	Dec	Hex		
DRR	32	20	Data receive register	BSP
DXR	33	21	Data transmit register	BSP
SPC	34	22	Serial port control register	BSP
SPCE	35	23	BSP control extension register	BSP
TIM	36	24	Timer register	Timer
PRD	37	25	Timer period counter	Timer
TCR	38	26	Timer control register	Timer
—	39	27	Reserved	
SWWSR	40	28	S/W wait-state register	External bus
BSCR	41	29	Bank switching control register	External bus
—	42 – 43	2A – 2B	Reserved	
HPIC	44	2C	HPI control register	HPI†
—	45 – 47	2D – 2F	Reserved	
TRCV	48	30	Data receive register	TDM
TDXR	49	31	Transmit register	TDM
TSPC	50	32	Serial port control register	TDM
TCSR	51	33	Channel select register	TDM
TRTA	52	34	Receive/transmit register	TDM
TRAD	53	35	Receive address register	TDM
—	54 – 55	36 – 37	Reserved	
AXR	56	38	ABU‡ transmit address register	BSP
BKX	57	39	ABU‡ transmit buffer size register	BSP
ARR	58	3A	ABU‡ receive address register	BSP
BKR	59	3B	ABU‡ receive buffer size register	BSP

† Host port interface (HPI) on 'LC545, 'VC545, only
‡ Auto-buffering unit (ABU)

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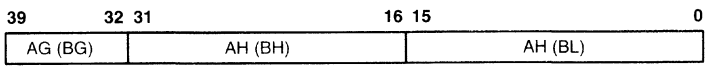
status register (ST0, ST1)

The status registers, ST0 and ST1, contain the status of the various conditions and modes for the 'C54x/'LC54x/'VC54x devices. ST0 contains the flags (OV, C, and TC) produced by arithmetic operations and bit manipulations in addition to the DP and the ARP fields. ST1 contains the various modes and instructions that the processor operates on and executes.

accumulators (AL, AH, AG, and BL, BH, BG)

The 'C54x/'LC54x/'VC54x devices have two 40-bit accumulators; accumulator A and accumulator B. Each accumulator is memory-mapped and partitioned into accumulator low word (AL, BL), accumulator high word (AH, BH), and accumulator guard bits (AG, BG).



auxiliary registers (AR0–AR7)

The eight 16-bit auxiliary registers (AR0–AR7) can be accessed by the CALU and modified by the auxiliary register arithmetic units (ARAUs). The primary function of the auxiliary registers is generating 16-bit addresses for data space. However, these registers also can act as general-purpose registers or counters.

temporary register (TREG)

The TREG is used to hold one of the multiplicands for multiply and multiply/accumulate instructions. It can hold a dynamic (execution-time programmable) shift count for instructions with shift operation such as ADD, LD, and SUB instructions. It also can hold a dynamic bit address for the BITT instruction. The EXP instruction stores the exponent value computed onto the TREG, while the NORM instruction uses the TREG value to normalize the number. For ACS operation of Viterbi decoding, TREG holds branch metrics used by the DADST and DSADT instructions.

transition register (TRN)

The TRN is a 16-bit register that is used to hold the transition decision for the path to new metrics to perform the Viterbi algorithm. The CMPS (compare, select, max, and store) instruction updates the contents of the TRN based on the comparison between the accumulator high word and the accumulator low word.

stack-pointer register (SP)

The SP is a 16-bit register that contains the address at the top of the system. The SP always points to the last element pushed onto the stack. The stack is manipulated by interrupts, traps, calls, returns, and the PUSHD, PSHM, POPD, and POPM instructions. Pushes and pops of the stack predecrement and postincrement, respectively, all 16 bits of the SP.

circular-buffer-size register (BK)

The 16-bit BK is used by the ARAUs in circular addressing to specify the data block size.

block repeat registers (BRC, RSA, REA)

The block-repeat counter (BRC) is a 16-bit register used to specify the number of times a block of code is to be repeated when performing a block repeat. The block-repeat start address (RSA) is a 16-bit register containing the starting address of the block of program memory to be repeated when operating in the repeat mode. The 16-bit block repeat-end address (REA) contains the ending address if the block of program memory is to be repeated when operating in the repeat mode.

interrupt registers (IMR, IFR)

The interrupt-mask register (IMR) is used to mask off specific interrupts individually at required times. The interrupt-flag register (IFR) indicates the current status of the interrupts.

processor mode status register (PMST)

The processor-mode status register (PMST) controls memory configurations of the 'C54x/'LC54x/'VC54x devices.

electrical characteristics and operating conditions ('C541, 'C542)

absolute maximum ratings over specified temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} ‡ ..... –0.3 V to 7 V
Input voltage range ..... –0.3 V to 7 V
Output voltage range ..... –0.3 V to 7 V
Operating case temperature range, T_C ..... –40°C to 100°C
Storage temperature range, T_{stg} ..... –55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.75	5	5.25	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	$\overline{RS}$, $\overline{INT}$n, $\overline{NMI}$,CNT,CLKMDn X2/CLKIN	3		V_{DD} + 0.3	V
		All other inputs	2		V_{DD} + 0.3	
V_{IL}	Low-level input voltage		–0.3		0.8	V
I_{OH}	High-level output current				–300	µA
I_{OL}	Low-level output current				2	mA
T_C	Operating case temperature		–40		100	°C

Refer to Figure 7 for 5-V device test load circuit values.

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electrical characteristics and operating conditions ('C541, 'C542) (continued)

electrical characteristics over recommended operating case temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage ‡		I_{OH} = –300 µA	2.4			V
V_{OL}	Low-level output voltage ‡		I_{OL} = 2 mA			0.6	V
I_{IZ}	Input current in high impedance		V_{DD} = 5.25 V, V_O = V_{SS} to V_{DD}	–20		20	µA
I_I	Input current (V_I = V_{SS} to V_{DD})	$\overline{TRST}$	With internal pulldown	–10		800	µA
		TMS, TCK, TDI	With internal pullups	–500		10	
		D[15:0]	Bus holders enabled, V_{DD} = Nom, V_I = V_{IL} Max			75	
			Bus holders enabled, V_{DD} = Nom, V_I = V_{IH} Min	–75			
		All other input-only pins		–10		10	
I_{DDC}	Supply current, core CPU		V_{DD} = 5 V, f_x = 40 MHz,§ T_A = 25°C		120¶		mA
I_{DDP}	Supply current, pins		V_{DD} = 5 V, f_x = 40 MHz,§ T_A = 25°C				mA
I_{DD}	Supply current, standby	IDLE2	PLL x 1 mode, 40 MHz input		4		mA
		IDLE3			5		µA
C_i	Input capacitance				10		pF
C_o	Output capacitance				10		pF

† All typical values are at V_{DD} = 5 V, T_A = 25°C.
‡ All input and output voltage levels except $\overline{RS}$, $\overline{INT0}$–$\overline{INT3}$, $\overline{NMI}$, CNT, X2/CLKIN, CLKMD0–CLKMD3 are TTL-compatible.
§ Clock mode: PLLx1 with external source
¶ This value was obtained with 50% usage of MAC and 50% usage of NOP instructions. Actual operating current varies with program being executed.

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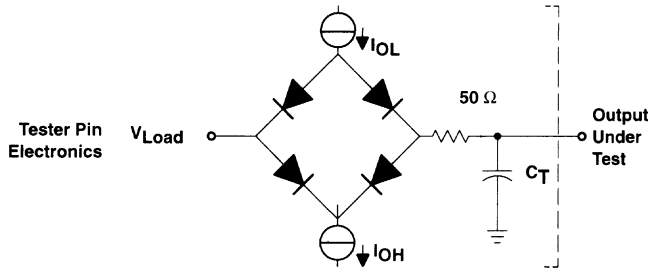
PARAMETER MEASUREMENT INFORMATION



Where: I_{OL} = 2 mA (all outputs)
I_{OH} = 300 μA (all outputs)
V_{Load} = 1.5 V
C_T = 40 pF typical load circuit capacitance.

Figure 7. 5-V Test Load Circuit

signal transition levels

TTL-level outputs are driven to a minimum logic-high level of 2.4 V and to a maximum logic-low level of 0.6 V. Output transition times are specified as follows.

For a high-to-low transition on a TTL-compatible output signal, the level at which the output is said to be no longer high is 2 V and the level at which the output is said to be low is 1 V. For a low-to-high transition, the level at which the output is said to be no longer low is 1 V and the level at which the output is said to be high is 2 V.

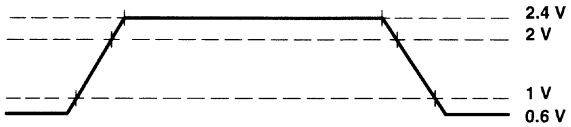


Figure 8. TTL-Level Outputs (5-V Devices)

Transition times for TTL-compatible inputs are specified as follows. For a high-to-low transition on an input signal, the level at which the input is said to be no longer high is 1.88 V and the level at which the input is said to be low is 0.92 V. For a low-to-high transition on an input signal, the level at which the input is said to be no longer low is 0.92 V and the level at which the input is said to be high is 1.88 V.

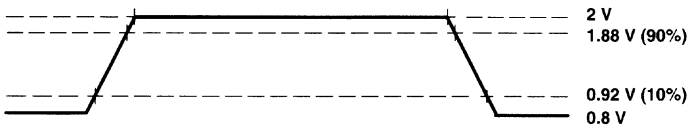


Figure 9. TTL-Level Inputs (5-V Devices)

electrical characteristics and operating conditions ('LC54x and 'VC54x only)

absolute maximum ratings over specified temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} ‡ . . . . . –0.3 V to 4.6 V
Input voltage range . . . . . –0.3 V to 4.6 V
Output voltage range . . . . . –0.3 V to 4.6 V
Operating case temperature range, T_C . . . . . –40°C to 100°C
Storage temperature range, T_{stg} . . . . . –55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	'LC54x	3	3.3	3.6	V
		'VC54x	2.7	3.0	3.3	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	$\overline{RS}$,$\overline{INT}$n,$\overline{NMI}$,CNT, X2/CLKIN, CLKMDn, V_{DD} = 3.3 ± 0.3 V	2.5		V_{DD} + 0.3	V
		$\overline{RS}$,$\overline{INT}$n,$\overline{NMI}$,CNT, X2/CLKIN, CLKMDn, V_{DD} = 2.7 V	2.2		V_{DD} + 0.3	
		All other inputs	2		V_{DD} + 0.3	
V_{IL}	Low-level input voltage		–0.3		0.8	V
I_{OH}	High-level output current				–300	µA
I_{OL}	Low-level output current				+1.5	mA
T_C	Operating case temperature		–40		100	°C

Refer to Figure 10 for 3.3-V and 2.7-V device test load circuit values.

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electrical characteristics and operating conditions ('LC54x and 'VC54x only) (continued)

electrical characteristics over recommended operating case temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage ‡		V_{DD} = 3.3 ± 0.3 V, I_{OH} = MAX	2.4			V
			V_{DD} = 2.7 V, I_{OH} = MAX	2.2			V
V_{OL}	Low-level output voltage ‡		I_{OL} = MAX			0.4	V
I_{IZ}	Input current in high impedance		V_{DD} = MAX, V_O = V_{SS} to V_{DD}	–10		10	µA
I_I	Input current (V_I = V_{SS} to V_{DD})	$\overline{TRST}$	With internal pulldown	–10		800	µA
		TMS, TCK, TDI	With internal pullups	–400		10	
		D[15:0]	Bus holders enabled, V_{DD} = Nom, V_I = V_{IL} Max			75	
			Bus holders enabled, V_{DD} = Nom, V_I = V_{IH} Min	–75			
		All other input-only pins		–10		10	
I_{DDC}	Supply current, core CPU		V_{DD} = 3.0 V, f_x = 40 MHz,§ T_A = 25°C		64¶		mA
I_{DDP}	Supply current, pins		V_{DD} = 3.0 V, f_x = 40 MHz,§ T_A = 25°C				mA
I_{DD}	Supply current, standby	IDLE2	PLL x 1 mode, 40 MHz input		2		mA
		IDLE3			5		µA
C_i	Input capacitance				10		pF
C_o	Output capacitance				10		pF

† All typical values are at V_{DD} = 3.3 V, T_A = 25°C.
‡ All input and output voltage levels except $\overline{RS}$, $\overline{INT0}$–$\overline{INT3}$, $\overline{NMI}$, CNT, X2/CLKIN, CLKMD0–CLKMD3 are LVTTL-compatible.
§ Clock mode: PLLx1 with external source
¶ This value was obtained with 50% usage of MAC and 50% usage of NOP instructions. Actual operating current varies with program being executed.

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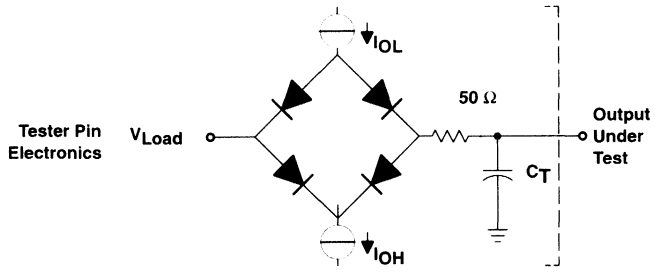

Where: I_{OL} = 1.5 mA (all outputs)
I_{OH} = 300 μA (all outputs)
V_{Load} = 1.5 V
C_T = 40 pF typical load circuit capacitance.

Figure 10. 3.3-V/2.7-V Test Load Circuit

signal transition levels

LVTTL-level outputs are driven to a minimum logic-high level of 2.4/2.2 V ('LC54x/'VC54x) and to a maximum logic-low level of 0.4 V. Output transition times are specified as follows.

For a high-to-low transition on a LVTTL-compatible output signal, the level at which the output is said to be no longer high is 2 V ('LC device) or 1.8 V ('VC device), and the level at which the output is said to be low is 0.8 V. For a low-to-high transition, the level at which the output is said to be no longer low is 0.8 V, and the level at which the output is said to be high is 2 V ('LC device) or 1.8 V ('VC device).

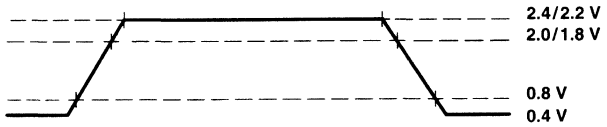

Figure 11. TTL-Level Outputs (3.3-V/2.7-V Devices)

LVTTL-compatible input transitions are specified as follows. For a high-to-low transition on an input signal, the level at which the input is said to be no longer high is 1.88 V and the level at which the input is said to be low is 0.92 V. For a low-to-high transition on an input signal, the level at which the input is said to be no longer low is 0.92 V and the level at which the input is said to be high is 1.88 V.

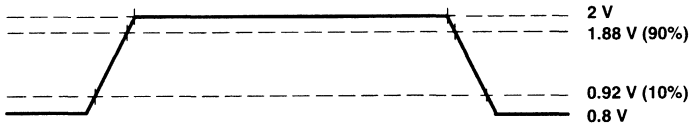

Figure 12. TTL-Level Inputs (3.3-V/2.7-V Devices)

ADVANCE INFORMATION

CLOCK CHARACTERISTICS AND TIMING

The 'C54x, 'LC54x and 'VC54x can use either an internal oscillator or an external frequency source for a clock. The clock mode is determined by the CLKMD1, CLKMD2 and CLKMD3 clock mode pins. Table 8 outlines the selection of the clock mode by these pins.

Table 8. Clock Mode Configurations

MODE-SELECT PINS			CLOCK MODE	
CLKMD1	CLKMD2	CLKMD3	OPTION†	OPTION 2†
0	0	0	PLL × 3 with external source	PLL × 5 with external source
1	1	0	PLL × 2 with extenal source	PLL × 4 with external source
1	0	0	PLL × 3 with internal source	PLL × 5 with internal source
0	1	0	PLL × 1.5 with external source	PLL × 4.5 with external source
0	0	1	Divide-by-two with external source	Divide-by-two with external source
0	1	1	Stop mode‡	Stop mode‡
1	0	1	PLL × 1 with external source	PLL × 1 with external source
1	1	1	Divide-by-two with internal source	Divide-by-two with internal source

† Option: Option 1 or option 2 can be selected when ordering the device.
‡ Stop mode: The function of the stop mode is equivalent to that of the power-down mode of IDLE3. The IDLE3 instruction is recommended, rather than the stop mode, to realize full power saving.

internal divide-by-two clock option with external crystal

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN. The frequency of CLKOUT is one-half the cystal's oscillating frequency. The crystal should be either fundamental or overtone operation, and parallel resonant, with an effective series resistance of 30 Ω and power dissipation of 1 mW; it should be specified at a load capacitance of 20 pF.

recommended operating conditions

	'C54x-40 'LC54x-40/'VC54x-40			'LC54x-50 'VC54x-50			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
f_X Input clock frequency	0§		80	0§		100	MHz
C1, C2		10			10		pF

§ This device utilizes a fully static design and therefore can operate with $t_{c(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz but is tested at a minimum of 3.3 MHz to meet device test time requirement.

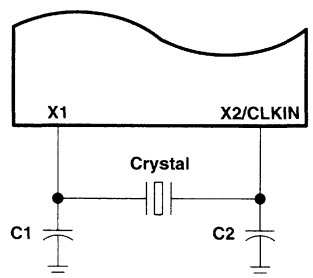

Figure 13. Internal Clock Option

external divide-by-two clock option

An external frequency source can be used by injecting the frequency directly into X2/CLKIN with X1 left unconnected, CLKMD1 and CLKMD2 set low, and CLKMD3 set high. This external frequency is divided by two to generate the internal machine cycle.

The external frequency injected must conform to specifications listed in the timing requirements table.

switching characteristics over recommended operating conditions [H = $0.5t_{c(CO)}$]

PARAMETER		'C54x-40 'LC54x-40/'VC54x-40			'LC54x-50 'VC54x-50			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	UNIT
$t_{c(CO)}$	Cycle time, CLKOUT	25	$2t_{c(CI)}$	†	20	$2t_{c(CI)}$	†	ns
$t_{d(CIH-CO)}$	Delay time, X2/CLKIN high to CLKOUT high/low	6	12	18	6	12	18	ns
$t_{f(CO)}$	Fall time, CLKOUT		2			2		ns
$t_{r(CO)}$	Rise time, CLKOUT		2			2		ns
$t_{w(COL)}$	Pulse duration, CLKOUT low	H–4	H–2	H	H–4	H–2	H	ns
$t_{w(COH)}$	Pulse duration, CLKOUT high	H–4	H–2	H	H–4	H–2	H	ns

† This device utilizes a fully static design and therefore can operate with $t_{c(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz but is tested at a minimum of 3.35 MHz to meet device test time requirements.

timing requirements over recommended operating conditions

		'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX	MIN	MAX	UNIT
$t_{c(CI)}$	Cycle time, X2/CLKIN	12.5	‡	10	‡	ns
$t_{f(CI)}$	Fall time, X2/CLKIN §		4		4	ns
$t_{r(CI)}$	Rise time, X2/CLKIN §		4		4	ns
$t_{w(CIL)}$	Pulse duration, X2/CLKIN low	3	‡	3	‡	ns
$t_{w(CIH)}$	Pulse duration, X2/CLKIN high	3	‡	3	‡	ns

‡ This device utilizes a fully static design and therefore can operate with $t_{c(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz but is tested at a minimum of 6.7 MHz to meet device test time requirements.

§ Values derived from characterization data and not tested.

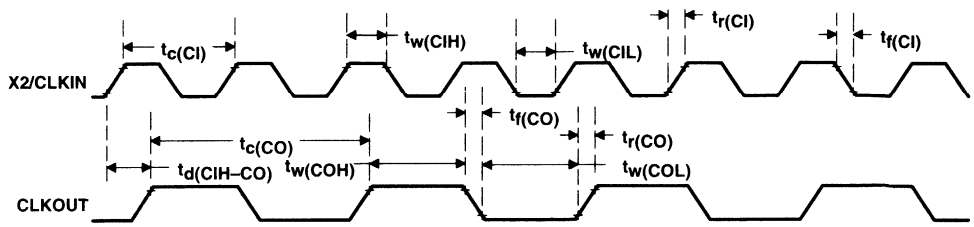

Figure 14. External Divide-by-Two Clock Timing

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external multiply-by-N clock option

An external frequency can be used by injecting the frequency directly into X2/CLKIN, with X1 left unconnected, CLKMD1, CLKMD2, and CLKMD3 set according to the clock mode configuration table (Table 8). This external frequency is multiplied by N to generate the internal machine cycle.

The external frequency injected must conform to specifications listed in the timing requirements table.

switching characteristics over recommended operating conditions [H = $0.5t_{c(CO)}$]

PARAMETER			'C54x-40 'LC54x-40/'VC54x-40			'LC54x-50 'VC54x-50			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(CO)}$	Cycle time, CLKOUT		25	$t_{c(CI)}/N$		20	$t_{c(CI)}/N$		ns
$t_{d(CIH-CO)}$	Delay time, X2/CLKIN low to CLKOUT high	N=1, 2, 3, 4, 5, 9	6	12	18	6	12	18	ns
$t_{d(CIH-CO)}$	Delay time, X2/CLKIN high to CLKOUT high/low	N=1. 5, 2.5, 4.5	6	12	18	6	12	18	ns
$t_{f(CO)}$	Fall time, CLKOUT			2			2		ns
$t_{r(CO)}$	Rise time, CLKOUT			2			2		ns
$t_{w(COL)}$	Pulse duration, CLKOUT low		H–4	H–2	H	H–4	H–2	H	ns
$t_{w(COH)}$	Pulse duration, CLKOUT high		H–4	H–2	H	H–4	H–2	H	ns
t_p	PLL lock-up time				50†			50†	µs

† Values derived from characterization data and not tested.

timing requirements over recommended operating conditions

			'C54x-40 'LC54x-40/'VC54x-40		'LC54x-50 'VC54x-50		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(CI)}$	Cycle time, X2/CLKIN	N=1, 2, 3, 4, 5, 9	25N	200N	20N	200N	ns
		N=1. 5, 2.5, 4.5	25N	100N	20N	100N	
$t_{f(CI)}$	Fall time, X2/CLKIN †			4		4	ns
$t_{r(CI)}$	Rise time, X2/CLKIN †			4		4	ns
$t_{w(CIL)}$	Pulse duration, X2/CLKIN low		8		6		ns
$t_{w(CIH)}$	Pulse duration, X2/CLKIN high		8		6		ns

† Values derived from characterization data and not tested.

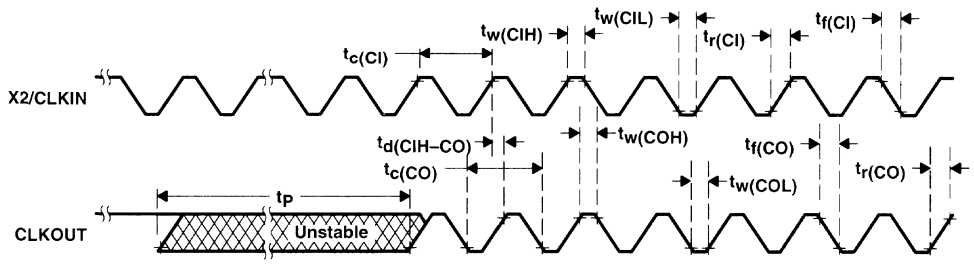

Figure 15. External Multiply-by-One Clock Timing

memory and parallel I/O interface timing

timing parameters for a memory ($\overline{\text{MSTRB}}$ = 0) read [H = 0.5 $t_{c(CO)}$]†‡ (see Figure 16)

		'LC542-40 'VC54x-40 'LC543-40		'C54x-40 'LC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)M}$	Access time, read data access from address valid		2H–12		2H–10		2H–10	ns
$t_{a(MSTRBL)}$	Access time, read data access from MSTRB low		2H–12		2H–10		2H–10	ns
$t_{su(D)R}$	Setup time, read data before CLKOUT low	7		5		5		ns
$t_{d(CLKL-A)}$	Delay time, address valid from CLKOUT low§	0¶	5	0¶	5	0¶	5	ns
$t_{d(CLKH-A)}$	Delay time, address valid from CLKOUT high (transition)#	0¶	5	0¶	5	0¶	5	ns
$t_{d(CLKL-MSL)}$	Delay time, $\overline{\text{MSTRB}}$ low from CLKOUT low	0	5	0	5	0	5	ns
$t_{d(CLKL-MSH)}$	Delay time, $\overline{\text{MSTRB}}$ high from CLKOUT low	– 2	3	– 2	3	– 2	3	ns
$t_{h(CLKL-A)R}$	Hold time, address valid after CLKOUT low	0	5¶	0	5¶	0	5¶	ns
$t_{h(CLKH-A)R}$	Hold time, address valid after CLKOUT high	0	5¶	0	5¶	0	5¶	ns
$t_{h(D)R}$	Hold time, read data time after CLKOUT low	0		0		0		ns
$t_{h(A-D)R}$	Hold time, read data after address invalid	0		0		0		ns

† A15–A0, $\overline{\text{PS}}$, and $\overline{\text{DS}}$ timings are all included in timings referenced as address.
‡ See Figure 20 for address bus timing variation with load capacitance.
§ In the case of a memory read preceded by a memory read
¶ Values derived from characterization data and not tested
# In the case of a memory read preceded by a memory write

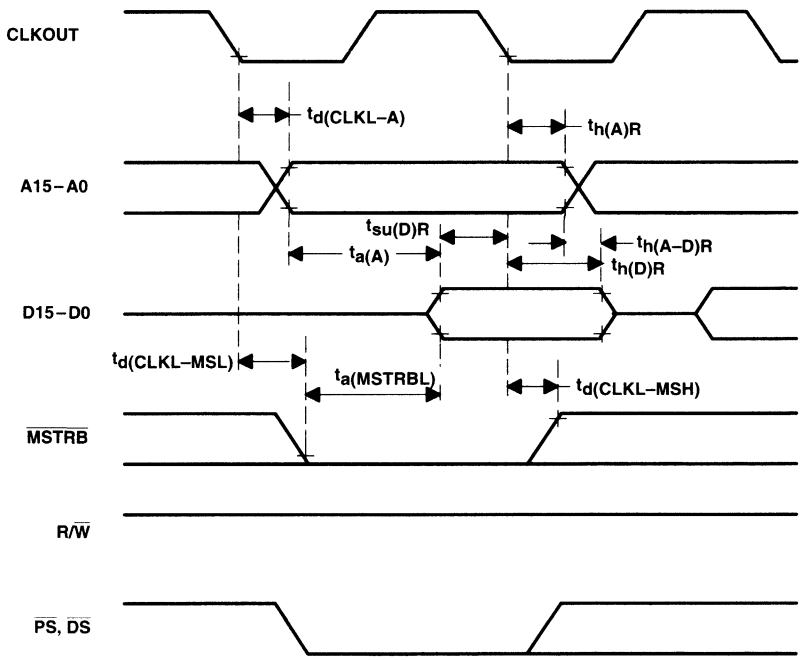

Figure 16. Memory Read ($\overline{\text{MSTRB}}$ = 0)

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memory and parallel I/O interface timing (continued)

timing parameters for a memory ($\overline{\text{MSTRB}}$ = 0) write [H = 0.5 $t_{c(CO)}$]†‡ (see Figure 17)

		'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX	MIN	MAX	
$t_{d(CLKH-A)}$	Delay time, address valid from CLKOUT high§	0¶	5	0¶	5	ns
$t_{d(CLKL-A)}$	Delay time, address valid from CLKOUT low (transition)#	0¶	5	0¶	5	ns
$t_{d(CLKL-MSL)}$	Delay time, $\overline{\text{MSTRB}}$ low from CLKOUT low	0	5	0	5	ns
$t_{d(CLKL-D)W}$	Delay time, data valid from CLKOUT low		10		10	ns
$t_{d(CLKL-MSH)}$	Delay time, $\overline{\text{MSTRB}}$ high from CLKOUT low	–2	3	–2	3	ns
$t_{d(CLKH-RWL)}$	Delay time, R/$\overline{\text{W}}$ low from CLKOUT high	0	5	0	5	ns
$t_{d(CLKH-RWH)}$	Delay time, R/$\overline{\text{W}}$ high from CLKOUT high	– 2	3	– 2	3	ns
$t_{h(A)W}$	Hold time, address valid after CLKOUT high	0	5¶	0	5¶	ns
$t_{h(D)MSH}$	Hold time, write data valid after $\overline{\text{MSTRB}}$ high	H–5	H+5¶	H–5	H+5¶	ns
$t_{w(SL)MS}$	Pulse duration, $\overline{\text{MSTRB}}$ low	2H–5		2H–5		ns
$t_{su(A)W}$	Setup time, address valid before $\overline{\text{MSTRB}}$ low	2H–5		2H–5		ns
$t_{su(D)MSH}$	Setup time, write data valid before $\overline{\text{MSTRB}}$ high	2H–10	2H+10¶	2H–10	2H+10¶	ns

† A15–A0,$\overline{\text{PS}}$, $\overline{\text{DS}}$ timings are all included in timings referenced as address.
‡ See Figure 20 for address bus timing variation with load capacitance.
§ In the case of a memory write preceded by a memory write.
¶ In the case of a memory write preceded by an I/O write.
# Values derived from characterization data and not tested

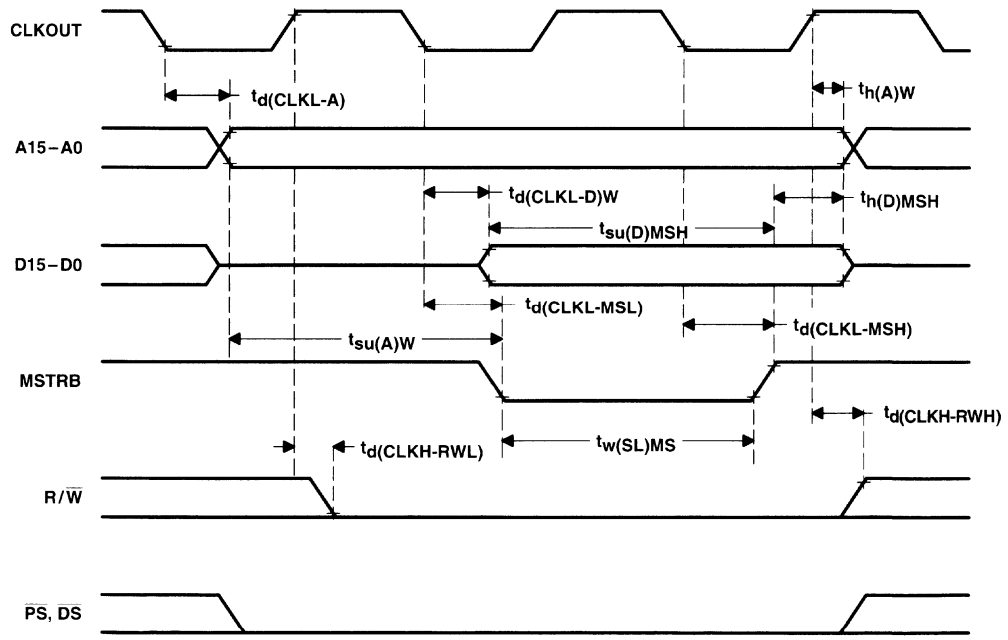

Figure 17. Memory Write ($\overline{\text{MSTRB}}$ = 0)

memory and parallel I/O interface timing (continued)

timing parameters for a parallel I/O port ($\overline{IOSTRB}$ = 0) read [H = 0.5 $t_{c(CO)}$]†‡ (see Figure 18)

		'LC542-40 'VC54x-40 'LC543-40		'C54x-40 'LC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)IO}$	Access time, read data access from address valid		3H–12		3H–10		3H–10	ns
$t_{a(ISTRBL)IO}$	Access time, read data access from $\overline{IOSTRB}$ low		3H–12		3H–10		3H–10	
$t_{su(D)IOR}$	Setup time, read data before CLKOUT high	7		5		5		
$t_{d(CLKL-A)}$	Delay time, address valid from CLKOUT low	0§	5	0§	5	0§	5	
$t_{d(CLKH-ISTRBL)}$	Delay time, $\overline{IOSTRB}$ low from CLKOUT high	0	5	0	5	0	5	
$t_{d(CLKH-ISTRBH)}$	Delay time, $\overline{IOSTRB}$ high from CLKOUT high	– 2	3	– 2	3	– 2	3	
$t_{h(A)IOR}$	Hold time, address after CLKOUT low	0	5§	0	5§	0	5§	
$t_{h(D)IOR}$	Hold time, read data after CLKOUT high	0		0		0		
$t_{h(ISTRBH-D)R}$	Hold time, read data after $\overline{IOSTRB}$ high	0		0		0		

† A15–A0 and $\overline{IS}$ timings are included in timings referenced as address.
‡ See Figure 20 for address bus timing variation with load capacitance.
§ Values derived from characterization data and not tested

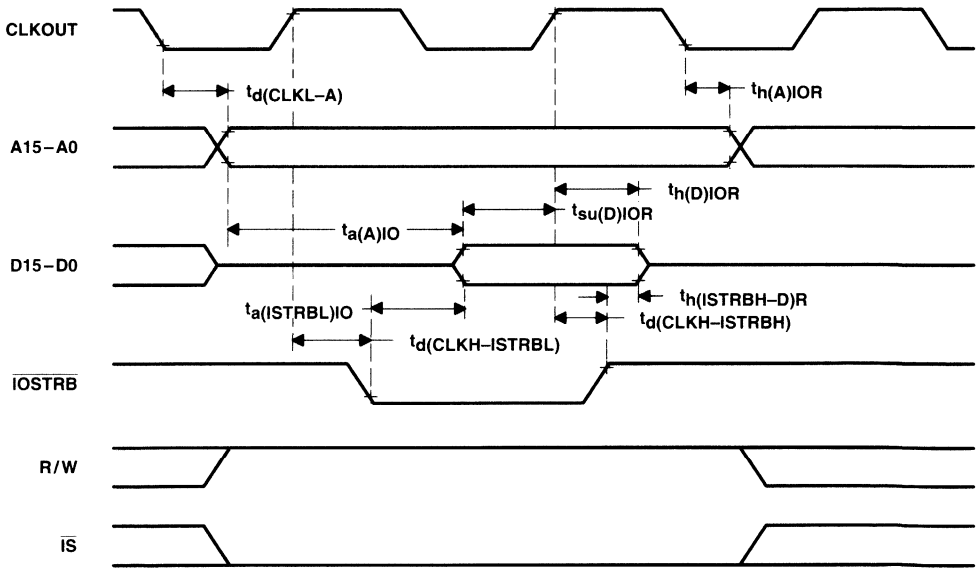

Figure 18. Parallel I/O Port Read ($\overline{IOSTRB}$ = 0)

ADVANCE INFORMATION

memory and parallel I/O interface timing (continued)

timing parameters for a parallel I/O port ($\overline{IOSTRB}$ = 0) write [H = 0.5 $t_{c(CO)}$] (see Figure 19)†

		'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX	MIN	MAX	
$t_{d(CLKL-A)}$	Delay time, address valid from CLKOUT low‡	0§	5	0§	5	ns
$t_{d(CLKH-ISTRBL)}$	Delay time, $\overline{IOSTRB}$ low from CLKOUT high	0	5	0	5	ns
$t_{d(CLKH-D)IOW}$	Delay time, write data valid from CLKOUT high	H–5§	H+10	H–5§	H+10	ns
$t_{d(CLKH-ISTRBH)}$	Delay time, $\overline{IOSTRB}$ high from CLKOUT high	–2	3	–2	3	ns
$t_{d(CLKL-RWL)}$	Delay time, R/$\overline{W}$ low from CLKOUT low	0	5	0	5	ns
$t_{d(CLKL-RWH)}$	Delay time, R/$\overline{W}$ high from CLKOUT low	–2	3	–2	3	ns
$t_{h(A)IOW}$	Hold time, address valid from CLKOUT low‡	0	5§	0	5§	ns
$t_{h(D)IOW}$	Hold time, write data after $\overline{IOSTRB}$ high	H–5	H+5§	H–5	H+5§	ns

† See Figure 20 for address bus timing variation with load capacitance.
‡ A15–A0, and $\overline{IS}$ timings are included in timings referenced as address.
§ Values derived from characterization data and not tested

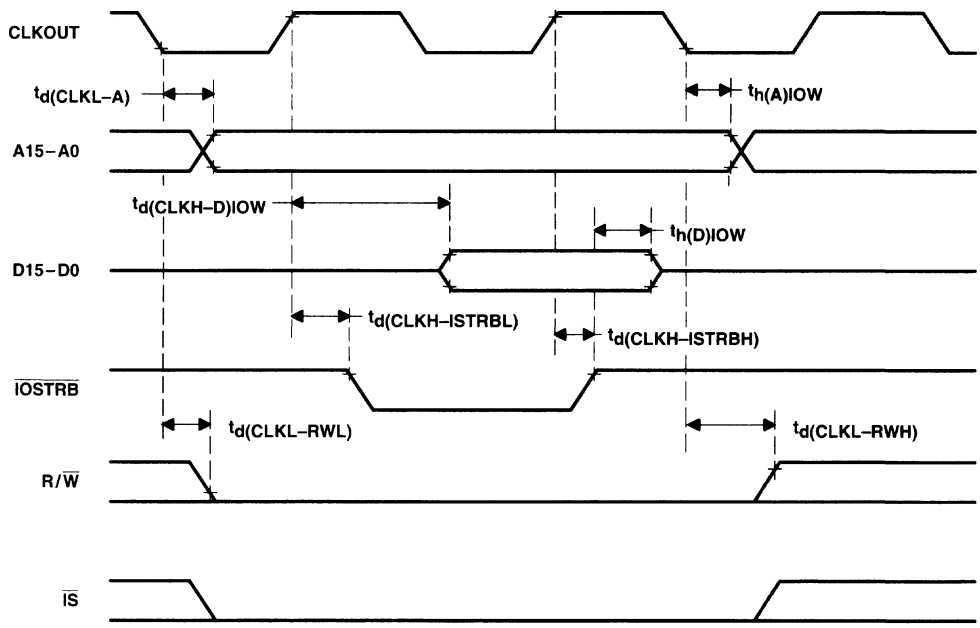

Figure 19. Parallel I/O Port Write ($\overline{IOSTRB}$ = 0)

ADVANCE INFORMATION

memory and parallel I/O interface timing (continued)

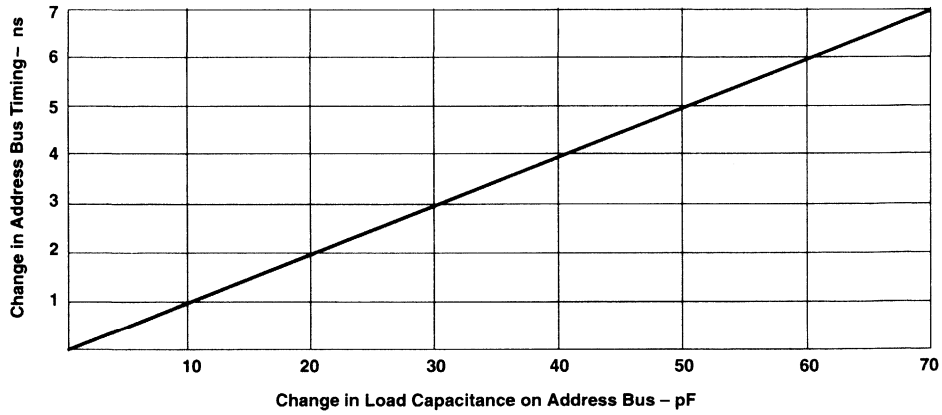

Figure 20. Address Bus Timing Variation with Load Capacitance

ready timing for externally generated wait states

timing parameters for externally generated wait states [H = 0.5 $t_{c(CO)}$]†

		'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX	MIN	MAX	
$t_{su(RDY)}$	Setup time, READY before CLKOUT low	10		8		ns
$t_{h(RDY)}$	Hold time, READY after CLKOUT low	0		0		ns
$t_{v(RDY)MSTRB}$	Valid time, READY after $\overline{MSTRB}$ low		4H–15		4H–15	ns
$t_{h(RDY)MSTRB}$	Hold time, READY after $\overline{MSTRB}$ low	4H		4H		ns
$t_{v(RDY)IOSTRB}$	Valid time, READY after $\overline{IOSTRB}$ low		5H–15		5H–15	ns
$t_{h(RDY)IOSTRB}$	Hold time, READY after $\overline{IOSTRB}$ low	5H		5H		ns
$t_{v(MSCL)}$	Valid time, $\overline{MSC}$ low after CLKOUT low	0	5	0	5	ns
$t_{v(MSCH)}$	Valid time, $\overline{MSC}$ high after CLKOUT low	–2	3	–2	3	ns

† The hardware wait states can be used only in conjunction with the software wait states to extend the bus cycles. To generate wait states by READY, at least two software wait states must be programmed. READY is not sampled until the completion of the software wait states.

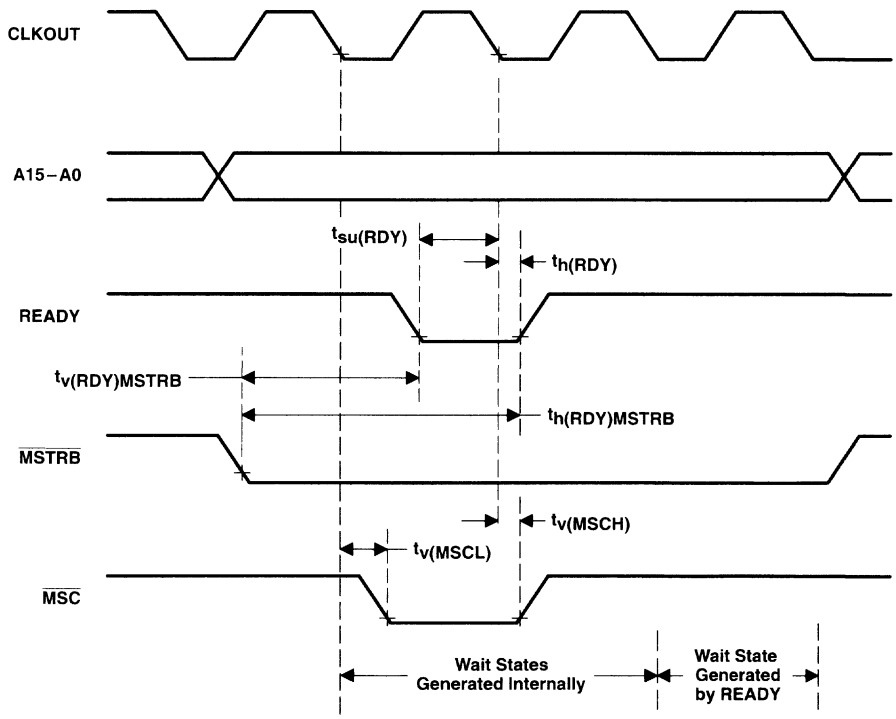

Figure 21. Memory Read With Externally Generated Wait States

ready timing for externally generated wait states (continued)

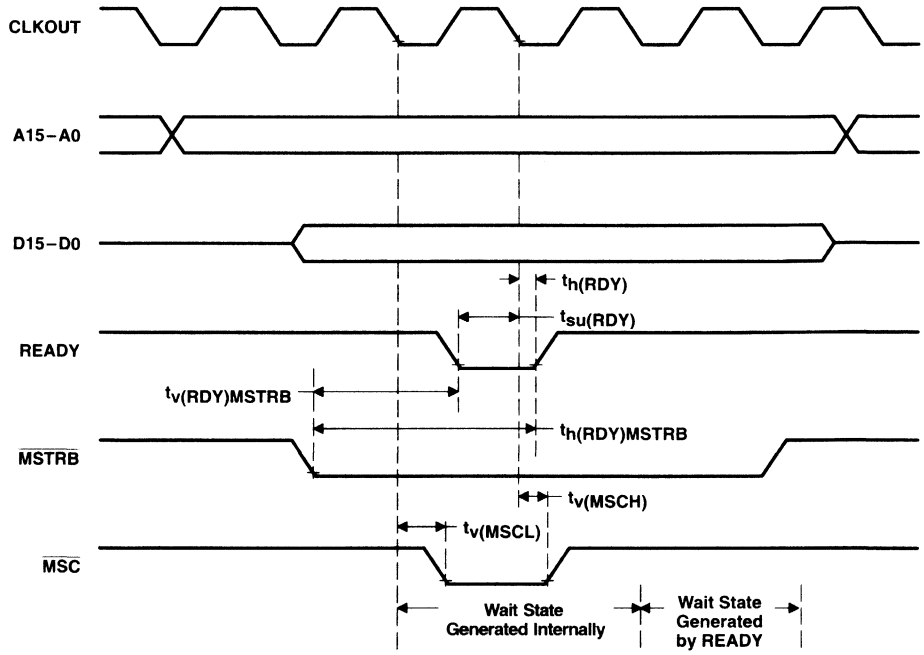

Figure 22. Memory Write With Externally Generated Wait States

ready timing for externally generated wait states (continued)

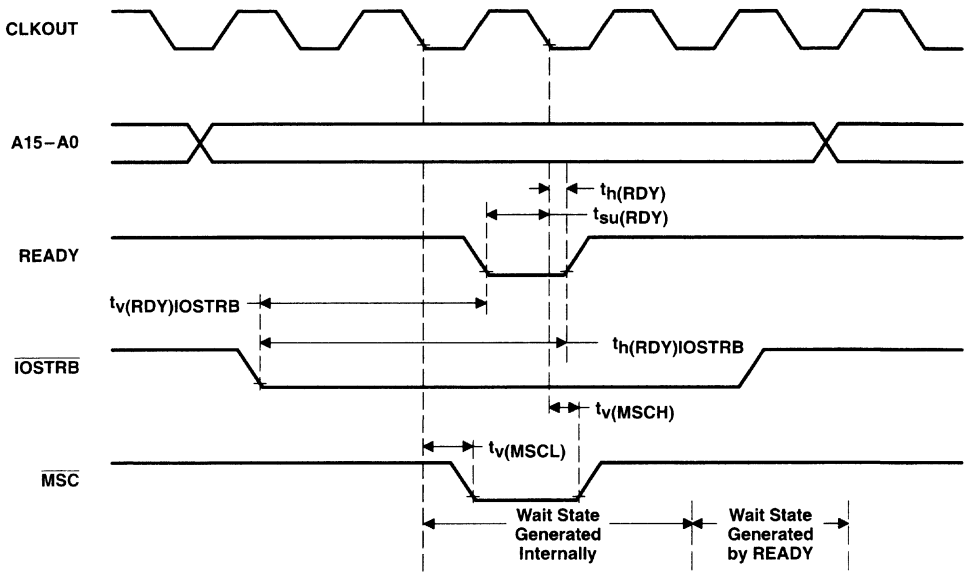

Figure 23. I/O Read With Externally Generated Wait States

ready timing for externally generated wait states (continued)

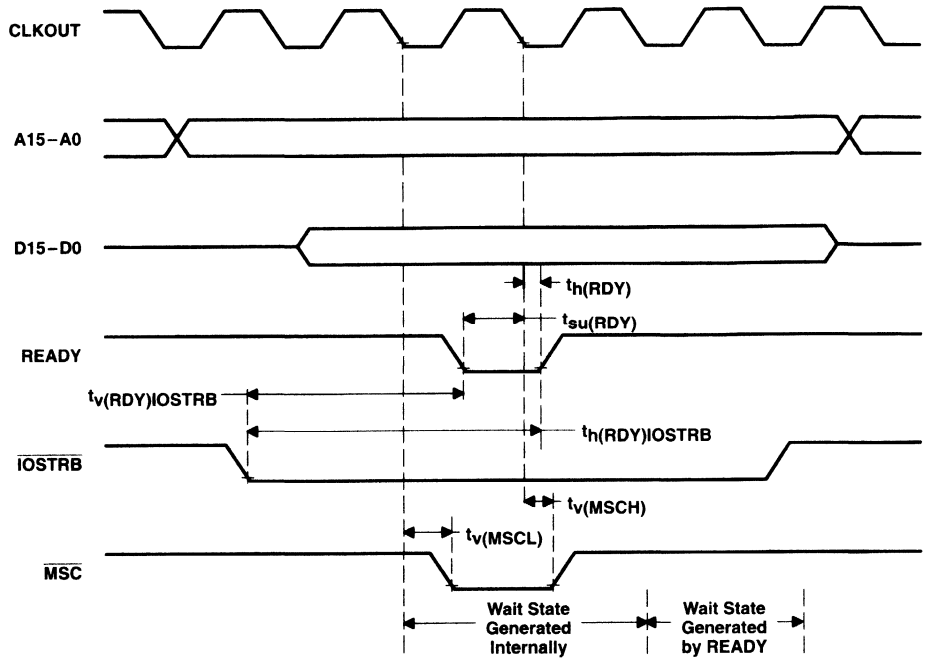

Figure 24. I/O Write With Externally Generated Wait States

HOLD and HOLDA Timing

timing parameters for HOLD and HOLDA [H = 0.5 $t_{c(CO)}$]

		'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX	MIN	MAX	
$t_{dis(CLKL-A)}$	Disable time, CLKOUT low to address, PS, DS, IS		5†		5†	ns
$t_{dis(CLKL-RW)}$	Disable time, CLKOUT low to R/W		5†		5†	ns
$t_{dis(CLKL-S)}$	Disable time, CLKOUT low to MSTRB, IOSTRB		5†		5†	ns
$t_{en(CLKL-A)}$	Enable time, CLKOUT low to address, PS, DS, IS		2H+5		2H+5	ns
$t_{en(CLKL-RW)}$	Enable time, CLKOUT low to R/W enabled		2H+5		2H+5	ns
$t_{en(CLKL-S)}$	Enable time, CLKOUT low to MSTRB, IOSTRB enabled		2H+5		2H+5	ns
$t_{w(HOLD)}$	Pulse duration, HOLD low duration	4H+10		4H+10		ns
$t_{w(HOLDA)}$	Pulse duration, HOLDA low duration	2H+10		2H+10		ns
$t_{su(HOLD)}$	Setup time, HOLD before CLKOUT low	10		10		ns
$t_{v(HOLDA)}$	Valid time, HOLDA after CLKOUT low	–2	5	–2	5	ns

† Values derived from characterization data and not tested.

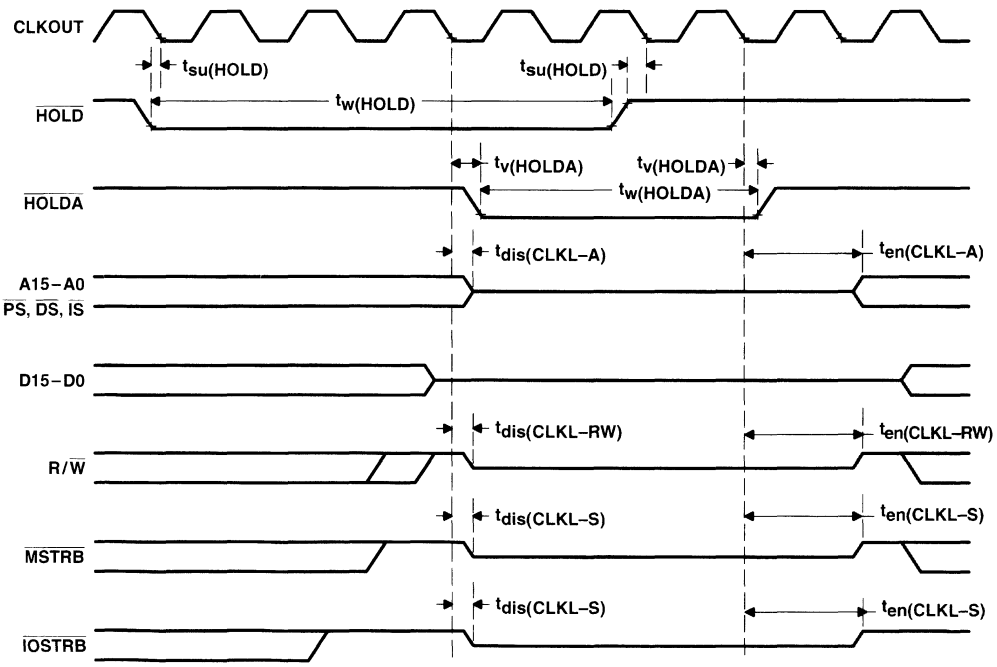

Figure 25. HOLD and HOLDA Timing (HM = 1)

reset, interrupt, $\overline{BIO}$, and MP/$\overline{MC}$ timings

timing parameters for reset, interrupt, $\overline{BIO}$, and MP/$\overline{MC}$ [H = 0.5 $t_{c(CO)}$]

		'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX	MIN	MAX	
$t_{h(RS)}$	Hold time, $\overline{RS}$ after CLKOUT low	0		0		ns
$t_{h(BIO)}$	Hold time, $\overline{BIO}$ after CLKOUT low	0		0		ns
$t_{h(INT)}$	Hold time, $\overline{INT}$n, $\overline{NMI}$, after CLKOUT low†	0		0		ns
$t_{h(MPMC)}$	Hold time, MP/$\overline{MC}$ after CLKOUT low‡	0		0		ns
$t_{w(RSL)}$	Pulse duration, $\overline{RS}$ low§¶	4H+10		4H+10		ns
$t_{w(BIO)S}$	Pulse duration, $\overline{BIO}$ low, synchronous	2H+15		2H+12		ns
$t_{w(BIO)A}$	Pulse duration, $\overline{BIO}$ low, asynchronous¶	4H		4H		ns
$t_{w(INTH)}$	Pulse duration, $\overline{INT}$n, $\overline{NMI}$ high					ns
$t_{w(INTL)S}$	Pulse duration, $\overline{INT}$n, $\overline{NMI}$ low (synchronous)	2H+15		2H+12		ns
$t_{w(INTL)A}$	Pulse duration, $\overline{INT}$n, $\overline{NMI}$ low (asynchronous)¶	4H		4H		ns
$t_{w(INTL)WKP}$	Pulse duration, $\overline{INT}$n, $\overline{NMI}$ low for IDLE2/IDLE3 wakeup‡	10		10		ns
$t_{su(RS)}$	Setup time, $\overline{RS}$ before X2/CLKIN low#	5		5		ns
$t_{su(BIO)}$	Setup time, $\overline{BIO}$ before CLKOUT low	15		12		ns
$t_{su(INT)}$	Setup time, $\overline{INT}$n, $\overline{NMI}$, $\overline{RS}$ before CLKOUT low	15		12		ns
$t_{su(MPMC)}$	Setup time, MP/$\overline{MC}$ before CLKOUT low‡	10		10		ns

† The external interrupts ($\overline{INT0}$–$\overline{INT3}$, $\overline{NMI}$) are synchnonized to the core CPU via a two flip-flop synchronizer which samples these inputs with consecutive falling edges of CLKOUT. The input to the interrupt pins is required to represent a 1–0–0 sequence at the timing that is corresponding to three CLKOUTs sampling sequence.

‡ Values ensured by design but not tested.

§ If the PLL mode is selected, then at power-on sequence, or at wakeup from IDLE3, $\overline{RS}$ must be held low for at least 50 µs to assure synchronization and lock-in of the PLL.

¶ Values derived from characterization data and not tested.

Divide-by-two mode

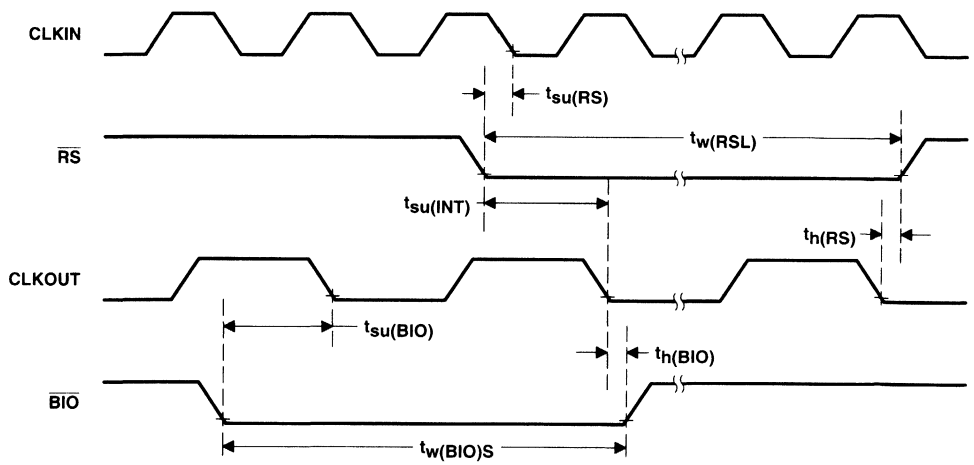

Figure 26. Reset and $\overline{BIO}$ Timings

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reset, interrupt, $\overline{BIO}$, and MP/$\overline{MC}$ timings (continued)

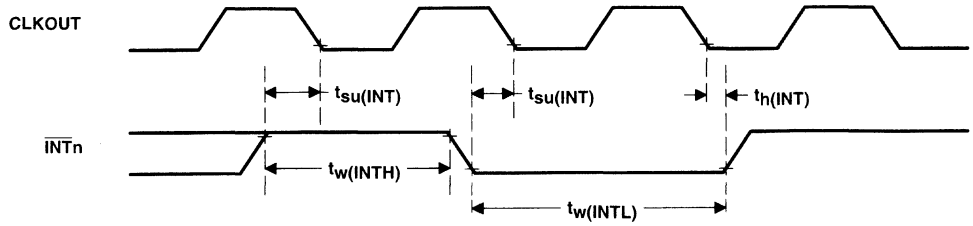

Figure 27. Interrupt Timing

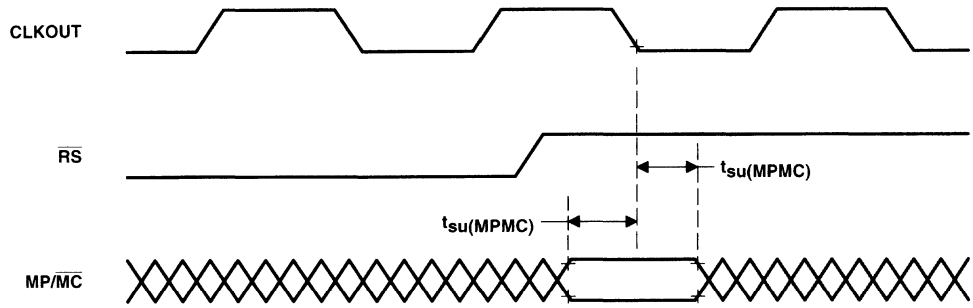

Figure 28. MP/$\overline{MC}$ Timing

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instruction acquisition ($\overline{IAQ}$), interrupt acknowledge ($\overline{IACK}$), external flag (XF), and TOUT timing

timing parameters for $\overline{IAQ}$ and $\overline{IACK}$ (H = 0.5 $t_{c(CO)}$) (see Figure 29)

		'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX	MIN	MAX	
$t_{d(CLKL-IAQL)}$	Delay time, $\overline{IAQ}$ valid from CLKOUT low	0	5	0	5	ns
$t_{d(CLKL-IAQH)}$	Delay time, $\overline{IAQ}$ high from CLKOUT low	– 2	3	– 2	3	ns
$t_{d(A)IAQ}$	Delay time, address valid after $\overline{IAQ}$ low		5		5	ns
$t_{d(CLKL-IACKL)}$	Delay time, $\overline{IACK}$ valid from CLKOUT low	0	5	0	5	ns
$t_{d(CLKL-IACKH)}$	Delay time , $\overline{IACK}$ high from CLKOUT low	– 2	3	– 2	3	ns
$t_{d(A)IACK}$	Delay time, address valid after $\overline{IACK}$ low		5		5	ns
$t_{h(A)IAQ}$	Hold time, address valid after $\overline{IAQ}$ high	0		0		ns
$t_{h(A)IACK}$	Hold time, address valid after $\overline{IACK}$ high	0		0		ns
$t_{w(IAQL)}$	Pulse duration, $\overline{IAQ}$ low	2H – 10		2H – 10		ns
$t_{w(IACKL)}$	Pulse duration, $\overline{IACK}$ low	2H – 10		2H – 10		ns

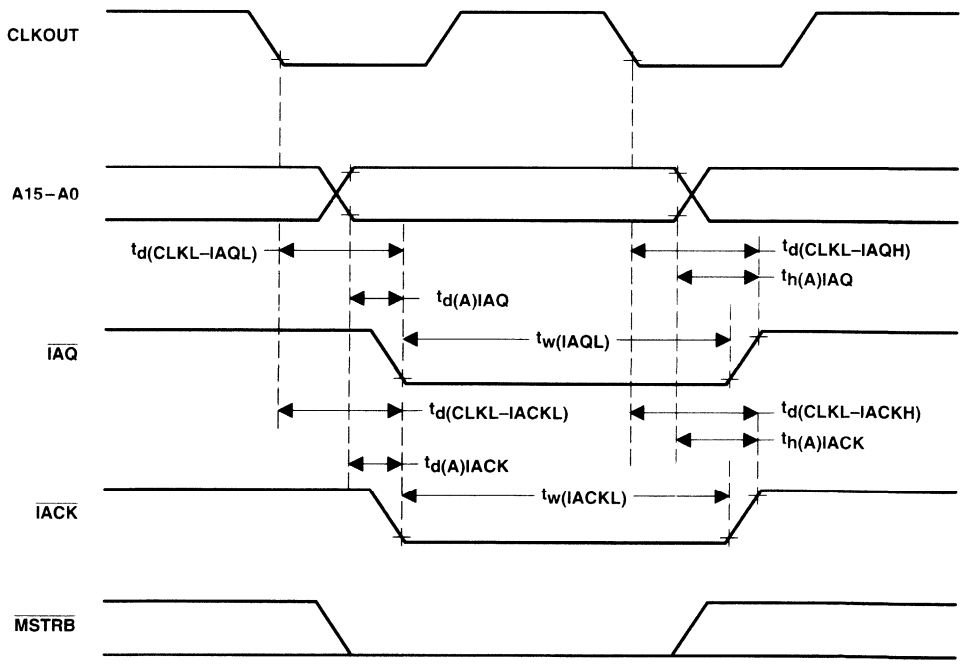

Figure 29. Instruction Acquisition ($\overline{IAQ}$) and Interrupt Acknowledge ($\overline{IACK}$) Timing

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instruction acquisition ($\overline{IAQ}$), interrupt acknowledge ($\overline{IACK}$), external flag (XF), and TOUT timing (continued)

timing parameters for external flag (XF) and TOUT [H = 0.5 $t_{c(CO)}$] (see Figure 30 and Figure 31)

		'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX	MIN	MAX	
$t_{d(XF)}$	Delay time, XF valid after CLKOUT low	−2	5	−2	5	ns
$t_{d(TOUTH)}$	Delay time, TOUT high after CLKOUT low	−2	3	−2	3	ns
$t_{d(TOUTL)}$	Delay time, TOUT low after CLKOUT low	0	5	0	5	ns
$t_{w(TOUT)}$	Pulse duration, TOUT	2H−10		2H−10		ns

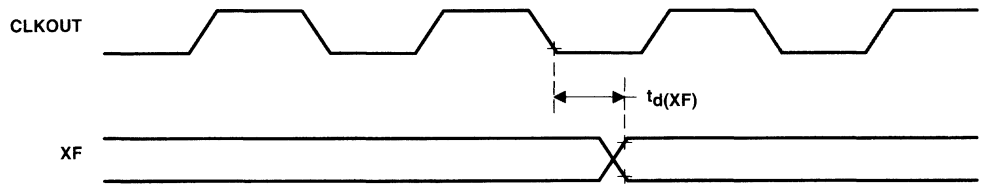

Figure 30. External Flag (XF) Timing

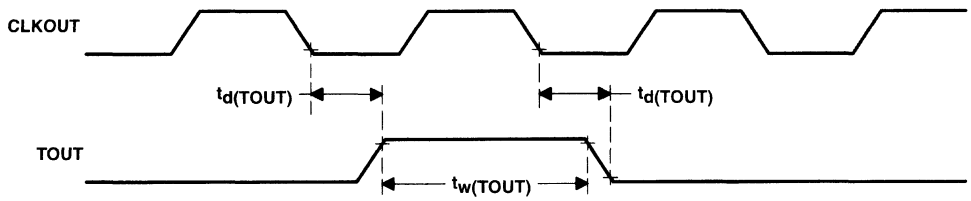

Figure 31. TOUT Timing

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serial port timing

timing parameters for serial port receive [H = 0.5 $t_{c(CO)}$] (see Figure 32)

		'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(SCK)}$	Cycle time, serial port clock	6H	†	6H	†	ns
$t_{f(SCK)}$	Fall time, serial port clock‡		6		6	ns
$t_{r(SCK)}$	Rise time, serial port clock‡		6		6	ns
$t_{w(SCK)}$	Pulse duration, serial port clock low/high	3H		3H		ns
$t_{h(FSR)}$	Hold time, FSR after CLKR falling edge	7		6		ns
$t_{h(DR)}$	Hold time, DR after CLKR falling edge	7		6		ns
$t_{su(FSR)}$	Setup time, FSR before CLKR falling edge	7		6		ns
$t_{su(DR)}$	Setup time, DR before CLKR falling edge	7		6		ns

† The serial port design is fully static and, therefore, can operate with $t_{c(SCK)}$ approaching ∞. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.
‡ Values ensured by design but not tested

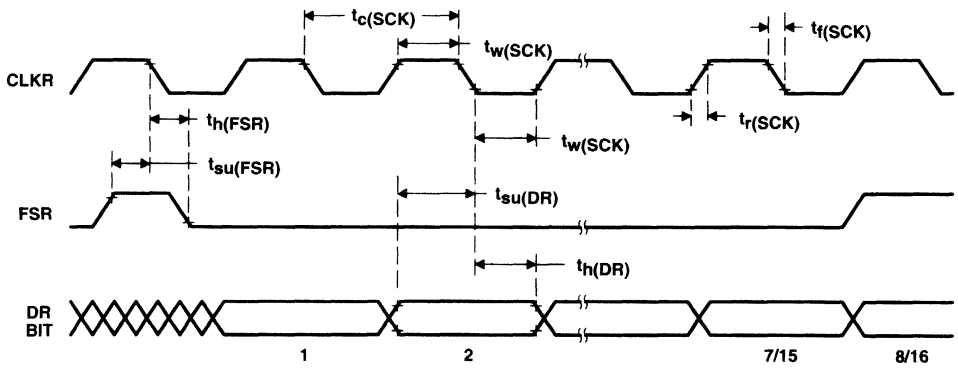


Figure 32. Serial Port Receive Timing

ADVANCE INFORMATION

serial port timing (continued)

timing parameters for serial port transmit with external clocks and frames [H = 0.5$t_{c(CO)}$] (see Figure 33)

		'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(SCK)}$	Cycle time, serial port clock	6H	†	6H	†	ns
$t_{d(DX)}$	Delay time, DX valid after CLKX rising		25		25	ns
$t_{d(FSX)}$	Delay time, FSX after CLKX rising edge		2H–8		2H–5	ns
$t_{dis(DX)}$	Disable time, DX after CLKX rising ‡		40		40	ns
$t_{h(DX)}$	Hold time, DX valid after CLKX rising	–5		–5		ns
$t_{h(FSX)}$	Hold time, FSX after CLKX falling edge (see Note 1)	7		6		ns
$t_{h(FSX)H}$	Hold time, FSX after CLKX rising edge (see Note 1)		2H–8§		2H–5§	ns
$t_{f(SCK)}$	Fall time, serial port clock ¶		6		6	ns
$t_{r(SCK)}$	Rise time, serial port clock ¶		6		6	ns
$t_{w(SCK)}$	Pulse duration, serial port clock low/high	3H		3H		ns

† The serial port design is fully static and, therefore, can operate with $t_{c(SCK)}$ approaching ∞. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.

‡ Values derived from characterization data and not tested.

§ If the FSX pulse does not meet this specification, the first bit of serial data is driven on DX until the falling edge of FSX. After the falling edge of FSX, data is shifted out on DX. The transmit buffer-empty interrupt is generated when the $t_{h(FS)}$ and $t_{h(FSX)H}$ specification is met.

¶ Values ensured by design but not tested.

NOTE 1: Internal clock with external FSX and vice versa are also allowable. However, FSX timings to CLKX always are defined depending on the source of FSX, and CLKX timings always are dependent upon the source of CLKX. Specifically, the relationship of FSX to CLKX is independent of the source of CLKX.

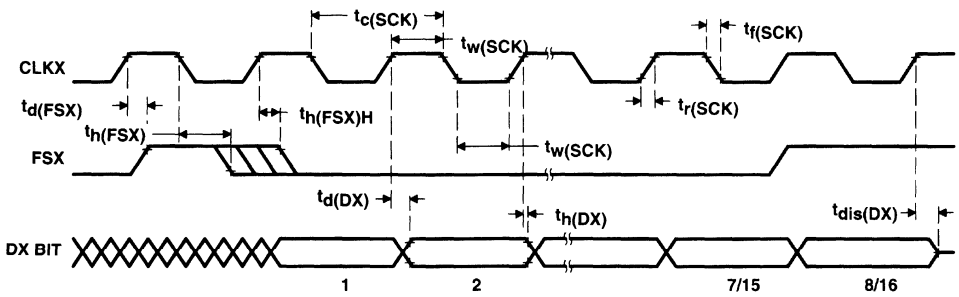


Figure 33. Serial Port Transmit Timing With External Clocks and Frames

ADVANCE INFORMATION

serial port timing (continued)

timing parameters for serial port transmit with internal clocks and frames [H = $0.5t_{c(CO)}$] (see Figure 34)

		'C54x-40 'LC54x-40/'VC54x-40			'LC54x-50 'VC54x-50			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(SCK)}$	Cycle time, serial port clock		8H			8H		ns
$t_{d(FSX)}$	Delay time, CLKX rising to FSX			15			15	ns
$t_{d(DX)}$	Delay time, CLKX rising to DX			15			15	ns
$t_{dis(DX)}$	Disable time, CLKX rising to DX †			20			20	ns
$t_{h(DX)}$	Hold time, DX valid after CLKX rising edge	–5			–5			ns
$t_{f(SCK)}$	Fall time, serial port clock		4			4		ns
$t_{r(SCK)}$	Rise time, serial port clock		4			4		ns
$t_{w(SCK)}$	Pulse duration, serial port clock low/high	4H–8			4H–8			ns

† Values derived from characterization data and not tested

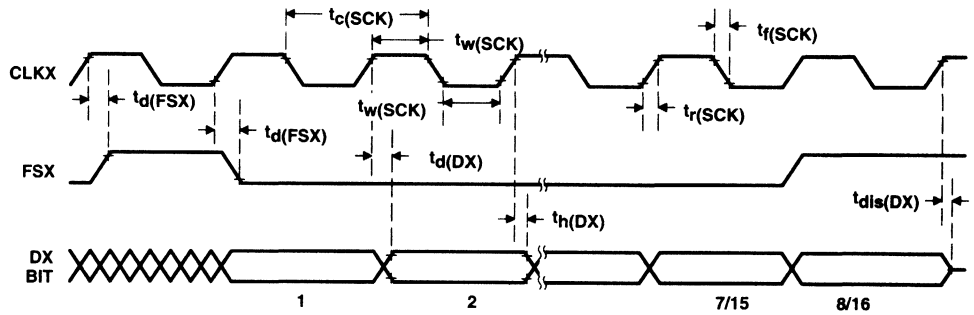


Figure 34. Serial Port Transmit Timing With Internal Clocks and Frames

ADVANCE INFORMATION

buffered serial port receive timing

timing requirements over recommended operating conditions (see Figure 35)

		'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(SCK)}$	Cycle time, serial port clock	25	†	20	†	ns
$t_{f(SCK)}$	Fall time, serial port clock ‡		4		4	ns
$t_{r(SCK)}$	Rise time, serial port clock ‡		4		4	ns
$t_{w(SCK)}$	Pulse duration, serial port clock low/high‡	8.5		6		ns
$t_{su(FSR)}$	Setup time, FSR before CLKR falling edge (see Note 2)	2		2		ns
$t_{h(FSR)}$	Hold time, FSR after CLKR falling edge (see Note 2)	10	$t_{c(SCK)}-2$§	10	$t_{c(SCK)}-2$§	ns
$t_{su(DR)}$	Setup time, DR before CLKR falling edge	0		0		ns
$t_{h(DR)}$	Hold time, DR after CLKR falling edge	10		10		ns

† The serial port design is fully static and therefore can operate with tc(SCK) approaching . It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.
‡ Values ensured by design but not tested
§ First bit is read when FSR is sampled low by CLKR clock.
NOTE 2: Timings for CLKR and FSR are given with polarity bits (CLKP and FSP) set to 0.

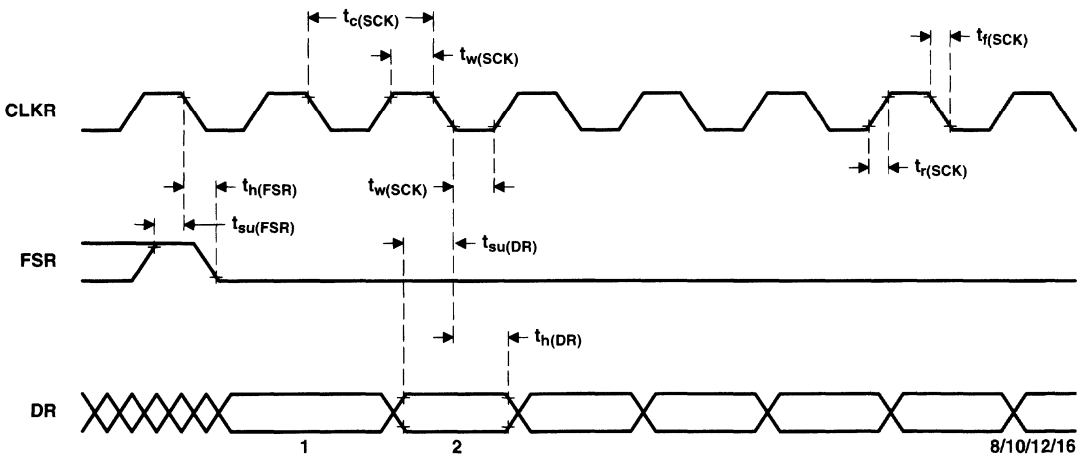


Figure 35. Serial Port Receive Timing

ADVANCE INFORMATION

buffered serial port transmit timing of external frames

switching characteristics over recommended operating conditions (see Figure 36)

PARAMETER		'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX	MIN	MAX	
$t_{d(DX)}$	Delay time, DX valid after CLKX rising		18		18	ns
$t_{dis(DX)}$	Disable time, DX after CLKX rising†	4	6	4	6	ns
$t_{dis(DX)pcm}$	Disable time, PCM mode,DX after CLKX rising†		6		6	ns
$t_{en(DX)pcm}$	Enable time, PCM mode,DX after CLKX rising†	8		8		ns
$t_{h(DX)}$	Hold Time, DX valid after CLKX rising	4		4		ns

† Values derived from characterization data but not tested.

timing requirements over recommended operating conditions (see Figure 36)

		'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(SCK)}$	Cycle time, serial port clock	25	‡	20	‡	ns
$t_{f(SCK)}$	Fall time, serial port clock §		4		4	ns
$t_{r(SCK)}$	Rise time, serial port clock§		4		4	ns
$t_{w(SCK)}$	Pulse duration, serial port clock low/high§	8.5		6		ns
$t_{h(FSX)}$	Hold time, FSX after CLKX falling edge (see Notes 1 and 3)	6	$t_{c(SCK)}-6$¶	6	$t_{c(SCK)}-6$¶	ns
$t_{su(FSX)}$	Setup time, FSX before CLKX falling edge (see Notes 1 and 3)	6		6		ns

‡ The serial port design is fully static and therefore can operate with tc(SCK) approaching . It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.

§ Values ensured by design but not tested.

¶ If FSX does not meet this specification, the first bit of the serial data is driven on DX until FSX goes low (sampled on falling edge of CLKX). After falling edge of the FSX, data will be shifted out on the DX pin.

NOTES: 1. Internal clock with external FSX and vice versa are also allowable. However, FSX timings to CLKX always are defined depending on the source of FSX, and CLKX timings always are dependant upon the source of CLKX. Specifically, the relationship of FSX to CLKX is independant of the source of CLKX.

3. Timings for CLKX and FSX are given with polarity bits (CLKP and FSP) set to 0.

ADVANCE INFORMATION

buffered serial port transmit timing of external frames (continued)

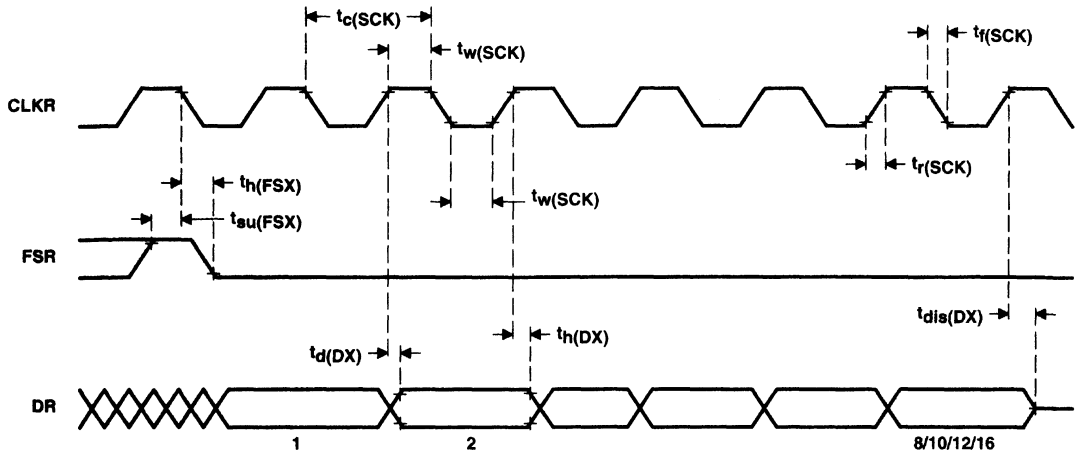


Figure 36. Serial Port Transmit Timing of External Clocks and External Frames

ADVANCE INFORMATION

buffered serial port transmit timing of internal frame and internal clock

switching characteristics over recommended operating conditions [H = 0.5tc(CO)] (see Figure 37)

PARAMETER		'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(SCK)}$	Cycle time, serial port clock	2H	62H	2H	62H	ns
$t_{d(FSX)}$	Delay time, FSX after CLKX rising edge (see Notes 1 and 3)		10		10	ns
$t_{d(DX)}$	Delay time, DX valid after CLKX rising edge		8		8	ns
$t_{dis(DX)}$	Disable time, DX after CLKX rising edge †	0	5	0	5	ns
$t_{dis(DX)pcm}$	Disable time, PCM mode, DX after CLKX rising edge †		5		5	ns
$t_{en(DX)pcm}$	Enable time, PCM mode, DX after CLKX rising edge †	7		7		ns
$t_{h(DX)}$	Hold time, DX valid after CLKX rising edge	0		0		ns
$t_{f(SCK)}$	Fall time, serial port clock ‡		4		4	ns
$t_{r(SCK)}$	Rise time, serial port clock ‡		4		4	ns
$t_{w(SCK)}$	Pulse duration, serial port clock low/high‡	H–4		H–4		ns

† Values derived from characterization data but not tested.
‡ Values ensured by design but not tested.
NOTES: 1. Internal clock with external FSX and vice versa are also allowable. However, FSX timings to CLKX always are defined depending on the source of FSX, and CLKX timings always are dependant upon the source of CLKX. Specifically, the relationship of FSX to CLKX is independant of the source of CLKX.
3. Timings for CLKX and FSX are given with polarity bits (CLKP and FSP) set to 0.

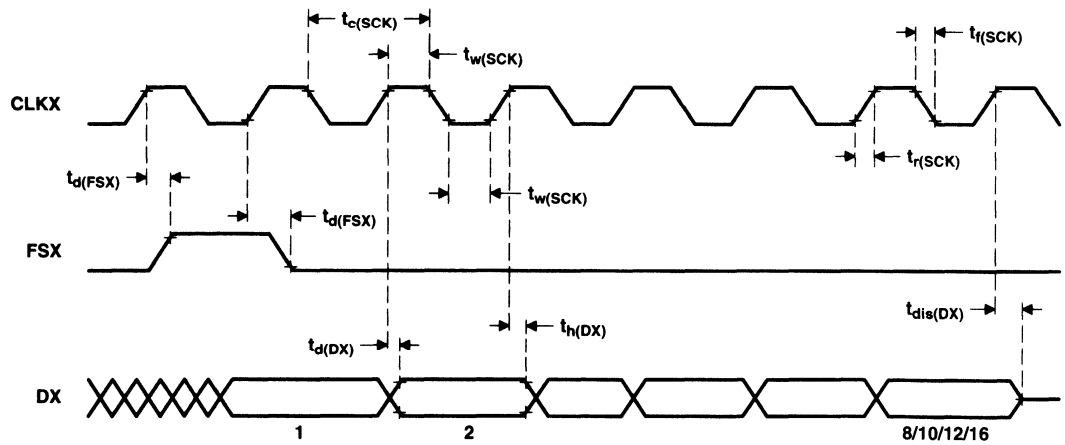


Figure 37. Serial Port Transmit Timing of Internal Clocks and Internal Frames

ADVANCE INFORMATION

serial-port receive timing in TDM mode

timing requirements over recommended ranges of supply voltage and operating free-air temperature [H = 0.5$t_{c(CO)}$] (see Figure 25)

		'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX†	MIN	MAX†	
$t_{c(SCK)}$	Cycle time, serial-port clock	8H	‡	8H	‡	ns
$t_{f(SCK)}$	Fall time, serial-port clock		6		6	ns
$t_{r(SCK)}$	Rise time, serial-port clock		6		6	ns
$t_{w(SCK)}$	Pulse duration, serial-port clock low/high	4H		4H		ns
$t_{su(TD-TCH)}$	Setup time, TDAT before TCLK rising edge	25		25		ns
$t_{h(TCH-TD)}$	Hold time, TDAT after TCLK rising edge	– 6		– 6		ns
$t_{su(TA-TCH)}$	Setup time, TADD before TCLK rising edge§	25		25		ns
$t_{h(TCH-TA)}$	Hold time, TADD after TCLK rising edge§	– 6		– 6		ns
$t_{su(TF-TCH)}$	Setup time, TFRM before TCLK rising edge¶	10		10		ns
$t_{h(TCH-TF)}$	Hold time, TFRM after TCLK rising edge¶	10		10		ns

† Values ensured by design and are not tested.

‡ The serial-port design is fully static and, therefore, can operate with $t_{c(SCK)}$ approaching infinity. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.

§ These parameters apply only to the first bits in the serial bit string.

¶ TFRM timing and waveforms shown in Figure 25 are for external TFRM. TFRM can also be configured as internal. The TFRM internal case is illustrated in the transmit timing diagram in Figure 26.

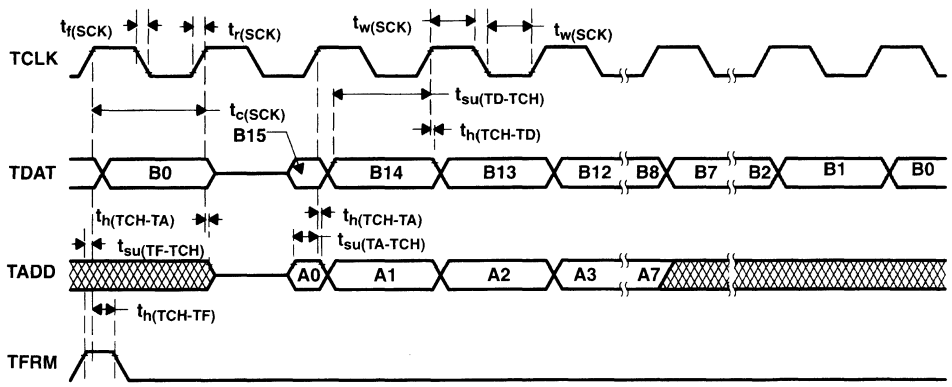


Figure 38. Serial-Port Receive Timing in TDM Mode

serial-port transmit timing in TDM mode (continued)

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] (see Figure 26)

PARAMETER		'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX	MIN	MAX	
$t_{h(TCH-TDV)}$	Hold time, external TDAT/TADD valid after TCLK rising edge	0		0		ns
$t_{h(TCH-TDV)}$	Hold time, internal TDAT/TADD valid after TCLK rising edge	– 5		– 5		ns
$t_{d(TCH-TFV)}$	Delay time, TFRM valid after TCLK rising edge, TCLK ext †	H	3H + 22	H	3H + 22	ns
	Delay time, TFRM valid after TCLK rising edge, TCLK int †	H	3H + 12	H	3H + 12	ns
$t_{d(TC-TDV)}$	Delay time, TCLK to valid TDAT/TADD, TCLK ext		22		22	ns
	Delay time, TCLK to valid TDAT/TADD, TCLK int		18		18	ns

† TFRM timing and waveforms shown in Figure 26 are for internal TFRM. TFRM can also be configured as external. The TFRM external case is illustrated in the receive timing diagram in Figure 25.

timing requirements over recommended ranges of supply voltage and operating free-air temperature [H = 0.5$t_{c(CO)}$] (see Figure 26)

		'C54x-40 'LC54x-40/ 'VC54x-40		'LC54x-50 'VC54x-50		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(SCK)}$	Cycle time, serial-port clock	8H‡	§	8H‡	§	ns
$t_{f(SCK)}$	Fall time, serial-port clock		6¶		6¶	ns
$t_{r(SCK)}$	Rise time, serial-port clock		6¶		6¶	ns
$t_{w(SCK)}$	Pulse duration, serial-port clock low/high	4H‡		4H‡		ns

‡ When SCK is generated internally this value is typical.

§ The serial-port design is fully static and, therefore, can operate with $t_{c(SCK)}$ approaching ∞. It is characterized approaching an input frequency of 0 Hz but tested as a much higher frequency to minimize test time.

¶ Values ensured by design but are not tested

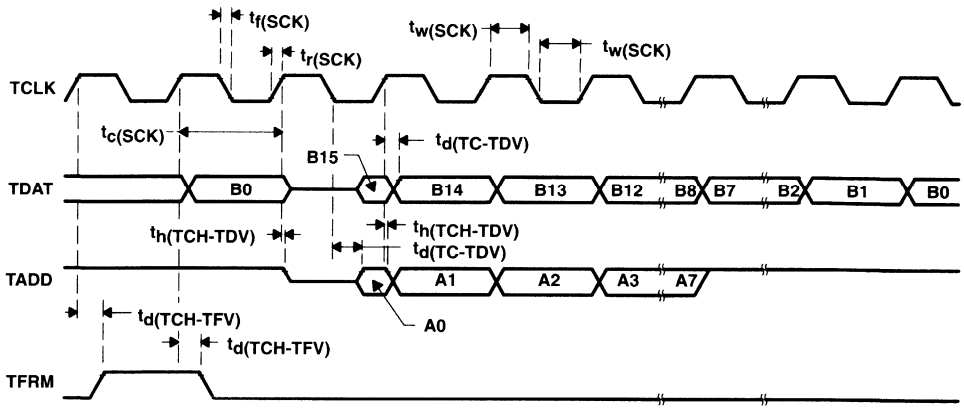


Figure 39. Serial-Port Transmit Timing in TDM Mode

ADVANCE INFORMATION

host port interface

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] (See Notes 11 and 12) (see Figure 30 through Figure 33)

	PARAMETER	MIN	MAX	UNIT
$t_{d(DSL-HDV)}$	Delay time, $\overline{DS}$ low to HD valid	5†	12‡	ns
$t_{d(HEL-HDV1)}$	Delay time, HDS falling to HD valid for first byte of a subsequent read: Case 1: Shared-access mode if $t_{w(HDS)h}$ < 7H §¶ Case 2: Shared-access mode if $t_{w(HDS)h}$ > 7H Case 3: Host-only mode if $t_{w(HDS)h}$ < 7H Case 4: Host-only mode if $t_{w(HDS)h}$ > 7H		7H+20–$t_{w(DSH)}$ 20‡ 40–$t_{w(DSH)}$ 20‡	ns
$t_{d(DSL-HDV2)}$	Delay time, $\overline{DS}$ low to HD valid, second byte	5¶	20	ns
$t_{d(DSH-HYH)}$	Delay time, $\overline{DS}$ high to HRDY high		10(6)H+10‡	ns
$t_{su(HDV-HYH)}$	Setup time, HD valid before HRDY rising edge	3H–10‡		ns
$t_{h(DSH-HDV)}$	Hold time, HD valid after $\overline{DS}$ rising edge	0	12†#	ns
$t_{d(COH-HYH)}$	Delay time, CLKOUT rising edge to HRDY high		10‡	ns
$t_{d(DSH-HYL)}$	Delay time, $\overline{HDS}$ or $\overline{HCS}$ high to HRDY low		12‡	ns
$t_{d(COH-HTX)}$	Delay time, CLKOUT rising edge to $\overline{HINT}$ change		15	ns

† Values derived from characterization data and not tested.
‡ Values ensured by design but not tested.
§ Host-only mode timings apply for read accesses to HPIC or HPIA, write accesses to BOB, and resetting DSPINT or HINT to 0 in shared-access mode. HRDY does not go low for these accesses.
¶ Shared-access mode timings will be met automatically if HRDY is used.
# HD release
NOTES: 4. SAM = shared-access mode, HOM = host-only mode
HAD stands for HCNTRL0, HCNTRL1, and HR/$\overline{W}$.
$\overline{HDS}$ refers to either $\overline{HDS1}$ or $\overline{HDS2}$.
$\overline{DS}$ refers to the logical OR of $\overline{HCS}$ and $\overline{HDS}$.
5. On host read accesses to the HPI, the setup time of HD before $\overline{DS}$ rising edge depends on the host waveforms and cannot be specified here.

timing requirements over recommended operating conditions [H = 0.5$t_{c(CO)}$] (See Note 11) (see Figure 30 through Figure 33)

		MIN	MAX	UNIT
$t_{su(HBV-DSL)}$	Setup time, HAD/HBIL valid before $\overline{DS}$ falling edge	10		ns
$t_{h(DSL-HBV)}$	Hold time, HAD/HBIL valid after $\overline{DS}$ falling edge	10		ns
$t_{su(HSL-DSL)}$	Setup time, $\overline{HAS}$ low before $\overline{DS}$ falling edge	12		ns
$t_{w(DSL)}$	Pulse duration, $\overline{DS}$ low	30‖		ns
$t_{w(DSH)}$	Pulse duration, $\overline{DS}$ high	10		ns
$t_{c(DSH-DSH)}$‖	Cycle time, $\overline{DS}$ rising edge to next $\overline{DS}$ rising edge: Case 1: When using HRDY (see Figure 39) Case 2a: SAM accesses and HOM active writes to DSPINT or HINT without using HRDY (see Figure 37 and Figure 38) Case 2b: When not using HRDY for other HOM accesses		50 10H‡ 50	ns
$t_{su(HDV-DSH)}$	Setup time, HD valid before $\overline{DS}$ rising edge	12		ns
$t_{h(DSH-HDV)}$	Hold time, HD valid after $\overline{DS}$ rising edge	0		ns

‡ Values ensured by design but not tested.
‖ A host not using HRDY should meet the 10H requirement all the time unless a software handshake is used to change the access rate according to the HPI mode.
NOTE 11: SAM = shared-access mode, HOM = host-only mode
HAD stands for HCNTRL0, HCNTRL1, and HR/$\overline{W}$.
$\overline{HDS}$ refers to either $\overline{HDS1}$ or $\overline{HDS2}$.
$\overline{DS}$ refers to the logical OR of $\overline{HCS}$ and $\overline{HDS}$.

ADVANCE INFORMATION

host port interface (continued)

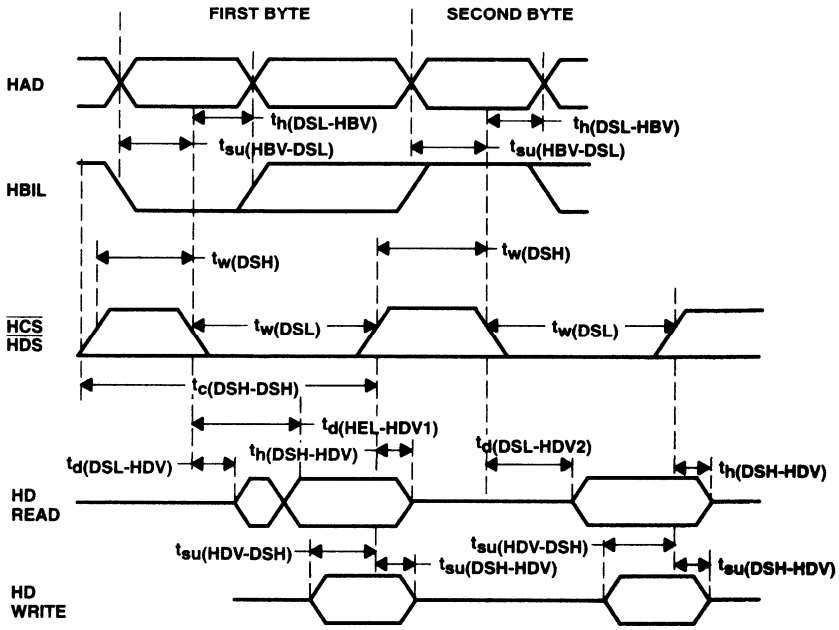


Figure 40. Read/Write Access Timings Without HRDY or $\overline{HAS}$

ADVANCE INFORMATION

host port interface (continued)

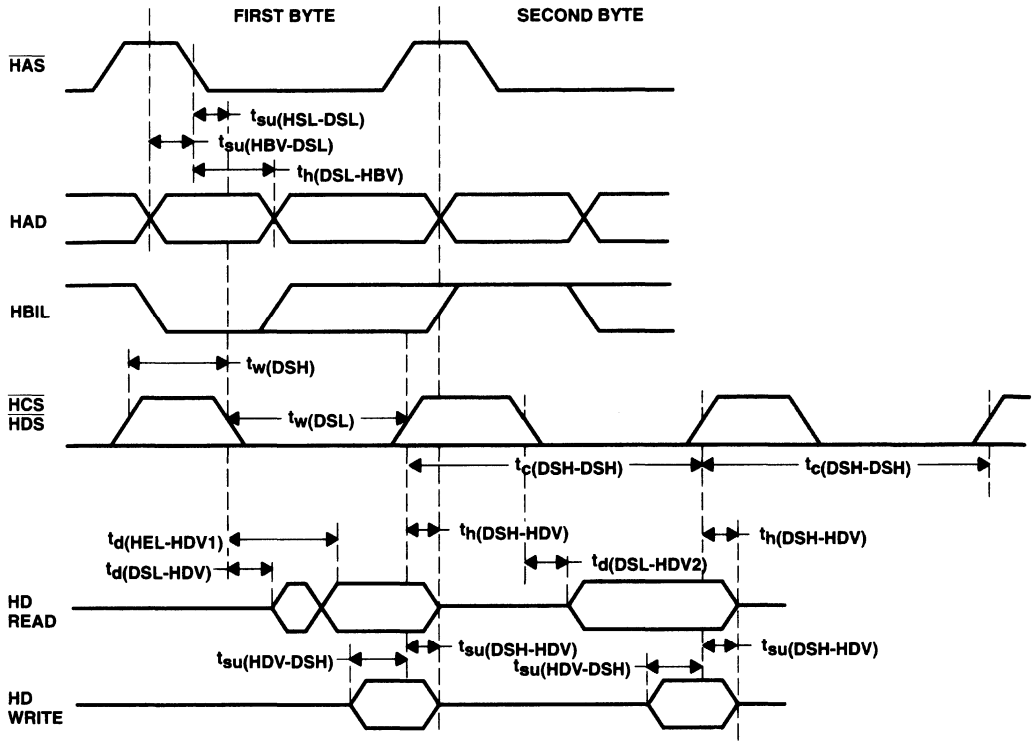
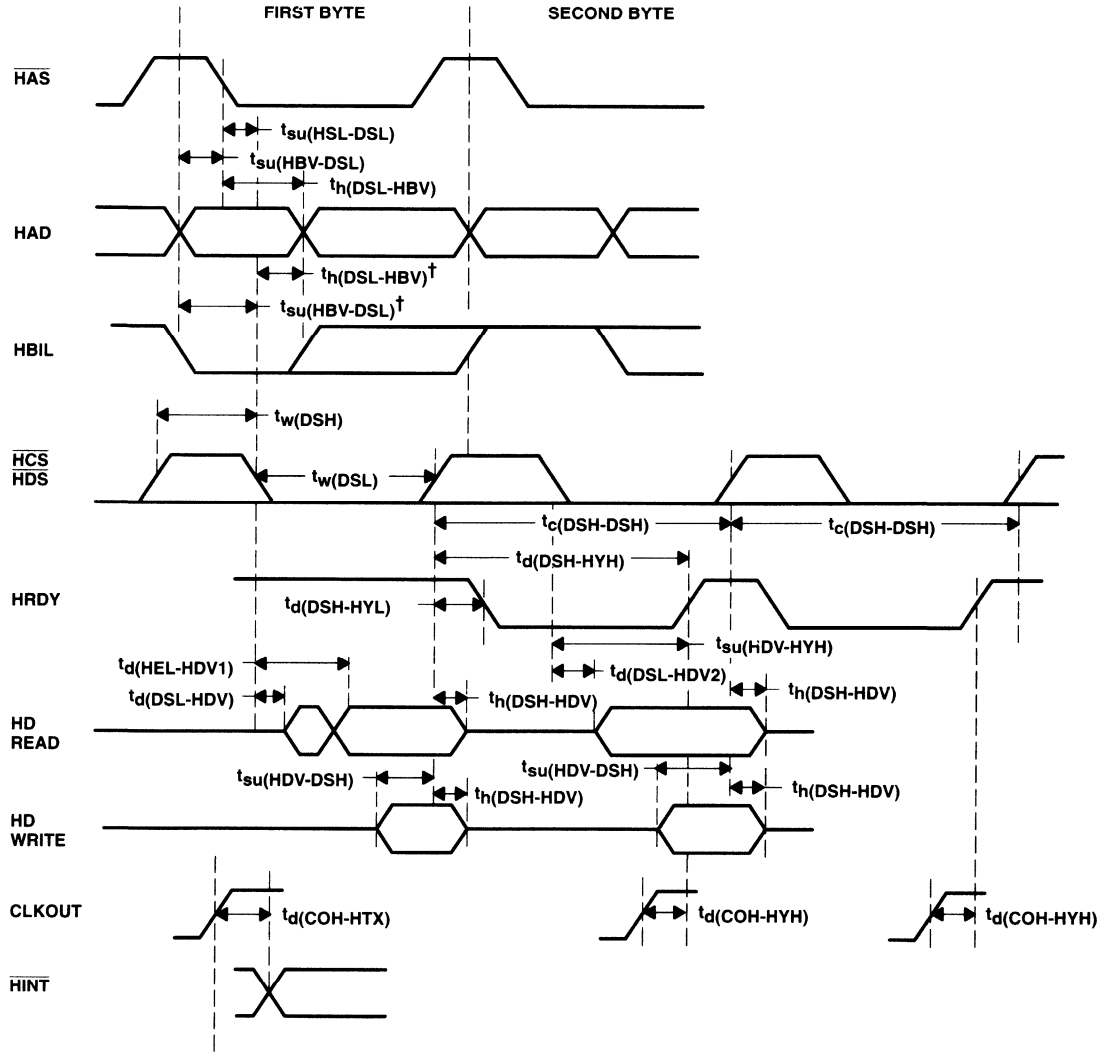


Figure 41. Read/Write Access Timings Using $\overline{\text{HAS}}$ Without HRDY

host port interface (continued)



† When $\overline{HAS}$ is tied to V_{DD}

Figure 42. Read/Write Access Timing With HRDY

ADVANCE INFORMATION

host port interface (continued)

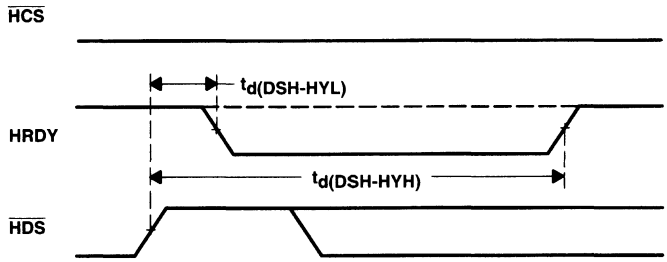


Figure 43. HRDY Signal When $\overline{HCS}$ Is Always Low

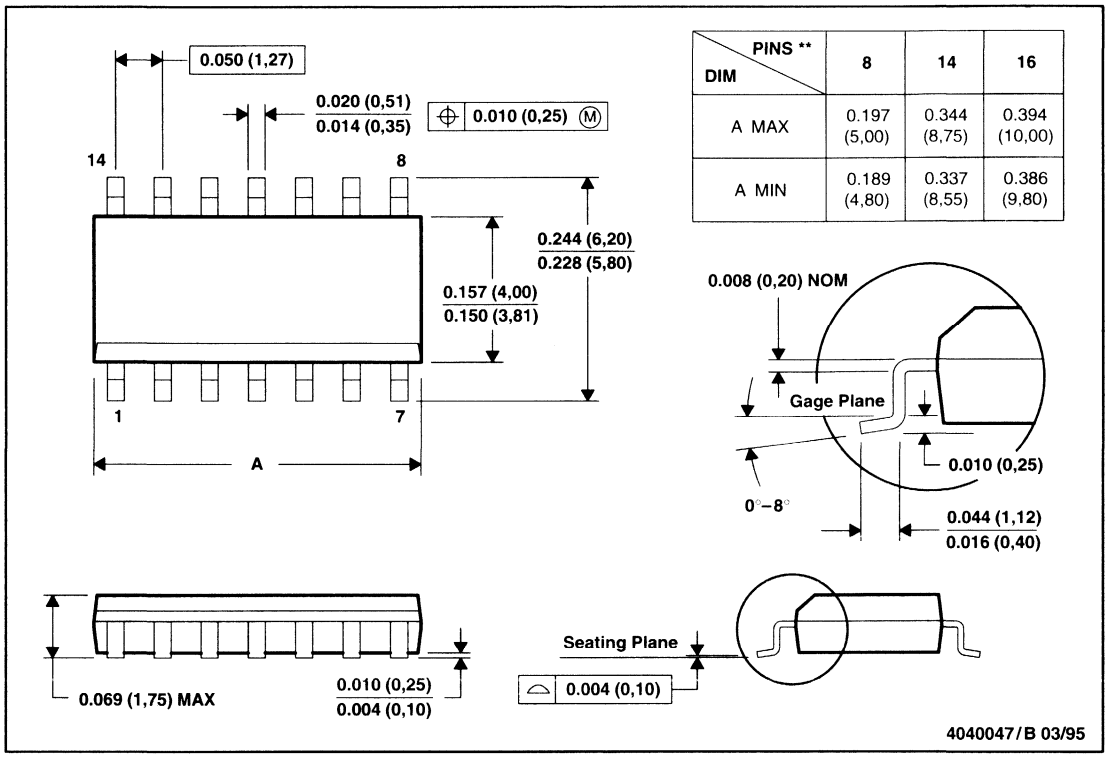
10 Mechanical Data

SLWD001 – JULY 1996

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN

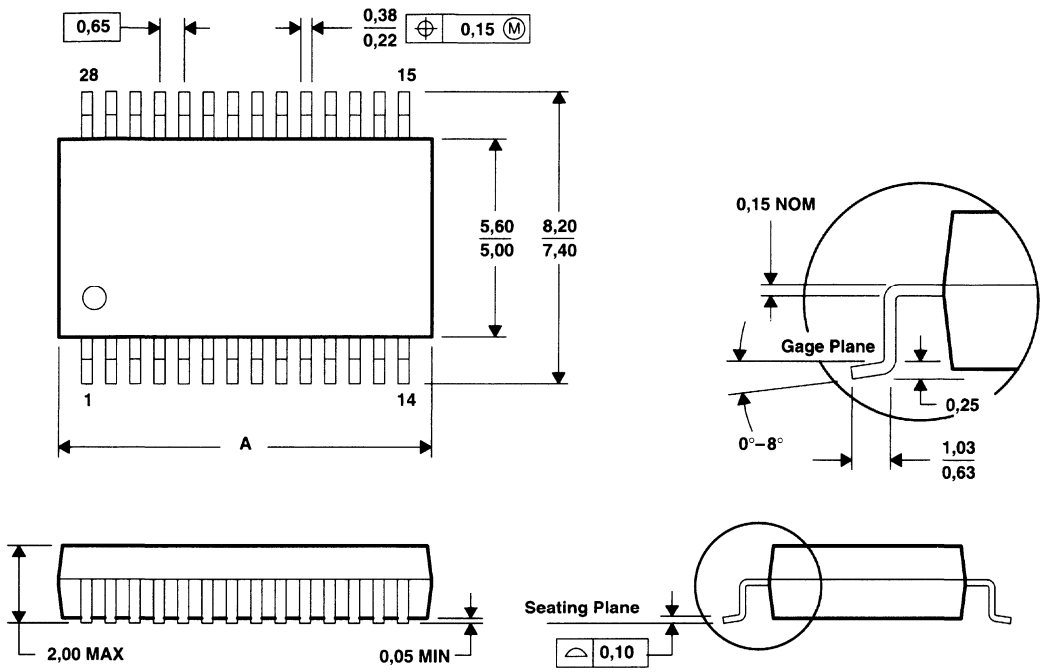


DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Four center pins are connected to die mount pad.
E. Falls within JEDEC MS-012

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

28 PIN SHOWN



DIM \ PINS **	8	14	16	20	24	28	30	38
A MAX	3,30	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	2,70	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 / C 10/95

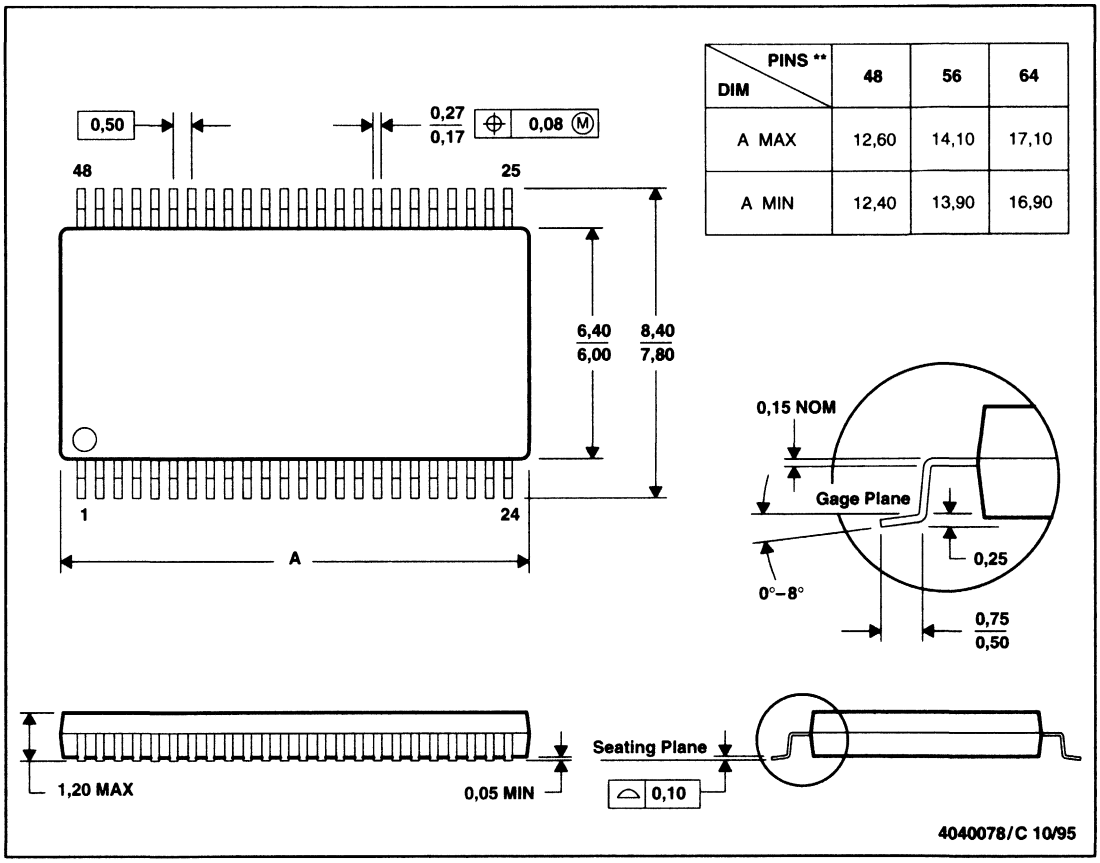
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

SLWD001 – JULY 1996

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PIN SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-153

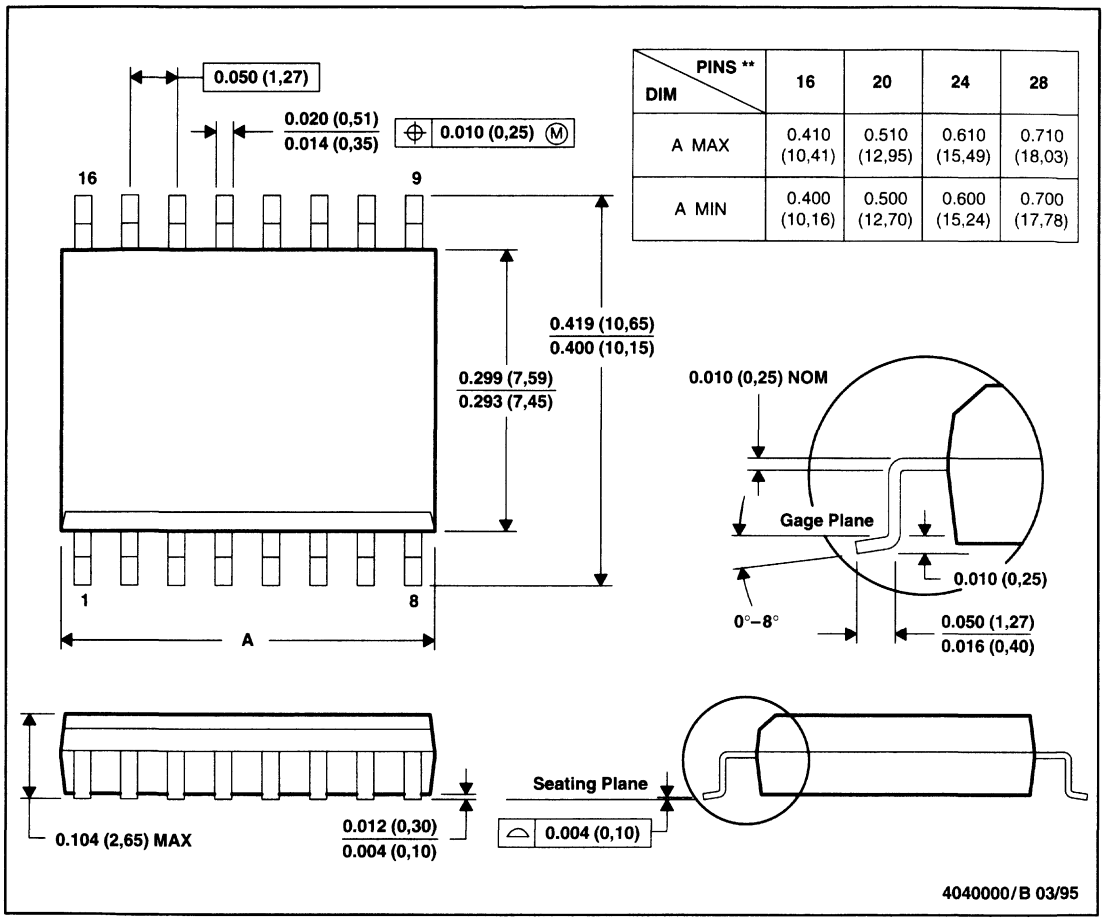
MECHANICAL DATA

SLWD001 – JULY 1996

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

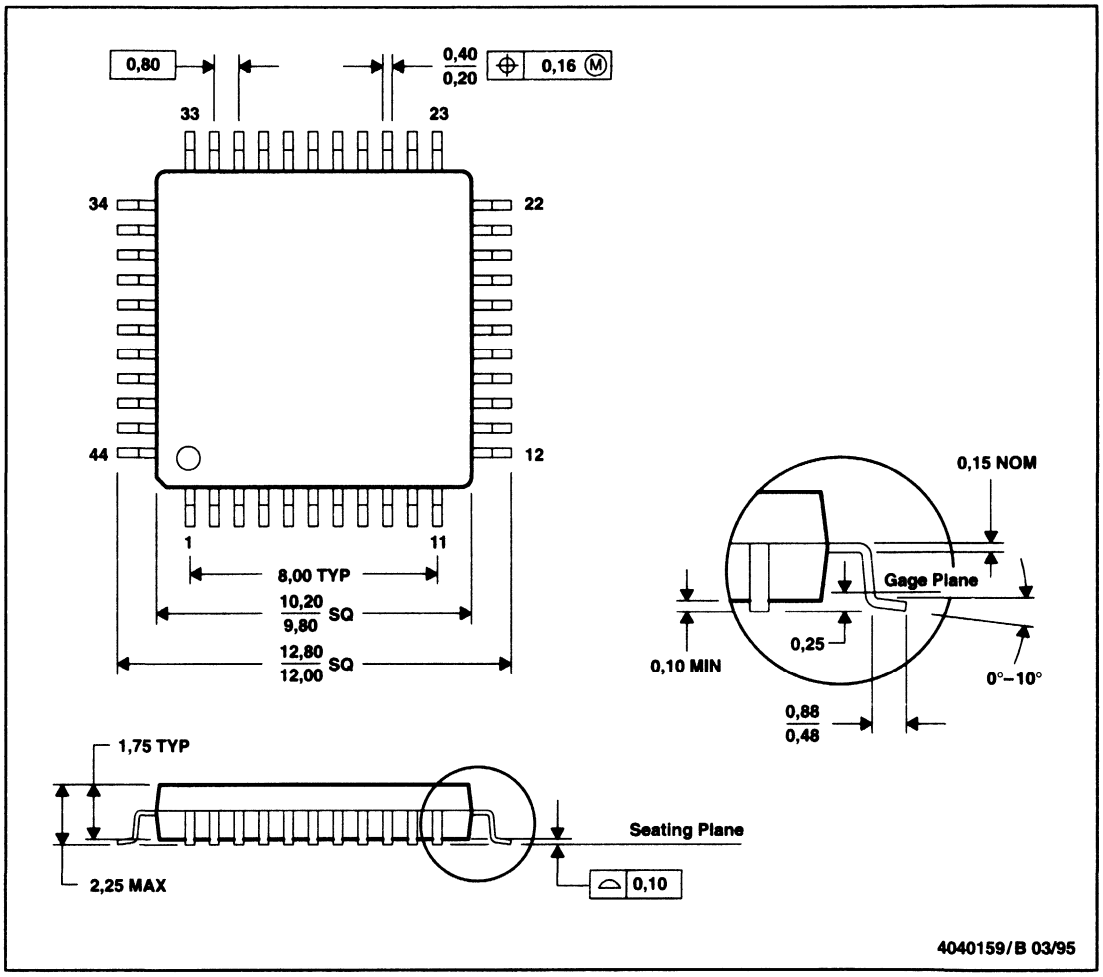
16 PIN SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

FR (S-PDFP-G44) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

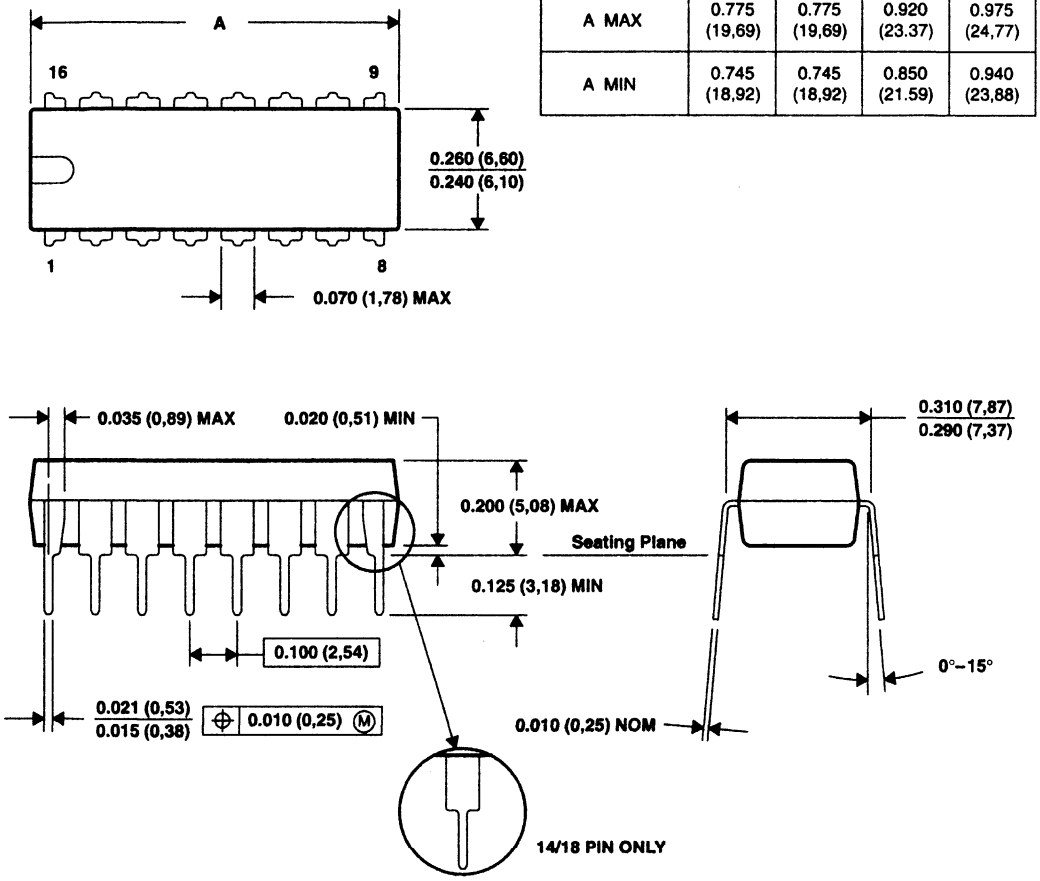
MECHANICAL DATA

SLWD001 – JULY 1996

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PIN SHOWN

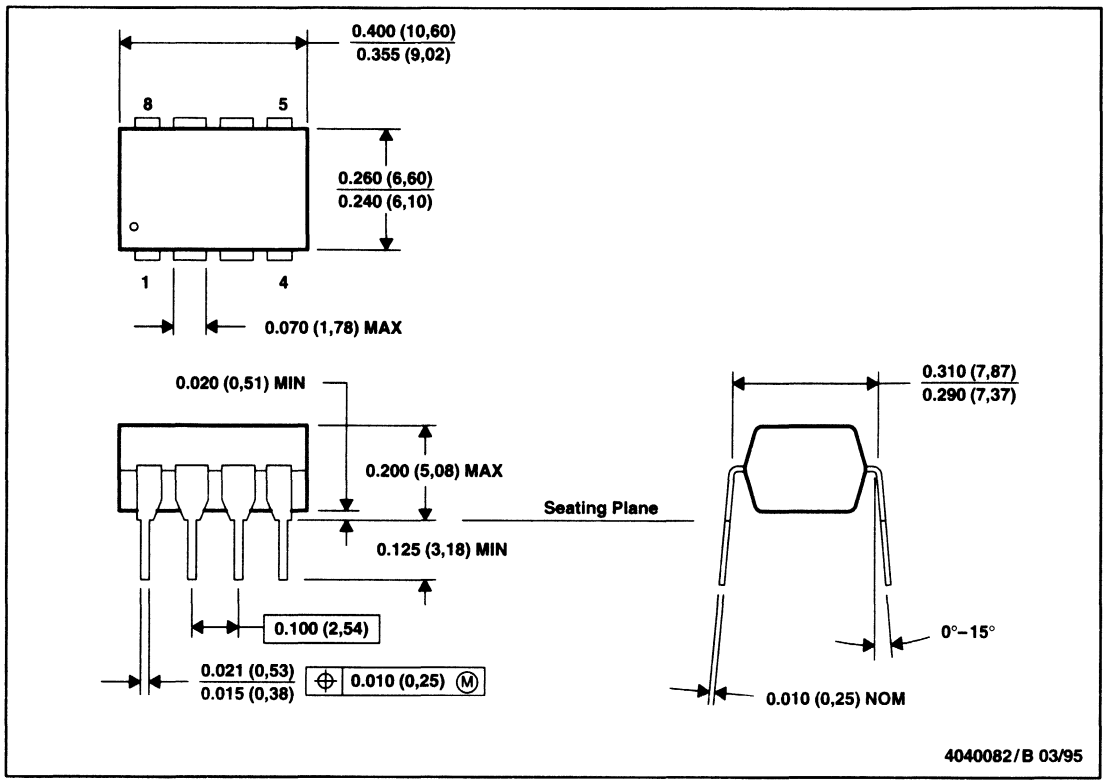
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20 pin package is shorter then MS-001.)

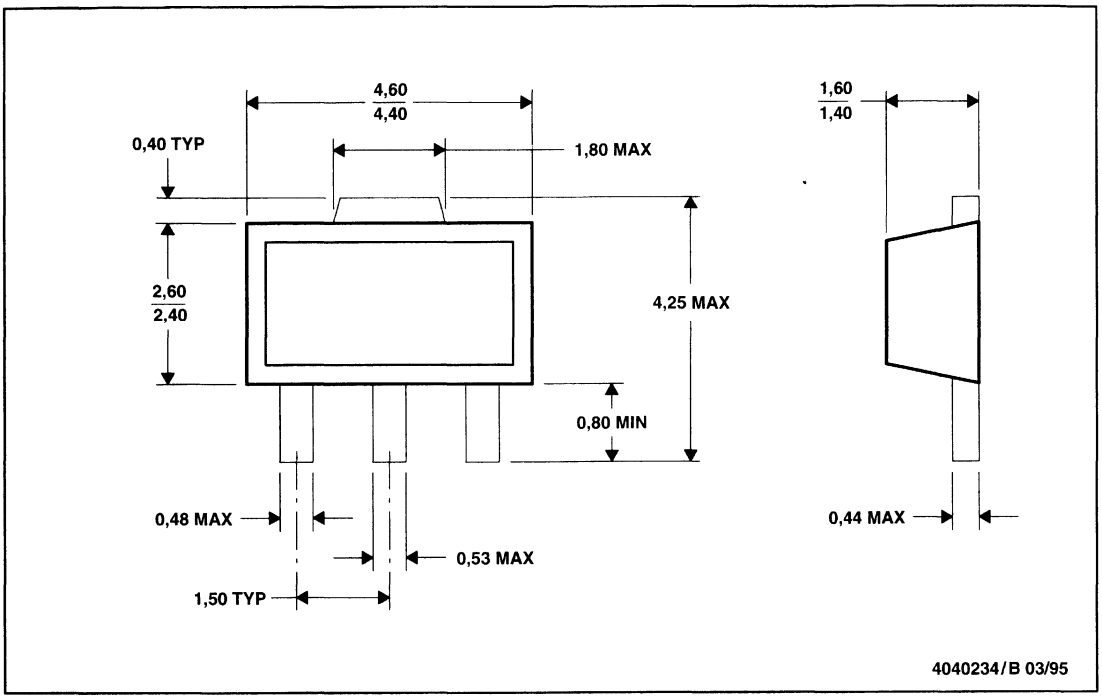
SLWD001 – JULY 1996

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE PACKAGE**



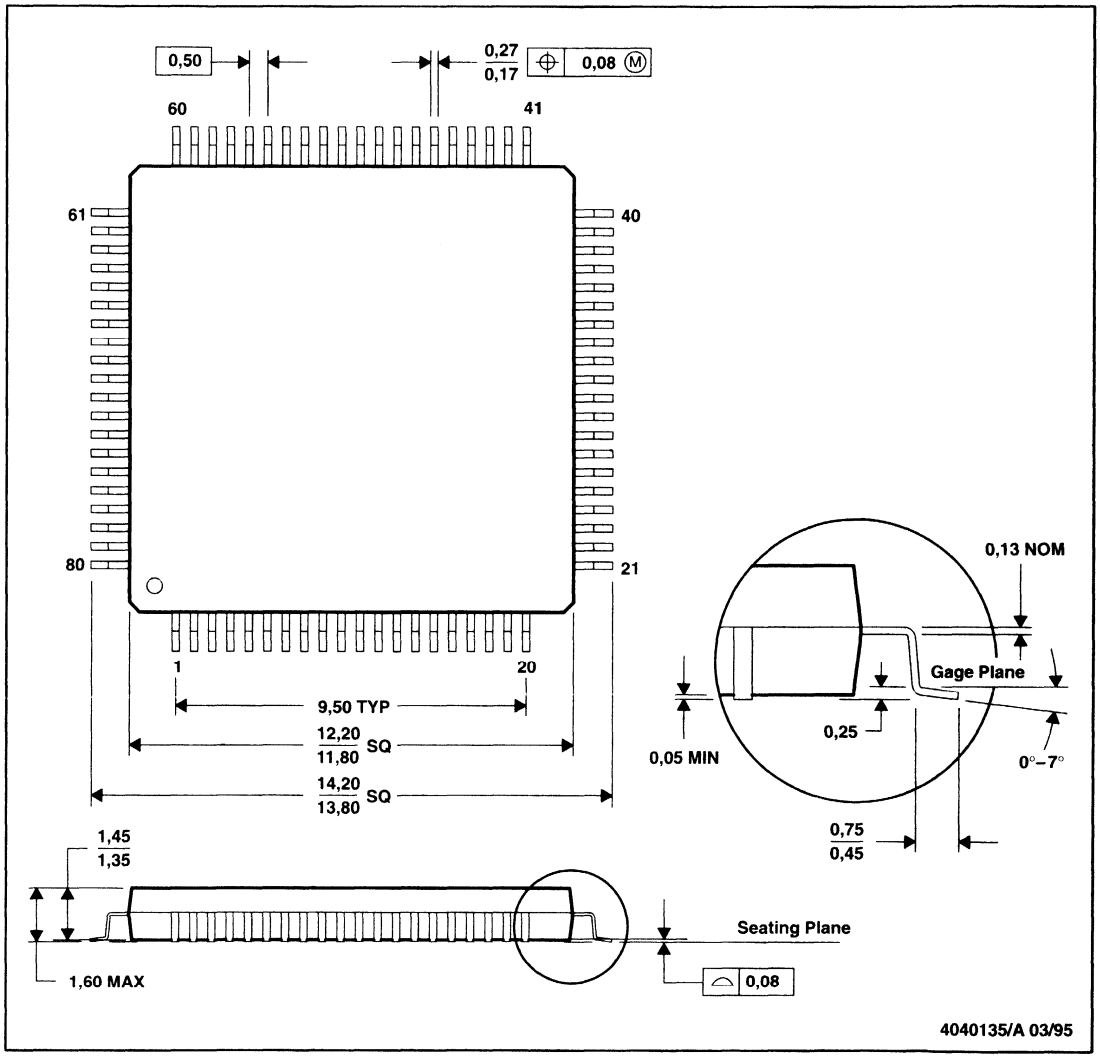
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

PK (R-PSSO-F3) **PLASTIC SINGLE-IN-LINE PACKAGE**



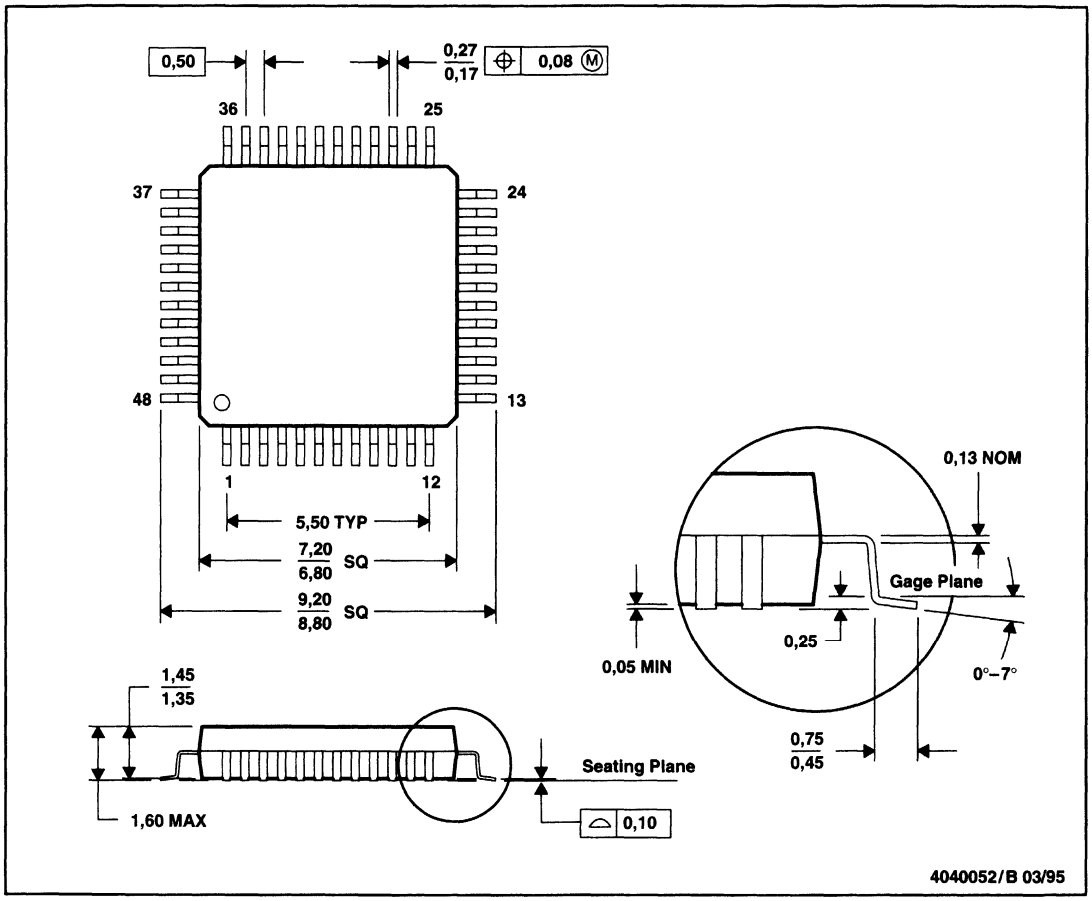
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the tab.

PN (S-PQFP-G80) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

PT (S-PQFP-G48) **PLASTIC QUAD FLATPACK**

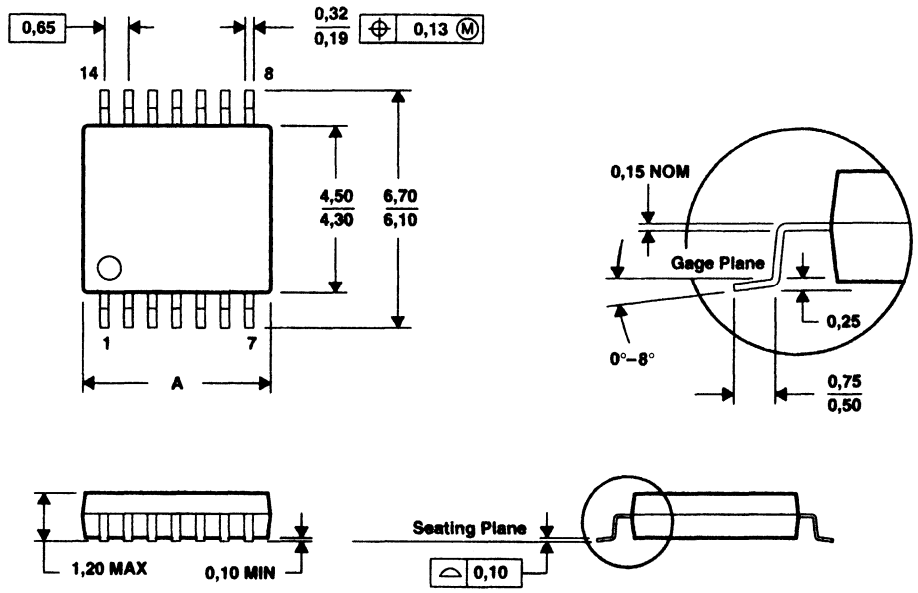


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136
D. This may also be a thermally-enhanced plastic package with leads connected to the die pads.

SLWD001 – JULY 1996

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/D 10/95

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

MECHANICAL DATA

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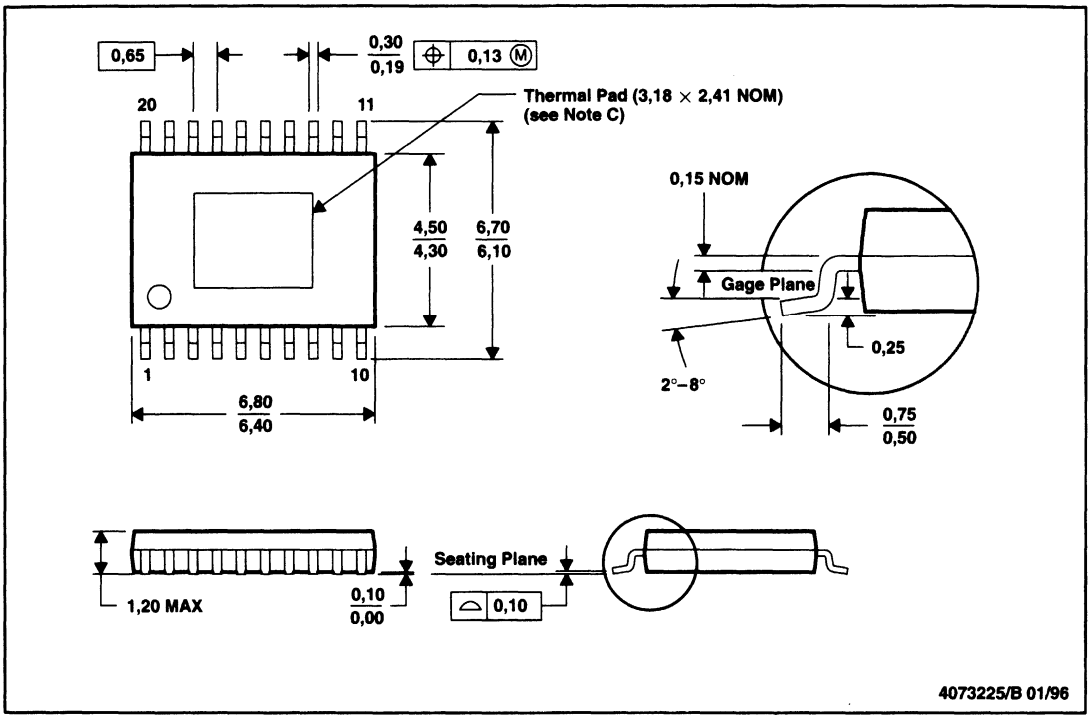
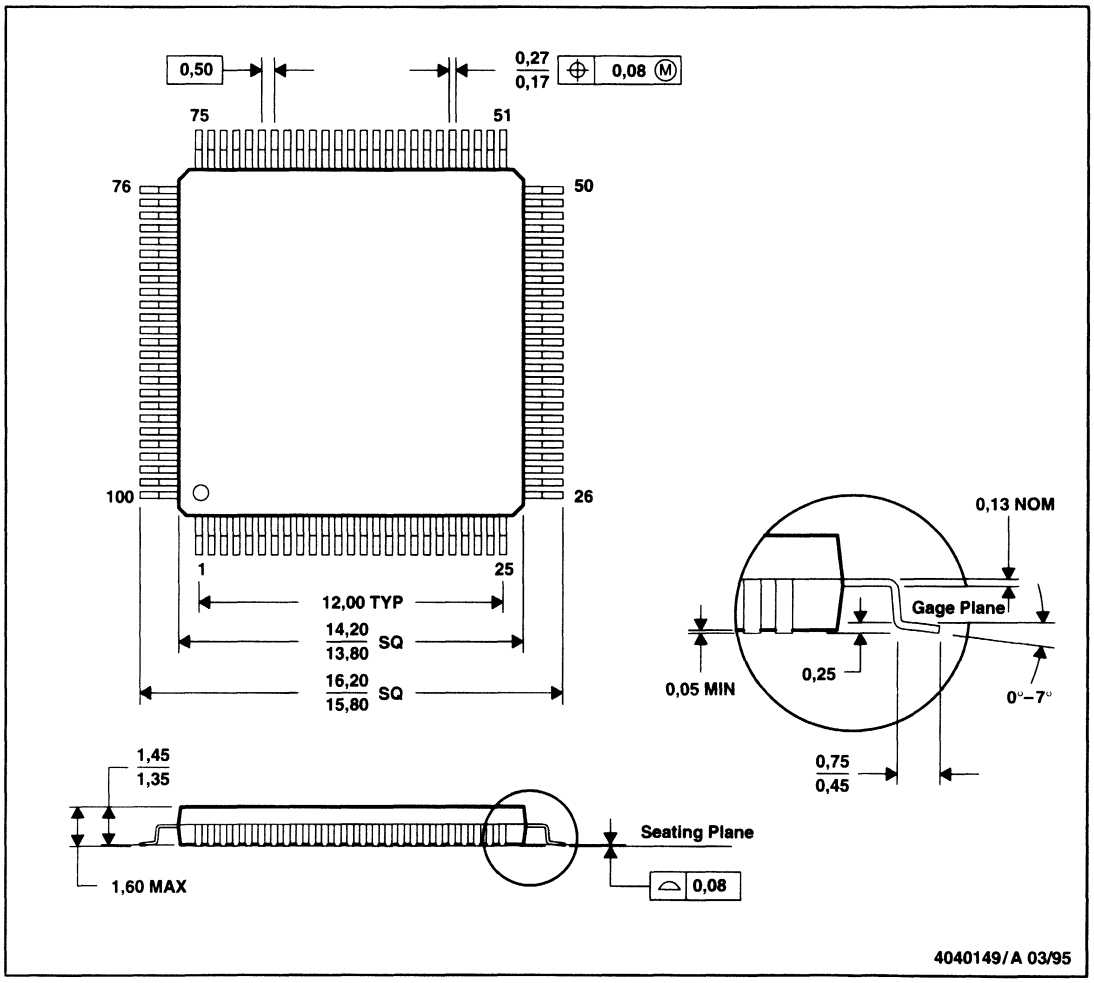
PWP (R-PDSO-G20) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This solderable pad is electrically and thermally connected to the backside of the die and leads 1, 2, 9, 10, 11, 12, 19 and 20.

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

NOTES

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